AOZ1360

28V Programmable Current-Limited Load Switch

General Description

The AOZ1360 is a member of Alpha and Omega Semiconductor's high-side load switch family intended for applications that require circuit protection. The device operates from a source voltage between 5.5V and 28V. The internal current limiting circuit protects the input supply voltage from large current load. The current limit can be set with an external resistor. The AOZ1360 provides thermal protection function that limits excessive power dissipation. The device employs internal soft-start circuitry to control in-rush current due to highly capacitive loads associated with hot-plug events. It features low quiescent current of 220 µA and the supply current reduces to less than 1 µA at shutdown.

The AOZ1360 is available in either an SO-8 or a DFN-10 4 mm x 4 mm package which can operate over a -40°C to +85°C temperature range.

Features

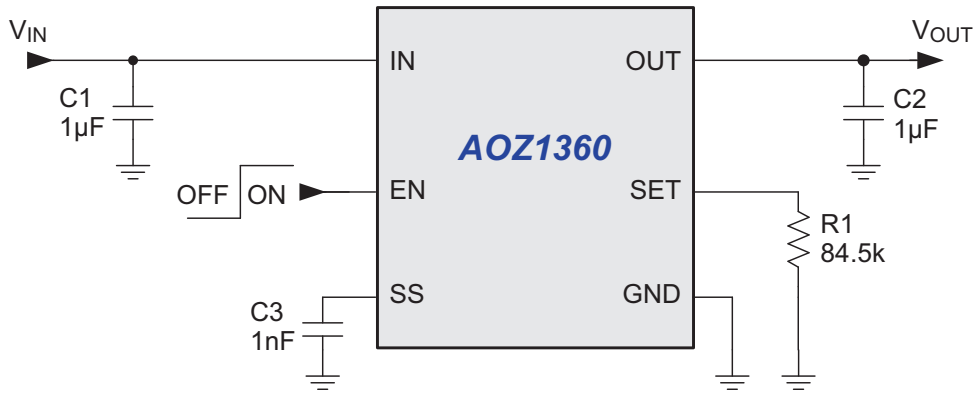
- 35mΩ maximum on resistance
- Programmable current limit
- 5.5V to 28V operating input voltage
- Low quiescent current
- Under-voltage lockout
- Thermal shutdown protection
- 2.5kV ESD rating
- Available in SO-8 or DFN-10 package

Applications

- Notebook PCs
- Hot swap supplies

Green Product

Typical Application

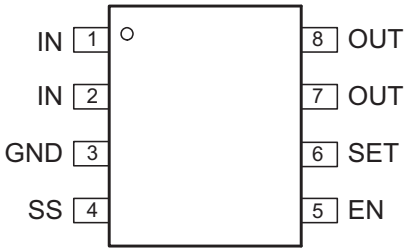


Ordering Information

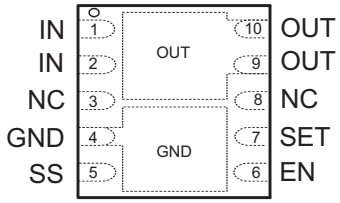
Part Number	Package	Temperature Range	Environmental
AOZ1360AIL	SO-8	-40 °C to +85 °C	Green Product
AOZ1360DIL	DFN-10 4x4		

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration



SO-8
(Top View)



DFN-10
(Top View)

Pin Description

Pin Name	Pin Number		Pin Function
	SO-8	DFN 4x4 10L	
IN	1, 2	1, 2	P-channel MOSFET source. Connect a 1 µF capacitor from IN to GND.
GND	3	4	Ground.
SS	4	5	Soft-Start Pin. Connect a capacitor from SS to GND to set the soft-start time. Connect SS to IN to set to the default soft-start time of 100us.
EN	5	6	Enable Input.
SET	6	7	Current Limit Set Pin. Connect a resistor from SET to GND to set the switch current limit.
NC		3, 8	No Connect
OUT	7, 8	9, 10	P-channel MOSFET Drain. Connect a capacitor with 0.1 µF or above from OUT to GND.

Functional Block Diagram

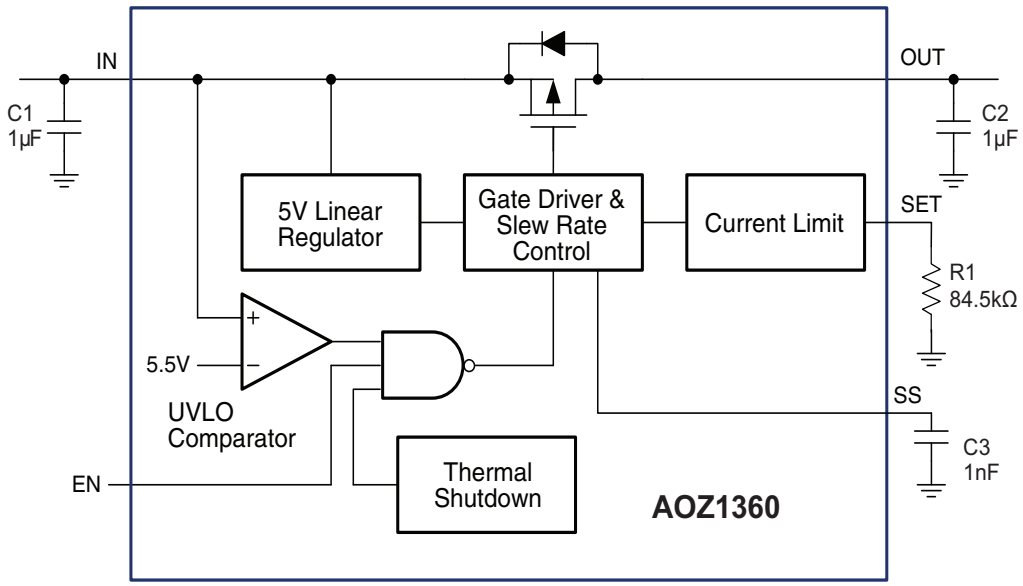


Figure 1. Functional Block Diagram

Timing Diagram

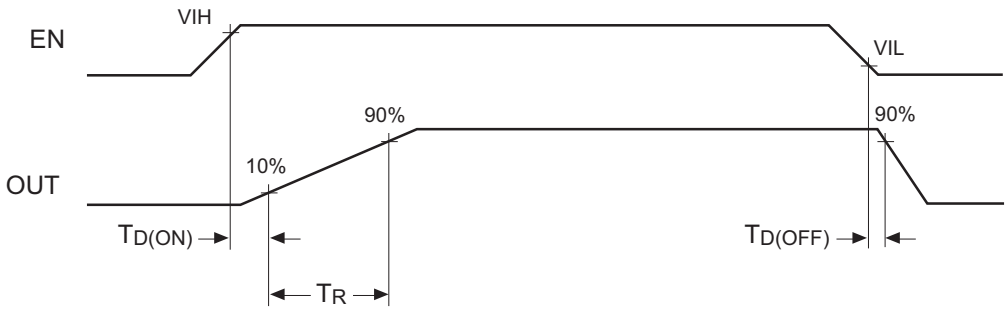


Figure 2. AOZ1360 Timing Diagram

Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings may damage the device.

Parameter	Rating
IN to GND	-0.3 V to +30 V
EN, OUT to GND	-0.3 V to V_{IN} + 0.3 V
SS, SET	-0.3 V to +6 V
Maximum Junction Temperature (T_J)	+150 °C
ESD Rating (Human Body Model)	2.5 kV

Recommended Operating Conditions

The device is not guaranteed to operate beyond the maximum Recommended Operating Conditions.

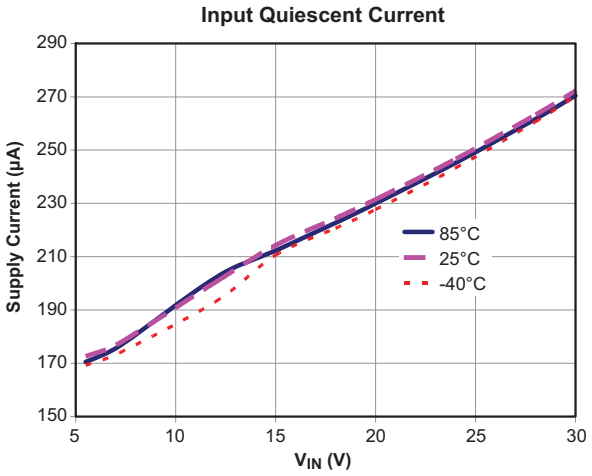
Parameter	Rating
Junction Temperature (T_J)	-40 °C to +125 °C
Thermal Resistance SO-8 (Θ_{JA}) DFN-10 (Θ_{JA})	 82 °C/W 63 °C/W

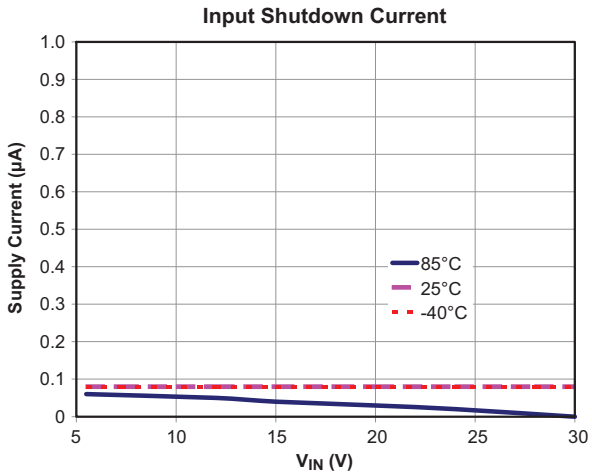
Electrical Characteristics

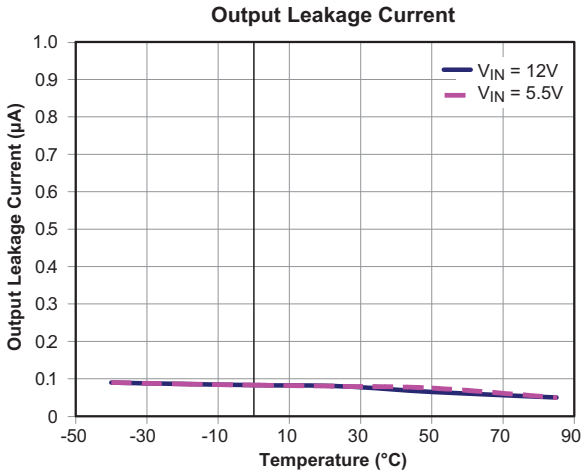
V_{IN} = 12V, T_A = 25°C unless otherwise stated.

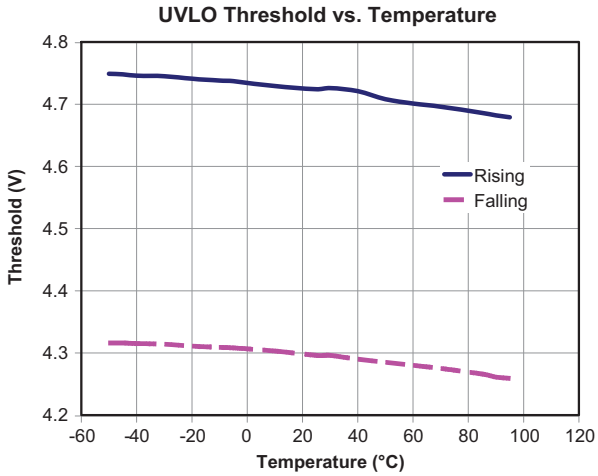
Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
V_{IN}	Input Supply Voltage		5.5		28	V
V_{UVLO}	Undervoltage Lockout Threshold	IN rising		4.9	5.4	V
V_{UVHYS}	Undervoltage Lockout Hysteresis			400		mV
I_{IN_ON}	Input Quiescent Current	EN = IN, no load		220	400	µA
I_{IN_OFF}	Input Shutdown Current	EN = GND, no load			1	µA
I_{LEAK}	Output Leakage Current	EN = GND, no load			1	µA
$R_{DS(ON)}$	Switch On Resistance	AOZ1360AI V_{IN} = 12 V		22	35	mΩ
$R_{DS(ON)}$	Switch On Resistance	AOZ1360AI V_{IN} = 5.5 V		33	43	mΩ
I_{LIM}	Current Limit	R_{SET} = 84.5 kΩ	2	2.7	3.4	A
V_{EN_L}	Enable Input Low Voltage				0.8	V
V_{EN_H}	Enable Input High Voltage		2.0			V
V_{EN_HYS}	Enable Input Hysteresis			100		mV
I_{EN_BIAS}	Enable Input Bias Current				1	µA
Td_on	Turn-On Delay Time EN_50% to OUT_10%	R_L = 120 Ω, C_L = 1 µF, SS = Floated		220		µs
t_{ON}	Turn-On Rise Time OUT_10% to 90%	R_L = 120 Ω, C_L = 1 µF, SS = Floated		280		µs
		R_L = 120 Ω, C_L = 1 µF, C_{SS} = 1 nF		360		
t_{OFF}	Turn-Off Fall Time	R_L = 120 Ω, C_L = 1 µF, SS = Floated		280		µs
T_{SD}	Thermal Shutdown Threshold			130		°C
T_{SD_HYS}	Thermal Shutdown Hysteresis			30		°C

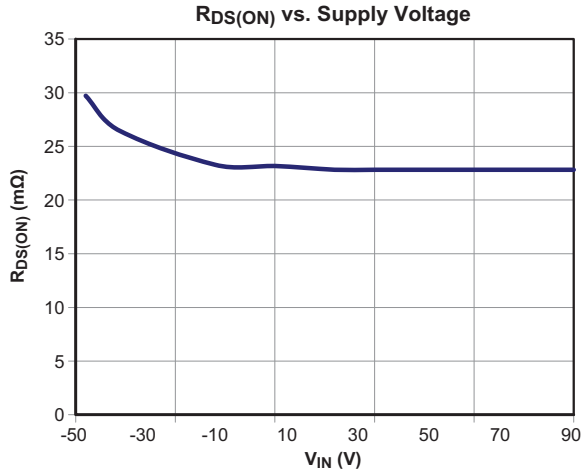
Typical Performance Characteristics

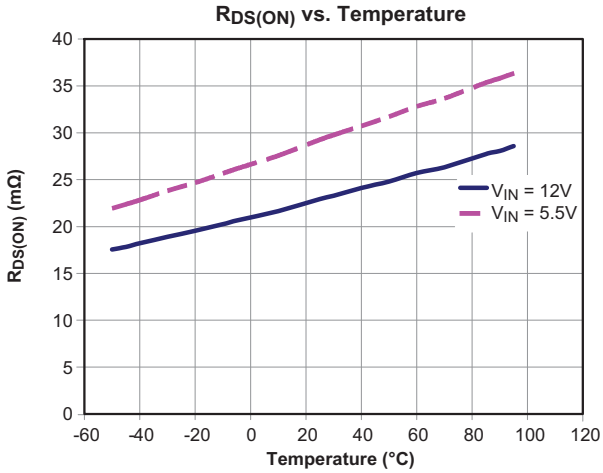






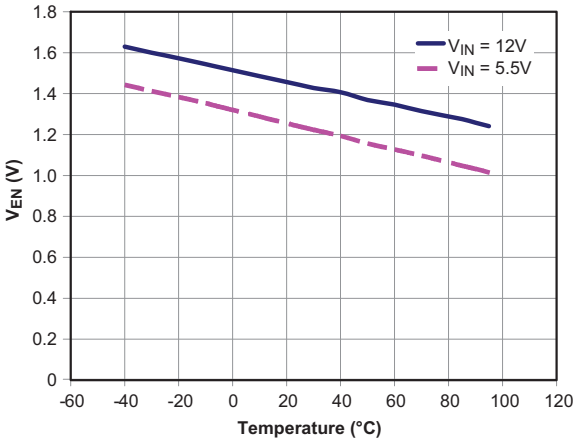




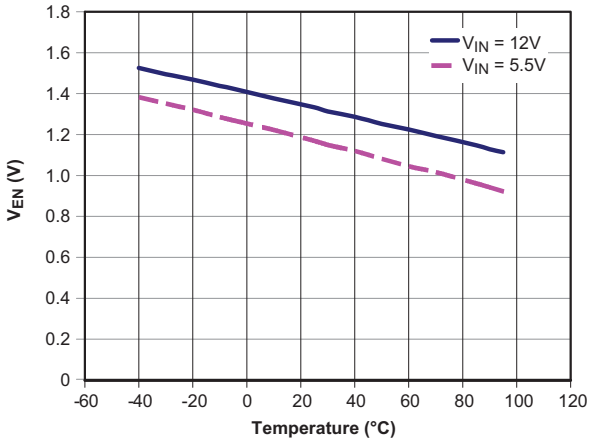


Typical Performance Characteristics *(Continued)*

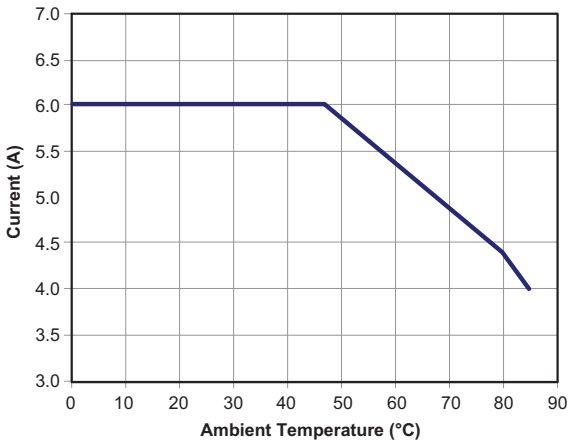
Enable Input Threshold (Rising) vs. Temperature



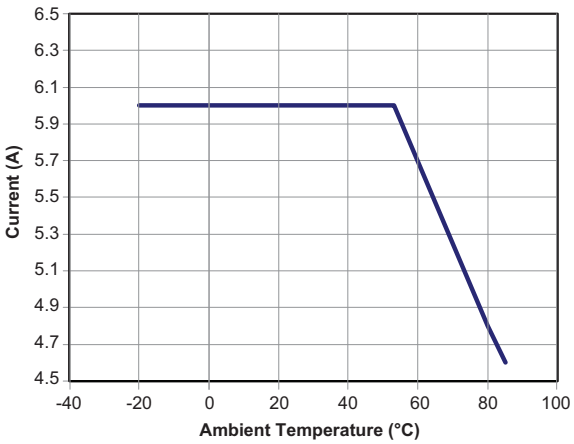
Enable Input Threshold (Falling) vs. Temperature



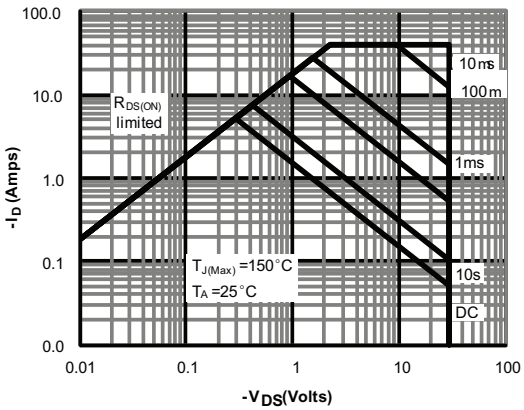
Current Derating Curve for SO8



Current Derating Curve for DFN-10 4x4

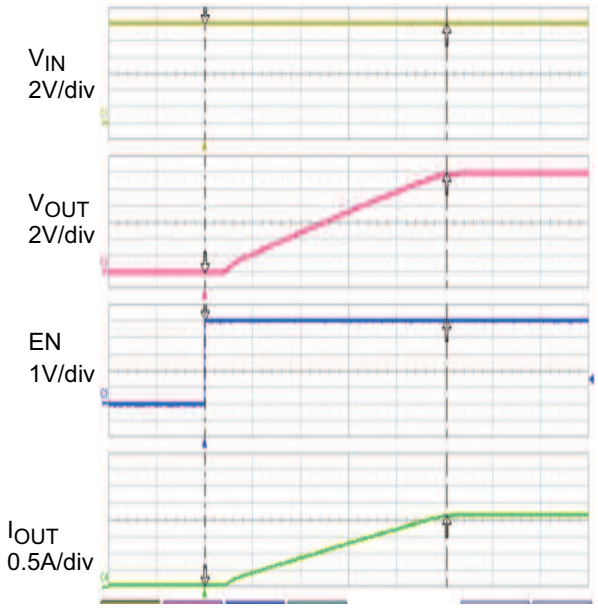


Internal Power MOSFET SOA

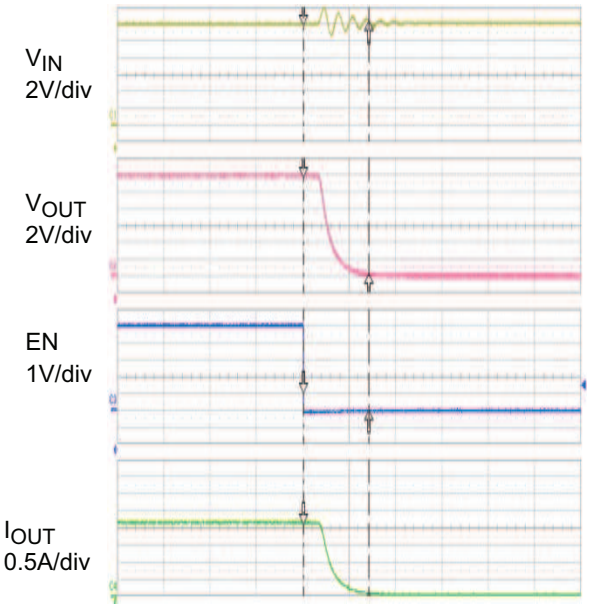


Typical Performance Characteristics *(Continued)*

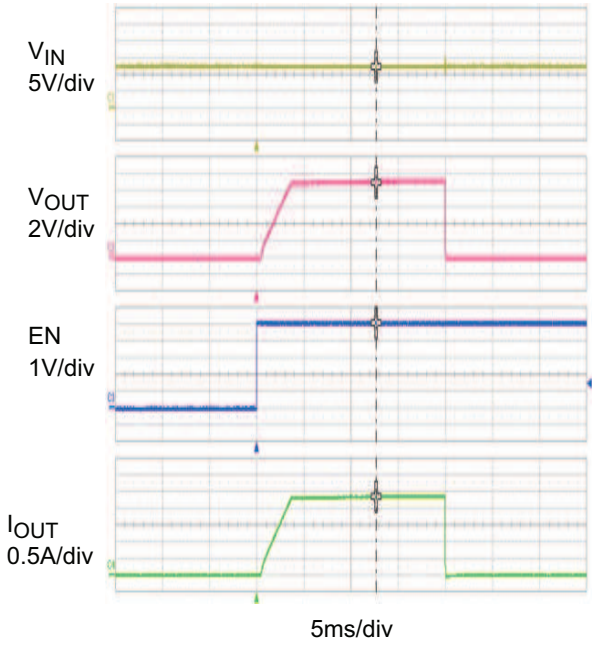
Turn-On
(V_{IN} = 12V, R = 5.6Ω)



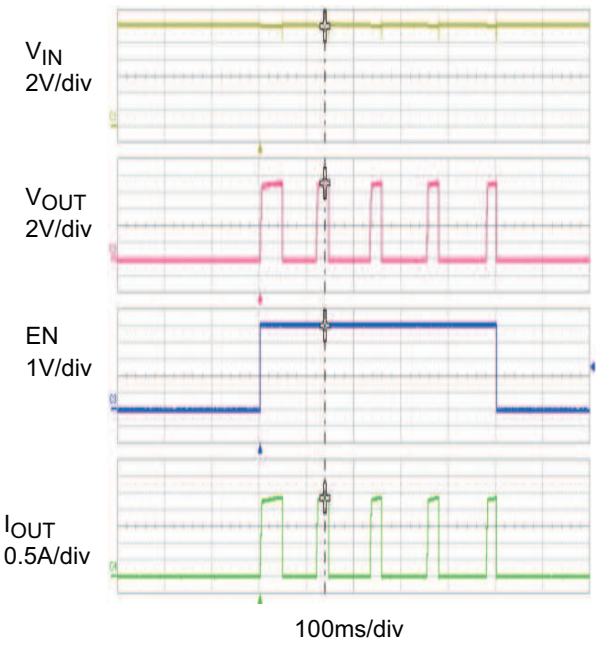
Turn-Off
(V_{IN} = 12V, R = 5.6Ω)



Current Limit
(V_{IN} = 12V, R = 3.6Ω)



Over Temperature
(V_{IN} = 12V, R = 3.6Ω)



Detailed Description

Introduction

The AOZ1360 is a 35 mΩ P-channel high-side load switch with adjustable soft-start slew-rate control, programmable current limit and thermal shutdown. It operates with an input voltage range from 5.5 V to 28 V.

Enable

The EN pin is the On/Off control for the output switch. It is an active-high input. The EN pin is active after V_{IN} is above the UVLO threshold of 4.9 V. Conversely, the EN pin will be deactivated if the V_{IN} falls below the UVLO of 2.0V. The EN pin must be driven to a logic high or logic low state to guarantee operation. While disabled, the AOZ1360 only draws approximately 1 µA supply current. The EN is a high impedance input with an ESD protection diode to ground and should not be forced below ground. This input level is compatible with most microcontroller outputs and other logic families.

Under-Voltage Lockout (UVLO)

The under-voltage lockout (UVLO) circuit of the AOZ1360 monitors the input voltage and prevents the output MOSFET from turning on until V_{IN} exceeds 4.9 V.

Adjustable Soft-Start Slew-Rate Control

When the EN pin is high, the slew rate control circuitry applies voltage on the gate of the PMOS switch in a manner such that the output voltage and current is ramped up linearly until it reaches the steady-state load current level. The slew rate can be adjusted by an external capacitor connected between the SS pin and ground.

The slew rate rise time, Ton, can be set using the following equation:

$$Ton = \frac{Css \times V_{IN}}{30\mu A}$$

Programmable Current Limit

The current limit is programmed by an external resistor connected between the SET pin and ground. This sets a reference voltage to the current limit error amplifier that compares it to a sensed voltage that is generated by passing a small portion of the load current through an internal amplifier. When the sensed load current exceeds the set current limit, the load current is then clamped at the set limit and the Vout drops to whatever voltage is necessary to clamp the load current. The AOZ1360 will stay in this condition until the load current no longer exceeds the current limit or if the thermal shutdown protection is engaged.

Thermal-Shutdown Protection

During current limit or short circuit conditions, the PMOS resistance is increased to clamp the load current. This increases the power dissipation in the chip causing the die temperature to rise. When the die temperature reaches 130 °C the thermal shutdown circuitry will shutdown the device. There is a 30 °C hysteresis after which the device will turn back on and go through soft start. The thermal shutdown will cycle repeatedly until the short circuit condition is resolved or the enable pin is pulled LOW externally.

Application Information

Input Capacitor Selection

The input capacitor prevents large voltage transients from appearing at the input and provides the instantaneous current needed each time the switch turns on. The input capacitor also limits input voltage drop and prevents high-frequency noise on the power line from passing through the output of the power side. The choice of input capacitor is based on its ripple current and voltage ratings rather than the actual capacitance value. The input capacitor should be located as close to VIN as possible. A 1 µF ceramic cap is recommended. However, higher capacitor values will further reduce the voltage drop at the input.

Output Capacitor Selection

The output capacitor acts in a similar way. A small 0.1 µF capacitor prevents high-frequency noise from going into the system. Also, the output capacitor has to supply enough current for any large load that may occur during system transients. This bulk capacitor must be large enough to supply fast transient load in order to prevent the output from dropping.

Current Limit Setting

The current limit is set by an external resistor connected to the SET pin. Refer to Figure 3 for current limit settings.

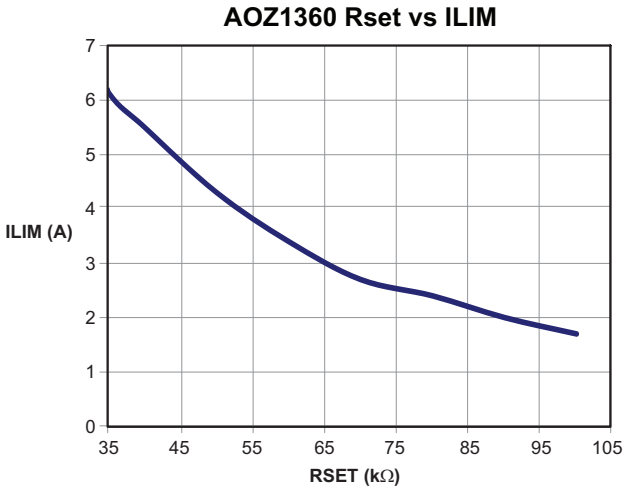


Figure 3

Slew Rate Setting

Slew rate is set by changing the capacitor value on the SS pin of the device. A capacitor connected between the SS pin and ground will reduce the output slew-rate. The capacitive range is 0.001 µF to 0.1 µF. Refer to Figure 4.

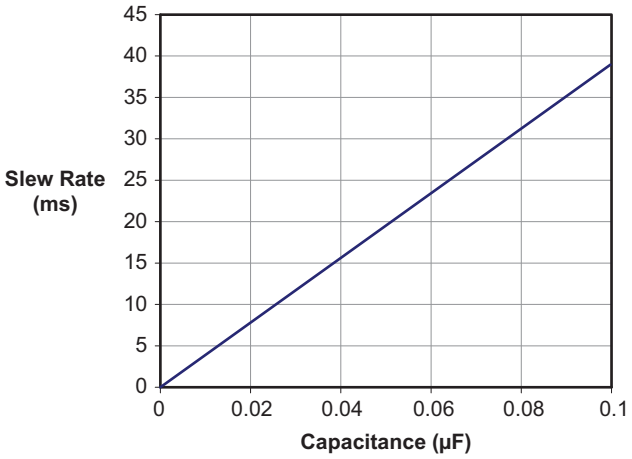


Figure 4. Output Slew Rate Adjustment vs. Capacitance

Power Dissipation Calculation

Calculate the power dissipation for normal load condition using the following equation:

$$P_D = R_{ON} \times (I_{OUT})^2$$

The worst case power dissipation occurs when the load current hits the current limit due to over-current or short circuit faults. The power dissipation under these conditions can be calculated using the following equation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{LIMIT}$$

Layout Guidelines

Proper PCB layout is important for improving the thermal and overall performance of the AOZ1360. To optimize the switch response time for outputting short-circuit conditions, keep all traces as short as possible. This will also reduce the effect of unwanted parasitic inductance.

Place the input and output bypass capacitors as close as possible to the IN and OUT pins. The input and output PCB traces should be as wide as possible for the given PCB space. Use a ground plane to enhance the power dissipation capability of the device.

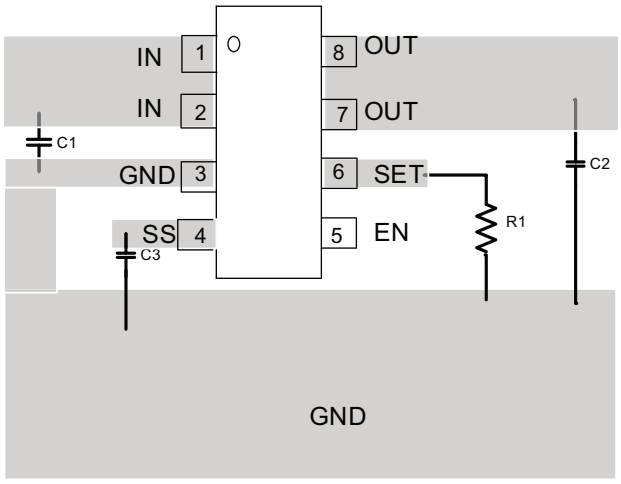


Figure 5. AOZ1360AI (SO-8) Layout

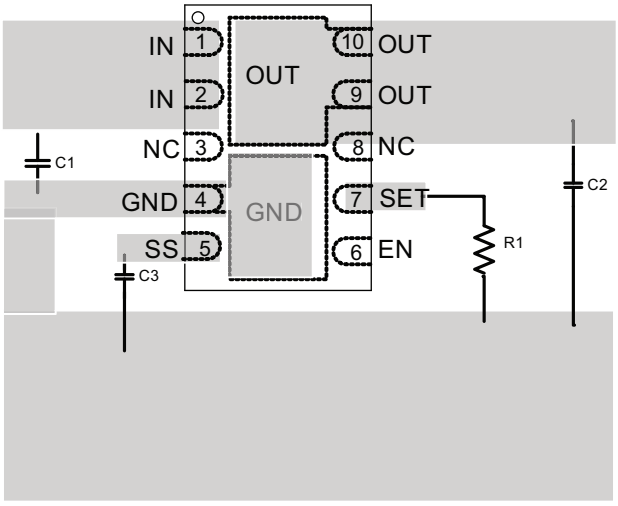
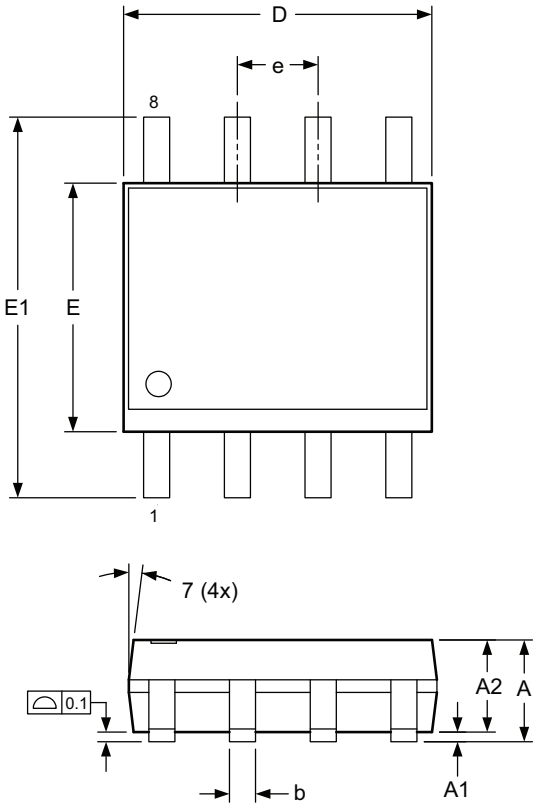
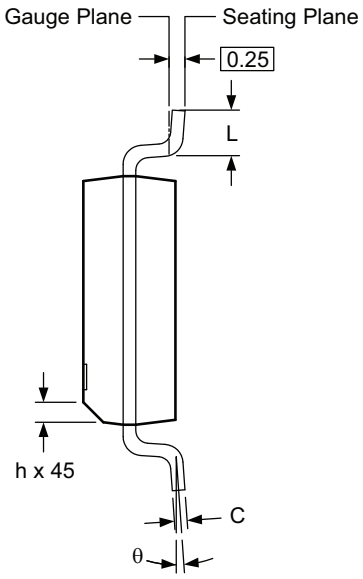


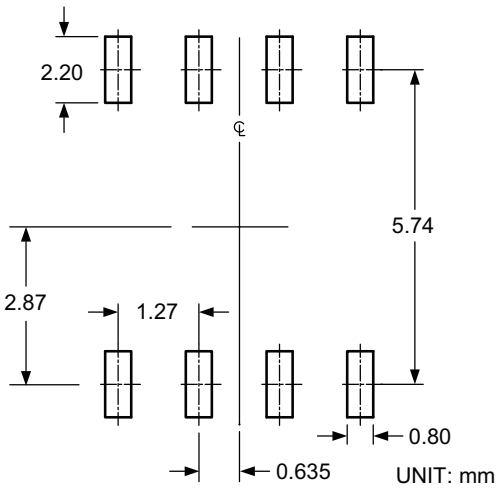
Figure 6. AOZ1360DI (DFN4x4 10L) Layout

Package Dimensions, SO-8L





RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	1.35	1.65	1.75
A1	0.10	—	0.25
A2	1.25	1.50	1.65
b	0.31	—	0.51
c	0.17	—	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
e	1.27 BSC		
E1	5.80	6.00	6.20
h	0.25	—	0.50
L	0.40	—	1.27
θ	0°	—	8°

Dimensions in inches

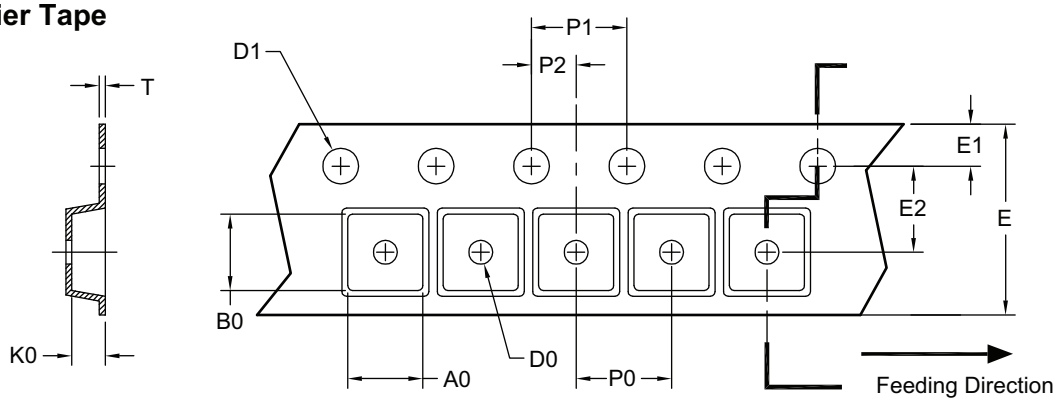
Symbols	Min.	Nom.	Max.
A	0.053	0.065	0.069
A1	0.004	—	0.010
A2	0.049	0.059	0.065
b	0.012	—	0.020
c	0.007	—	0.010
D	0.189	0.193	0.197
E	0.150	0.154	0.157
e	0.050 BSC		
E1	0.228	0.236	0.244
h	0.010	—	0.020
L	0.016	—	0.050
θ	0°	—	8°

Notes:

1. All dimensions are in millimeters.
2. Dimensions are inclusive of plating
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

Tape and Reel Dimensions, SO-8

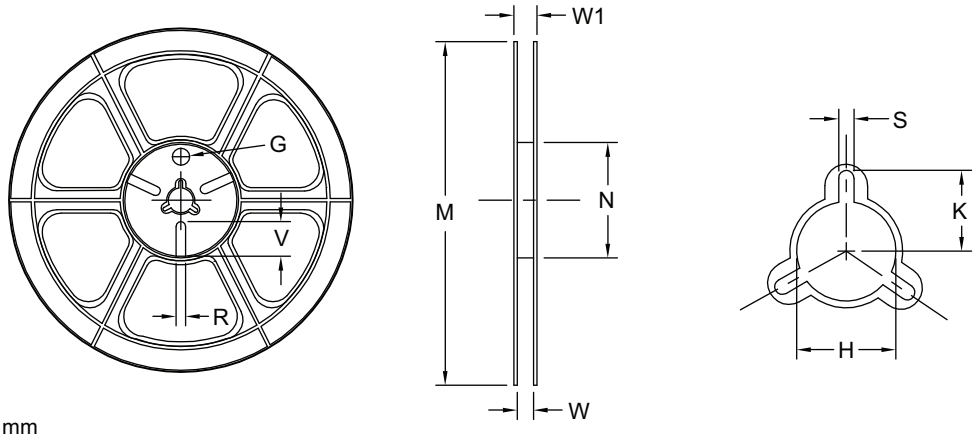
Carrier Tape



UNIT: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SO-8 (12mm)	6.40 ±0.10	5.20 ±0.10	2.10 ±0.10	1.60 ±0.10	1.50 ±0.10	12.00 ±0.10	1.75 ±0.10	5.50 ±0.10	8.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.25 ±0.10

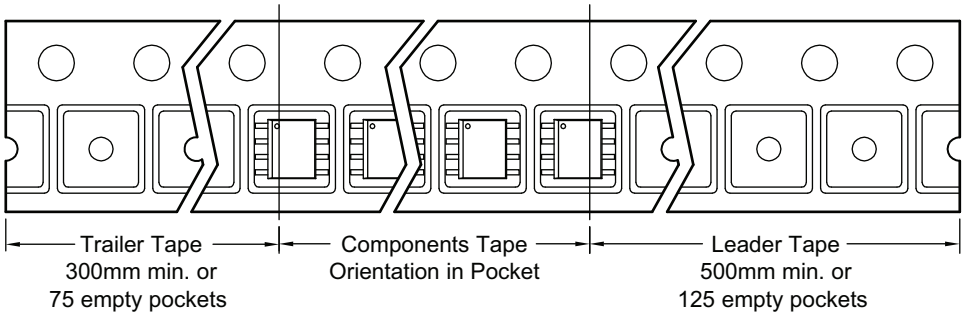
Reel



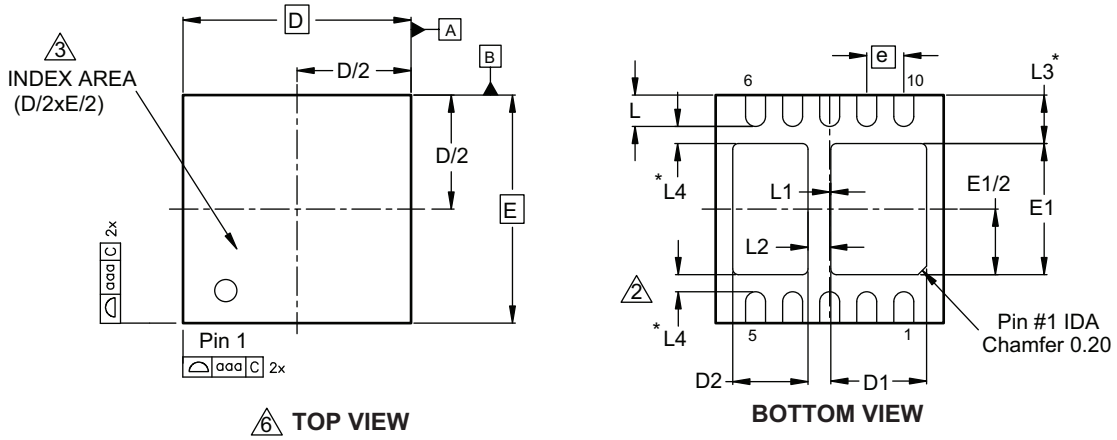
UNIT: mm

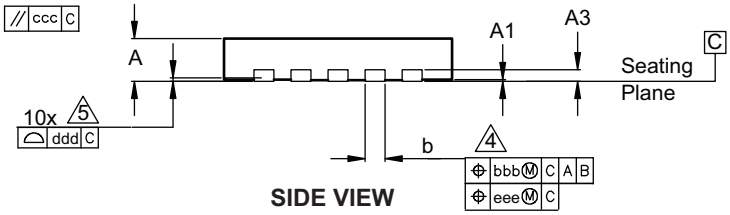
Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
12mm	ø330	ø330.00 ±0.50	ø97.00 ±0.10	13.00 ±0.30	17.40 ±1.00	ø13.00 +0.50/-0.20	10.60	2.00 ±0.50	—	—	—

Leader/Trailer and Orientation

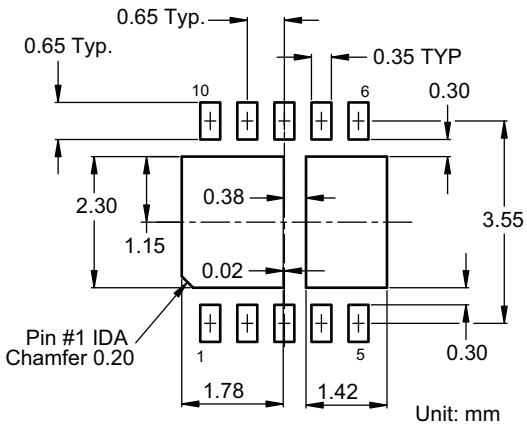


Package Dimensions, DFN-10L, 4x4





RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.30	0.35	0.40
D	3.95	4.00	4.05
D1	1.58	1.68	1.78
D2	1.22	1.32	1.42
E	3.95	4.00	4.05
E1	2.20	2.30	2.40
e		0.65 BSC	
L	0.50	0.55	0.60
L1	—	0.02	0.12
L2	0.28	0.38	0.48
L3		0.85 REF	
L4		0.30 REF	
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.08	
eee		0.05	

Dimensions in inches

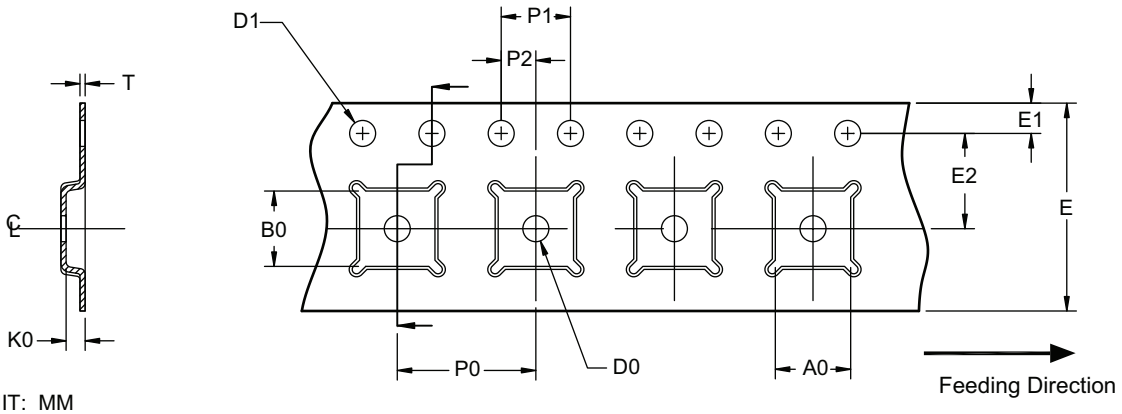
Symbols	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3		0.008 REF	
b	0.012	0.014	0.016
D	0.156	0.157	0.159
D1	0.062	0.066	0.070
D2	0.048	0.052	0.056
E	0.156	0.157	0.159
E1	0.087	0.091	0.094
e		0.026 BSC	
L	0.020	0.022	0.024
L1	—	0.001	0.005
L2	0.011	0.015	0.019
L3		0.033 REF.	
L4		0.012 REF	
aaa		0.006	
bbb		0.004	
ccc		0.004	
ddd		0.003	
eee		0.002	

Notes:

1. All dimensions are in millimeters.
2. The dimensions with * are just for reference.
3. The location of the terminal #1 identifier and terminal numbering convention conforms to JEDEC publication 95 SPP-002.
4. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, then dimension b should not be measured in that radius area.
5. Coplanarity applies to the terminals and all other bottom surface metallization.
6. Drawings shown are for illustration only.

Tape and Reel Dimensions, DFN-10L, 4x4

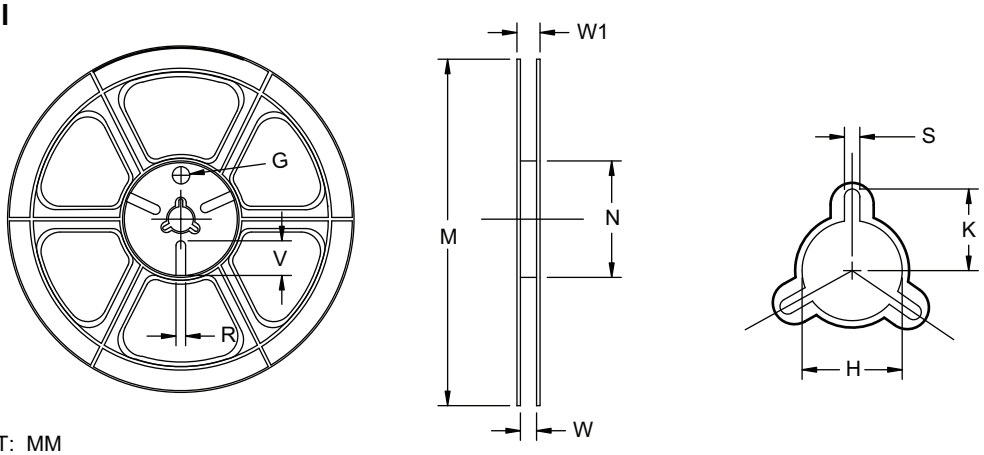
Carrier Tape



UNIT: MM

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DFN 4x4 (12mm)	4.35 ±0.10	4.35 ±0.10	1.10 ±0.10	1.50 Min.	1.50 +0.1/-0.0	12.0 ±0.3	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

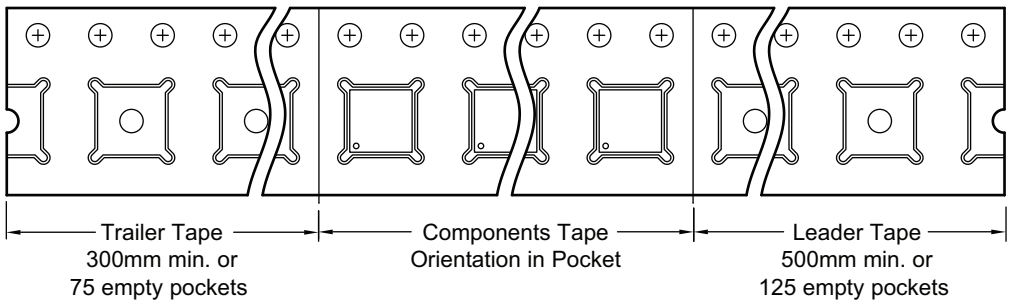
Reel



UNIT: MM

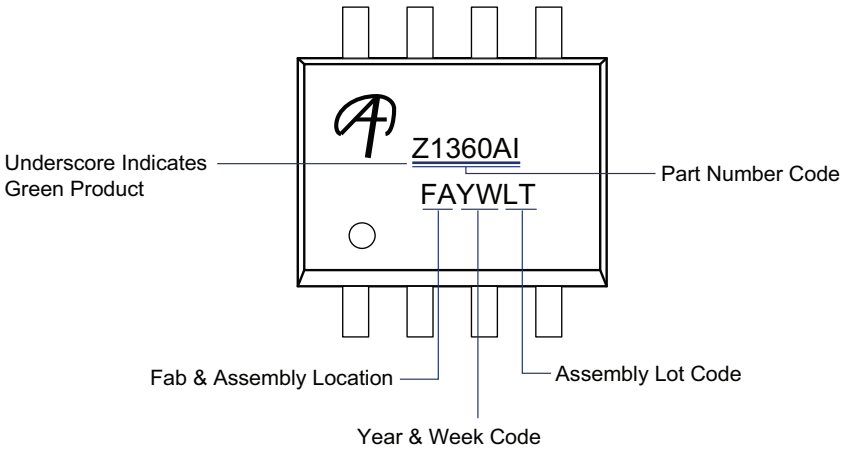
Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330.0 ±2.0	ø79.0 ±1.0	12.4 +2.0/-0.0	17.0 +2.6/-0.0	ø13.0 ±0.5	10.5 ±0.2	2.0 ±0.5	—	—	—

Leader/Trailer and Orientation

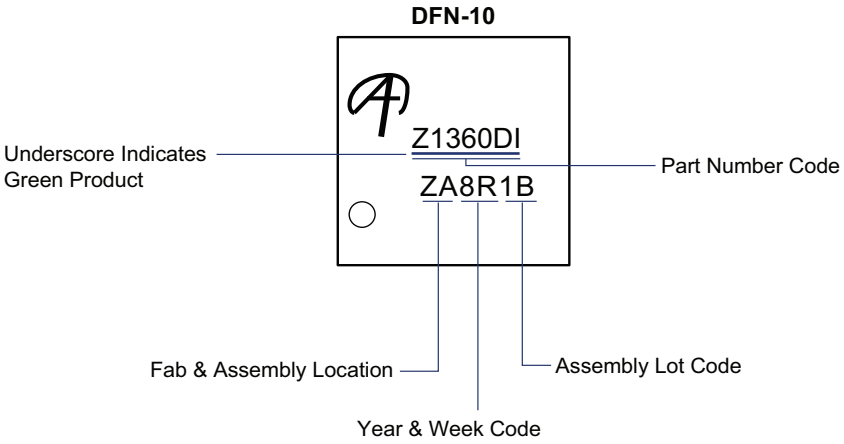


Part Marking

SO-8



DFN-10



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