DataSheet

, AS1151
Quad LVDS Receivers

1 General Description

The AS1150 and AS1151 are quad flow-through LVDS (low-voltage differential signaling) receivers which accept LVDS differential inputs and convert them to LVCMOS outputs. The receivers are perfect for low-power low-noise applications requiring high signaling rates and reduced EMI emissions.

The devices are guaranteed to receive data at speeds up to 500Mbps (250MHz) over controlled impedance media of approximately 100Ω. Supported transmission media are PCB traces, backplanes, and cables.

The AS1150 uses high impedance inputs and requires an external termination resistor when used in a point-to-point connection. The AS1151 features integrated parallel termination resistors (nominally 107Ω), which eliminate the requirement for discrete termination resistors, and reduce stub lengths.

The integrated failsafe feature sets the output high if the inputs are open, undriven and terminated, or undriven and shorted. Enable inputs (EN and ENn – internally pulled down to GND) control the high-impedance output and are common to all four receivers. All inputs conform to the *ANSI TIA/EIA- 644* LVDS standards. Flow-through pinout simplifies PC board layout and reduces crosstalk by separating the LVDS inputs and LVCMOS outputs.

The devices are available in a 16-pin TSSOP package.

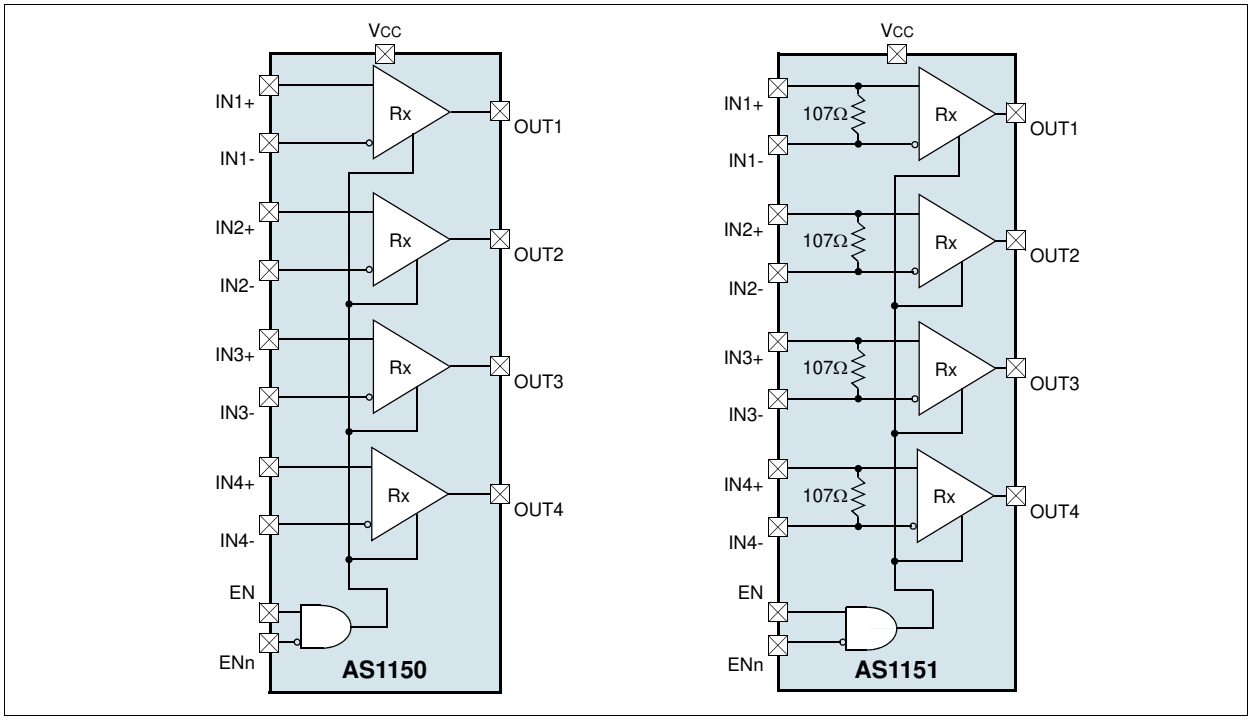
2 Key Features

- Flow-Through Pinout
- Guaranteed 500Mbps Data Rate
- 300ps Pulse Skew (Max)
- Conform to *ANSI TIA/EIA-644* LVDS Standards
- Single +3.3V Supply
- Operating Temperature Range: -40 to +85ºC
- Failsafe Circuit
- Integrated Termination (AS1151)
- 16-pin TSSOP Package

3 Applications

The devices are ideal for digital copiers, laser printers, cellular phone base stations, add/drop muxes, digital cross-connects, dslams, network switches/routers, backplane interconnect, clock distribution computers, intelligent instruments, controllers, critical microprocessors and microcontrollers, power monitoring, and portable/battery-powered equipment.

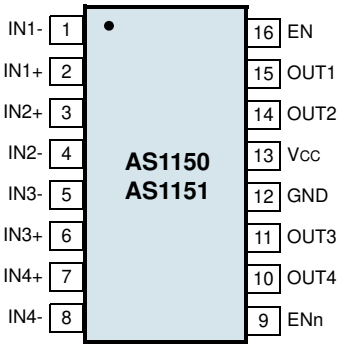
Figure 1. Block Diagrams



4 Pinout

Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Description
1	IN1-	**Inverting Differential Receiver Input**
2	IN1+	**Noninverting Differential Receiver Input**
3	IN2+	**Noninverting Differential Receiver Input**
4	IN2-	**Inverting Differential Receiver Input**
5	IN3-	**Inverting Differential Receiver Input**
6	IN3+	**Noninverting Differential Receiver Input**
7	IN4+	**Noninverting Differential Receiver Input**
8	IN4-	**Inverting Differential Receiver Input**
9	ENn	**Receiver Enable Input**. Internally pulled down to GND. When EN = high and ENn = low or open, the receiver outputs are active. For other combinations of EN and ENn, the outputs are disabled and in high impedance.
10	OUT4	**LVCMOS/LVTTL Receiver Output**
11	OUT3	**LVCMOS/LVTTL Receiver Output**
12	GND	**Ground**
13	VCC	**Power-Supply Input**. Bypass VCC to GND with 0.1µF and 0.001µF ceramic capacitors.
14	OUT2	**LVCMOS/LVTTL Receiver Output**
15	OUT1	**LVCMOS/LVTTL Receiver Output**
16	EN	**Receiver Enable Input**. Internally pulled down to GND. When EN = high and ENn = low or open, the receiver outputs are active. For other combinations of EN and ENn, the outputs are disabled and in high impedance.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
VCC to GND	-0.3	+5.0	V	
IN*x*+, IN*x*- to GND	-0.3	+5.0	V	
EN, ENn to GND	-0.3	VCC + 0.3	V	
OUT*x* to GND	-0.3	VCC + 0.3	V	
Continuous Power Dissipation (TAMB = +70ºC)		750	mW	Derate 9.4mW/°C Above +70°C
Storage Temperature Range	-65	+150	ºC	
Maximum Junction Temperature		+150	ºC	
Operating Temperature Range	-40	+85	ºC	
ESD Protection	-4	+4	kV	Human Body Model, IN*x*+, IN*x*-
Package Body Temperature		260	ºC	The reflow peak soldering temperature (body temperature) specified is in compliance with *IPC/JEDEC J-STD-020C "Moisture/ Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices"*.

6 Electrical Characteristics

DC Electrical Characteristics

V_{CC} = +3.0 to +3.6V, Differential Input Voltage $|V_{ID}|$ = 0.1 to 1.0V, Common-Mode Voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$, T_{AMB} = -40 to +85ºC. Typical values are at V_{CC} = +3.3V, T_{AMB} = +25ºC (unless otherwise specified).[1]

Table 3. DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
LVDS Inputs (IN*x*+, IN*x*-)							
Differential Input High Threshold	V_{TH}					100	mV
Differential Input Low Threshold	V_{TL}			-100			mV
Input Current (AS1150)	I_{INx+}, I_{INx-}	0.1V ≤ $\|V_{ID}\|$ ≤ 0.6V		-20		20	µA
		0.6V ≤ $\|V_{ID}\|$ ≤ 1.0V		-25		25	µA
Power-Off Input Current (AS1150)	I_{INOFF}	0.1V ≤ $\|V_{ID}\|$ ≤ 0.6V, V_{CC} = 0		-20		20	µA
		0.6V ≤ $\|V_{ID}\|$ ≤ 1.0V, V_{CC} = 0		-25		25	µA
Input Resistor 1 (AS1150)	R_{IN1}	V_{CC} = 3.6V or 0, Figure 16 on page 9 [1]		35			kΩ
Input Resistor 2 (AS1150)	R_{IN2}	V_{CC} = 3.6V or 0, Figure 16 on page 9 [1]		132			kΩ
Common Mode Input Resistance	R_{INCM}	AS1151: Input = 0		150			kΩ
Differential Input Resistance	R_{DIFF}	AS1151: V_{CC} = 3.6V or 0, Figure 16 on page 9		90	107	132	Ω
LVCMOS/LVTTL Outputs (OUT*x*)							
Output High Voltage (Table 5)	V_{OH}	I_{OH} = -4.0mA (AS1150)	Open, undriven short, or undriven 100Ω parallel termination	2.7	3.2		V
			V_{ID} = +100mV	2.7	3.2		
		I_{OH} = -4.0mA (AS1151)	Open or Undriven Short	2.7	3.2		
			V_{ID} = +100mV	2.7	3.2		
Output Low Voltage	V_{OL}	I_{OL} = +4.0mA, V_{ID} = -100mV			0.1	0.25	V
Output Short-Circuit Current [2]	I_{OS}	Enabled, V_{ID} = 0.1V, V_{OUTx} = 0		15		160	mA
Output High-Impedance Current	I_{OZ}	Disabled, V_{OUTx} = 0 or V_{CC}		-10		10	µA
Logic Inputs (EN, ENn)							
Input High Voltage	V_{IH}			2.0		V_{CC}	V
Input Low Voltage	V_{IL}			0		0.8	V
Input Current	I_{IN}	V_{INx} = V_{CC} or 0		-15		15	µA
Supply							
Supply Current	I_{CC}	Enabled, Inputs Open			5	11	mA
		average value, $\|V_{ID}\|$ = 200mV			8	15	
Disabled Supply Current	I_{CCZ}	Disabled, Inputs Open			300	500	µA

Notes:

1. Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except V_{TH}, V_{TL}, and V_{ID}.
2. Short only one output at a time. Do not exceed the absolute maximum junction temperature specification.

AC Electrical Characteristics

V_{CC} = +3.0 to +3.6V, C_{LOAD} = 15pF, Differential Input Voltage $|V_{ID}|$ = 0.2 to 1.0V, Common-Mode Voltage V_{CM} = $|V_{ID}/2|$ to 2.4V -$|V_{ID}/2|$, Input Rise and Fall Time = 1ns (20 to 80%), Input Frequency = 100MHz, T_{AMB} = -40 to +85ºC. Typical values are at V_{CC} = +3.3V, V_{CM} = 1.2V, $|V_{ID}|$ = 0.2V, T_{AMB} = +25ºC (unless otherwise specified). [1, 2]

Table 4. AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Differential Propagation Delay High-to-Low	t_{PHLD}	Figure 18 on page 11 and Figure 19 on page 12	1.6	2.0	3.1	ns
Differential Propagation Delay Low-to-High	t_{PLHD}	Figure 18 on page 11 and Figure 19 on page 12	1.6	2.0	3.1	ns
Differential Pulse Skew (t_{PHLD} - t_{PLHD}) [3]	t_{SKD1}	Figure 18 on page 11 and Figure 19 on page 12		140	300	ps
Differential Channel-to-Channel Skew [4]	t_{SKD2}	Figure 18 on page 11 and Figure 19 on page 12			400	ps
Differential Part-to-Part Skew [5]	t_{SKD3}	Figure 18 on page 11 and Figure 19 on page 12			0.8	ns
Differential Part-to-Part Skew [6]	t_{SKD4}	Figure 18 on page 11 and Figure 19 on page 12			1.5	ns
Rise Time	t_{TLH}	Figure 18 on page 11 and Figure 19 on page 12		0.5	1.0	ns
Fall Time	t_{THL}	Figure 18 on page 11 and Figure 19 on page 12		0.5	1.0	ns
Disable Time High-to-Z	t_{PHZ}	R_{LOAD} = 2kΩ, Figure 20 on page 12 and Figure 21 on page 12			14	ns
Disable Time Low-to-Z	t_{PLZ}	R_{LOAD} = 2kΩ, Figure 20 on page 12 and Figure 21 on page 12			14	ns
Enable Time Z-to-High	t_{PZH}	R_{LOAD} = 2kΩ, Figure 20 on page 12 and Figure 21 on page 12			70	ns
Enable Time Z-to-Low	t_{PZL}	R_{LOAD} = 2kΩ, Figure 20 on page 12 and Figure 21 on page 12			70	ns
Maximum Operating Frequency [7, 8]	f_{MAX}	All Channels Switching	250	300		MHz

Notes:

1. AC parameters are guaranteed by design and characterization.
2. C_L includes scope probe and test jig capacitance.
3. t_{SKD1} is the magnitude difference of differential propagation delays in a channel. t_{SKD1} = $|t_{PHLD} - t_{PLHD}|$.
4. t_{SKD2} is the magnitude difference of the t_{PLHD} or t_{PHLD} of one channel and the t_{PLHD} or t_{PHLD} of any other channel on the same device.
5. t_{SKD3} is the magnitude difference of any differential propagation delays between devices operating over rated conditions at the same V_{CC} and within 5ºC of each other.
6. t_{SKD4} is the magnitude difference of any differential propagation delays between devices operating over rated conditions.
7. f_{MAX} generator output conditions:
   a. Rise time = fall time = 1ns (0 to 100%)
   b. 50% duty cycle
   c. V_{OH} = +1.3V
   d. V_{OL} = +1.1V
8. Output criteria:
   a. Duty cycle = 60% to 40%
   b. V_{OL} = 0.4V (max)
   c. V_{OH} = 2.7V (min)
   d. Load = 15pF

7 Typical Operating Characteristics

V_{CC} = +3.3V, V_{CM} = +1.2V, $|V_{ID}|$ = 0.2V, C_{LOAD} = 15pF, T_{AMB} = +25ºC, unless otherwise noted.

Figure 3. Supply Current vs. Frequency

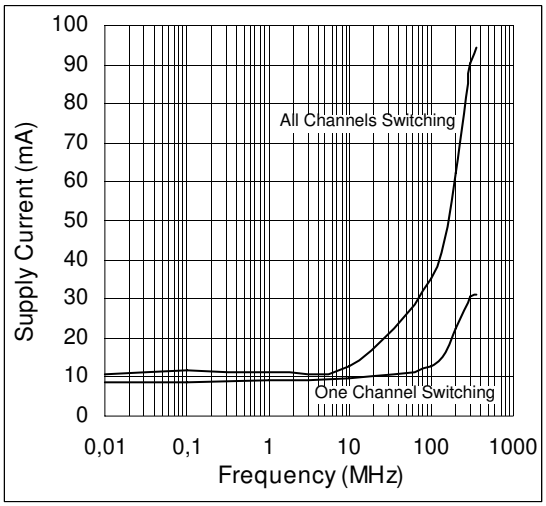


Figure 4. Supply Current vs. Temperature

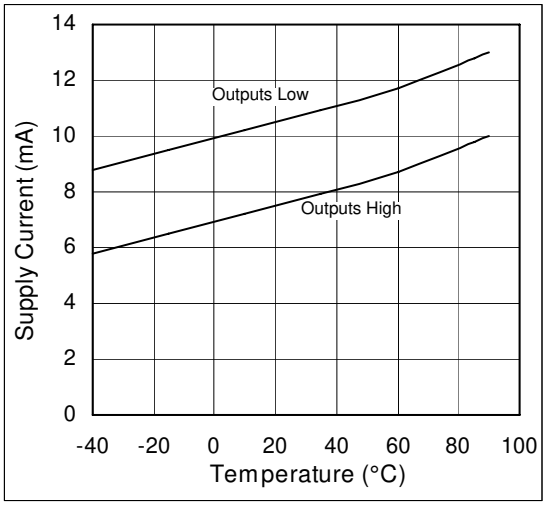


Figure 5. Diff. Threshold Voltage vs. V_{CC}

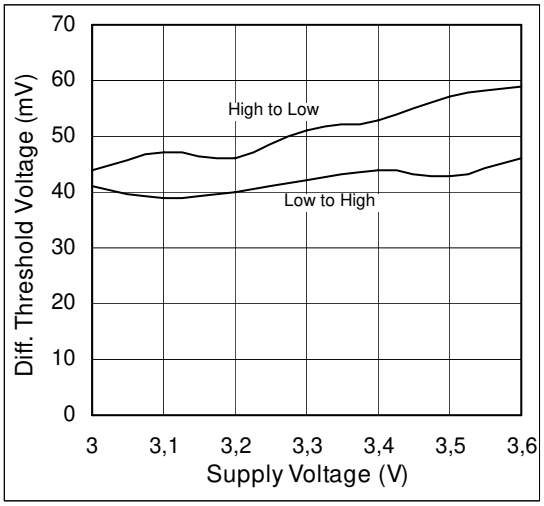


Figure 6. Output Short-Circuit Current vs. V_{CC}

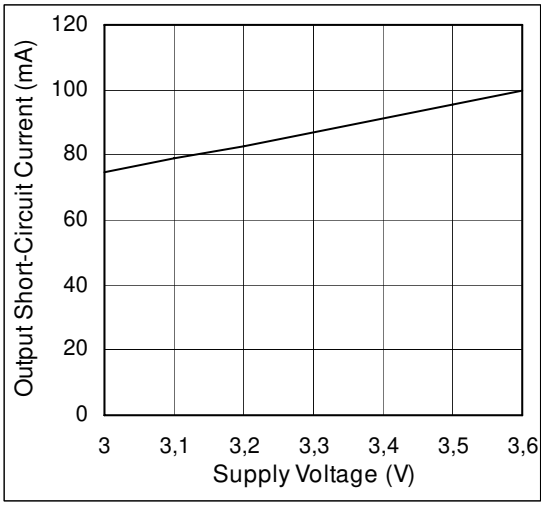


Figure 7. Output Low Voltage vs. V_{CC}

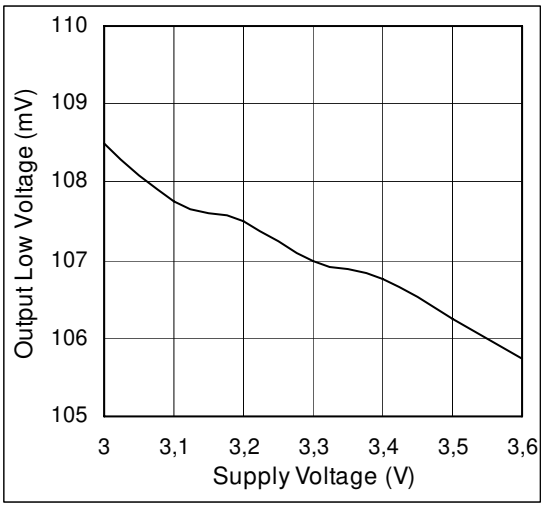


Figure 8. Output High Voltage vs. V_{CC}

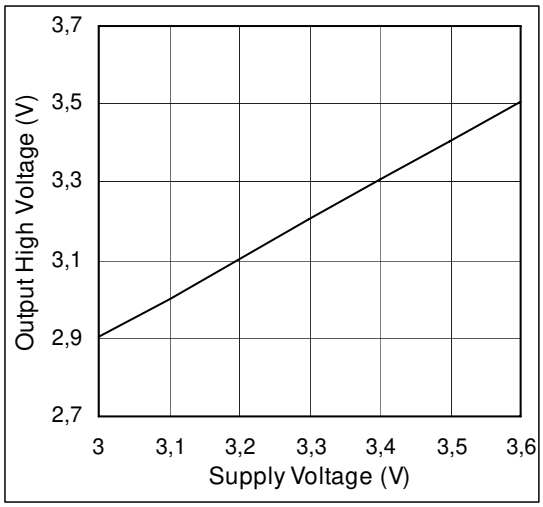


Figure 9. Differential Propagation Delay vs. VCC Temperature

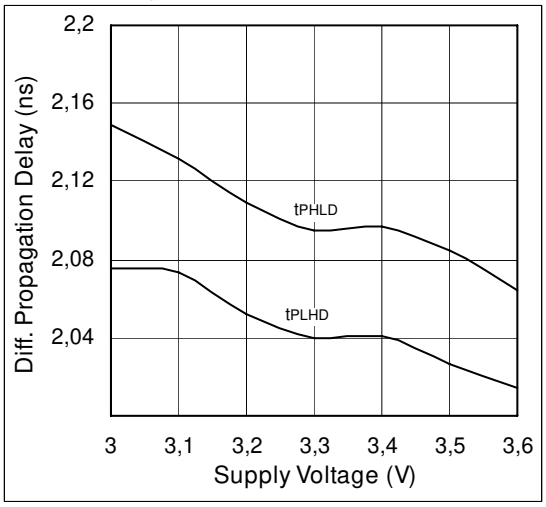


Figure 10. Differential Propagation Delay vs.

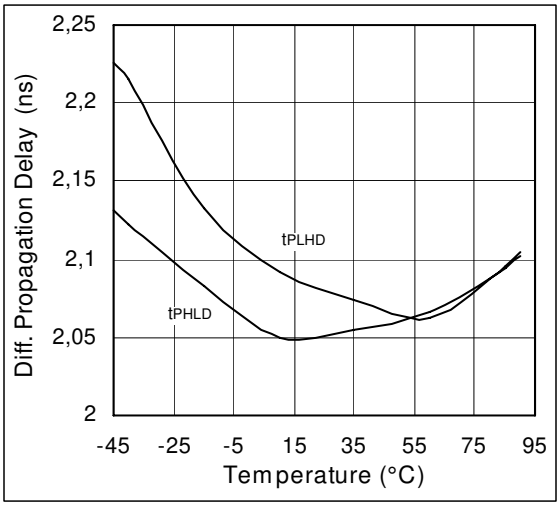


Figure 11. Differential Propagation Delay vs. VCM

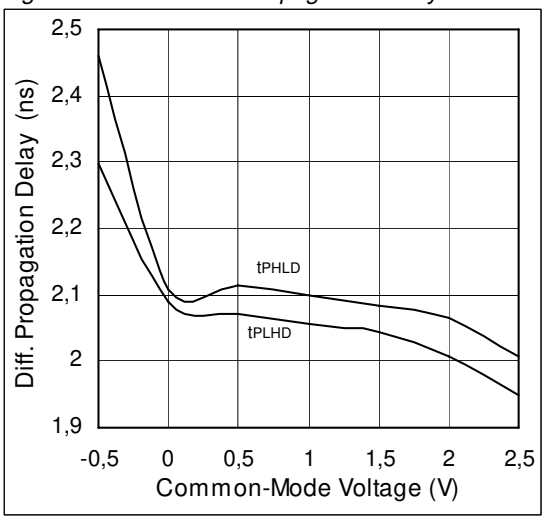


Figure 12. Differential Propagation Delay vs. VID

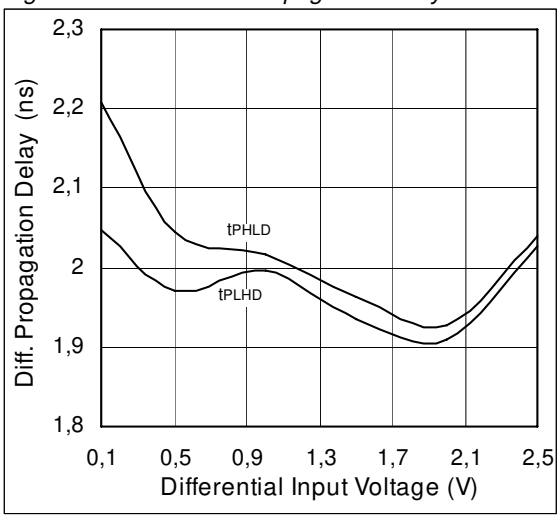


Figure 13. Differential Pulse Skew vs. VCC

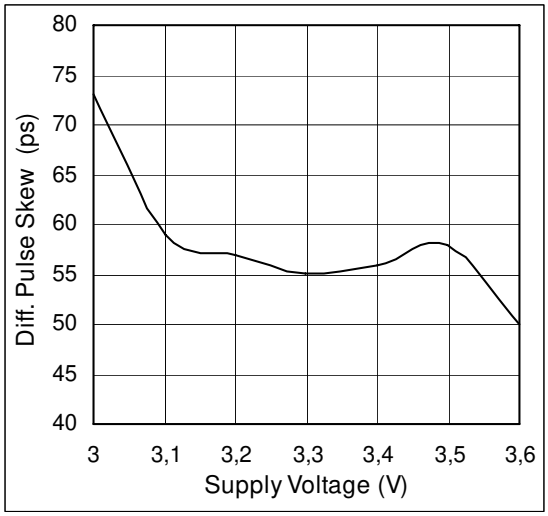


Figure 14. Transition Time vs. VCC

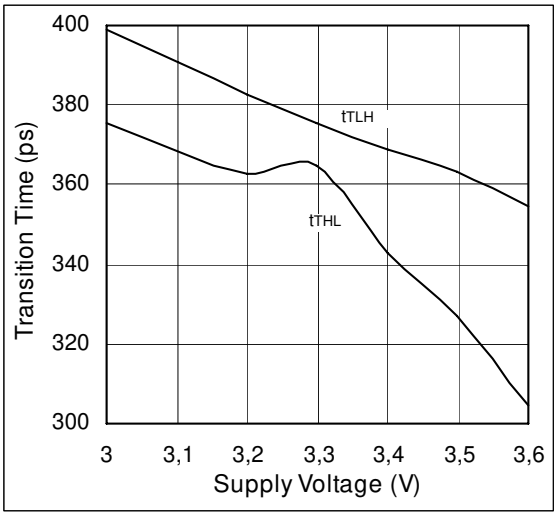
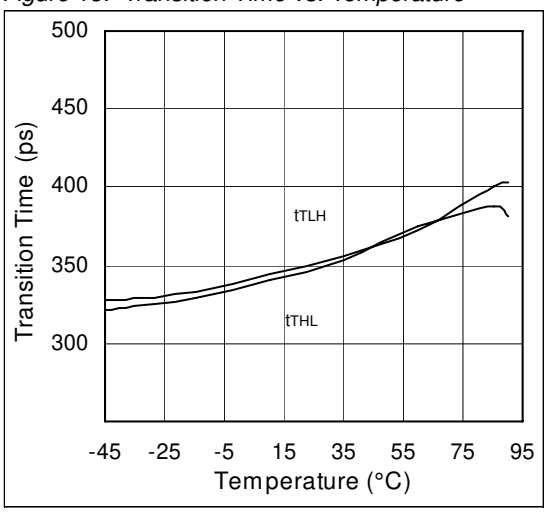


Figure 15. Transition Time vs. Temperature



8 Detailed Description

The AS1150 and AS1151 are 500Mbps, four-channel LVDS receivers intended for high-speed, point-to-point, low-power applications. Each independent channel accepts and converts an LVDS input to an LVTTL/LVCMOS output. The devices are capable of detecting differential signals from 100mV to 1V within an input voltage range of 0 to 2.4V.

The 250 to 450mV differential output of an LVDS driver is nominally centered around 1.25V. Due to the receiver input voltage range, a ±1V voltage shift in the signal relative to the receiver is allowed. Thus, a difference in ground references of the transmitter and the receiver, as well as the common mode effect of coupled noise, can be tolerated.

LVDS Interface

The LVDS Interface Standard is a signaling method defined for point-to-point communication over a controlled-impedance medium as defined by the *ANSI TIA/EIA-644* and *IEEE 1596.3* standards. The LVDS standard uses a lower voltage swing than other common communication standards, resulting in higher data rates, reduced power consumption and EMI emissions, and less susceptibility to noise.

The devices fully comply with the LVDS standard input voltage range of 0 to +2.4V referenced to receiver ground.

The AS1151 has an integrated termination resistors connected internally across each receiver input. This internal termination saves board space, eases layout, and reduces stub length compared to an external termination resistor. In other words, the transmission line is terminated on the IC.

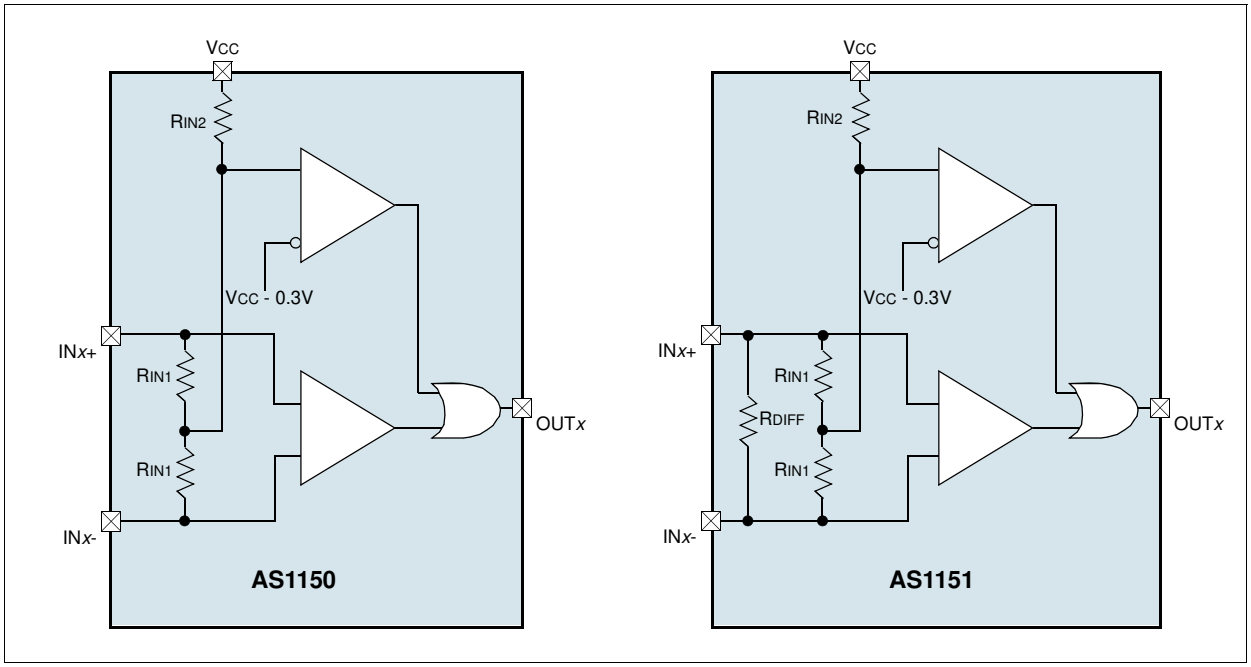
Failsafe Circuit

The devices contain an integrated failsafe circuit to prevent noise at inputs that are open, undriven and terminated, or undriven and shorted.

Open or undriven terminated input conditions can occur if there is a cable failure or when the LVDS driver outputs are high impedance. A short condition also can occur because of a cable failure. The failsafe circuit of the AS1150/AS1151 automatically sets the output high if any of these conditions are true.

The failsafe input circuit (see Figure 16) samples the input common-mode voltage and compares it to VCC - 0.3V (nominal). If the input is driven to levels specified in the LVDS standards, the input common-mode voltage is less than VCC - 0.3V and the failsafe circuit is not activated. If the inputs are open, undriven and shorted, or undriven and parallel terminated, there is no input current. In this case, a pullup resistor in the failsafe circuit pulls both inputs above VCC - 0.3V, activating the failsafe circuit and thus forcing the device output high.

Figure 16. Failsafe Input Circuit

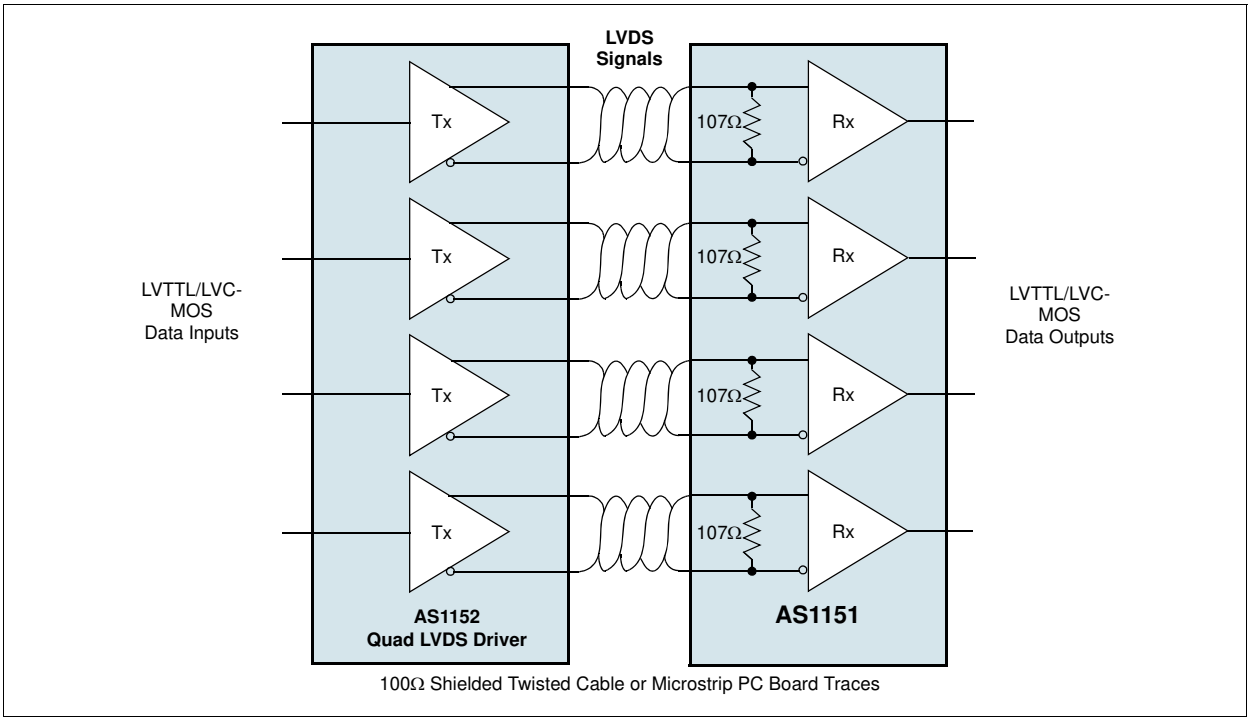


9 Applications

Table 5. Function Table

Enable Pins		Input		Output
EN	**ENn**	**IN*x*+**	**IN*x*-**	**OUT*x***
H	L or Open	$V_{ID} \geq +100mV$		H
		$V_{ID} \leq +100mV$		L
		AS1150 – Open, undriven short, or undriven 100Ω parallel termination		H
		AS1151 – Open or undriven short		
Other Combinations of Enable Pin Settings		Don't Care		Z

Figure 17. Typical Application Circuit



Power-Supply Bypassing

To bypass V_{CC}, use high-frequency surface-mount ceramic 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smaller valued capacitor closest to pin V_{CC}.

Differential Traces

Input trace characteristics can adversely affect the performance of the AS1150 and AS1151.

- Use controlled-impedance PC board traces to match the cable characteristic impedance. The termination resistor must also be matched to this characteristic impedance.
- Eliminate reflections and ensure that noise couples as common mode by running differential traces close together.
- Reduce skew by using matched trace lengths. Tight skew control is required to minimize emissions and proper data recovery of the devices.
- Route each channel's differential signals very close to each other for optimal cancellation of their respective external magnetic fields. Use a constant distance between the differential traces to avoid irregularities in differential impedance.
- Avoid 90° turns (use two 45° turns).
- Minimize the number of vias to further prevent impedance irregularities.

Cables and Connectors

Supported transmission media include printed circuit board traces, backplanes, and cables.

- Use cables and connectors with matched differential impedance (typically 100Ω) to minimize impedance mismatches.
- Balanced cables such as twisted pair offer superior signal quality and tend to generate less EMI due to magnetic field canceling effects. Balanced cables pick up noise as common mode, which is rejected by the LVDS receiver.
- Avoid the use of unbalanced cables such as ribbon cable or simple coaxial cable.

Termination

Due to the high data rates of LVDS drivers, matched termination will prevent the generation of any signal reflections, and reduce EMI.

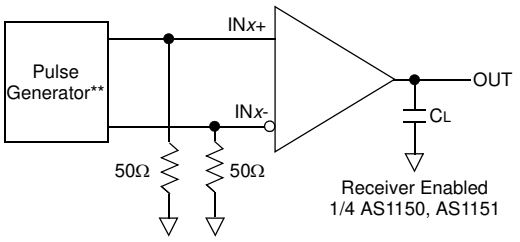
- The AS1151 has integrated termination resistors connected across the inputs of each receiver. The value of the integrated resistor is specified in Table 3 on page 4.
- The AS1150 requires an external termination resistor. The termination resistor should match the differential impedance of the transmission line and be placed as close to the receiver inputs as possible. Termination resistance values may range between 90 to 132Ω depending on the characteristic impedance of the transmission medium. Use 1% surface-mount resistors.

Board Layout

The device should be placed as close to the interface connector as possible to minimize LVDS trace length.

- Keep the LVDS and any other digital signals separated from each other to reduce crosstalk.
- Use a four-layer PC board that provides separate power, ground, LVDS signals, and input signals.
- Isolate the input LVDS signals from each other and the output LVCMOS/LVTTL signals from each other to prevent coupling.
- Separate the input LVDS signals from the output signals planes with the power and ground planes for best results.

Figure 18. Propagation Delay and Transition Time Test Circuit



* 50Ω required for pulse generator.
** When testing the AS1151, adjust the pulse generator output to account for internal termination resistor.

Figure 19. Propagation Delay and Transition Time Waveforms

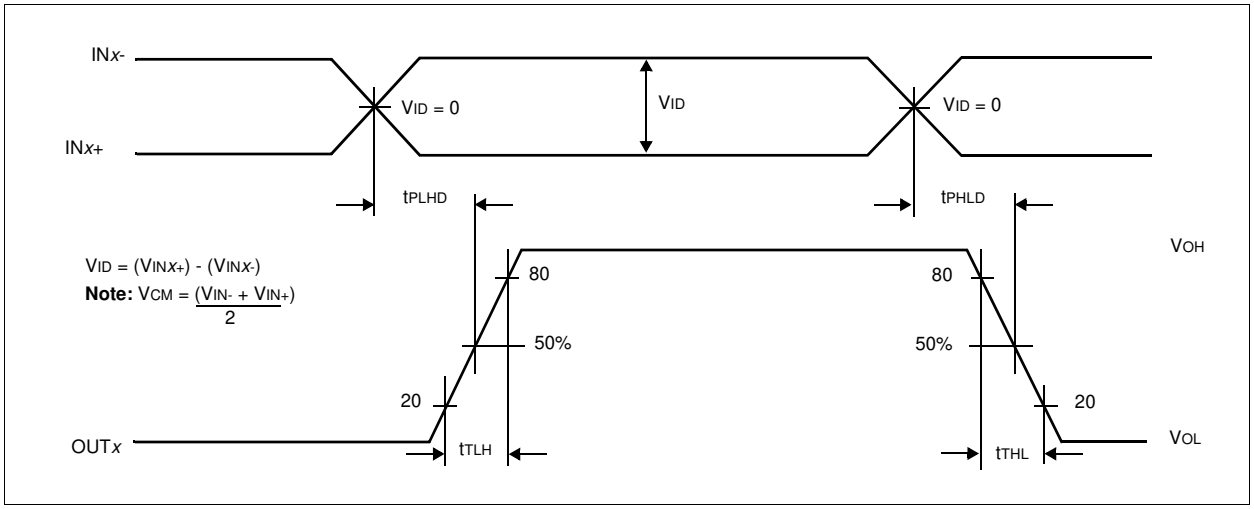


Figure 20. High Impedance Delay Test Circuit

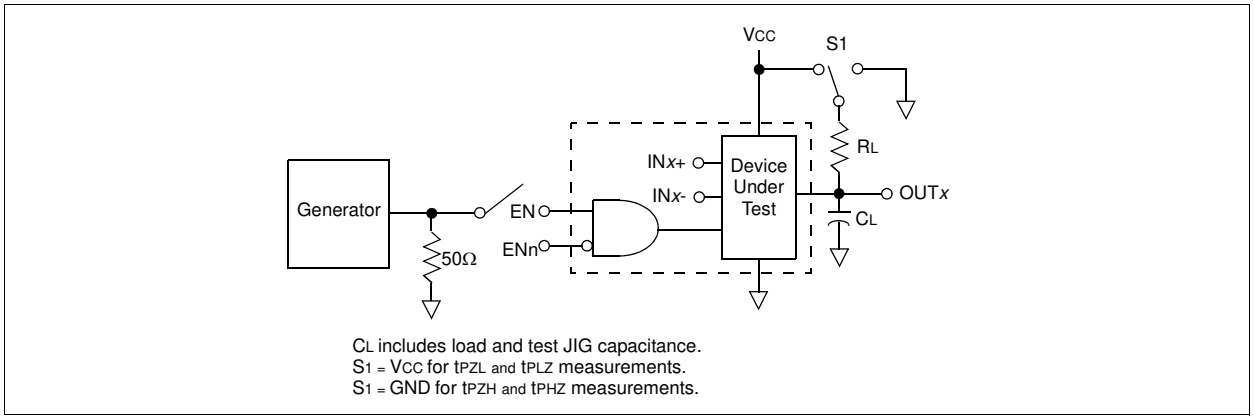
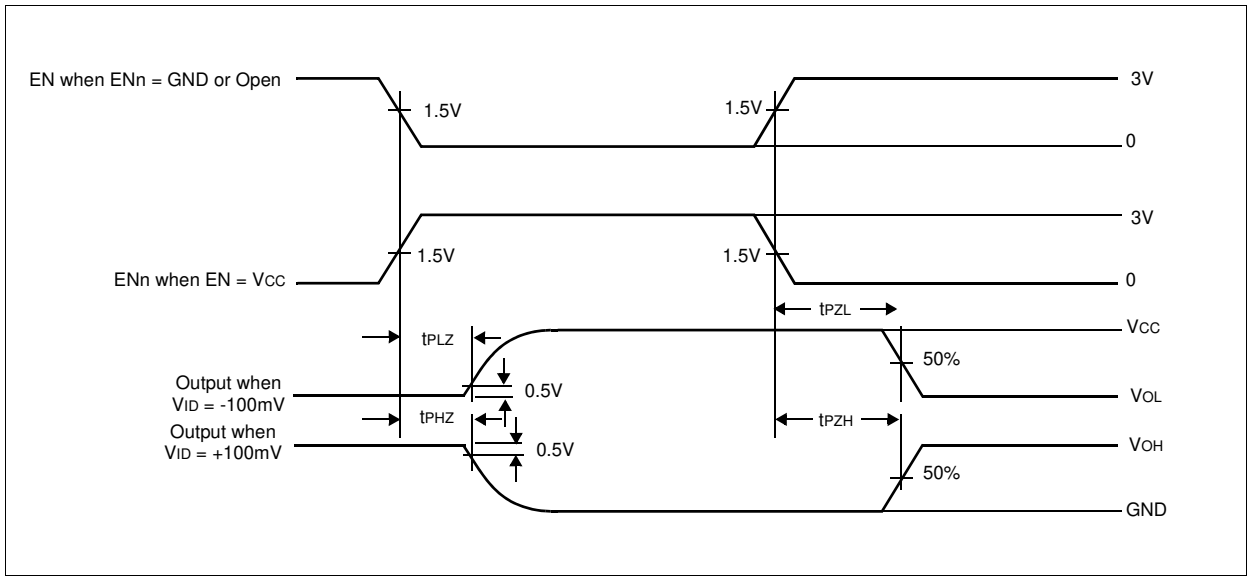
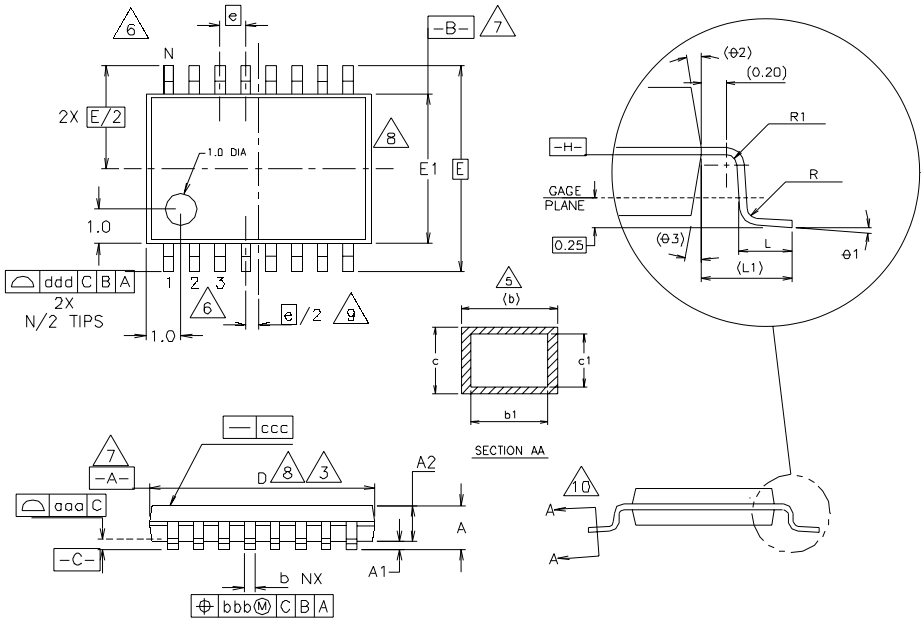


Figure 21. High Impedance Delay Waveforms



10 Package Drawings and Markings

Figure 22. 16-Pin TSSOP Package



Symbol	0.65mm Lead Pitch [1, 2]			Note	Symbol	0.65mm Lead Pitch [1, 2]			Note
	Min	Nom	Max			Min	Nom	Max	
A	-	-	1.10		θ1	0º	-	8º	
A1	0.05	-	0.15		L1		1.0 Ref		
A2	0.85	0.90	0.95		aaa		0.10		
L	0.50	0.60	0.75		bbb		0.10		
R	0.09	-	-		ccc		0.05		
R1	0.09	-	-		ddd		0.20		
b	0.19	-	0.30	5	e		0.65 BSC		
b1	0.19	0.22	0.25		θ2		12º Ref		
c	0.09	-	0.20		θ3		12º Ref		
c1	0.09	-	0.16						
Variations									
D	4.90	5.00	5.10	3, 8	e		0.65 BSC		
E1	4.30	4.40	4.50	4, 8	N		16		6
E		6.4 BSC							

Notes:

1. All dimensions are in millimeters; angles in degrees.
2. Dimensions and tolerancing per *ASME Y14.5M-1994*.
3. Dimension D does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15mm per side.
4. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
5. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of dimension b at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm for 0.5mm pitch packages.
6. Terminal numbers shown are for reference only.
7. Datums A and B to be determined at datum plane H.
8. Dimensions D and E1 to be determined at datum plane H.
9. This dimension applies only to variations with an even number of leads per side. For variations with an odd number of leads per package, the center lead must be coincident with the package centerline, datum A.
10. Cross section A-A to be determined at 0.10 to 0.25mm from the leadtip.

11 Ordering Information

Model	Description	Package Type	Delivery Form
AS1150	Quad low-voltage differential signaling receiver	16-pin TSSOP	Tubes
AS1150-T	Quad low-voltage differential signaling receiver	16-pin TSSOP	Tape and Reel
AS1151	Quad low-voltage differential signaling receiver with integrated termination	16-pin TSSOP	Tubes
AS1151-T	Quad low-voltage differential signaling receiver with integrated termination	16-pin TSSOP	Tape and Reel

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