AS1524/AS1525

150ksps, 12-Bit, 1-Channel Pseudo/True-Differential and 2-Channel Single-Ended ADCs

1 General Description

The AS1524/AS1525 are low-power, 12-bit analog-to-digital converters (ADCs) designed to operate with a single +2.7V to +5.25V supply. Excellent dynamic performance, low power consumption, and simplicity make these devices perfect for portable battery-powered data-acquisition applications.

The devices are available as the standard products listed in Table 1.

Table 1. Standard Products

Model	Input Type	Input Voltage
AS1524	1-Channel, Pseudo / True-Differential	0 to V_{REF} / -V_{REF}/2 to V_{REF}/2
AS1525	2-Channel, Single-Ended	0 to V_{REF}

The devices feature a successive-approximation register (SAR), automatic shutdown, fast wakeup (1.4µs), and low-power consumption at the maximum sampling rate of 150ksps.

Automatic shutdown (0.2µA) between conversions results in reduced power consumption (at slower throughput rates).

Data access are made via an external clock through the SPI-/QSPI-/MICROWIRE-compatible 3-wire high-speed serial interface.

The AS1525/AS1524 are available in a 8-pin TDFN (3x3mm) package.

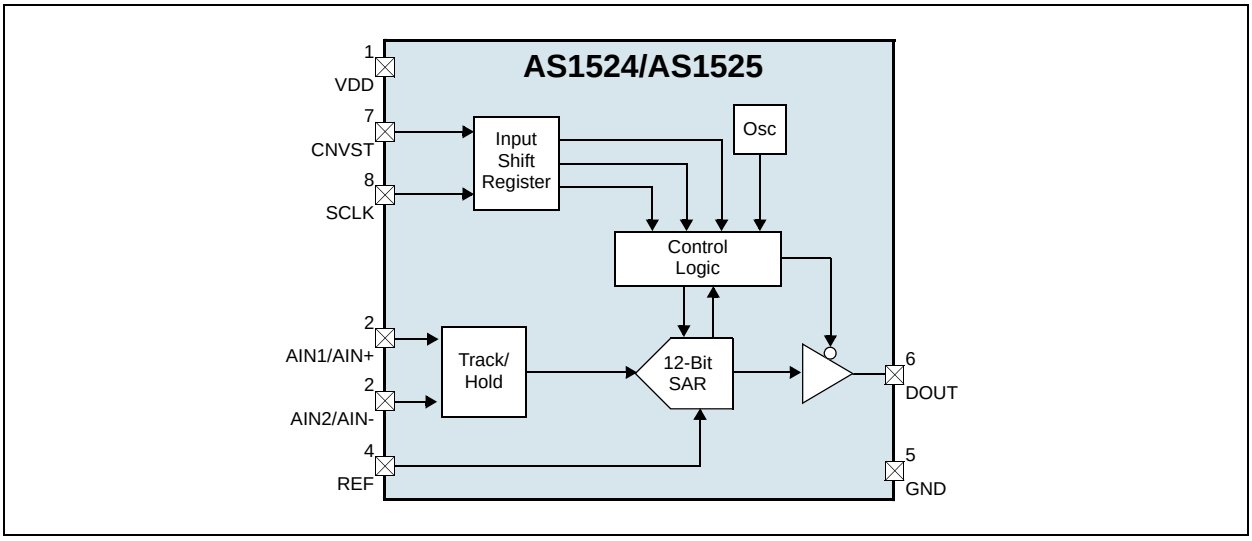
2 Key Features

- Single-Supply Operation: +2.7V to +5.25V
- Automatic Shutdown Between Conversions
- Low Power Consumption
  - 350µA @ 150ksps
  - 245µA @ 100ksps
  - 24µA @ 10ksps
  - 2.5µA @ 1ksps
  - 200nA in Automatic Shutdown Mode
- True-Differential Track/Hold, 150kHz Sampling Rate Software-Configurable Unipolar/Bipolar Conversion (AS1524)
- Input Common Mode Range from GND to V_{DD}
- 3-Wire SPI-/QSPI-/MICROWIRE-Compatible Serial Interface
- Internal Conversion Clock
- 8-pin TDFN (3x3mm) Package

3 Applications

The devices are ideal for remote sensors, data-acquisition, data logging devices, lab instruments, or for any other space-limited A/D devices with low power consumption and single-supply requirements.

Figure 1. AS1524/AS1525 - Block Diagram



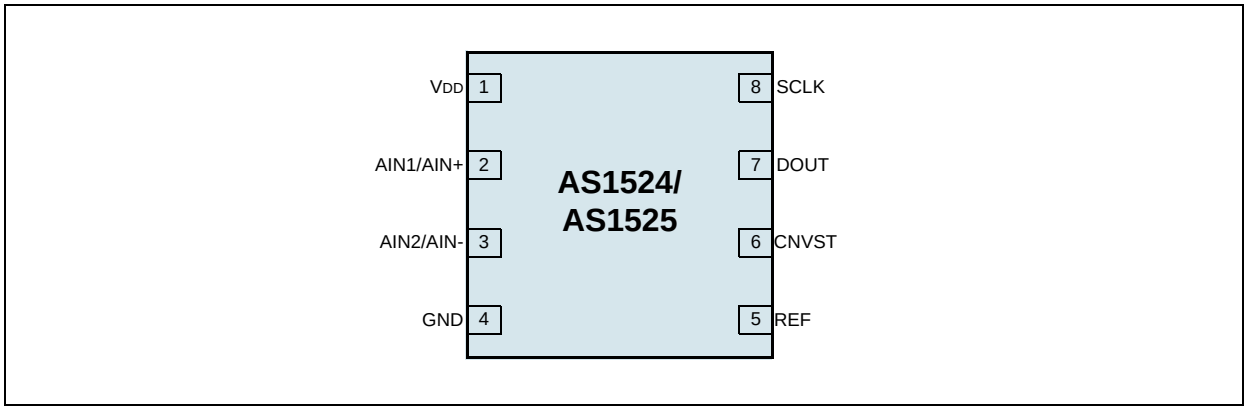
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4 Pinout

Pin Assignment

Figure 2. Pin Assignments (Top View)



Pin Description

Table 2. Pin Description

Pin Number	Pin Name	Description
1	VDD	**Positive Supply Voltage.** +2.7V to +5.25V. **Note:** Bypass with a 0.1µF capacitor to GND.
2	AIN1/AIN+	**Analog Input Channel 1 (AS1525) or Positive Analog Input (AS1524)**
3	AIN2/AIN-	**Analog Input Channel 2 (AS1525) or Negative Analog Input (AS1524)**
4	GND	**Ground**
5	REF	**External Reference Voltage Input.** Sets the analog voltage range. **Note:** Bypass with a 4.7µF capacitor to GND.
6	CNVST	**Conversion Start**. A rising edge powers up the device and puts the track/hold circuitry in track mode. At the falling edge of this pin, the device enters hold mode and begins a conversion. **Note:** This pin also selects the input channel (AS1525) or input polarity (AS1524).
7	DOUT	**Serial Data Output.** This pin transitions the falling edge of SCLK and goes low at the start of a conversion and delivers the MSB at the completion of a conversion. **Note:** This pin goes high impedance once data has been fully clocked out.
8	SCLK	**Serial Clock Input.** Clocks out data at DOUT with the MSB first.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 5 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
VDD to GND	-0.3	+6	V	
CNVST, SCLK, DOUT, REF, AIN1/ AIN+, AIN2/AIN- to GND	-0.3	V_{DD} + 0.3	V	
Current into Any Pin		50	mA	
Continuous Power Dissipation	1491		mW	T_{AMB} = +70ºC; derate 19.5mW/ºC above +70ºC
Operating Temperature Range	-40	+85	ºC	
Storage Temperature Range	-60	+150	ºC	
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020D "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices"*. The lead finish for Pb-free leaded packages is matte tin (100% Sn).

6 Electrical Characteristics

V_{DD} = +2.7 to +5.25V, V_{REF} = +2.5V, 4.7µF Capacitor at REF; f_{SCLK} = 8MHz (50% Duty Cycle); AIN- = GND (AS1524) T_{AMB} = T_{MIN} to TMAX (unless otherwise specified). Typical Values at T_{AMB} = +25ºC. Unipolar Mode (AS1524).

Table 4. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
DC Accuracy						
	Resolution		12			Bits
INL	Relative Accuracy				±1.0	LSB
DNL	Differential Non-Lineraity	No Missing Codes Over Temperature	-0.99		+1.0	LSB
	Offset Error			±1	±4	LSB
	Gain Error [1]			±1	±4	LSB
	Gain Temp Coefficient			±0.3		ppm/ºC
	Offset Temp Coefficient			±0.3		ppm/ºC
	Channel-to-Channel Offset Match			±0.1		LSB
	Channel-to-Channel Gain Match			±0.1		LSB
Dynamic Specifications – (f_{IN} (sinewave) = 10kHz, V_{IN} = 2.5V_{P-P}, 150ksps, f_{SCLK} = 8MHz (50% duty cycle), AIN- = GND (AS1524)						
SINAD	Signal-to-Noise Plus Distortion			72.5		dB
THD	Total Harmonic Distortion (to the 5th Harmonic)			-79.5		dB
SFDR	Spurious-Free Dynamic Range			84		dB
	Full Power Bandwidth	-3dB Point		20		MHz
	Full Linear Bandwidth	-0.1dB Point		400		kHz
Conversion Rate						
t_{CONV}	Conversion Time	Exclusive of t_{ACQ}		3.3	3.7	µs
t_{ACQ}	Track/Hold Acquisition Time				1.4	µs
	Aperture Delay			30		ns
f_{SCLK}	Max Serial Clock Frequency				8	MHz
	Serial Clock Duty Cycle		30		70	%
Analog Input						
	V_{IN} Range [2]	Unipolar	0		V_{REF}	V
		Bipolar	-V_{REF}/2		V_{REF}/2	
	Input Leakage Current	No Channel Selected or Conversion Halted		±0.01	±1	µA
	Input Capacitance	Track Mode		20		pF
		Hold Mode		5		pF
External Reference Input						
V_{REF}	V_{IN} Range		1.0		V_{DD} + 50mV	V
I_{REF}	Input Current	V_{REF} = +2.5V @ 150ksps		11	25	µA
		V_{REF} = +4.096V @ 150ksps		19		
		Acquisition Between Conversions	0	+2	+5	

Table 4. Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Digital Inputs/Outputs (CNVST, SCLK, DOUT)						
V_{IL}	Input Low Voltage				0.3V_{DD}	V
V_{IH}	Input High Voltage		0.7V_{DD}			V
I_{LEAK}	Input Leakage Current			±0.01	±1.0	µA
C_{IN}	Input Capacitance			15		pF
V_{OL}	Output Low Voltage	I_{SINK} = 2mA			0.4	V
		I_{SINK} = 4mA			0.8	
V_{OH}	Output High Voltage	I_{SOURCE} = 1.5mA	0.7V_{DD}			V
	Tri-State Leakage Current	CNVST = GND		±0.05	±5	µA
	Tri-State Output Capacitance	CNVST = GND		15		pF
Power Requirements						
V_{DD}	Positive Supply Voltage		2.7		5.25	V
I_{DD}	Positive Supply Current	V_{DD} = +3V, f_{SAMPLE} = 150ksps		350	425	µA
		V_{DD} = +3V, f_{SAMPLE} = 100ksps		245		
		V_{DD} = +3V, f_{SAMPLE} = 10ksps		24		
		V_{DD} = +3V, f_{SAMPLE} = 1ksps		2.5		
		V_{DD} = +5V, f_{SAMPLE} = 150ksps		485	550	
		V_{DD} = +5V, f_{SAMPLE} = 100ksps		330		
		V_{DD} = +5V, f_{SAMPLE} = 10ksps		33		
		V_{DD} = +5V, f_{SAMPLE} = 1ksps		3.7		
		Automatic Shutdown Mode		0.2	1	
PSR	Power Supply Rejection	V_{DD} = +5V ±5%, Full Scale Input		±0.3		mV
		V_{DD} = +2.7V to 3.6V, Full Scale Input		±0.4		

1. Offset nulled.
2. The absolute input voltage range for the analog inputs is from GND to V_{DD}.

Timing Characteristics

V_{DD} = +2.7 to +5.25V, V_{REF} = +2.5V, 4.7µF Capacitor at REF; f_{SCLK} = 8MHz (50% Duty Cycle); AIN- = GND (AS1524) T_{AMB} = T_{MIN} to TMAX (unless otherwise specified). Typical Values at T_{AMB} = +25ºC.

Table 5. Timing Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SCLK Pulse Width High	tCH		38			ns
SCLK Pulse Width Low	tCL		38			ns
SCLK Falling-to-DOUT Transition	tDOT	CLOAD = 30pF (see Figure 3, Figure 4, Figure 19 on page 12, Figure 20 on page 12)		28	60	ns
SCLK Rising-to-DOUT[1] Disable	tDOD	CLOAD = 30pF (see Figure 3, Figure 4, Figure 19 on page 12, Figure 20 on page 12)	100	200	500	ns
CNVST Falling-to-MSB Vlid	tCONV	CLOAD = 30pF (see Figure 3, Figure 4, Figure 19 on page 12, Figure 20 on page 12)		3.3	3.7	µs
CNVST Pulse Width	tCSW		30			ns

1. Guaranteed by Design and Characterisation.

Figure 3. DOUT Enable/Disable Time Load Circuits

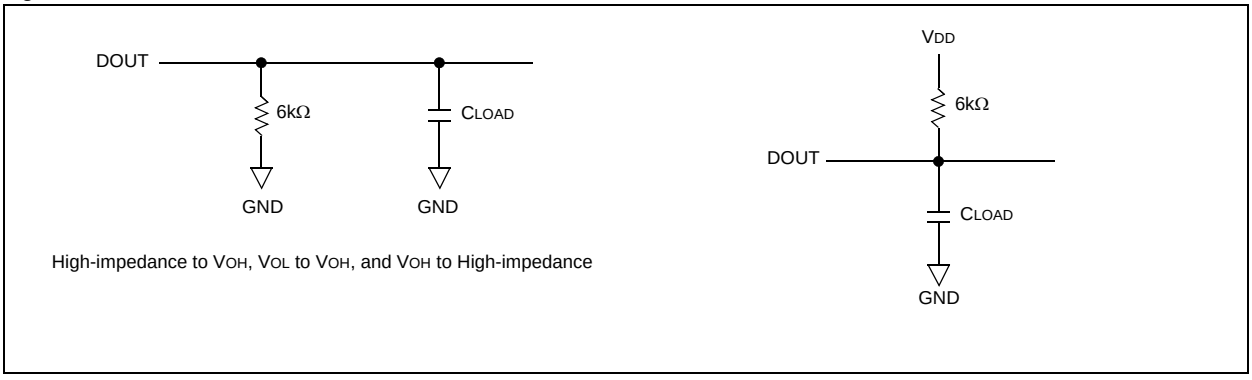
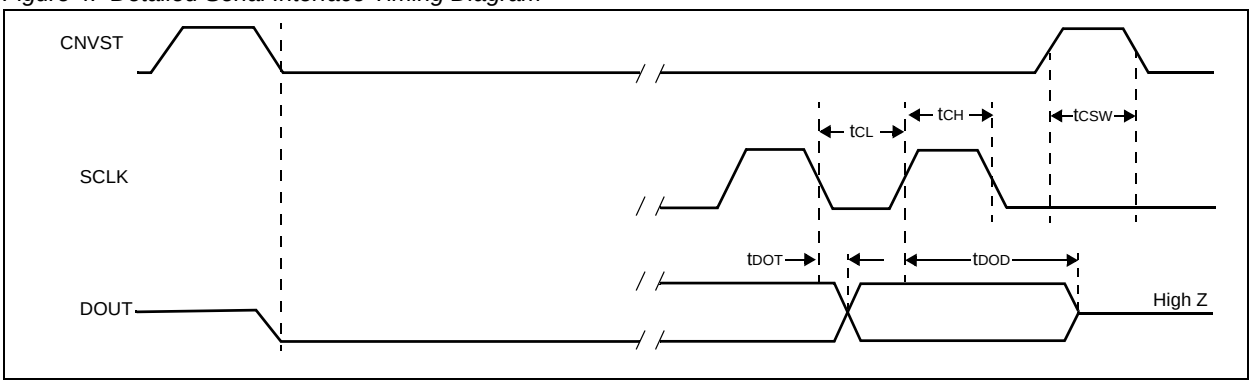


Figure 4. Detailed Serial Interface Timing Diagram



7 Typical Operating Characteristics

V_{DD} = 5V; V_{REF} = 2.5V, f_{SCLK} = 8MHz(50% duty), C_{REF} = 4.7µF, T_{AMB} = +25ºC (unless otherwise specified).

Figure 5. Integral Nonlinearity vs. Digital Output Code

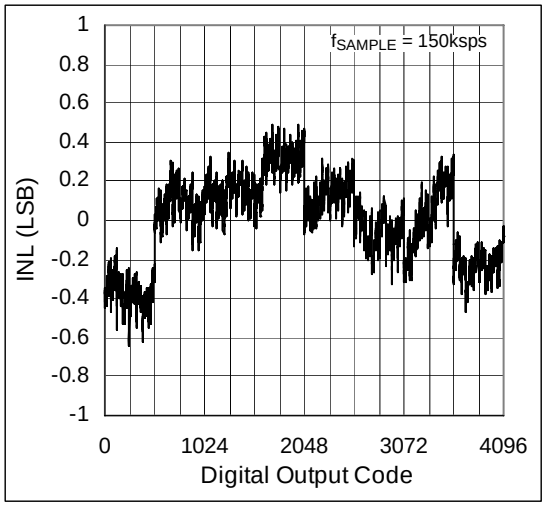


Figure 6. Differential Nonlinearity vs. Digital Output Code

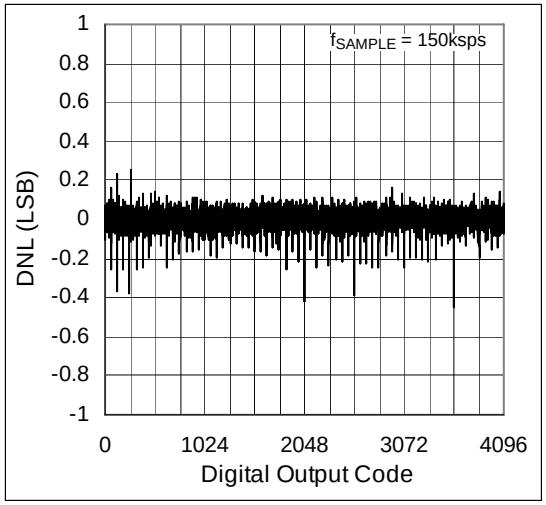


Figure 7. Supply Current vs. Supply Voltage

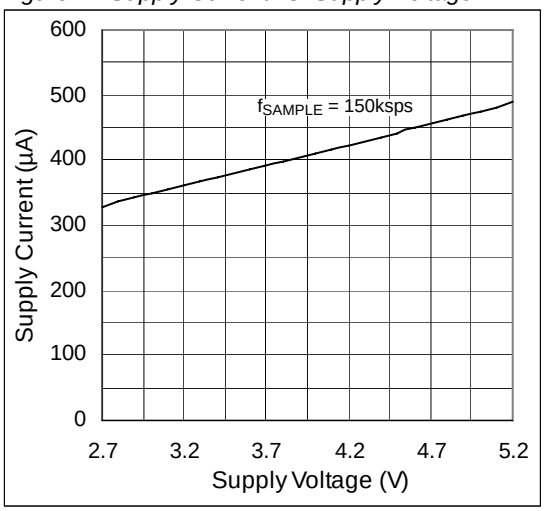


Figure 8. Supply Current vs. Temperature

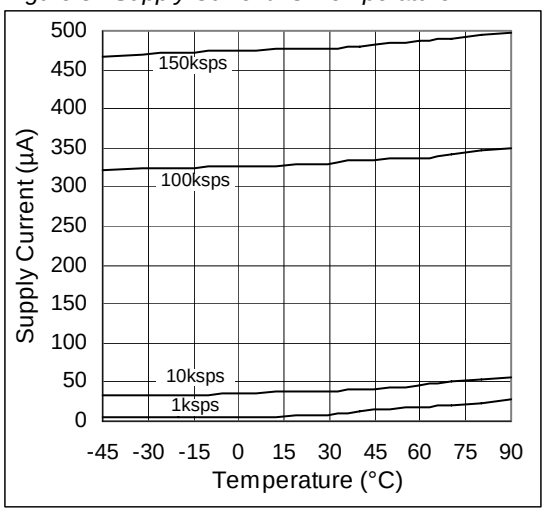


Figure 9. Supply Current vs. Temperature, V_{DD} = 3V

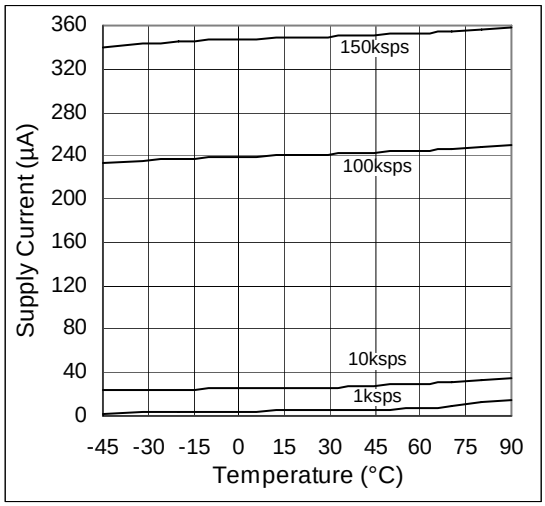


Figure 10. Supply Current vs. Sampling Rate

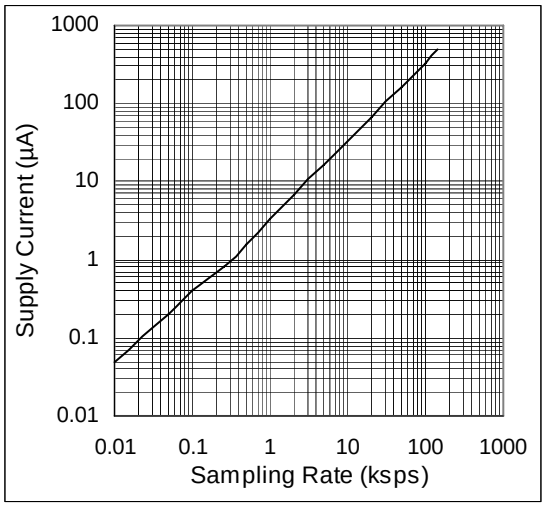


Figure 11. Shutdown Current vs. Supply Voltage

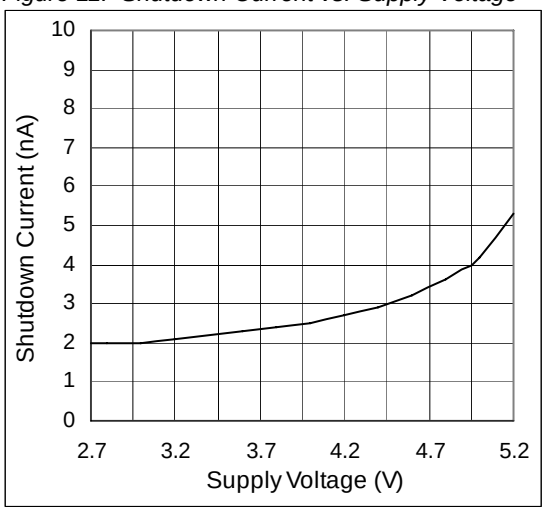


Figure 12. Shutdown Current vs. Temperature

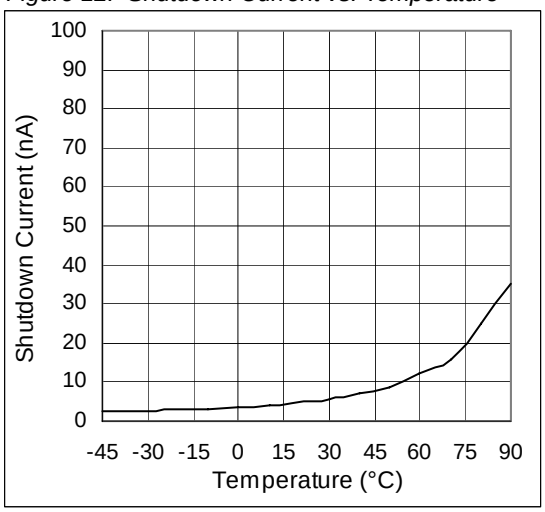


Figure 13. Offset Error vs. Supply Voltage

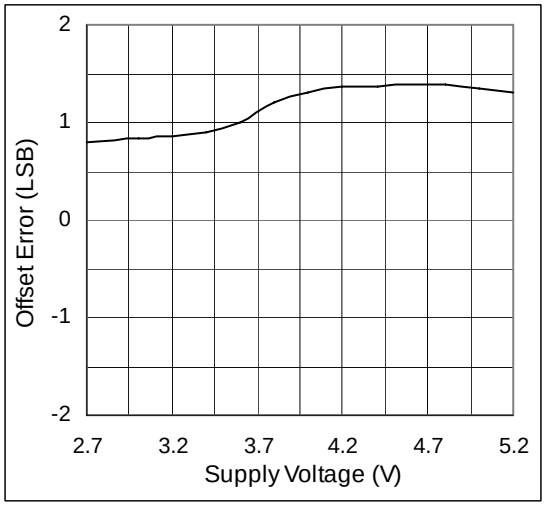


Figure 14. Offset Error vs. Temperature

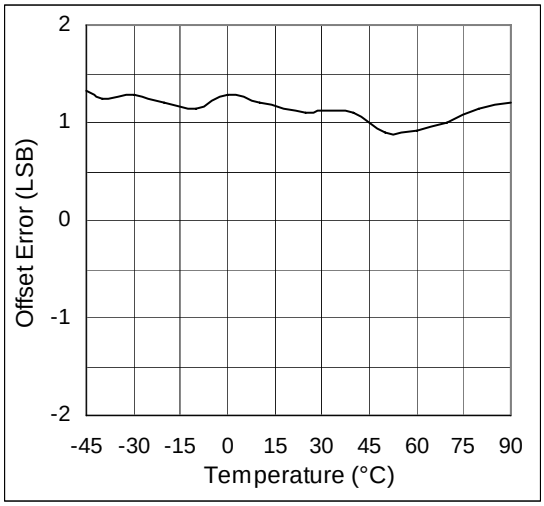


Figure 15. Gain Error vs. Supply Voltage

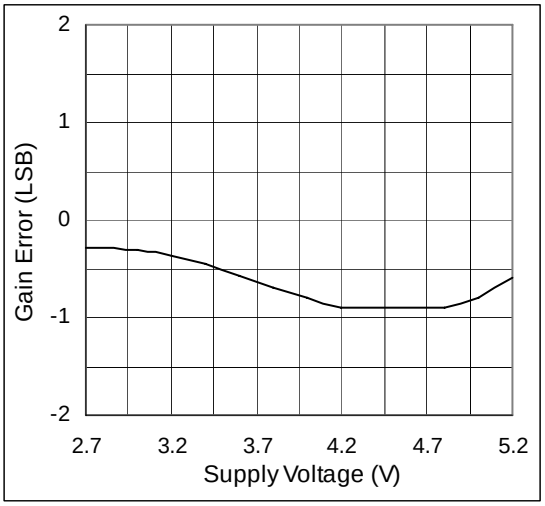


Figure 16. Gain Error vs. Temperature

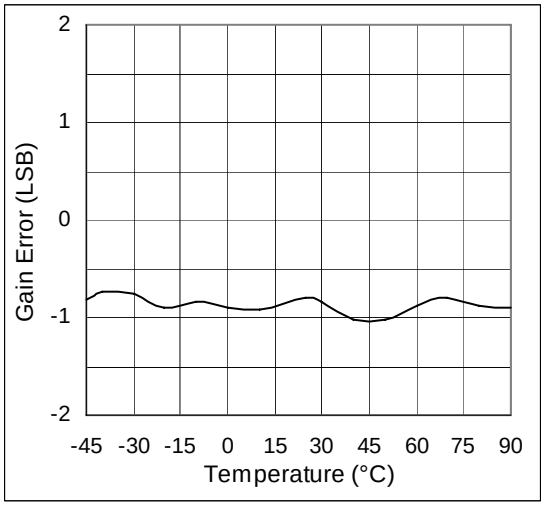
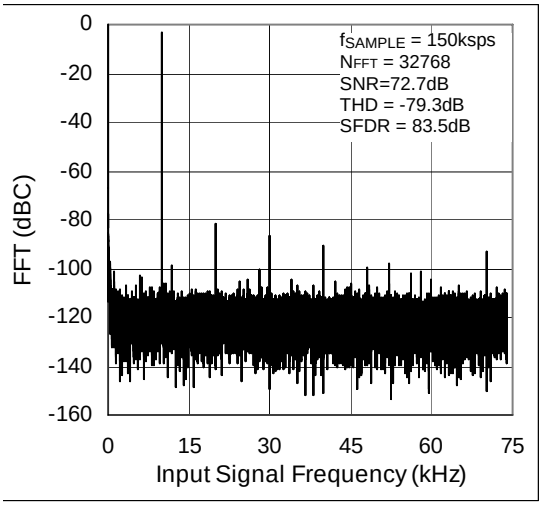


Figure 17. FFT @ 10kHz



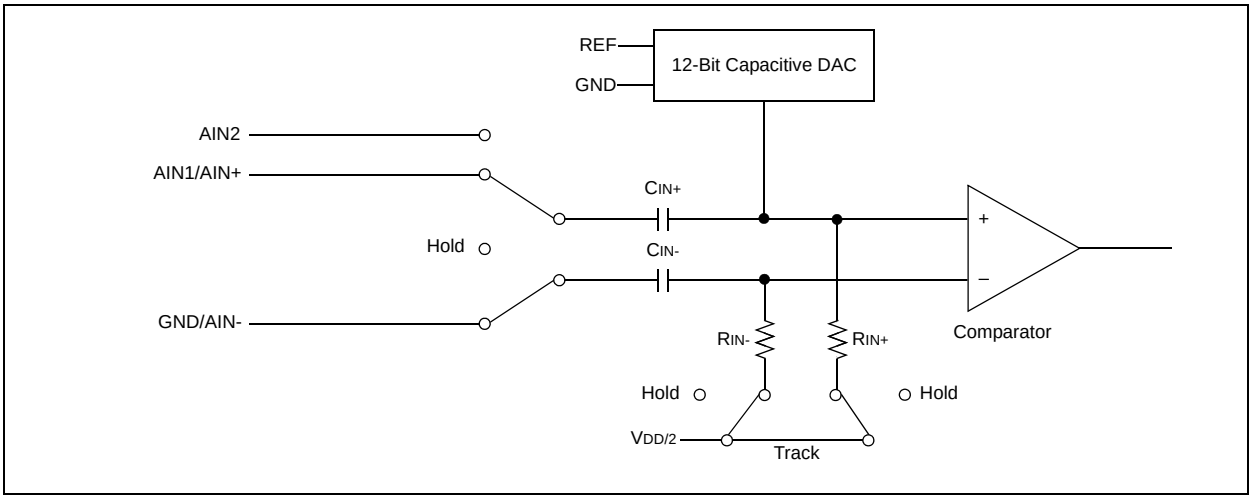
8 Detailed Description

The AS1524/AS1525 employ a successive approximation conversion (SAR) technique and integrated track/hold circuitry to convert analog signals into 12-bit digital output. The serial interface provides easy interfacing to microprocessors. Figure 18 shows the simplified internal structure for the AS1525 (2-channels, single ended) and the AS1524 (1-channel, true differential).

True Differential Analog Input Track/Hold

The equivalent circuit of Figure 18 shows the device input architecture which is composed of track/hold circuitry, input multiplexer, comparator, and switched-capacitor DAC. The track/hold circuitry enters its tracking mode on the rising edge of CNVST. The positive input capacitor is connected to AIN1 or AIN2 (AS1525) or AIN+ (AS1524). The negative input capacitor is connected to GND (AS1525) or AIN- (AS1524).

Figure 18. Equivalent Input Circuit



The track/hold circuitry enters its hold mode on the falling edge of CNVST and the difference between the sampled positive and negative input voltages is converted. The time required for the track/hold to acquire an input signal is determined by how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens, and CNVST must be held high for a longer period of time. The acquisition time (t_{ACQ}) is the maximum time needed for the signal to be acquired, plus the power-up time. t_{ACQ} is calculated by:

$$t_{ACQ} = 9 \times (R_S + R_{IN}) \times 20pF + t_{PWR} \qquad \textit{(EQ 1)}$$

Where:

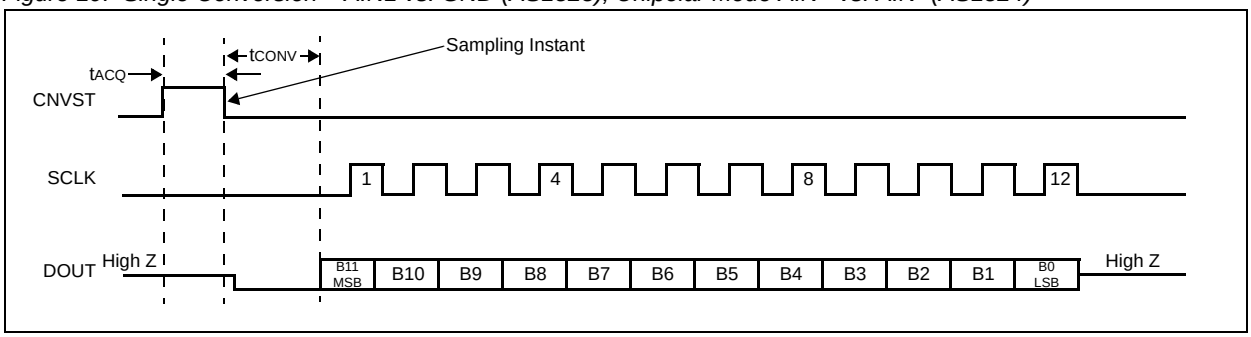
R_S is the source impedance of the input signal;
R_{IN} = 1.5kΩ;
t_{PWR} of 1µs is the power-up time of the device.

Note: t_{ACQ} is never less than 1.4µs and any source impedance below 300. does not significantly affect the AS1524/AS1525 AC performance. A high-impedance source can be accommodated either by lengthening t_{ACQ} or by placing a 1µF capacitor between the positive and negative analog inputs.

Selecting AIN1 or AIN2 (AS1525)

Select one of the AS1525 two positive input channels using the CNVST pin (see page 3). If AIN1 is selected (see Figure 19), drive CNVST high to power up the AS1525 and place the track/hold circuitry in track mode with AIN1 connected to the positive input capacitor. Hold CNVST high for t_{ACQ} to fully acquire the signal. Drive CNVST low to place the track/hold circuitry in hold mode. The AS1525 then performs a conversion and shutdown automatically. The MSB is available at DOUT after 3.7µs. Data can then be clocked out using SCLK. Clock out all 12 bits of data before driving CNVST high for the next conversion. If all 12 bits of data are not clocked out before CNVST is driven high, AIN2 is selected for the next conversion.

Figure 19. Single Conversion – AIN1 vs. GND (AS1525), Unipolar Mode AIN+ vs. AIN- (AS1524)



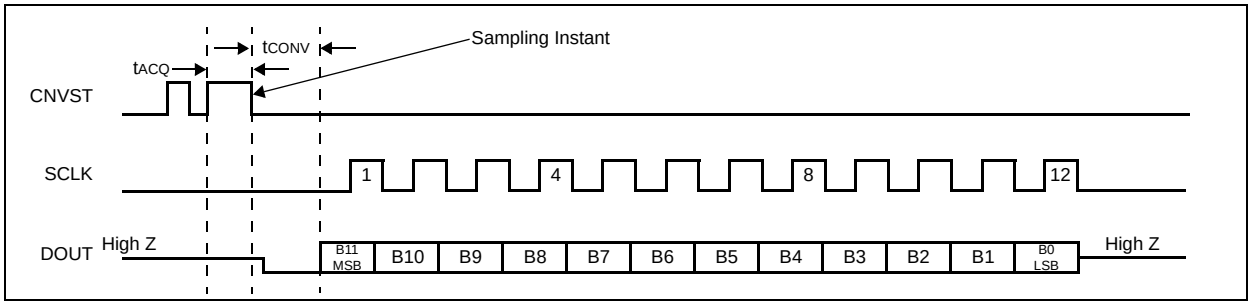
If AIN2 is selected (see Figure 20), drive CNVST high for at least 30ns. Next, drive CNVST low for at least 30ns, and then high again. This powers up the AS1525 and places the track/hold circuitry in track mode with AIN2 connected to the positive input capacitor. Next hold CNVST high for tACQ to fully acquire the signal. Drive CNVST low to place the track/hold circuitry in hold mode. The AS1525 then performs a conversion and shuts down automatically. The MSB is available at DOUT after 3.7µs. Data can then be clocked out using SCLK.

Note: If all 12 bits of data are not clocked out before CNVST is driven high, AIN2 is selected for the next conversion.

Selecting Unipolar or Bipolar Conversions (AS1524)

True-differential conversion (with the AS1524 unipolar and bipolar modes) is selected using pin CNVST (see page 3). AIN+ and AIN- are sampled at the falling edge of CNVST. In unipolar mode, AIN+ can exceed AIN- by up to VREF. The output format is straight binary. In bipolar mode, either input can exceed the other by up to $V_{REF/2}$. The output format is two's complement. In both modes, the input common mode range can go from GND to V_{DD}.

Figure 20. Single Conversion – AIN2 vs. GND (AS1525), Bipolar Mode AIN+ vs. AIN- (AS1524)



Note: In unipolar and bipolar modes, AIN+ and AIN- must not exceed V_{DD} by more than 50mV or be lower than GND by more than 50mV.

If unipolar mode is selected (see Figure 19), drive CNVST high to power up the AS1524 and place the track/hold circuitry in track mode with AIN+ and AIN- connected to the input capacitors. Hold CNVST high for tACQ to fully acquire the signal. Drive CNVST low to place the track/hold circuitry in hold mode. The AS1524 then performs a conversion and shutdown automatically. The MSB is available at DOUT after 3.7µs. Data can then be clocked out using SCLK.

Clock out all 12 bits of data before driving CNVST high for the next conversion. If all 12 bits of data are not clocked out before CNVST is driven high, bipolar mode is selected for the next conversion.

If bipolar mode is selected (see Figure 20), drive CNVST high for at least 30ns. Next, drive CNVST low for at least 30ns and then high again. This places the track/hold circuitry in track mode with AIN+ and AIN- connected to the input capacitors.

Next hold CNVST high for tACQ to fully acquire the signal. Drive CNVST low to place the track/hold circuitry in hold mode. The AS1524 then performs a conversion and shuts down automatically. The MSB is available at DOUT after 3.7µs. Data can then be clocked out using SCLK.

Note: If all 12 bits of data are not clocked out before CNVST is driven high, bipolar mode is selected for the next conversion.

Input Bandwidth

The AS1524/AS1525 input tracking circuitry has a 20MHz small signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the AS1524/AS1525 sampling rate by using undersampling techniques.

Note: To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Protection

Internal protection diodes that clamp the analog input to V_{DD} and GND allow the analog input pins to swing from GND - 0.3V to V_{DD} + 0.3V without damage. Both inputs must not exceed V_{DD} by more than 50mV or be lower than GND by more than 50mV for accurate conversions.

Note: If an off-channel analog input voltage exceeds the supply voltages, the input current should be limited to 2mA.

Internal Clock

The AS1524/AS1525 operate from an internal clock, which is accurate within 5% of the 4MHz clock rate. This results in a worst-case conversion time of 3.7µs. The internal clock releases the system microprocessor from running the SAR conversion clock and allows the conversion results to be read back at the processor's convenience, at any clock rate from 0 to 8MHz.

Output Data Format

Figure 19 on page 12 and Figure 20 on page 12 illustrate the conversion timing for the AS1524/AS1525. The 12-bit conversion result is output in MSB-first format. Data on DOUT transitions on the falling edge of SCLK. All 12 bits must be clocked out before CNVST transitions again.

For the AS1524, data is straight binary for unipolar mode and two's complement for bipolar mode. For the AS1525, data is always straight binary.

Transfer Function

Figure 21 on page 13 shows the unipolar transfer function for the AS1524/AS1525. Figure 22 on page 14 shows the bipolar transfer function for the AS1524. Code transitions occur halfway between successive-integer LSB values.

Figure 21. AS1524/AS1525 Unipolar Transfer Function

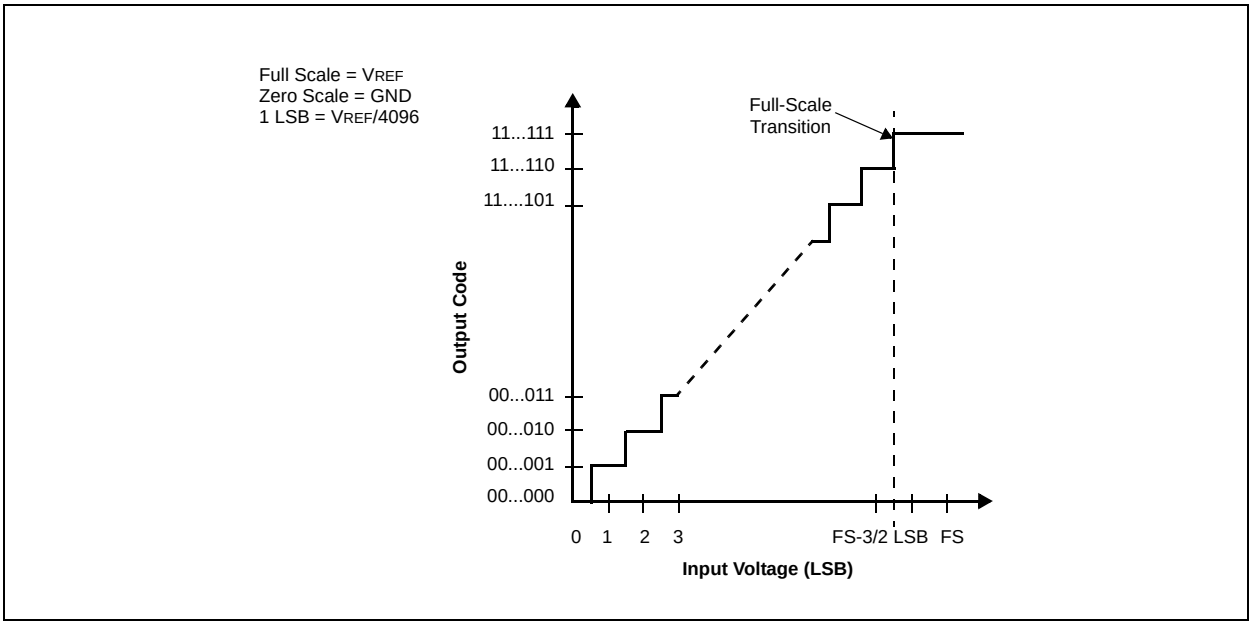
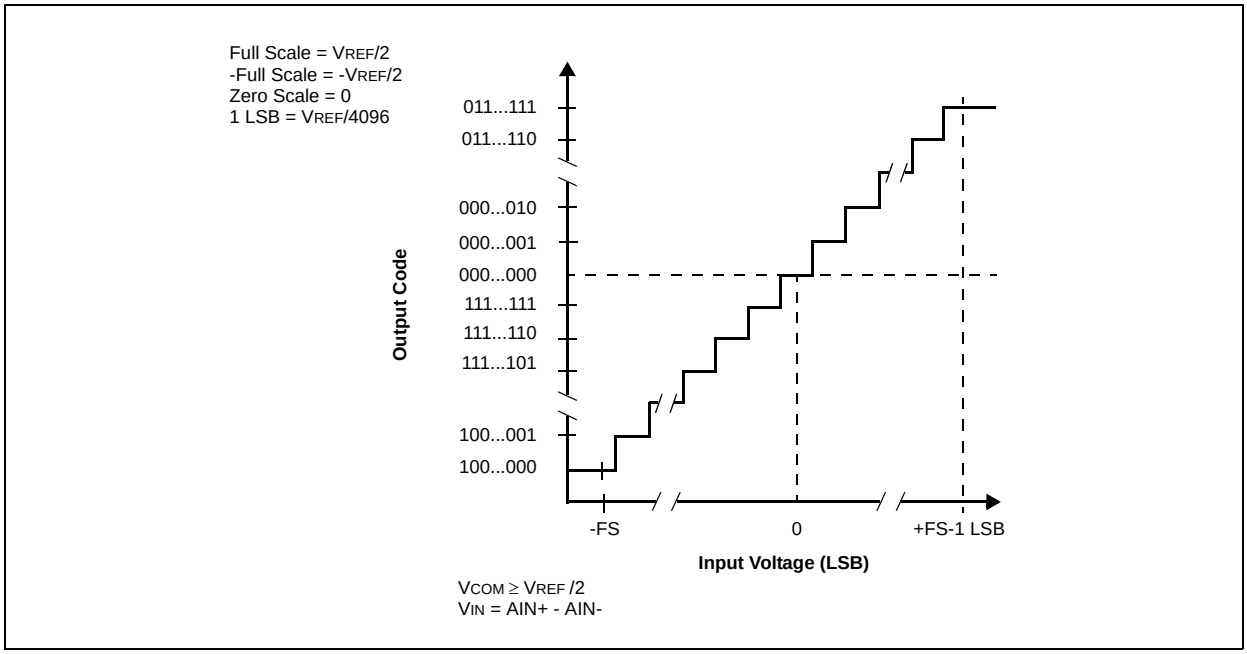


Figure 22. AS1524 Bipolar Transfer Function



9 Application Information

Automatic Shutdown Mode

With CNVST low, the AS1524/AS1525 default to automatic shutdown (< 0.2µA) mode after power-up and between conversions. After detecting a rising edge of CNVST, the AS1524/AS1525 powers up, sets DOUT low, and enters track mode.

After detecting a falling edge of CNVST, the device enters hold mode and begins the conversion. A maximum of 3.7µs later, the device completes conversion, enters shutdown, and MSB is available at DOUT.

External Reference

An external reference is required for the AS1524/AS1525. Use a 4.7µF bypass capacitor for best performance. The reference input structure allows a voltage range of +1V to V_{DD} + 50mV.

Performing a Conversion

1. Use a general-purpose I/O line on the CPU to hold CNVST low between conversions.
2. Drive CNVST high to acquire AIN1(AS1525) or unipolar mode (AS1524). To acquire AIN2 (AS1525) or bipolar mode (AS1524), drive CNVST low and high again.
3. Hold CNVST high for 1.4µs.
4. Drive CNVST low and wait approximately 3.7µs for conversion to complete. After 3.7µs, the MSB is available at DOUT.
5. Activate SCLK for a minimum of 12 rising clock edges. DOUT transitions on SCLK's falling edge and is available in MSB-first format. Observe the SCLK to DOUT valid timing characteristic. Clock data into the µP on SCLK's rising edge.

Standard Interface Connections

The AS1524/AS1525 serial interface is fully compatible with SPI, QSPI, and MICROWIRE. If a serial interface is available, establish the processor's serial interface as a master so that the CPU generates the serial clock for the AS1524/AS1525 and select a clock frequency up to 8MHz.

SPI and Microwire Interface

When using an SPI (Figure 23) or Microwire interface (Figure 24), set CPOL = CPHA = 0. Two 8-bit readings are necessary to obtain the entire 12-bit result from the AS1524/AS1525. DOUT data transitions on the serial clock's falling edge and is clocked into the processor on SCLK's rising edge. The first 8-bit data stream contains the first 8-bits of DOUT starting with the MSB. The second 8-bit data stream contains the remaining four result bits. DOUT then goes high impedance.

Figure 23. SPI Serial Interface Connections

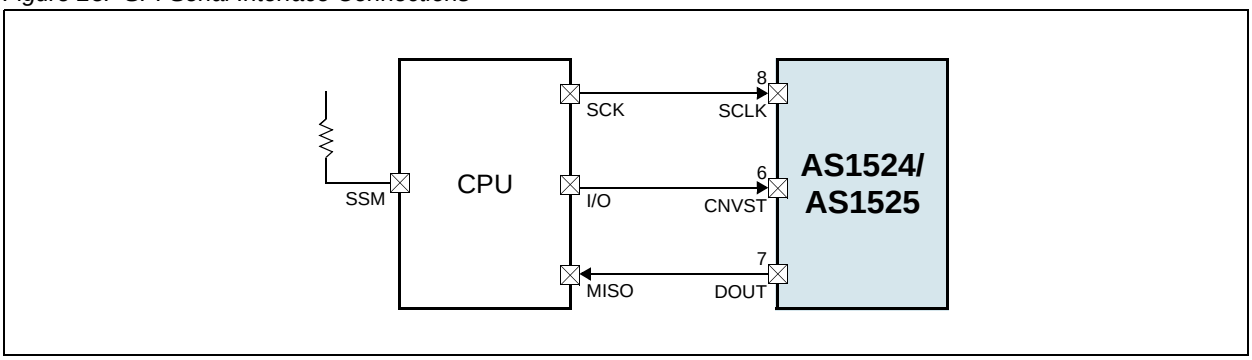


Figure 24. Microwire Serial Interface Connections

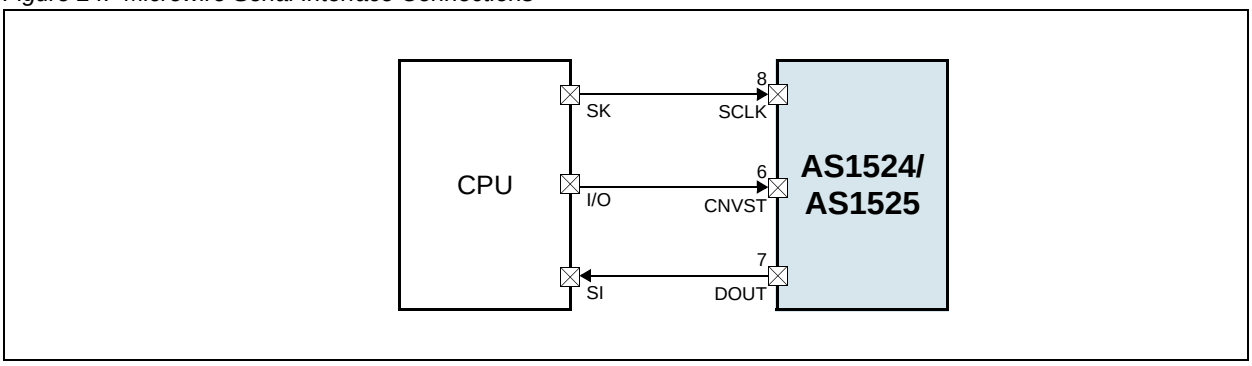
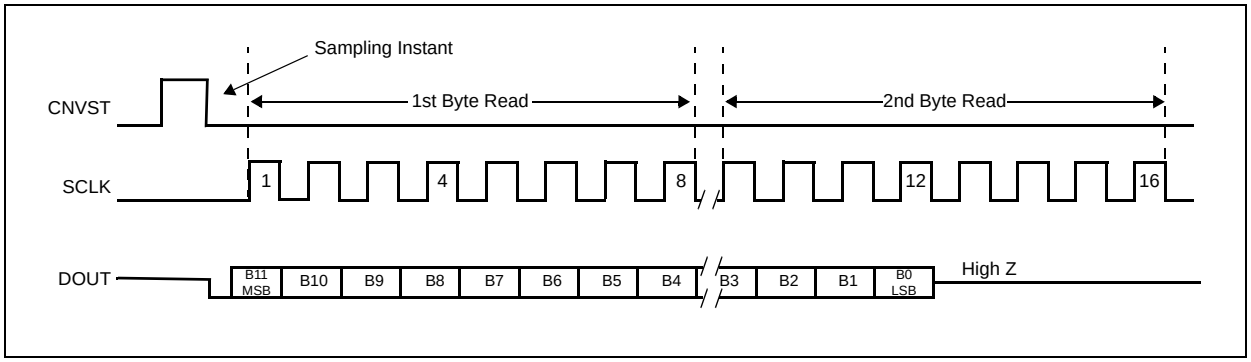


Figure 25. SPI/Microwire Interface Timing Diagram (CPOL = CPHA = 0)



QSPI Interface

Using the high-speed QSPI interface (Figure 26) with CPOL = 0 and CPHA = 0, the AS1524/AS1525 support a maximum f_{SCLK} of 8MHz. One 12- to 16-bit reads are necessary to obtain the entire 12-bit result from the AS1524/AS1525.

DOUT data transitions on the serial clock's falling edge and is clocked into the processor on SCLK's rising edge. The first 12 bits are the data. DOUT then goes high impedance (see Figure 24).

Figure 26. QSPI Serial Interface Connections

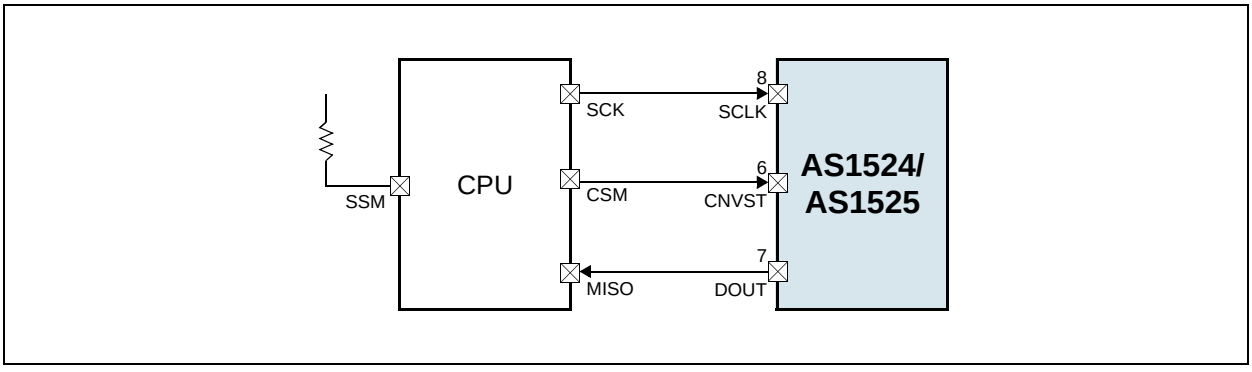
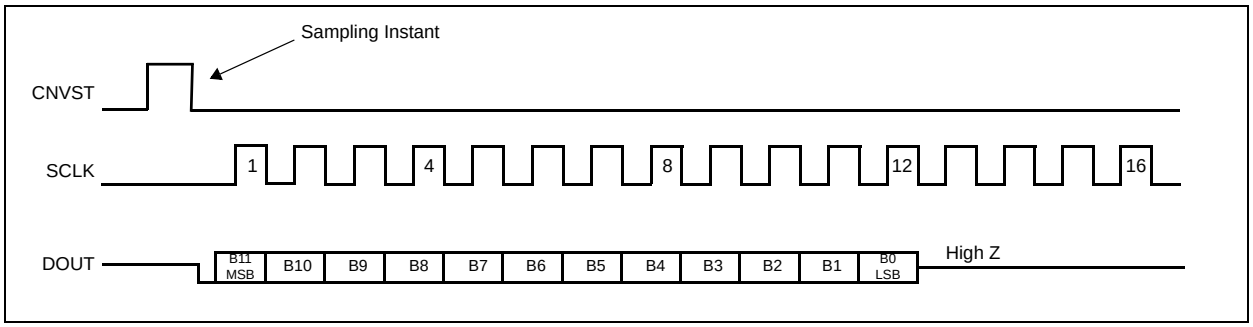


Figure 27. QSPI Serial Interface Timing (CPOL = CPHA = 0)

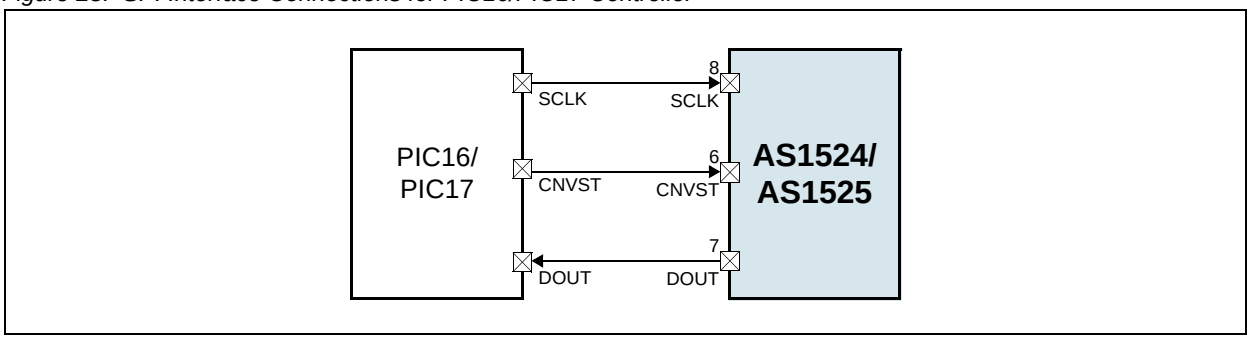


PIC16 and SSP Module and PIC17 Interface

The AS1524/AS1525 are compatible with a PIC16/PIC17 controllers, using the synchronous serial port (SSP) module

To establish SPI communication, connect the PIC16/PIC17 controllers as shown in Figure 28 and configure the PIC16/PIC17 as system master. This is done by initializing its synchronous serial port control register (SSPCON) and synchronous serial port status register (SSPSTAT) to the bit patterns shown in Table 6 on page 18 and Table 7 on page 18.

Figure 28. SPI Interface Connections for PIC16/PIC17 Controller



In SPI mode, the PIC16/PIC17 processor allow 8 bits of data to be synchronously transmitted and received simultaneously. Two consecutive 8-bit readings (see Figure 29) are necessary to obtain the entire 12-bit result from the AS1524/AS1525. DOUT data transitions on the serial clock's falling edge and is clocked into the processor on SCLK's rising edge.

The first 8-bit data stream contains the first 8 data bits starting with the MSB. The second data stream contains the remaining bits, D3 through D0.

Figure 29. SPI Interface Timing with PIC16/PIC17 in Master Mode (CKE = 1. CKP = 0. SMP = 0, SSPM3:SSPM0 = 0001)

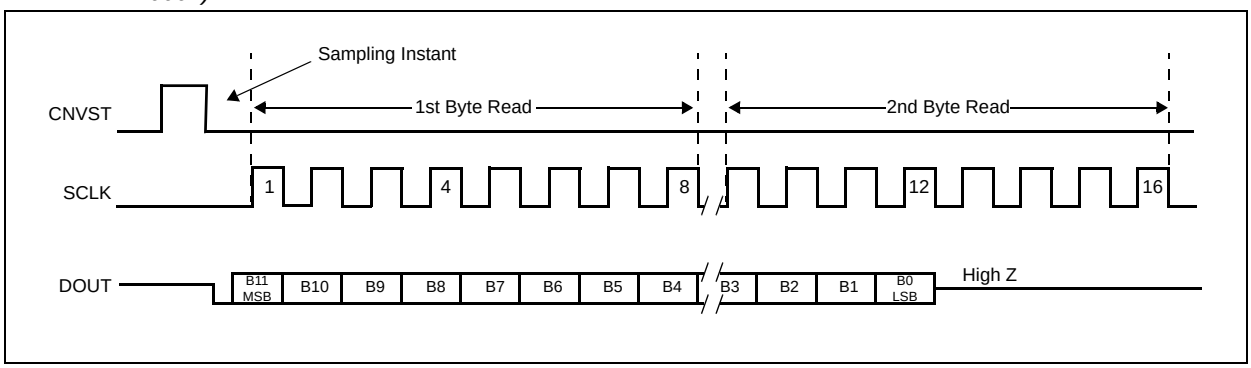


Table 6. SSPCON Register Settings

Control Bit		AS1524/AS1525 Setting	Synchronous Serial Port Control Register (SSPCON)
WCOL	Bit 7	X	**Write Collision Detection Bit**
SSPOV	Bit 6	X	**Receive Overflow Detect Bit**
SSPEN	Bit 5	1	**Synchronous Serial Port Enable** 0: Disables serial port and configures these pins as I/O port pins. 1: Enables serial port and configures SCK, SDO, and SCI pins as serial port pins.
CKP	Bit 4	0	**Clock Polarity Select Bit**. CKP = 0 for SPI master mode selection.
SSPM3:1	Bit 3:1	0	**Synchronous Serial Port Mode Select Bit.** Sets SPI master mode and selects FCLK = fOSC / 16.
SSPM0	Bit 0	1	

Table 7. SSPSTAT Register Settings

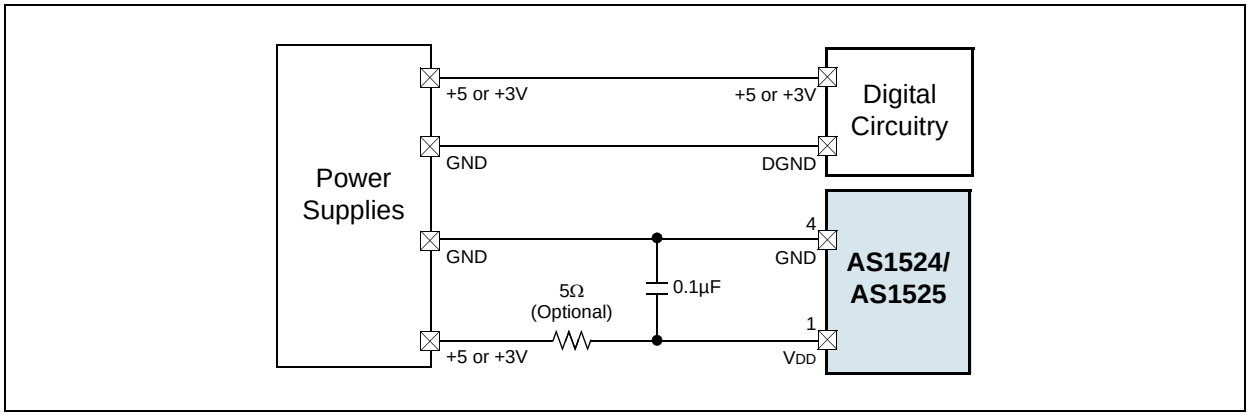
Control Bit		AS1524/AS1525 Setting	Synchronous Serial Status Register (SSPSTAT)
SMP	Bit 7	0	**SPI Data Input Sample Phase.** Input data is sampled at the middle of the data output time.
CKE	Bit 6	1	**SPI Clock Edge Select Bit.** Data is transmitted on the rising edge of the serial clock.
D/A	Bit 5	X	**Data Address Bit**
P	Bit 4	X	**Stop Bit**
S	Bit 3	X	**Start Bit**
R/W	Bit 2	X	**Read/Write Bit Information**
UA	Bit 1	X	**Update Address**
BF	Bit 0	X	**Buffer Full Status Bit**

Layout and Grounding Considerations

The AS1524/AS1525 require proper layout and design procedures for optimum performance.

- Use printed circuit boards; wirewrap boards should not be used.
- Separate analog and digital traces from each other. Analog and digital traces should not run parallel to each other (especially clock traces).
- Digital traces should not run beneath the AS1524/AS1525.
- Use a single-point analog ground at GND, separate from the digital ground (see Figure 30). Connect all other analog grounds and DGND to this star ground point for further noise reduction. No other digital system ground should be connected to this single-point analog ground. The ground return to the power supply for this ground should be low impedance and as short as possible for noise-free operation.
- High-frequency noise in the V_{DD} power supply may affect the AS1524/AS1525 high-speed comparator. Bypass this supply to the single-point analog ground with 0.1µF and 4.7µF bypass capacitors (see Figure 30). The bypass capacitors should be placed as close to the device as possible for optimum power supply noise-rejection. If the power supply is very noisy, a 10Ω resistor can be connected as a low-pass filter to attenuate supply noise
- Power components such as the inductor, converter IC, filter capacitors, and output diode should be placed as close together as possible, and their traces should be kept short, direct, and wide.
- Keep the voltage feedback network very close to the device, within 5mm (0.2”) of the pin.
- Keep noisy traces, such as those from the pin LX, away from the voltage feedback network and guarded from them using grounded copper traces.

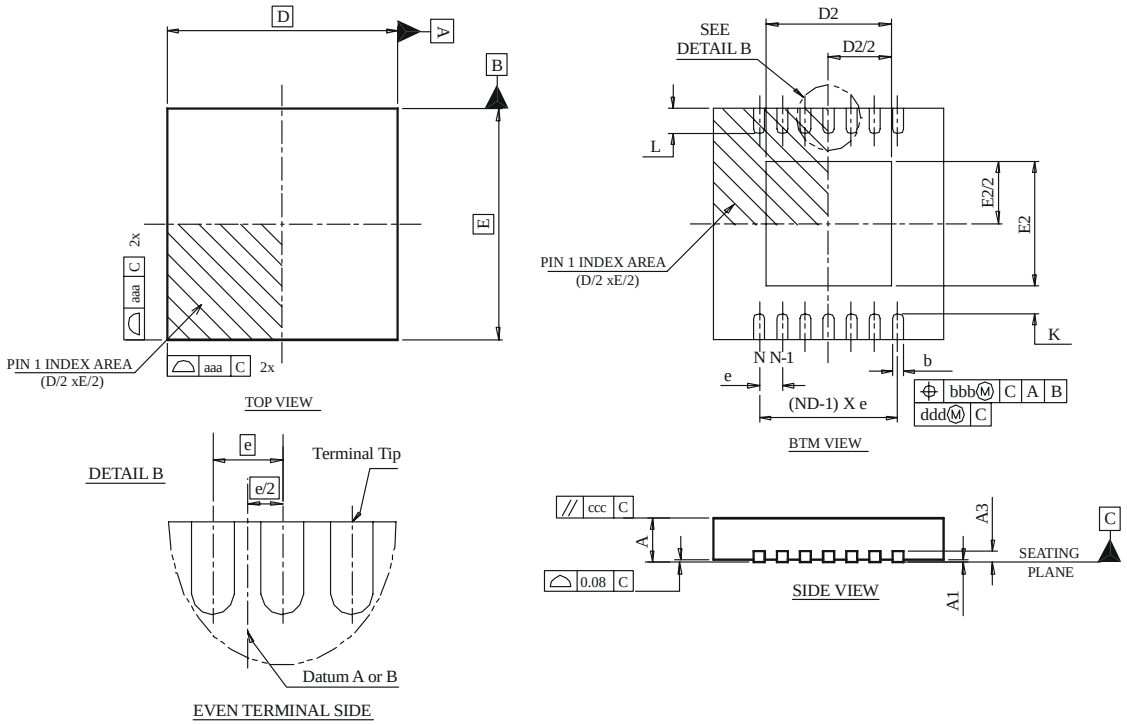
Figure 30. Recommended Ground Design



10 Package Drawings and Markings

The devices are available in a 8-pin TDFN (3x3mm) package.

Figure 31. 8-pin TDFN (3x3mm) Packagee



Symbol	Min	Typ	Max	Notes
A	0.70	0.75	0.80	1, 2
A1	0.00	0.02	0.05	1, 2
A3		0.20 REF		1, 2
L1			0.15	1, 2
L2			0.13	1, 2
aaa		0.15		1, 2
bbb		0.10		1, 2
ccc		0.10		1, 2
ddd		0.05		1, 2
eee		0.08		1, 2
ggg		0.10		1, 2

Symbol	Min	Typ	Max	Notes
D BSC		3.00		1, 2
E BSC		3.00		1, 2
D2	1.60		2.50	1, 2
E2	1.35		1.75	1, 2
L	0.30	0.40	0.50	1, 2
θ	0º		14º	1, 2
K	0.20			1, 2
b	0.25	0.30	0.35	1, 2, 5
e		0.65		
N		8		1, 2
ND		4		1, 2, 5

Notes:

1. Figure 31 is shown for illustration only.
2. All dimensions are in millimeters; angles in degrees.
3. Dimensioning and tolerancing conform to *ASME Y14.5 M-1994*.
4. N is the total number of terminals.
5. The terminal #1 identifier and terminal numbering convention shall conform to *JEDEC 95-1, SPP-012*. Details of terminal #1 identifier are optional, but must be located within the zone indicated. The terminal #1 identifier may be either a mold or marked feature.
6. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
7. ND refers to the maximum number of terminals on side D.
8. Unilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals

11 Ordering Information

The devices are available as the standard products shown in Table 8.

Table 8. Ordering Information

Ordering Code	Description	Delivery Form	Package
AS1524-BTDT	150ksps, 12-Bit, 1-Channel True-Differential ADC	Tape & Reel	8-pin TDFN (3x3mm)
AS1524-BTDR	150ksps, 12-Bit, 1-Channel True-Differential ADC	Tray	8-pin TDFN (3x3mm)
AS1525-BTDT	150ksps, 12-Bit, 2-Channel Single-Ended ADC	Tape & Reel	8-pin TDFN (3x3mm)
AS1525-BTDR	150ksps, 12-Bit, 2-Channel Single-Ended ADC	Tray	8-pin TDFN (3x3mm)

Note: All products are RoHS compliant and Pb-free.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

For further information and requests, please contact us mailto:sales@austriamicrosystems.com
or find your local distributor at http://www.austriamicrosystems.com/distributor

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