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Contact information:

Headquarters:
ams AG
Tobelbaderstrasse 30
8141 Unterpremstaetten, Austria
Tel: +43 (0) 3136 500 0
e-Mail: ams_sales@ams.com

Please visit our website at **www.ams.com**

AS3610/11

Switching Charger for Li-Ion/LiPo/LiFePO4 powered devices

1 General Description

The AS3610/11 is a highly integrated standalone or optional I²C controlled step down charger. All supervision and regulation functions are realized internal and independent from the processor.

The 100/500mA USB current limit can be set via a dedicated control pin. Other limits like 900mA can be programmed in the OTP ROM.

In addition, the Charger can generate a 5.05V output supply at VBUS for USB OTG.

AS3610 features an I2C interface which can be used by a micro-controller to fully control all functionality of the chip. Charging current and EOC current can be set with external resistors and adjusted via register settings if needed.

AS3611 is a stand-alone version of this charger IC. Charging and EOC current is set by resistor only. Functions like OTG boost mode or max current limit for wall adapter mode can be enabled using dedicated pins.

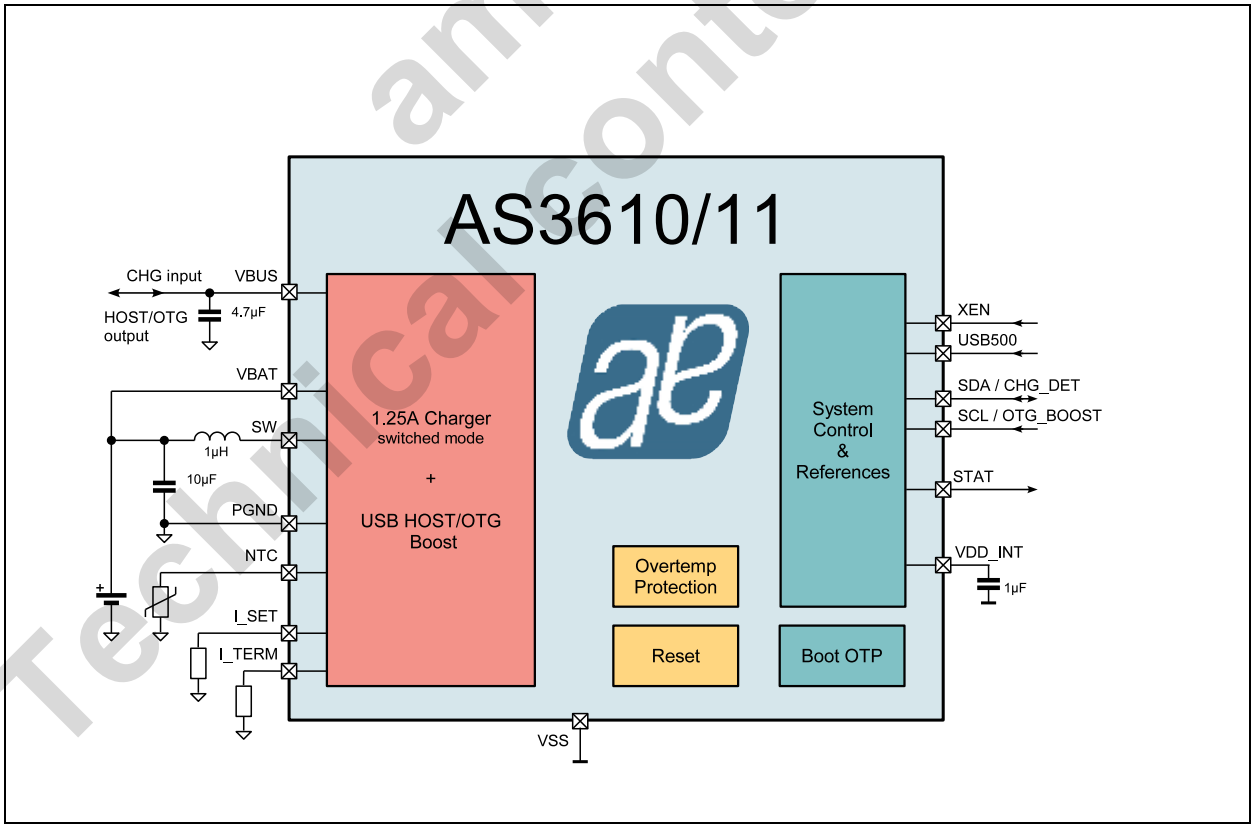
2 Key Features

- DCDC USB Charger
- 1.25A, 3MHz DCDC Charger
- OTG Boost with low IQ (700µA) up to 500mA
- 22V over voltage protection
- Seamless 100% Mode
- Reverse Polarity protection on VBUS
- NTC support
- Low side LED driver
- No external shunt resistor required
- "No Battery" operation without voltage drop
- Package: MLPD14 3x3mm

3 Application

The device is ideal as 1 Cell LiIon, LiPo or LiFePO4 charger for mobile phones and portable devices.

Figure 1. AS3610/11 Block Diagram



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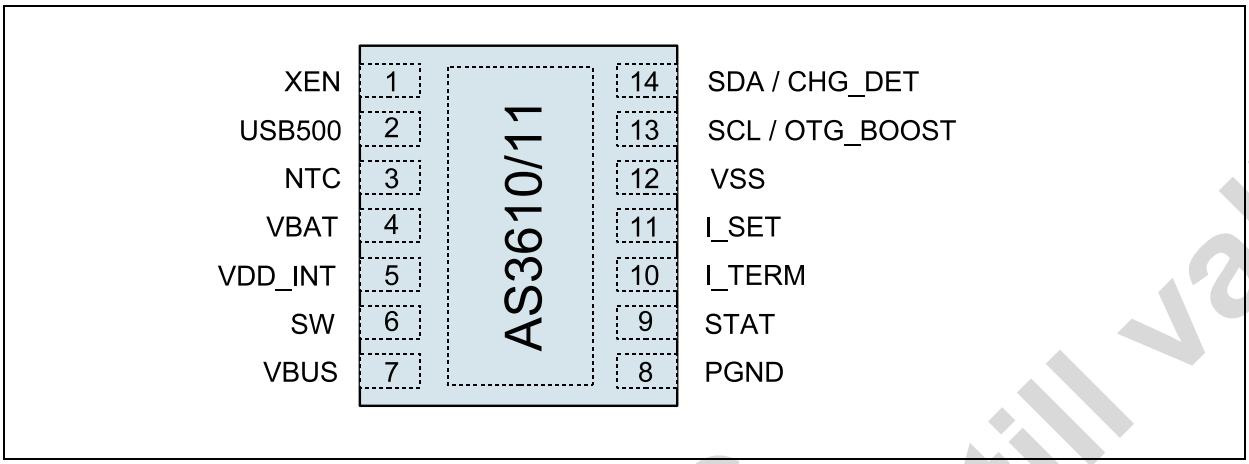
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4 Pin Assignments

Figure 2. AS3610/11 Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name AS3610	Pin Name AS3611	Pin Type	Supply	Description
1	XEN	XEN	I	VBAT	XEnable pin for step down charger
2	USB500	USB500		VBAT	Set current limit in charger mode. 100mA / 500mA USB current limit.
3	NTC	NTC	Analog pin	VDD_INT	NTC input
4	VBAT	VBAT			Analog Sense input
5	VDD_INT	VDD_INT			Connect 1µF (0402) for internal LDO supply 2.5V
6	SW	SW	Power pin		SW node of step down charger. Connect to 1µH inductor (chip coil)
7	VBUS	VBUS			Charger input (USB voltage or charger voltage)
8	PGND	PGND			Power GND connection of step down charger
9	STAT	STAT	Digital Open Drain Output pin		Pulled to GND for error / status indication via LED
10	I_TERM	I_TERM	Analog pin	VBAT	Sets trickle / EOC current
11	I_SET	I_SET		VBAT	Sets charging current (Constant current)
12	VSS	VSS			Analog VSS
13	SCL		Digital Open Drain Output pin; Requires an external pull-up resistor	VBAT	I²C clock line
		OTG_BOOST	I	VBAT	switches mode to OTG boost
14	SDA		Digital Open Drain Output pin; Requires an external pull-up resistor	VBAT	I²C data line
		CHG_DET	I	VBAT	selects the highest input current limit for wall adapter charging

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5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Operating Conditions on page 5 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
V_HV20	High voltage pins	-2	22	V	Applicable to high voltage pins: VBUS, SW, STAT
V_MV	5V pins	-0.3	7.0	V	Applicable to 5V-pins: VBAT, XEN, SDA, SCL, USB500, I_SET, I_TERM
V_LV	3.3V pins	-0.3	5.0	V	Applicable to 3.3V-Pins: VDD_INT, NTC
IIN	Input pin current	-100	+100	mA	Norm: JEDEC JESD78
Electrostatic Discharge					
VESD	Electrostatic discharge	+/-1500[1]		V	Norm: JEDEC JESD22-A114F
Temperature Ranges and Storage Conditions					
SCSB	Operating Temperature	-40	+85	°C	
TJ	Junction Temperature		+110	°C	
	Storage Temperature Range	-55	+150	°C	
	Humidity non-condensing	5	85	%	
Temperature (soldering)					
TBODY	Package Body Temperature		260	°C	Norm IPC/JEDEC J-STD-020[2] The lead finish for Pb-free leaded packages is matte tin (100% Sn)
	Moisture Sensitive Level	3			Represents a max. floor life time of 168h

1. pin STAT is +/-750V only
2. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices”

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6 Electrical Characteristics

VBAT=+2.7V...+5.5V, T_A =-40ºC...+85ºC. Typical values are at VBAT=+3.6V, T_A=+25ºC, unless otherwise specified.

The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Table 3. Operating Conditions

Symbol	Parameter	Notes	Min	Typ	Max	Unit
Operating Range						
V_{HV20}	High voltage pins	Applicable to high voltage pins: VBUS, SW.	-2	5.0	20	V
V_{MV}	5V pins	Applicable to 5V pins: VBAT, XEN, SDA, SCL, USB500, I_SET, I_TERM	-0.3		5.5	V
V_{LV}	3.3V pins	Applicable to 3.3V-Pins: VDD_INT, NTC	-0.3		3.6	V
T_{AMB}	Ambient Temperature		-40	25	85	deg
Operating Currents						
I_{VBUS_ACT}	VBUS current, if step down charger is active	I_{USB} limit > 100mA		10		mA
		I_{USB} limit < 100mA		5		mA
I_{BOOST}	VBAT current, if boost active without load	V_{BAT}=4.2V		700		µA
I_{VBUS_OFF}	VBUS current in OFF mode	V_{BUS}=5V, T_J < 85ºC		16		µA
I_{VBAT}	VBAT quiescent current in OFF mode	V_{BAT}=4.2V, T_J < 85ºC Including leakage current to V_{BUS}		16		µA
Charging Mode Parameter						
V_{BUS_UVLO}	VBUS undervoltage lockout	Step Down charger disabled below this threshold. -150mV hysteresis	3.7	3.8	3.9	V
V_{BUS_OV}	VBUS overvoltage off mode	Step Down charger disabled above this threshold. -140mV hysteresis	6.3	6.5	6.7	V
V_{BUS_min}	VBUS minimum voltage to regulate current to VBAT	Programmable (2-bit)	Vnom - 0.12	3.9 4.2 4.5 4.7	Vnom+ 0.12	V
I_{CHARGE}	Charge current accuracy of mean output current	Current selected by resistor on I_{SET} pin: I_{CHARGE} = 21450/R_{SET} and register const_curr<1:0>	-8%	550… 1250	+8%	mA
I_{TERM}	Termination and trickle (precharge) current	Current selected by resistor on I_{TERM} pin: I_{TERM} = 1200/R_{TERM}	-40mA or -30%	50… 200	+40mA or +30%	mA
I_{USB}	USB input current limit resistor	100mA USB current limit	88	93	105	mA
		500mA USB current limit	450	475	500	mA
		900mA USB current limit	800	850	900	mA
V_{SOFT}	Apply I_{SOFT} current below this VBAT voltage	Hysteresis -100mV	1.9	2.0	2.1	V
I_{SOFT}	Soft current, if VBAT is below V_{SOFT}		25	38	55	mA
$V_{TRICKLE}$	Apply trickle current (=I_{TERM}) below this VBAT voltage		-0.1	2.9	+0.1	V
V_{CHARGE}	End of charge voltage	20mV steps Programmable		3.5...4.44		
	End of charge accuracy	4.2V EOC voltage, -40..85°C	-1		+1	%
V_{CHDET}	Charge detect voltage difference	V_{BUS}-V_{BAT}	+1	+40	+100	mV

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Table 3. Operating Conditions

Symbol	Parameter	Notes	Min	Typ	Max	Unit
V_{RESUME}	Resume voltage	$V_{THRESHOLD} = V_{CHARGE} - V_{RESUME}$		120		mV
R_{PMOS}	Resistance of PMOS switch			300		mΩ
R_{NMOS}	Resistance of NMOS switch			300		mΩ
f_{OSC}	Switching frequency		2.7	3.0	3.3	MHz
D_{MAX}	Maximum duty cycle	Smooth transition. No skipmode.			100	%
T_{MIN}	Minimum ON time of PMOS	Minimum ON time of PMOS. Below this value, transition to pulseskip mode		60		nsec
I_{COIL}	Coil current limit			1.7		A
Boost Mode Parameter						
V_{BOOST}	VBUS regulated voltage in boost mode		4.9	5.05	5.2	V
I_{BOOST}	Boost current	2.7<V_{BAT}<4.5 (boost_lowcurr=1)	200			mA
I_{HBOOST}	Boost current (high current mode)	3.2<V_{BAT}<4.5 (boost_lowcurr=0)	500			mA
I_{COIL}	Coil current limit			0.75 1.5		A
I_{SU}	Stepup no load current on VBAT	V_{BAT}=4.2V		700		µA
Thermal Limitation						
T_{REG}	Thermal current regulation for charger mode			110		°C
T_{SHDOWN}	Thermal shutdown limit			140		°C
NTC Charging Temperature Range						
$V_{BATTEMP_ON}$	Battery Temperature high level (50 or 55 ºC) NTCbeta = 4200	ntc_temp=0		500 or 400		mV
$V_{BATTEMP_OFF}$	Battery Temperature low level (45 or 50 ºC) NTCbeta = 4200	ntc_temp=1		600 or 500		mV
$I_{BATTEMP}$	NTC Bias Current	100kΩ NTC	-14%	15	+14%	µA
$I_{BATTEMP}$	NTC Bias Current	10kΩ NTC	-10%	150	+10%	µA
IO characteristics						
V_{IL}	SCL/CHG_DET, SDA/OTG_BOOST, USB500, XEN Low Level input voltage		-0.3		0.4	V
V_{IH}	SCL/CHG_DET, SDA/OTG_BOOST, USB500, XEN High Level input voltage		1.4		VBAT	V

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7 Typical Operating Characteristics

C_{VBAT}=10µF, C_{VBUS}=10µF, L=1µH,

Figure 3. USB Current (100mA limit)

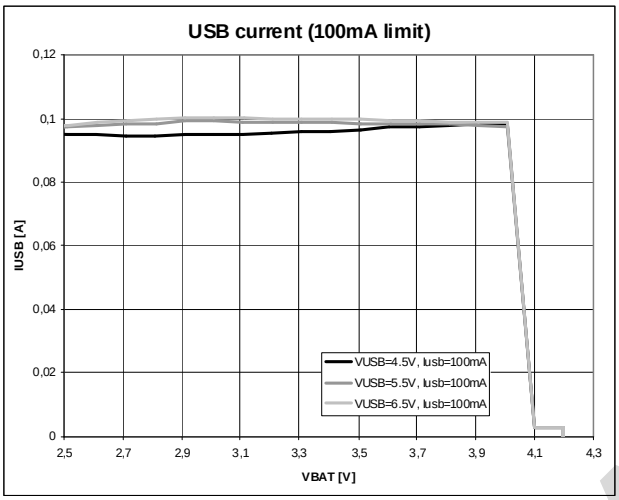


Figure 4. USB Current (500mA limit)

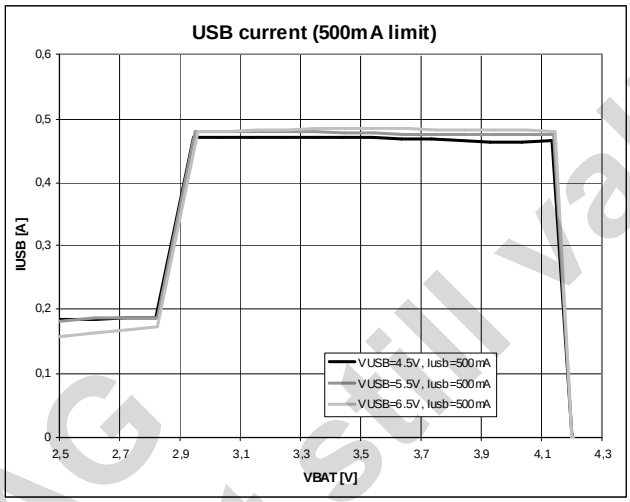


Figure 5. Current into Battery (100mA limit)

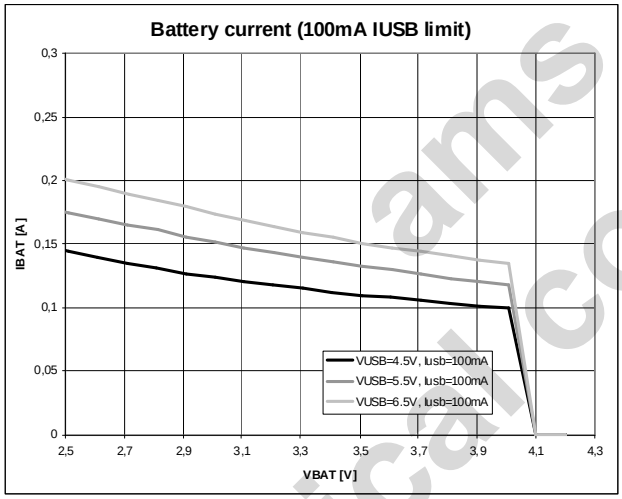
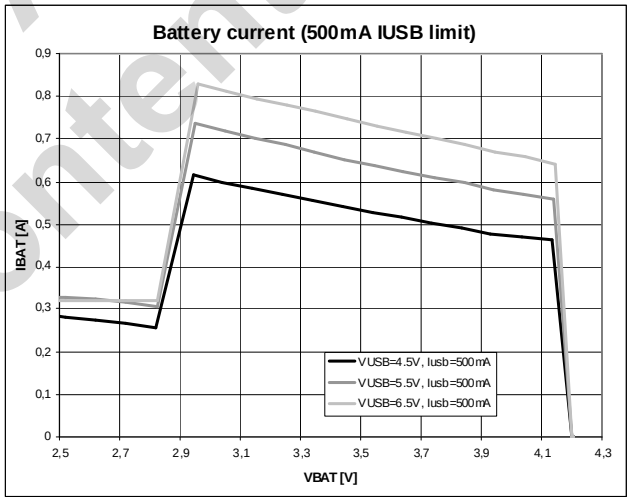


Figure 6. Current into Battery (500mA limit)



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Figure 7. Charging Cycle 1

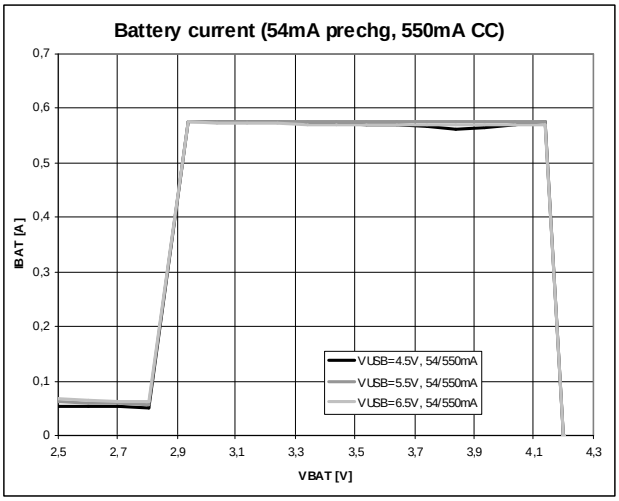


Figure 8. Charging Cycle 2

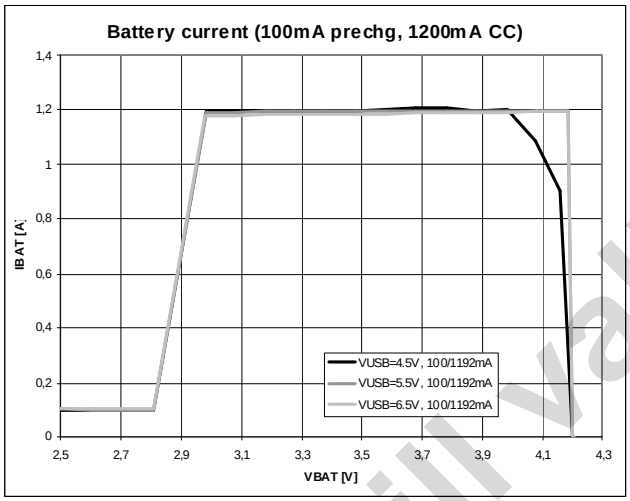


Figure 9. Efficiency @550mA

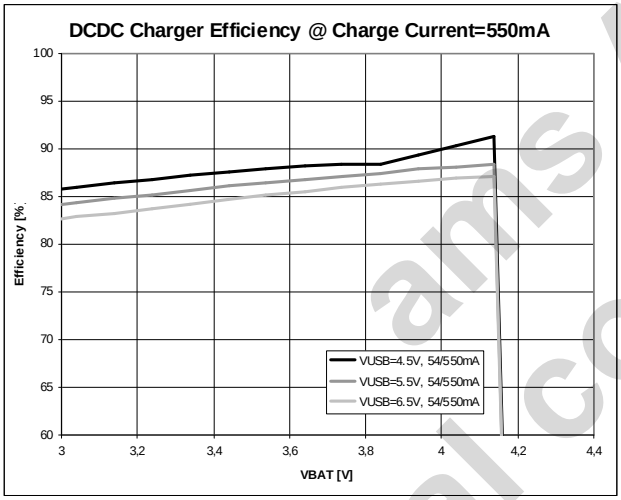


Figure 10. Efficiency @1.2A

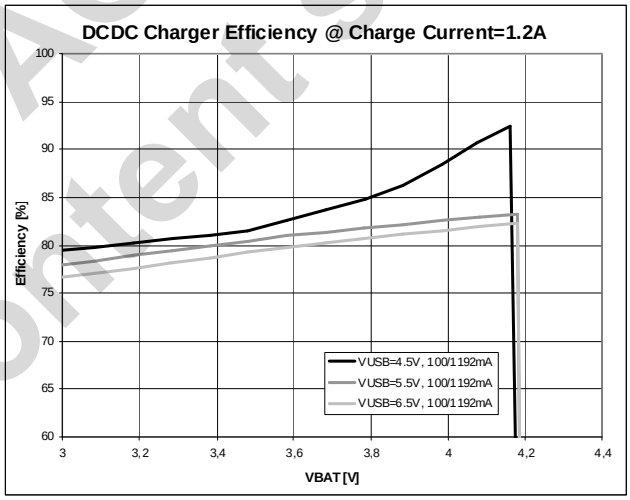


Figure 11. Boost Efficiency

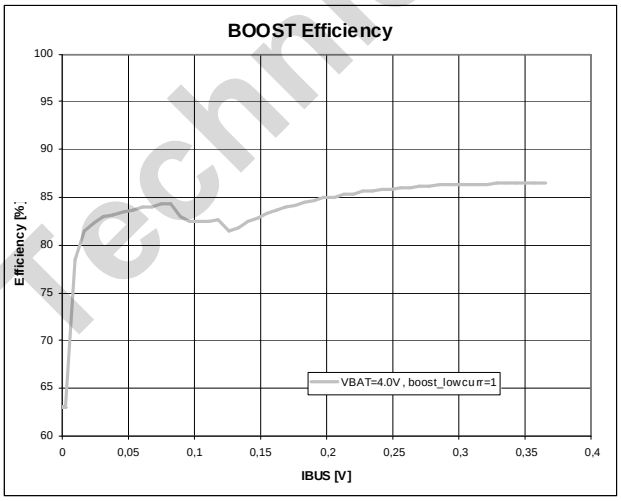
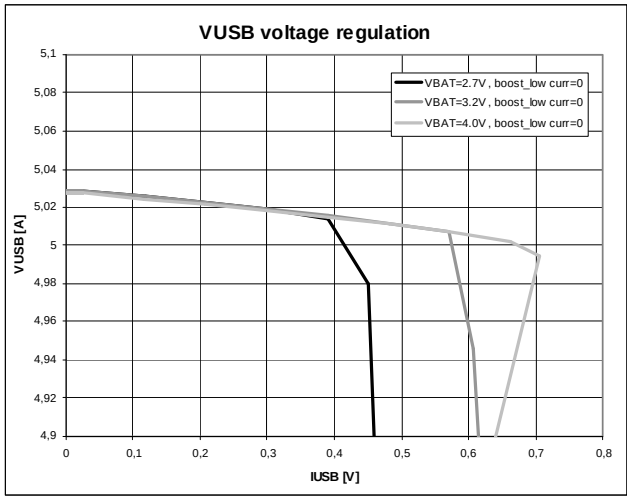


Figure 12. Booster Output Voltage



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8 Detailed Description

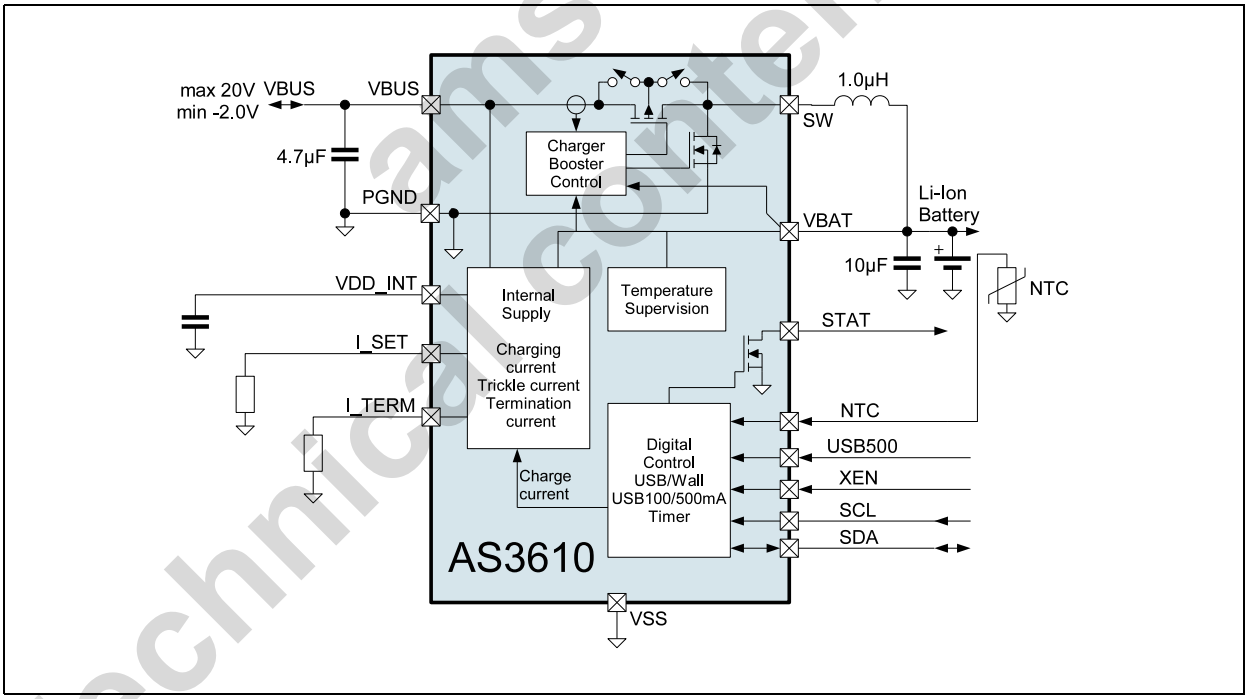
8.1 Charge Controller

8.1.1 General Description

The AS3610/11 device serves as a standalone battery charge controller supporting rechargeable Lithium Ion (Li+) batteries. Requiring only a few external components, a full-featured battery charger with a high degree of flexibility can easily be realized. The main features of the controller are:

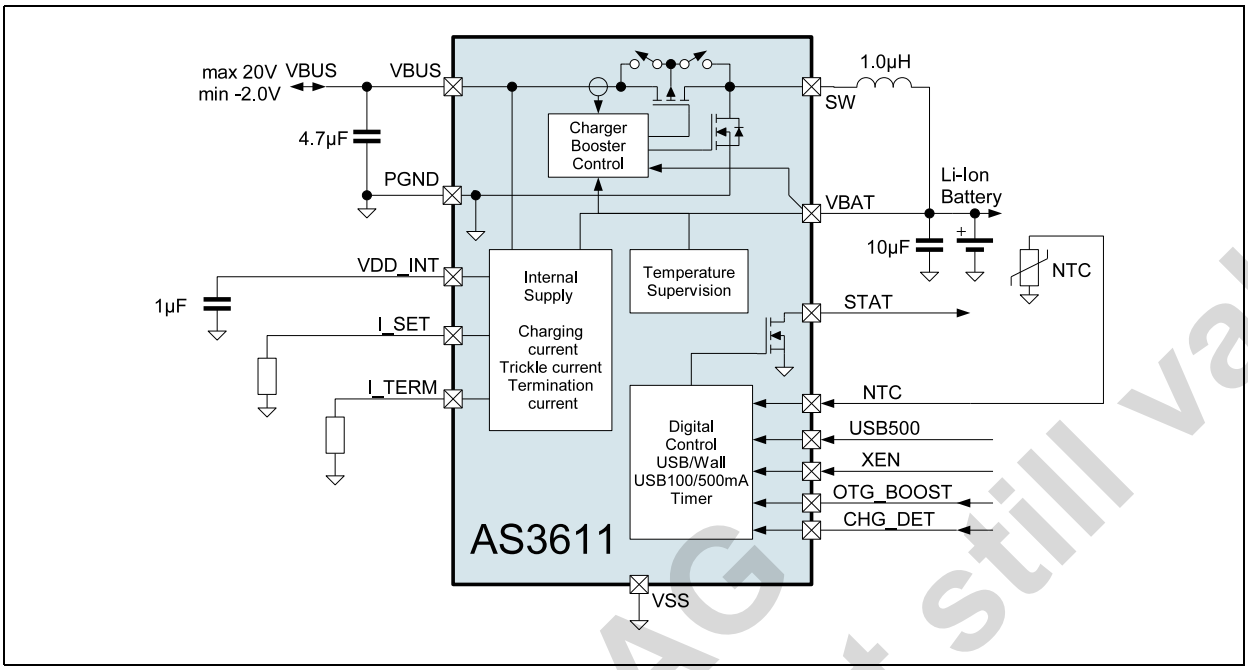
- Charge adapter detection
- Internal voltage regulator
- Low current (soft) charging
- Low current (trickle) charging
- Constant current charging
- Constant voltage charging
- 22V input overvoltage protection
- Battery presence indication
- Operation without battery
- Input current limitation
- Input voltage drop regulation

Figure 13. Detailed Block Diagram



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Figure 14. Detailed Block Diagram



8.1.2 Charging Cycle Description

8.1.2.1 Charge adapter detection

The charger uses an integrated detection circuit to determine if an external charge adapter has been applied to the VBUS pin. If the VBUS voltage exceeds the battery voltage at pin VBUS by V_{CHDET} the *ChDet* bit in the *ChargerStatus1* register will be set. That detection de-bounce time is approx. 300msec for rising *ChDet* and approx. 30msec for falling *ChDet* signal (*debounce_timer*=00b).

8.1.2.2 Low current soft charging

When the charger is detected and enabled (*chg_en*=1), no stop charging condition is active and the battery voltage is below V_{SOFT}, the charging cycle is started with soft_charging. In that mode the charger is acting as a linear charger down to VBAT. With a current of I_{SOFT}

8.1.2.3 (Trickle) Pre-charging

If the battery voltage exceeds V_{SOFT}, but is below $V_{TRICKLE}$, and the bit *prechg_en* is set, the trickle charging is started.

In that mode the charging current is defined by the external resistor on pin I_TERM or the input current limit if e.g. 100mA input current limit is active.

8.1.2.4 Constant current charging

If the battery voltage is above $V_{TRICKLE}$ and below V_{EOC} (or above V_{SOFT} if *prechg_en*=0) the charging current is defined by the resistor on pin I_SET. In addition the current can be reduced by I2C with the register setting of *constcurr*. (AS3610 only)

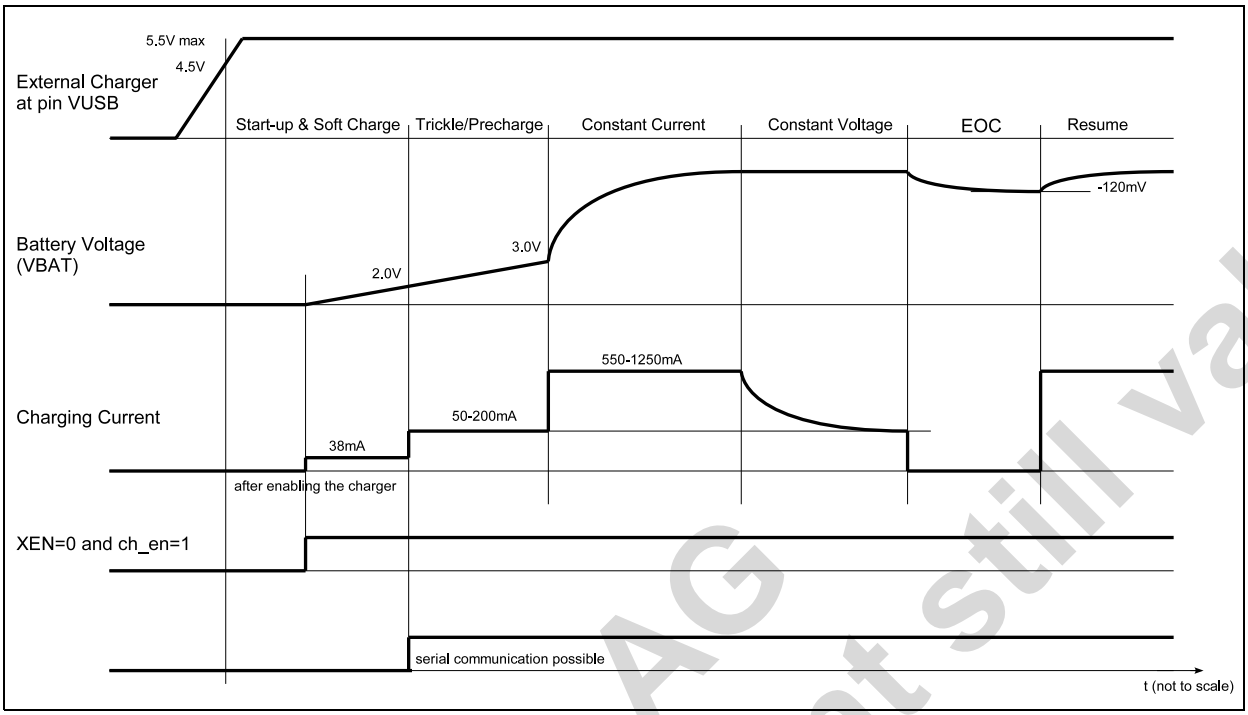
8.1.2.5 Constant voltage charging

Constant voltage charge mode is initiated, if the battery voltage has reached the V_{EOC} threshold.

The charge current is monitored during constant voltage charging. It will be decreasing from its initial value during constant current charging and eventually drop below the value set by the resistor on pin I_TERM. If the measured charge current is less than or equal to I_{TERM}, the charging cycle is terminated and *EOC* is set. The termination current may be reduce by a factor of 2 by setting the *eoccurr* bit to 1.

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8.1.3 Charger States



8.1.4 Stop charging conditions

There are multiple safety features implemented that trigger a stop_charging condition:

These are the following:

- Battery temperature too high. If *ntc_on*=1 and voltage at pin NTC is below $V_{BATTEMP}$
- Timeout timer expired (If *ch_timeout*>0 and charging time has been exceeded). Can be reset by unplugging the charger, setting *chg_en*=0 or writing *charging_tmax*=0
- V_{BUS_OV} exceeded
- VBUS_UVLO reached
- Die temp>140deg (ov_temp_140 set)

8.1.5 Battery presence indication and operation without battery

After EOC state is reached a timer for NOBAT detection is started. If there is no battery present, the voltage will drop to V_{NOBAT_REG}. Depending on the load on VBAT and the capacitor on VBAT this might take some milliseconds to 1 second. The charger will restart charging (ConstantCurrent charging) after 100msec.

The 100msec dead time is necessary to get a battery oscillation frequency of below 10Hz, if there is no battery present and NTC battery detection is not enabled.

If No_bat_det=1 and the NOBAT detection timer is below 2 seconds after reaching EOC state, and this happens 2 times in serial, the state “operation without battery” is entered.

If the nobat_ntc_det bit is set the looping described above will be stopped and a NTC detection is started.

A pull up current of 0.5uA is applied to NTC. If the NTC voltage is above 1.8V, the state machine stays in the no bat state. If the BATTEMP voltage is below 1.8V, a charging cycle is restarted.

8.1.6 VBUS undervoltage regulation

If the voltage on VBUS drops below Vchg_min the current is regulated down to avoid overloading of the input source.

8.1.7 Charger overvoltage protection

This blocks checks if the charger voltage V_{BUS} is above V_{BUS_OV}. In that case the bit stop_charging is set and the charging is stopped until V_{BUS} is below V_{BUS_OV}.

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8.1.8 NTC supervision

This charger block also features a supply for an external NTC resistor to measure the battery temperature while charging. If the temperature is too high (voltage on NTC pin is below VBATTEMP_ON) the charger will stop operation (stop_charging=1).

When the battery temperature drops, the voltage on NTC pin will rise above VBATTEMP_OFF and the charger will start charging again. This is forming a temperature hysteresis of about 3 to 5°C to avoid an oscillation of the charger.

The levels for switching off the charger (**ntc_temp**: 45ºC or 55ºC) as well as the type of NTC (**ntc_10k**: 10k or 100k) can be selected via register settings. The battery temperature supervision via the NTC can be switched off (**ntc_on** = 0).

The supply for the NTC will be only on when a charger is detected and **ntc_on** bit is set.

8.2 Step up converter mode (OTG Boost)

The step down charger can also be used in a boost mode providing an output voltage V_{BOOST} on pin V_{BUS} typ 5.05V. In that mode the current direction is inverted to the charging mode providing current from the battery to the V_{BUS} pin. To enable that mode, it's necessary that the charger is disabled (XEN=1 or chg_en=0) and the bit boost_en is set (and for AS3611 the pin OTG_BOOST=1). The bit boost_lowcurr selects the output current capability between 200mA and 500mA.

8.2.1 Softstart of OTG booster

There is a softstart implemented to reduced inrush current on the V_{BAT} input. For approx. 1msec after the booster is enabled the output current is limited below 100mA. After that startup time the full current is available.

8.2.2 Short-circuit and overvoltage protection circuit

To protect the booster, the battery capacity and the circuit connected to V_{BUS} there are multiple protection circuits implemented:

- VBAT drops below 2.6V (typ)
- VBUS is above 5.3V (typ)
- Booster is in current limit operation (e.g. output V_{BUS} is overloaded or shorted to GND)

If one of these conditions is valid for more that 30msec debounce time (*debounce_timer*=00b), the booster is stopped and the boost_error bit is set. To restart the booster it's necessary to set boost_en=0 and 1 again. (For AS3611 the OTG_BOOST pin has to be set to 0 and 1 again).

If the die Temp is above 140deg the booster is stopped and restarted automatically when the die temperature drops.

8.3 2-Wire-Serial Control Interface

8.3.1 Feature List

- Fast-mode capability (max. SCL-frequency is 400 kHz)
- 7+1-bit addressing mode
- 60h x 8-bit data registers (word address 0x00 - 0x60)
- Write formats: Single-Byte-Write, Page-Write
- Read formats: Current-Address-Read, Random-Read, Sequential-Read
- SDA input delay and SCL spike filtering by integrated RC-components

8.3.2 Protocol

Table 4. 2-Wire Serial Symbol Definition

Symbol	Definition	RW	Note
S	Start condition after stop	R	1 bit
Sr	Repeated start	R	1 bit
DW	Device address for write	R	1000 1100b (8Ch)
DR	Device address for read	R	1000 1101b (8Dh)
WA	Word address	R	8 bit
A	Acknowledge	W	1 bit
N	No Acknowledge	R	1 bit

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Table 4. 2-Wire Serial Symbol Definition

Symbol	Definition	RW	Note
reg_data	Register data/write	R	8 bit
data (n)	Register data/read	W	8 bit
P	Stop condition	R	1 bit
WA++	Increment word address internally	R	during acknowledge

Figure 15. Byte Write

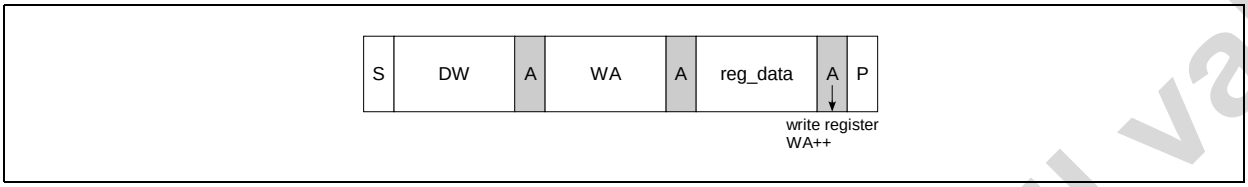
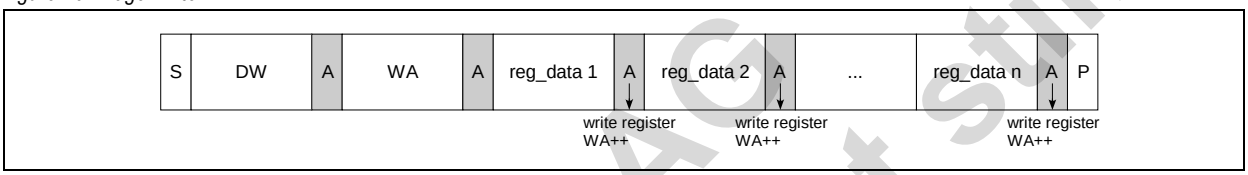


Figure 16. Page Write

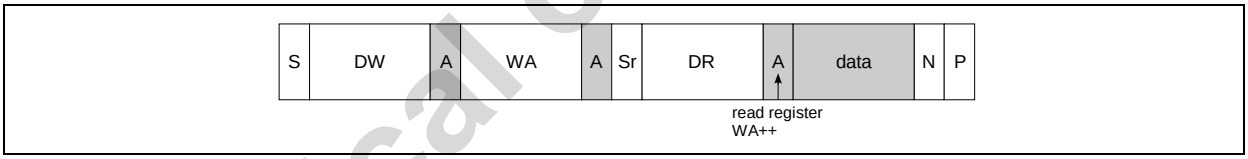


Byte Write and Page Write formats are used to write data to the slave.

The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

Figure 17. Random Read

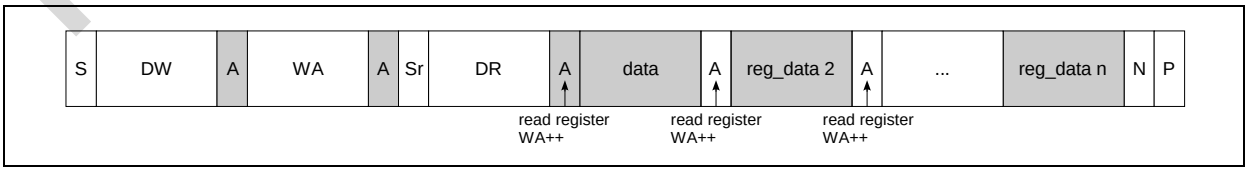


Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

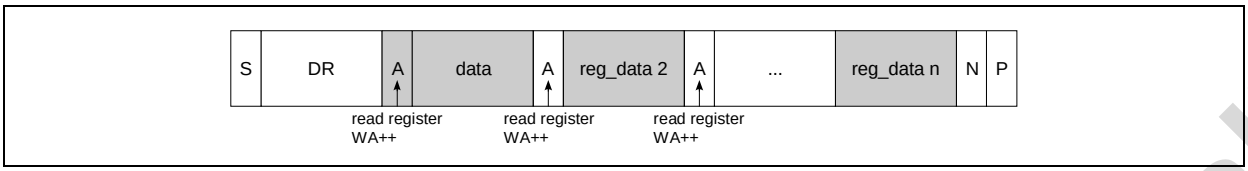
Figure 18. Sequential Read



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Sequential Read is the extended form of Random Read, as more than one register-data bytes are transferred subsequently. In difference to the Random Read, for a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and generate the STOP condition subsequently.

Figure 19. Current Address Read



To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address. Analogous to Random Read, a single byte transfer is terminated with a not-acknowledge after the 1st register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes has to be responded with an acknowledge from the master. For termination of the transmission the master sends a not-acknowledge following the last data byte and a subsequent STOP condition.

The AS3610 is compatible to the NXP two wire specification http://www.nxp.com/acrobat_download2/literature/9398/39340011.pdf Version 2.1 January 2000 for standard and fast mode (no high speed mode).

8.4 AS3611 pre-programmed variants

AS3611 is intended to work stand-alone with out an micro-controller. For this use case some of the basic configurations have to be pre-programmed into the device. Two basic configurations are shown in the tables below. Adaptations to these configurations are possible upon request.

Table 5. AS3611-A stand alone version for Li-Ion/LiPo,100kOhm NTC

Reg. Addr.	Value	Description	Reg. Name
0	7Fh	standalone mode=1, Boost_en=1, prechg_en=1, nobat_det=0	Charger Control
1	63h	Veoc=4.2V, Vchg_min=4.2	Charger Voltage Control
2	00h		Charger Current Control
3	05h	100kOhm NTC, low_temp range (45/50°C)	NTC Supervision
4	8Ah	ch_timeout=5h, stat_mode: charging=on; EOC=1Hz blinking, stop_charging or boost_error=5Hz	Charger supervision

Table 6. AS3611-B stand alone version for Li-Ion/LiPo,10kOhm NTC

Reg. Addr.	Value	Description	Reg. Name
0	7Fh	standalone mode=1, Boost_en=1, prechg_en=1, nobat_det=0	Charger Control
1	63h	Veoc=4.2V, Vchg_min=4.2	Charger Voltage Control
2	00h		Charger Current Control
3	07h	10kOhm NTC, low_temp range (45/50°C)	NTC Supervision
4	8Ah	ch_timeout=5h, stat_mode: charging=on; EOC=1Hz blinking, stop_charging or boost_error=5Hz	Charger supervision

Table 7. AS3611-C stand alone version for FePO4, 10kOhm NTC

Reg. Addr.	Value	Description	Reg. Name
0	7Fh	standalone mode=1, Boost_en=1, prechg_en=1, nobat_det=0	Charger Control
1	47h	Veoc=3.64V, Vchg_min=4.2	Charger Voltage Control
2	01h	eoccurr=1	Charger Current Control
3	05h	100kOhm NTC, low_temp range (45/50°C)	NTC Supervision
4	A6h	ch_timeout=3h, stat_mode: ch_det=on; EOC=1Hz blinking, stop_charging or boost_error=5Hz	Charger supervision

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8.5 Register Description

Charger Control Register (Address 0).

Addr: 0		Charger Control			
		This register controls the mode of the charger and the charger state machine.			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
0	Chg_en	1b/ROM	R/W	ON/OFF control of USB charger input	
				0 **1**	Charger disabled **Charger enabled, if XEN=0**
1	Boost_en	0b/ROM	R/W	ON/OFF control of Step up for USB OTG Normal operation (usb current=0..6):	
				0 1	**Step up disabled** Step up enabled
				AS3611 standalone charger operation only w/o I²C (usb current=7)	
				0 1	**Step up disabled** Step up enabled, if OTG_BOOST=1, Step up disabled, if OTG_BOOST=0
4:2	usb_current	000b/ROM	R/W	USB input current limit, AS3610 I²C version only	
				000b	**100mA, if pin USB500=0** **500mA, if pin USB500=1**
				001b 010b 011b 100b 101b 110b	100mA 500mA limit 900mA limit unlimited NA unlimited
				111b	AS3611 stand alone charger only w/o I²C CHG_DET=1 and USB500=0 → 100mA limit CHG_DET=1 and USB500=1 → 500mA limit CHG_DET=0 and USB500=1 → unlimited current
5	prechg_en	1b/ROM	R/W	0	Pre-charge (trickle charge) disabled. Charger starts with constant current, if V_{BAT}>2.0V (current set by resistor I_SET)
				1	**Pre-charge (trickle charge) enabled. Charger starts with trickle current, if 2.9V>V_{BAT}>2.0V (Current set by resistor I_term)**
6	disable_toff	1b/ROM	R/W	0	Off time of step down charger enabled. If 100% pmos on mode is needed, off pulses are skipped
				1	**Off time of step down charger disabled. Smooth transition to 100% pmos on if needed (V_{BUS}-V_{BAT} is small)**
7	No_bat_det	1b/ROM	R/W	0	Nobat detection disabled.
				1	**Nobat detection enabled. If No Battery is detected a small current through NTC (approx. 0.5µA), checks if a battery is connected again. A NTC is necessary for that setting.**

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Charger Voltage Control Register (Address 1).

Addr: 1		Charger Voltage Control		
		This register controls the charger voltages.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
5:0	Veoc	100011b/ ROM	R/W	End of charge voltage on VBAT 0: 3.5V ...: ... **35: 4.2V** ...: ... 47: 4.44V
7:6	Vchg_min	00b/ROM	R/W	Minimum charger (VBUS) voltage. Current is regulated down, if VBUS voltage drops below this level: **0: VBAT < 3.9V** 1: VBAT < 4.2V 2: VBAT < 4.5V 3: VBAT < 4.7V

Charger Current Control Register (Address 2).

Addr: 2		Charger Current Control		
		This register controls the charger currents.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
0	eoccurr	0b/ ROM	R/W	Current ratio selection between trickle and EOC current (defined by resistor R_{TERM}) **0: EOC current = I_{TERM}, Trickle current = I_{TERM}** 1: EOC current = I_{TERM} / 2, Trickle current = I_{TERM}
2:1	constcurr	00b/ROM	R/W	ConstantCurrent setting **0: Constant Current = I_{CHARGE}** 1: Constant Current = 0.81*I_{CHARGE} 2: Constant Current = 0.60*I_{CHARGE} 3: Constant Current = 0.40*I_{CHARGE}
3	boost_lowcurr	0b/ROM	R/W	Current selection for boost mode **0: 500mA maximum current** 1: 200mA maximum current
4	NA	NA	NA	NA
5	en_pon	0b/ROM	R/W	Enables 100% on mode of PMOS **0: 100% mode disabled (smooth 100% mode, if disable_toff=1)** 1: 100% mode enabled.
7:6	deb_timer	00b/ROM	R/W	Select debounce timer **0: 30msec debounce timer for comparator output** 1: 3msec debounce timer 2: NA 3: NA

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NTC Supervision Register (Address 03).

Addr: 03		NTC Supervision		
		These bits define the battery temperature supervision.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
0	ntc_on	1b/ROM	R/W	ON/OFF control of battery NTC supervision 0 Disabled **1 Enabled**
1	ntc_10k	1b/ROM	R/W	Select NTC resistor type 0 100kΩ **1 10kΩ**
2	ntc_temp	1b/ROM	R/W	Select NTC temperature shutdown 0 high temperature range (50 or 55 °C) **1 low temperature range (45 or 50 °C)**

Charger Supervision Register (Address 04).

Addr: 04		Charger Supervision		
		These bits define charging timer settings.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3:0	ch_timeout	1010b/ROM	R/W	Charging timeout timer 0 Charging timer disabled 1 0.5 hour 2 1 hour 3 1.5 hour 4 2 hour 5 2.5 hour 6 3 hour 7 3.5 hour 8 4 hour 9 4.5 hour **10 5 hour** 11 5.5 hour 12 6 hour 13 6.5 hour 14 7 hour 15 7.5 hour
4	charging_tmax	0b/ROM	R/W	**0 Read: no timeout reached** **Write: reset charger timeout counter** 1 $t_{CHARGING,MAX}$ timeout reached and charging stopped
7:5	stat_mode	010b/ROM	R/W	Function of Status pin: 0 always off 1 ch_det=ON 2 ch_det=ON, stop_charging or boost_error=5Hz blinking 3 Charging=ON, stop_charging or boost_error=5Hz blinking **4 Charging=ON, EOC=1Hz blinking, stop_charging or boost_error=5Hz blinking** 5 ch_det =ON, EOC=1Hz blinking, stop_charging or boost_error=5Hz blinking

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Charger Status1 Register (Address 05).

Addr: 05		Charger Status1		
		These bits show the status of the charger.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
0	ChDet	NA	R	Bit is set when charge adapter has been detected on pin VBUS
1	CCM	NA	R	Bit is set when charger is in Constant current mode
2	Resume	NA	R	Bit is set when battery voltage has dropped below resume level
3	Trickle	NA	R	Bit is set when charger is in trickle charge mode
4	CVM	NA	R	Bit is set when charger is in top-off charge mode (constant voltage mode)
5	EOC	NA	R	Bit is set when charging has been terminated. Bit is cleared automatically when chg_en is cleared or charging is resumed.
6	Battemp_hi	NA	R	Bit is set, if temperature is greater than 50 or 55°C. Bit is evaluated if charger is detected.
7	NoBat	NA	R	Bit is set when battery detection circuit indicates that no battery is connected to the system. This is done by measuring the NTC value. ntc_on has to be 1.

Charger Status2 Register (Address 06).

Addr: 06		Charger Status2		
		These bits show the status of the charger.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
0	LowBat	NA	R	Set, if V_{BAT}<2V
1	OVBat	NA	R	Set, if V_{BAT}> 1.17*V_{CHARGE}
2	LowBus	NA	R	Set, if V_{BUS}<3.8V
3	OVBus	NA	R	Set, if V_{BUS}>6.5V
4	UVLBus	NA	R	Set, if V_{BUS}<3.3V
5	Boost_act	NA	R	Set, if boost mode active
6	Boost_err	NA	R	Set, if boost error active. (Overcurrent of booster for more than debounce time, V_{BAT}<2.5V, V_{BUS}>6.5V or current limit is active
7	Stop charging	NA	R	Set if charger is stopped because of the following reason: - Timeout timer expired - NTC temperature error (Hightemp) - OVBus set - OVBat set - UVLBus set - Die temp>140deg (ov_temp_140 set)

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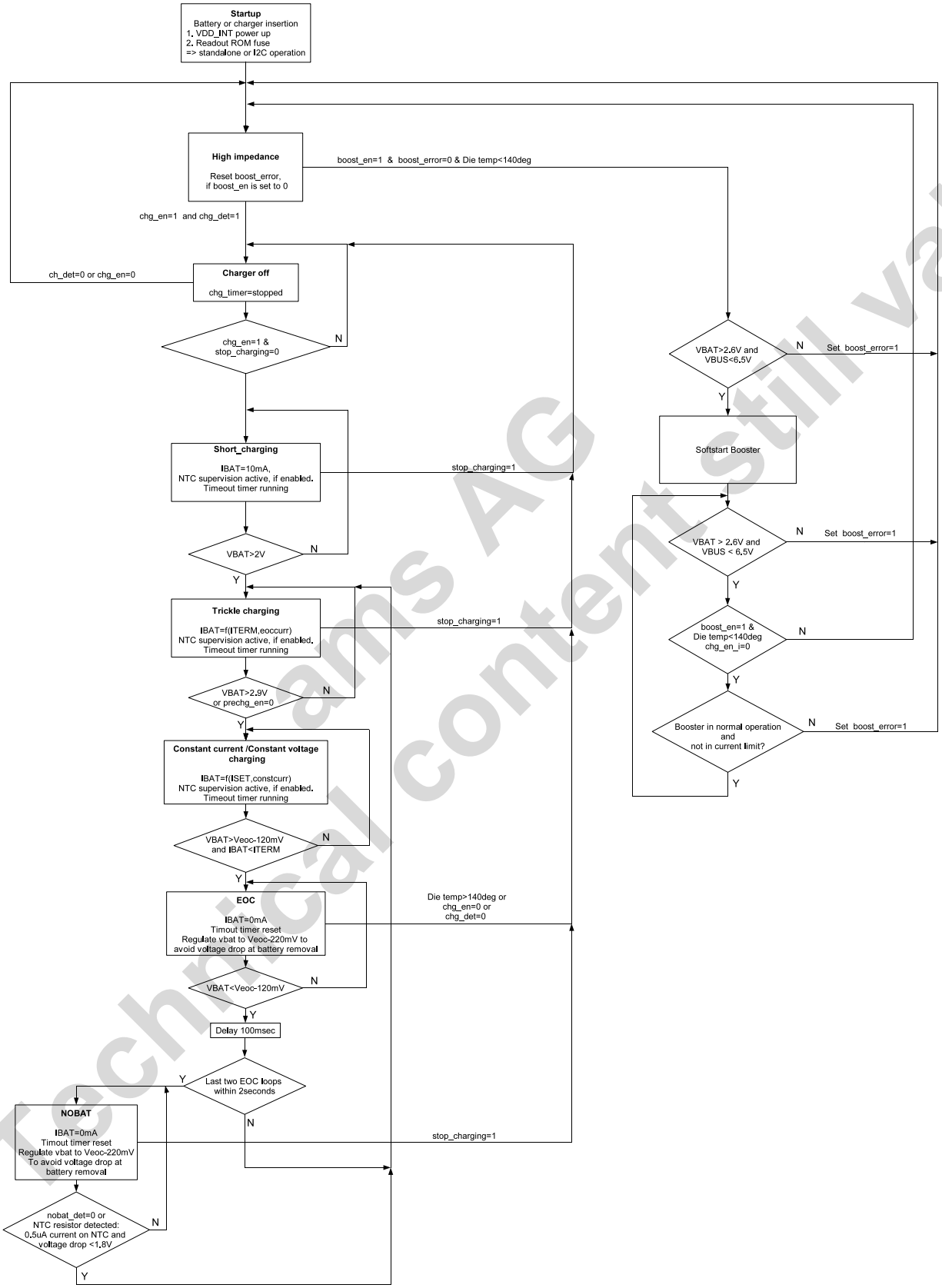
8.6 Register Overview

Table 8. Register table

Register	dec	hex	Default	b7	b6	b5	b4	b3	b2	b1	b0
ChargerControl1	0	0h	E1h	No_bat_det	disable_toff	prechg_en	usb_current<2:0>			Boost_en	Chg_en
Charger Voltage Control	1	1h	63h	Vchg_min		Veoc					
Charger Current Control	2	2h	10h	deb_timer		en_pon		boost_low curr	constcurr		eoccurr
NTC supervision	3	3h	01h						ntc_temp	ntc_10k	ntc_on
Charger supervision	4	4h	4Ah	stat_mode			charging_tmax	ch_timeout			
ChargerStatus1	5	5h	NA	NoBat	Battemp_hi	EOC	CVM	Trickle	Resume	CCM	ChDet
ChargerStatus2	6	6h	NA	bat_precheg	Boost_err	Boost_act	UVLBus	OVBus	LowBus	OVBat	LowBat
ASIC_ID1	62	3Eh		1	1	0	0	1	0	1	1
ASIC_ID2	63	3Fh		0	1	0	1	revision			

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Figure 20. AS3610/11 State Diagram



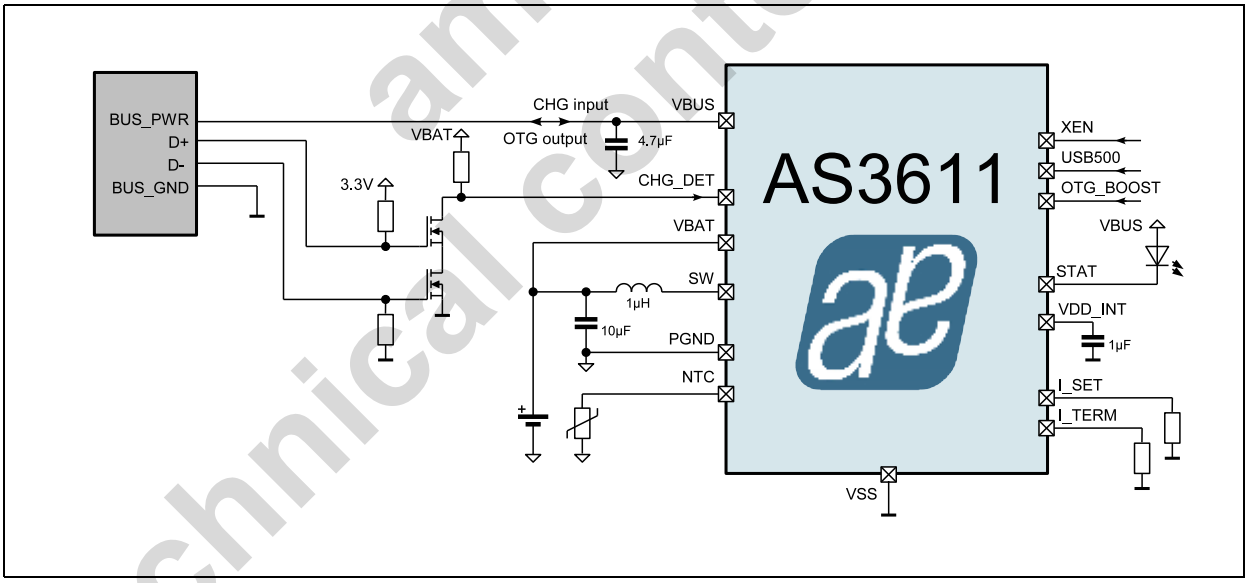
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9 Application Information

Table 9. External Components

Symbol	Parameter	Note	Min	Typ	Max	Unit
C_{VBUS}	Input capacitor	Ceramic X5R or X7R, 16 or 25V	-20%	4.7	+120%	µF
C_{VBAT}	Output capacitor	Ceramic X5R or X7R, 6.3V	-20%	10	+120%	µF
C_{VDD_INT}	Output capacitor	Ceramic X5R or X7R	-20%	1	+100%	µF
L	Inductor (chip coil)	LQM2HPN1R0MJ0 (Murata), Isat=1.5A, ESR=0.85mOhm MLP2520S1R0M (TDK), Isat=1.5A, ESR=0.85mOhm		1		µH
R_{SET}	Resistor for CC current setting	550mA 650mA 750mA 850mA 950mA 1050mA 1150mA 1250mA		39,0 33,0 28,6 25,2 22,6 20,4 18,7 17,2		kΩ
R_{TERM}	Resistor for trickle / EOC current setting	50mA 100mA 150mA 200mA		24 12 8 6		kΩ
R_{NTC}	NTC Thermistor	@25°C		10 / 100		kΩ

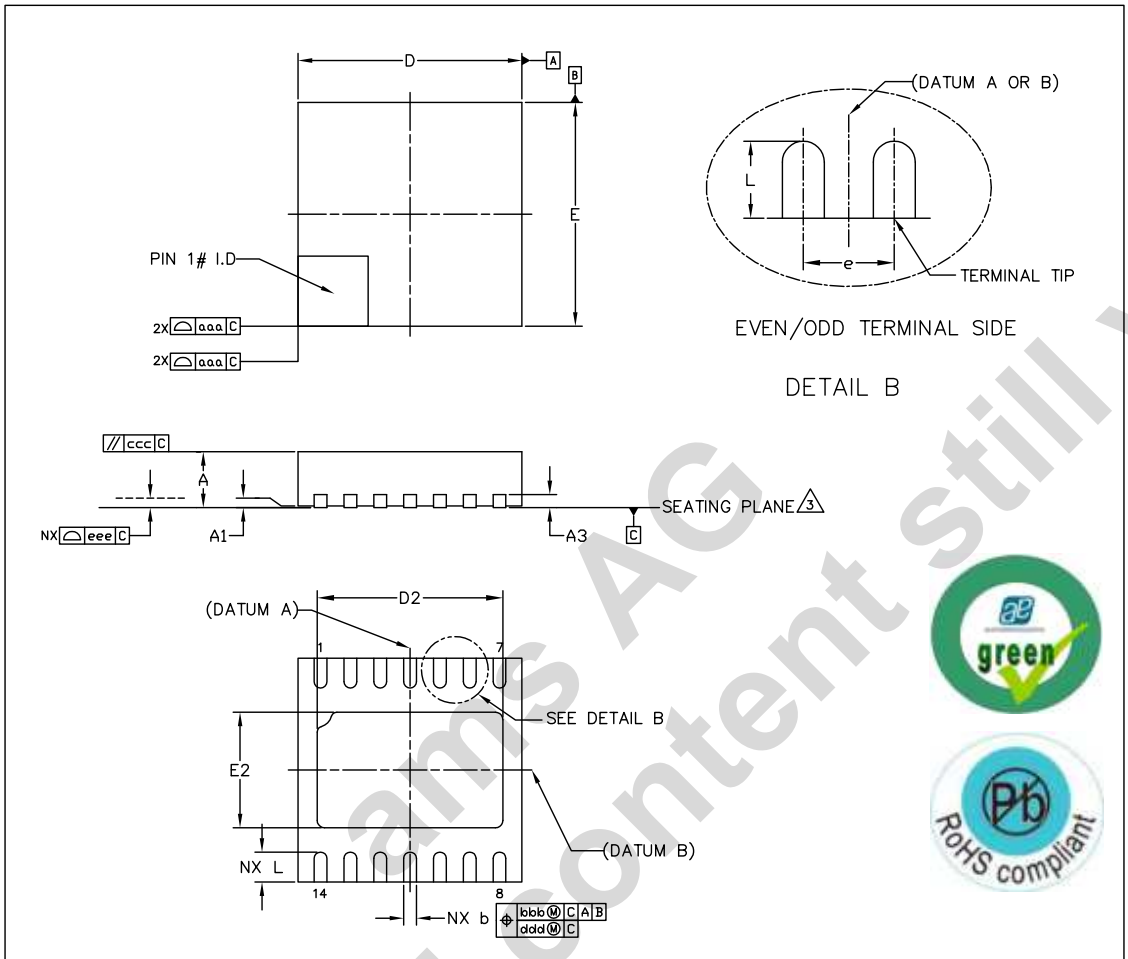
Figure 21. AS3611 USB detection



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10 Package Drawings and Markings

Figure 22. MLPD14 3x3mm *Package Drawings and Dimensions*



REF.	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20 REF	
L	0.30	0.40	0.50
b	0.15	0.20	0.25
D		3.00 BSC	
E		3.00 BSC	
e		0.40 BSC	
D2	2.34	2.49	2.59
E2	1.40	1.55	1.65
aaa	–	0.15	–
bbb	–	0.07	–
ccc	–	0.10	–
ddd	–	0.05	–
eee	–	0.08	–
N		14	

NOTE:

1. DIMENSIONS & TOLERANCEING CONFIRM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGELS ARE IN DEGREES.
3. COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.
4. RADIUS ON TERMINAL IS OPTIONAL.
5. N IS THE TOTAL NUMBER OF TERMINALS.

austriamicrosystems a leap ahead in analog			ASSEMBLY ENGINEERING	
DRAWN RH8	DATE 2011.02.02	REV. N/C	TITLE MLPD 3x3x0.75mm, 14 LEAD, 2.49x1.55mm ePAD	REFERENCE DOCUMENT JEDEC MO – 229 LATEST REVISION
CHECKED GBO	DATE 2011.02.02		DRAWING NO. QKF	UNIT
APPROVED MKR	DATE 2011.02.02	SHEET 1 OF 1	DIMENSION AND TOLERANCE	SCALE NOT IN SCALE

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Revision History

Revision	Date	Owner	Description
0.6	11.5.2011	pkm	Initial draft
0.7	1.9.2011	pkm	fixed typos, extended detailed description
0.9	16.9.2011	pkm	fixed typos, changed ESD level for STAT pin, removed 0.5% EOC voltage limits
1.0	20.09.2011	cwo	update values for pre-programmed variants, final release
1.01	28.12.2011	cwo	Typos correction
1.1	15.3.2012	pkm	added C-Version for FePO4 batteries

Note: Typos may not be explicitly mentioned under revision history.

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11 Ordering Information

The devices are available as the standard products shown in Table 10.

Table 10. Ordering Information

Ordering Code	Marking	Description	Delivery Form	Package
AS3610-BDFP	AS10	Switching Charger for Li-Ion/LiPo/LiFePO4 powered devices (I2C control)	Tape & Reel in Dry Pack	MLPD14 3x3mm
AS3611-BDFP-A	AS1A	Switching Charger for Li-Ion/LiPo powered devices (stand alone)	Tape & Reel in Dry Pack	MLPD14 3x3mm
AS3611-BDFP-B	AS1B	Switching Charger for Li-Ion/LiPo powered devices (stand alone)	Tape & Reel in Dry Pack	MLPD14 3x3mm
AS3611-BDFP-C	AS1C	Switching Charger for LiFePO4 powered devices (stand alone)	Tape & Reel in Dry Pack	MLPD14 3x3mm

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or find your local distributor at http://www.austriamicrosystems.com/distributor

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Contact Information

Headquarters

austriamicrosystems AG
Tobelbaderstrasse 30
A-8141 Unterpremstaetten, Austria

Tel: +43 (0) 3136 500 0
Fax: +43 (0) 3136 525 01

For Sales Offices, Distributors and Representatives, please visit:

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