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PRELIMINARY

Coverpage: AS89020 Datasheet

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DATASHEET
AS89020

4-channel, current input 12 bit analog-to-digital converter (ADC)
SSOP20
Order No.: 305040004
Status: preliminary

FEATURES

- Conversion of 4 sensor signals of photodiodes (e.g. RGB/XYZ color plus one blank channel for compensation of parasitic currents or temperature conversion) or other sensors with current signal output
- 12 bit signal resolution at an achievable sensitivity of up to 2.8 pA/LSB
- Programmable full-scale range from 11.7 nA to 12 µA
- Sampling rate up to 100 kS/s for all channels
- Measurement of positive and negative currents
- Up to 16 MHz fast SPI-interface
- High amplification linearity, no cross talk
- High absolute accuracy and reliability without additional sources
- Supply and temperature independent performance
- Supply voltage from 2.7 V to 3.6 V
- Temperature range from -25 °C to 85 °C
- Deliverable in standard SSOP20 package

APPLICATIONS

- Precise conversion of photo current for optical sensors and arrays (e.g. UV, VIS, IR) and other sensors with current output
- In combination with ams Sensors Germany's color sensors or other multi-channel pin-diodes: measurement of surfaces and distances
- In combination with ams Sensors Germany's color sensors: measurement of light – chromaticity coordinates (XYZ CIE1931, DIN5033 and similar) or color temperatures to control and process displays and backlights (e.g. LED, CCFL)
- In combination with ams Sensors Germany's color and spectral sensors: measurement of reflective and/or transmitted light – chromaticity coordinates (XYZ CIE1931, DIN5033 and similar) measurement of objects and surfaces for analyses, quality management, sorting, etc.

TYPICAL MARKETS

- Lighting SSL and photometry
- Industrial/commercial lighting
- Chemical and biochemical analyses
- Industrial process control
- Medical and environment instrumentation
- Infotainment (backlights and video walls) and monitors
- High quality consumer displays and tablets

PRELIMINARY

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PRELIMINARY

1 GENERAL DESCRIPTION

Transimpedance amplifiers (TIA) used as current-voltage converters ensure continuous signal processing at high signal frequencies, thus meeting the demands of e.g. automated processes. They are best suited to synchronous measuring procedures in the kilohertz range, where fast converters are required to scan optical signals. Examples include sensors for quality testing in inline manufacturing processes or those in touchless handheld devices. ams Sensors Germany offers several multichannel TIAs with digital and analog interface.

The AS89020 is a 12 bit, 4 channel, current input analog-to-digital converter (ADC). It combines current-to-voltage (TIA) and analog-to-digital (AD) conversion, so that 4 separate current output devices (e.g. photodiodes) can be directly connected to its inputs and digitized.

For each of the 4 inputs the AS89020 provides an input amplifier with a track and hold circuit. The outputs of the track and hold stages are serial converted to 12 bit digital words using an analog-to-digital converter (ADC).

The 12 bit conversion results are available via SPI at a frequency up to 16 MHz and a conversion time as low as 1 µs per channel.

The input amplifier is separately programmable for each channel in 17 stages. This results in a programmable full-scale range for the ADC from 11.7 nA to 12 µA and a sensitivity up to 2.8 pA/LSB.

Input currents of both polarities can be fed to each of the input amplifiers. The adjustment is realized by digital programming of each channel separately via standard SPI-interface.

All reference voltages are implemented internally; only some external passive devices are needed to complete their operating mode.

The AS89020 supports *Power Down* functions for low power solutions.

Based on the high flexibility the AS89020 is suitable as a converter for a wide range of multi-channel optoelectronic sensors (UV, VIS, NIR, IR) or other sensors with current output. The device achieves a high dynamic range.

The combination of ams Sensors Germany’s color sensors with AS89020 is excellently suited especially for fast color measurement and control in printing and automation, for mobile color measurement devices but also for photometry applications (brightness, color coordinate and/or color temperature), for determining current values for control of spectrally mixed LED light sources or as sensors for display and (back)light calibration and mobile devices for light measurement.

The sensor compact signal IC is available in a SSOP20 package and or as bar die on request.

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2 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings

Violations of absolute maximum conditions are not allowed under any circumstances; otherwise the IC can be destroyed.

All voltages are referenced to VSSA = VSS = 0 V.

Table 1: Maximum conditions

PARAMETER	NAME	MIN	MAX	UNIT
Power Supply (analog)	VDDA	-0.5	5.0	V
Input and Output Voltages (analog)	VIOA	-0.5	VDDA+0.5	V
Power Supply (digital)	VDD	-0.5	5.0	V
Input and Output Voltages (digital)	VIOD	-0.5	VDD+0.5	V
Supply Voltage Difference VDDD-VDDA[1]	DIFF_VDD		0.3	V
Storage Temperature	TSTG	-55	+150	°C
Weight	m		0.12	g

2.2 Recommended Operating Conditions

Table 2: Operational conditions; VSSA=VSS=0 V

PARAMETER	NAME	MIN	TYP	MAX	UNIT	CONDITION
Supply Voltage	VDDA VDD	2.7	3.3	3.6	V	|VDDA-VDD| < 0.3 V
Operating Temperature	T_{AMB}	-25		+85	°C	
External Resistor [2]	R_{EXT}	198	200	202	kΩ	
Temperature Coefficient of R_{EXT}	TC_{REXT}			15	ppm/K	
Input Capacitance at IN0 to IN3	CPD		50	80	pF	
Output Capacitance at VBH	CLVBH	1		10	µF	
Output Capacitance at VRT	CLVRT	0.5		5	µF	
Output Capacitance at VRH	CLVRH	0.5		5	µF	
Output Capacitance at VRL	CLVRL	0.5		5	µF	

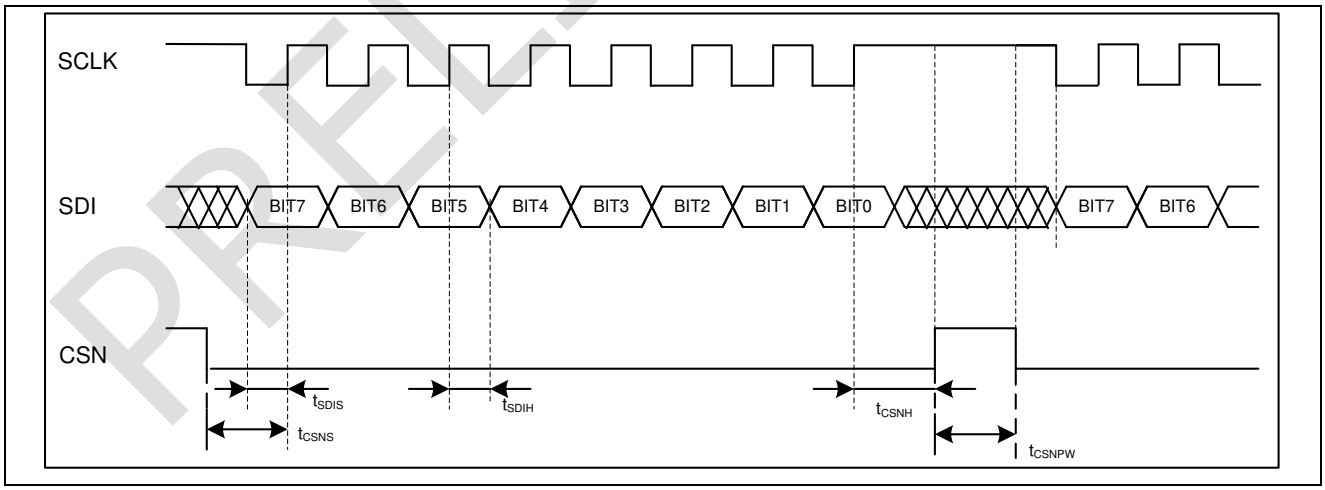
[1] For the digital supply voltage VDD it is not allowed to use a voltage above VDDA + 0.3 V. This condition must also be observed during the ramp-up time of the supply voltages.

[2] The resistor influences the TOLIFSR of the reference current for the signal conversion directly. Therefore the temperature coefficient of the resistance plays an important role. The smaller the temperature coefficient and the resistor value tolerance (1 % is better than 5 %, etc.), the more accurate the result is of the conversion process.

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PARAMETER	NAME	MIN	TYP	MAX	UNIT	CONDITION
Input High Level	V_{IH}	0.7*VDD			V	
Input Low Level	V_{IL}			0.3*VDD	V	
Input Hysteresis	V_{HYST}		0.3*VDD		V	Pin CONVN VDD = 3.3 V
Output High Level	V_{OH}	0.8*VDD			V	I_{Load} = 1.0 mA
Output Low Level	V_{OL}			0.4	V	I_{Load} = 1.0 mA
SPI Clock Frequency	f_{SCLK}	0.5	10	16	MHz	up to 10 MHz is re-commended for 12 Bit accuracy
SPI Setup Time SDI	t_{SDIS}	30			ns	
SPI Setup Time CSN	t_{CSNS}	30	2500		ns	min. 2.5 µs is recommended for 12 Bit accuracy
SPI Hold Time SDI	t_{SDIH}	30			ns	
SPI Hold Time CSN	t_{CSNH}	30			ns	
SPI Pulse Width CSN	t_{CSNPW}	62.5			ns	
Tracking Time[3]	t_{TRACK}	6	10		µs	
Pause Time[4]	$T_{PAUSESCLK}$		$1/f_{SCLK}$		s	recommended for 12 Bit accuracy

Figure 1: SPI Timing



[3] The time between two subsequent conversions where bit TRACK = ‚1' (see 5.2

[4] The recommended pause time between two bytes of channel data during the conversation in the measurement state

2.3 Electrical Characteristics

Table 3: Specifications; VSSA = VSS = 0 V; VDDA = VDD = 2.7 V to 3.6 V REXT = 200 kΩ; TAMB = –25 °C to 85 °C, unless otherwise noted

PARAMETER	NAME	MIN	TYP	MAX	UNIT	CONDITION[5]
Supply Current	IVDD			10.5	mA	VDD = VDDA = 3.6 V T_{AMB} = 25°C
Power Down Supply Current	IPD			1	µA	OSR:PD = ‚1' and / or PDN = VSS @ T_{AMB} = 25°C
Input Current of Pull-Up Pins: SCLK, SDI, CSN, CONVN, PDN	I_{ILPU}	0.5		2	µA	VIN = VSS
		11.4	12	13.2		SW_RX = ‚00hex'
		5.7	6	6.6		SW_RX = ‚01hex'
		2.85	3	3.3		SW_RX = ‚02hex'
		1.425	1.5	1.65		SW_RX = ‚03hex'
		712.5	750	825		SW_RX = ‚04hex'
		356.25	375	412.5		SW_RX = ‚05hex'
		178.125	187.5	206.25		SW_RX = ‚06hex'
		89.062	93.75	103.125		SW_RX = ‚07hex'
		44.531	46.875	51.563		SW_RX = ‚08hex'
		22.265	23.4375	25.782		SW_RX = ‚09hex'
		11.132	11.71875	12.891		SW_RX = ‚0Ahex' to ‚0Fhex'
		475	500	550		SW_RX = ‚10hex' to ‚14hex'
		237.5	250	275		SW_RX = ‚15hex'
		118.75	125	137.5		SW_RX = ‚16hex'
		59.375	62.5	68.75		SW_RX = ‚17hex'
		29.687	31.25	34.375		SW_RX = ‚18hex'
		14.843	15.625	17.188		SW_RX = ‚19hex' to ‚1Fhex'
			0.1			SW_RX = ‚00hex'
			0.2			SW_RX = ‚01hex'
			0.4			SW_RX = ‚02hex'
			0.8			SW_RX = ‚03hex'
			1.6			SW_RX = ‚04hex'
			3.2			SW_RX = ‚05hex'
			6.4			SW_RX = ‚06hex'
			12.8			SW_RX = ‚07hex'
			25.6			SW_RX = ‚08hex'

[5] For OSR:PD see 6.2 for SW_RX see 6.5

[6] See also Table 11

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PARAMETER	NAME	MIN	TYP	MAX	UNIT	CONDITION[5]
			51.2			SW_RX = ‚09hex'
			102.4			SW_RX = ‚0Ahex' to ‚0Fhex'
			2.4			SW_RX = ‚10hex' to ‚14hex'
			4.8			SW_RX = ‚15hex'
			9.6			SW_RX = ‚16hex'
			19.2			SW_RX = ‚17hex'
			38.4			SW_RX = ‚18hex'
			76.8			SW_RX = ‚19hex' to ‚1Fhex'
		170	340			SW_RX = ‚00hex'
		100	210			SW_RX = ‚01hex'
		50	130			SW_RX = ‚02hex'
		40	80			SW_RX = ‚03hex'
		25	55			SW_RX = ‚04hex'
		15	35			SW_RX = ‚05hex'
		12	23			SW_RX = ‚06hex'
		8	15			SW_RX = ‚07hex'
		4	8			SW_RX = ‚08hex'
		2	4			SW_RX = ‚09hex'
		1.2	2.5			SW_RX = ‚0Ahex' to ‚0Fhex'
		20	40			SW_RX = ‚10hex' to ‚14hex'
		12	25			SW_RX = ‚15hex'
		10	20			SW_RX = ‚16hex'
		6	11			SW_RX = ‚17hex'
		3	5			SW_RX = ‚18hex'
		1.5	3			SW_RX = ‚19hex' to ‚1Fhex'
Temperature Coefficient of Overall Response (TOP = -25 °C to 85 °C, TCOMPENA = ‚1')	TC		50	100	ppm/K	Temperature Dependency of R_{EXT} and Photodiodes not included
Temperature Coefficient of Transimpedance RX without the internal Temperature Compensation (TOP = -20 °C to 85°C, TCOMPENA = ‚0')	TCR		-4300		ppm/K	

PARAMETER	NAME	MIN	TYP	MAX	UNIT	CONDITION[5]
Absolute Tolerance of the equivalent ADC Reference Current	TOL_{IFSR}	-5		10	%	R_{EXT} = 200 kΩ T_{AMB} = 25°C
		-1.5		1.5		SW_RX ≤ ‚01hex‘
		-1		1		SW_RX > ‚01hex‘
Gain Matching Error	E_{GMATCH}	-2.5		2.5	%	
Linearity Error	LIN	-0.5		0.5	%	
Start-Up Time after switch off Power Down Mode	$t_{SUPDOFF}$	200			ms	Start-Up Time after OSR:PD = from ‚1‘ to ‚0‘ and/or PDN = from VSS to VDD – depends on CLVBH, CLVRT, CLVRH and CLVRL

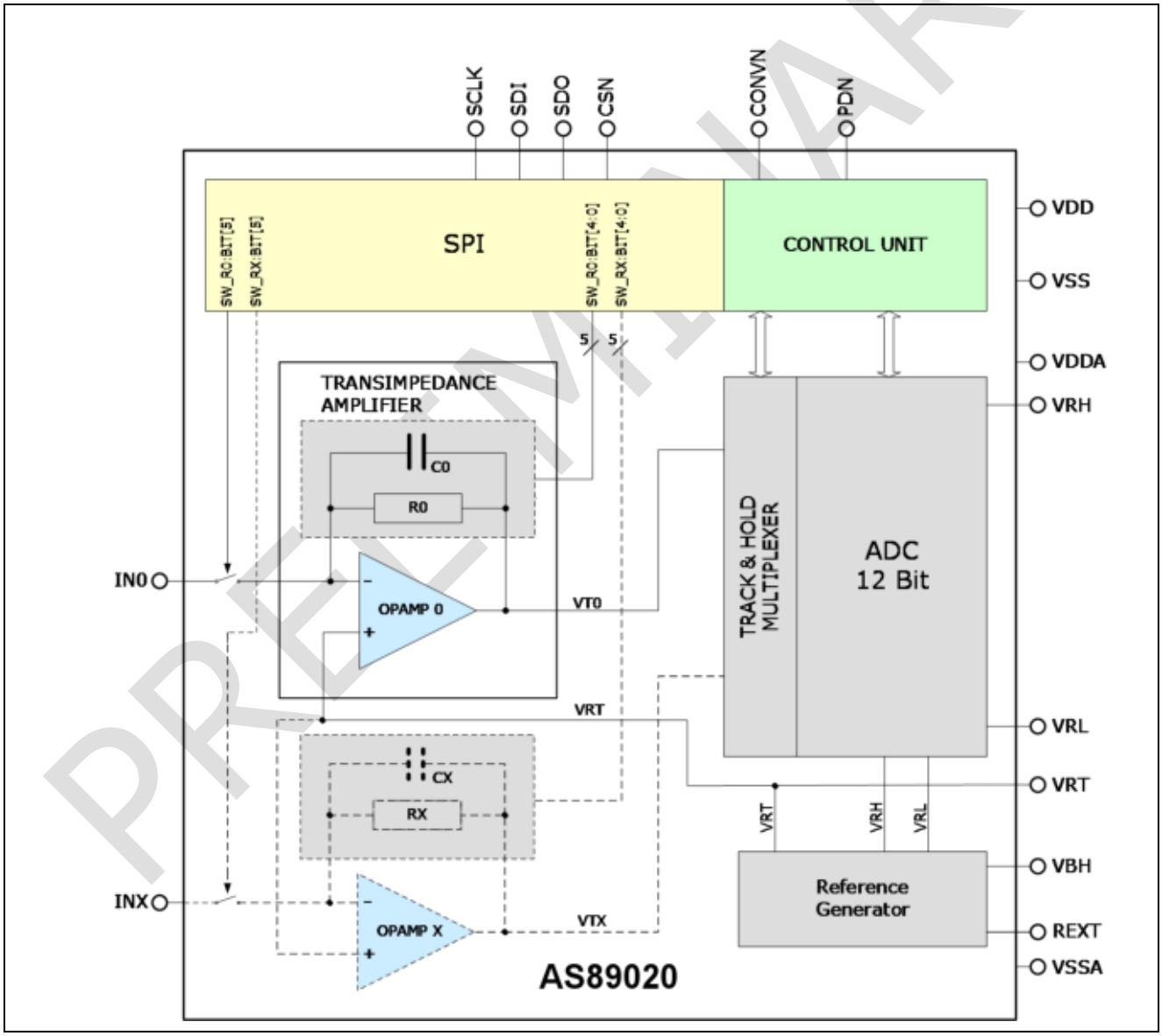
PRELIMINARY

3 BLOCK DIAGRAM

The main components of the AS89020 are shown in Figure 2. The input currents are amplified by independently programmable transimpedance amplifiers. All channels are simultaneously sampled and sequentially converted to digital data by a 12 bit successive approximation analog-to-digital converter (SAR). The integrated SPI interface is used to program the trans-impedance amplifiers and control the analog-to-digital converter. The results of the analog-to-digital conversion are also available via SPI interface. Reference currents (pin REXT) and reference voltages (VBH, VRH, VRL, VRT) for the ADC and the transimpedance amplifiers are all implemented internally. It is recommended to use the voltage VRT as a reference voltage for the external photodiodes. External capacitances are required on four reference voltage pins to achieve an optimal noise suppression for the analog-to-digital conversion.

The input CONVN can be used for externally triggered sampling of the input signal currents. The AS89020 can be switched into the Power Down mode via the pin PDN.

Figure 2: Block Diagram



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4 PIN ASSIGNMENT

The pin assignment is shown in the following table.

Table 4: Pin assignment (Analog/Digital)

PIN	TYPE	A/D	DESCRIPTION
VDDA	power	A	analog power supply voltage
VSSA	power	A	analog ground voltage
VDD	power	D	digital power supply voltage (VDDA = VDD)
VSS	power	D	digital ground voltage (VSSA = VSS)
IN0, IN1, IN2, IN3	input	A	current inputs
REXT	input	A	constant reference current (6 µA) for setting the full-scale ratio (FSR) of AD conversion (200 kΩ resistor R_{EXT} to VSSA has to be connected)
VRT	output	A	TIA reference voltage – recommended as external photodiodes bias voltage (cathodes or anodes)
VRH	output	A	ADC high reference voltage
VRL	output	A	ADC low reference voltage
VBH	output	A	internal reference voltage
SCLK	input	D	SPI and ADC clock input (pull-up)
SDI	input	D	SPI data input (pull-up)
SDO	output	D	SPI data output
CSN	input	D	SPI chip select (pull-up and low-active)
CONVN	input	D	start AD conversion (pull-up and low-active)
PDN	input	D	Power Down mode (pull-up and low-active)

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5 DESCRIPTION OF FUNCTION

5.1 Description

The AS89020 is a 4 channel, current input analog-to-digital converter (ADC). For each of 4 inputs the AS89020 provides a transimpedance amplifier (TIA). The gain of transimpedance amplifier is separately programmable for each channel. The transimpedance of the input amplifier for channels is selectable in 17 stages. In exactly the same way the FSR current (Full-Scale-Range current) of the ADC is adjusted. This adjustment can be performed for every channel separately by programming the corresponding register SW_RX. The AD conversion is started and controlled via the SPI and the channels are successive converted. The channel order of the conversion process can be chosen and programmed via SPI using register CH_ORDER. The AS89020 has implemented a temperature compensation of the transimpedance input amplifier to achieve a high absolute accuracy and temperature stability of converted value.

The output signal of the transimpedance amplifier (VTX) is subsequently converted by an analog-to-digital converter (ADC) to a 12 bit digital word. The input of the ADC is realized as a 4 channel track and hold circuit, which can be switched into the track or hold mode by the signal CONVN or the signal CSN (part of the SPI-interface). The track and hold circuit takes samples of each channel at the same time and holds them internally stored in an analog memory.

The power supply for the device is typically 2.7 V to 3.6 V. The digital and the analog supplies are separated to minimize the crosstalk of both parts inside the AS89020 circuitry.

5.2 Operational States

The AS89020 has 2 operational states – configuration and measurement. It is possible to toggle between these two states by programming the bits 2 to 0 of register OSR. The configuration state is the default state after the power-up phase including an internal power-on-reset. The configuration registers are set to their default values after the power-on-reset. They can be changed via SPI command. All settings for the measurement must be made in the configuration mode (e.g. setting FSR of ADC). During the configuration mode the ADC is in reset state and the track and hold circuit is inactive.

The track and hold circuit and the ADC are active only in the measurement mode. Before the real ADC conversion can be started, a tracking phase must occur (OSR: TRACK must be ‚1b') with the minimum length of $t_{TRACK.}$ With the falling edge of CSN or CONV (depending on the setting of CREG: STARTSIG) the tracking phase is stopped and the 4 input signals for the ADC are sampled (hold phase of track and-hold circuit) and the ADC conversion is started. The capture of input signals occurs simultaneously for all channels. For one AD conversion (one channel), a 2-byte SPI communication is needed (equal to 16 SPI clock cycles). The configuration registers are not readable and not writable while the AS89020 is in the measurement state. The bit OSR:TRACK defines whether the next conversion or a new tracking follows after the next falling edge of CSN.

5.3 Power Down Mode

The Power Down mode is selected by setting the PDN input level to ZERO or by programming a ‚1b' into the corresponding register OSR:PD or CH_PD. The register CH_PD affects only the transimpedance amplifiers. The Power Down mode via PDN or register OSR:PD switches off the functionality of the full analog part of the AS89020. The functionality of the digital Part and the SPI communication is not interrupted during this mode. The device stays idle and the SPI-interface is enabled. The operational state, which was used before the Power Down mode has been switched on, is preserved. Setting one or more channels into Power Down via register CH_PD switches only the selected channels. If the Power Down mode ends the AS89020 starts with all actual register settings. The device needs a start-up time of typically 200 ms. This time is at least necessary to load all external capacitors to their typical values for a proper operation of the circuit (see also Table 3).

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5.4 AD Converter

The AS89020 utilizes the ADC for the on-chip analog-to-digital conversion of the input current. The full-scale range current of the ADC is defined by 2 values. One important value is the current, which flows through the pin REXT (direction out of the pin).The second part of the definition of full-scale range current of ADC is the adjustment of the full-scale range using register SW_RX (see Table 3 and Table 11).

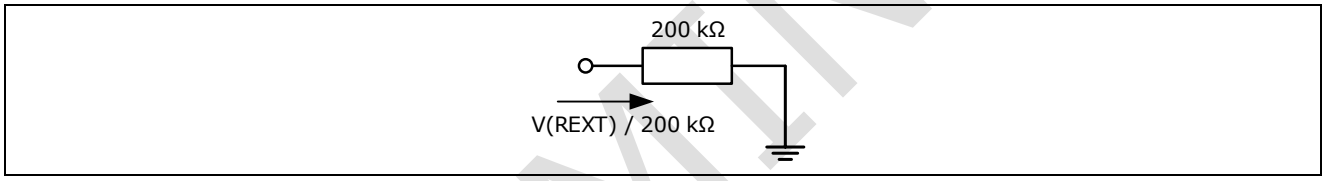
The digital data of the ADC output can be defined as

$$OUTX = \frac{I(INX)}{IREFX} \times 2^{12} + DOFFGEN$$

I(INX):	input current at pin INX
IREFX:	equivalent reference current or equivalent FSR for channel X (see chapter 2.3 Table 3)
DOFFGEN:	0 if bit CREG:OFFGEN =,0b ’ 63 if bit CREG:OFFGEN =,1b’ (see Table 10 and see chapter 6.4)
OUTX:	digital result of the AD conversion for channel X (possible values: ,000h’ to ,FFFh’)

The accuracy of the reference current source at pin REXT has a direct influence on the overall ADC characteristic. This pin has to be connected as suggested by Figure 3. An internal voltage is generated at pin REXT (typically 1.2 V). The resulting reference current is equal to V(REXT) / 200 kΩ, which is 6 µA. The overall ADC accuracy is directly influenced by the performance of the external resistor (temperature coefficient and absolute value and its tolerance).

Figure 3: External Wiring of Pin REXT



5.5 AD Conversion

The AD conversion is only possible in measurement mode (OSR register bit 2 to bit 0 setting to ,011b’). The operation of conversion is controlled by the signals CSN or CONV (depending on setting of CREG:STARTSIG), SCLK and the settings in register OSR. The conversion process consist of 2 parts. At first the output voltages of input amplifiers are simultaneously sampled. Afterwards the sampled values are converted one after another with the successive approximation (SAR-) ADC.
Every conversion process starts with a tracking phase at a duration of minimal t_{TRACK} (bit OSR:TRACK =,1b’). The falling edge of CSN or CONV takes a sample of each channel. The sampling occurs only if the bit OSR:TRACK is set to ,1b.’
The signal SCLK controls the actual analog-to-digital conversion. SCLK is not only the SPI clock during the conversion, but also the clock signal for the ADC. Parallel to the conversion the transfer of output data takes place via SPI interface. 16 clock cycles are needed for the conversion of one channel (one sample) and the transfer of the result. The format of result output is described in Table 14. The further behavior of the IC is defined by sending 2 byte over SDI for programming the OSR register during the conversion. The setting ,00h’ of the OSR defines that the conversion of the next channel follows (corresponding to the order in register CH_ORDER). A setting of ,80h’ starts a new tracking phase after the actual conversion ended. Figure 4 shows the timing diagram of the conversion cycle in the measurement state. Figure 5 shows the different sample points for CONVN and CSN. If bit CREG:STARTSIG=,1b’ the signal CONVN can be used to synchronize the input sampling time point at an external event. If bit CREG:STARTSIG=,0b’ the signal CSN acts as part of a software command for the start of the conversion while CONVN must stay high in that case.

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Figure 4: timing diagram of the analog-to-digital conversion

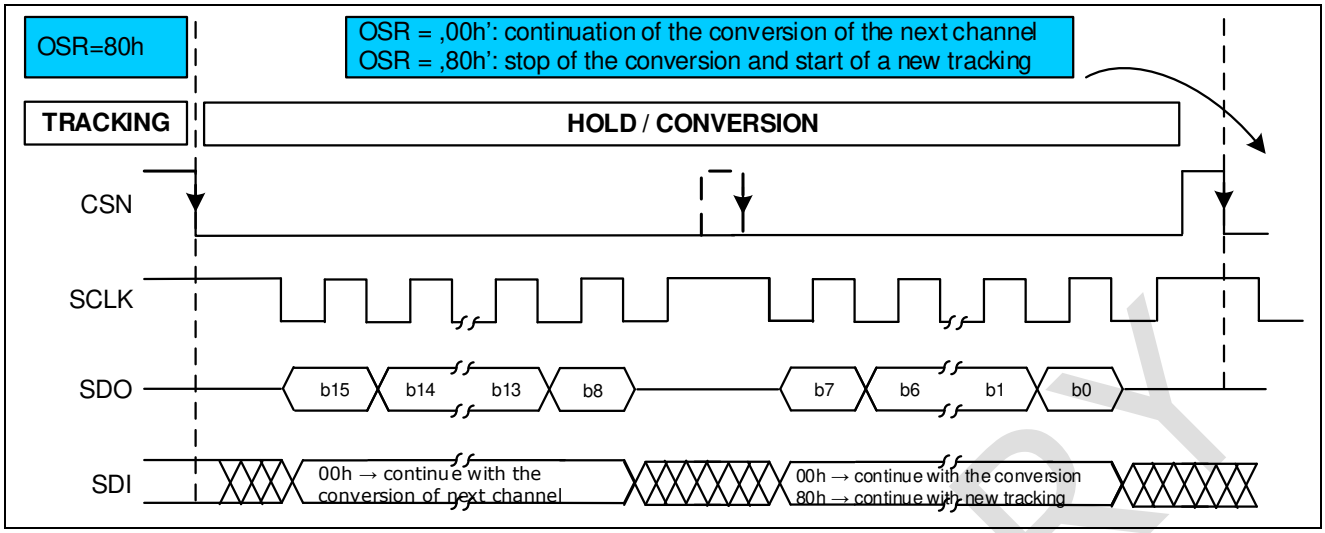
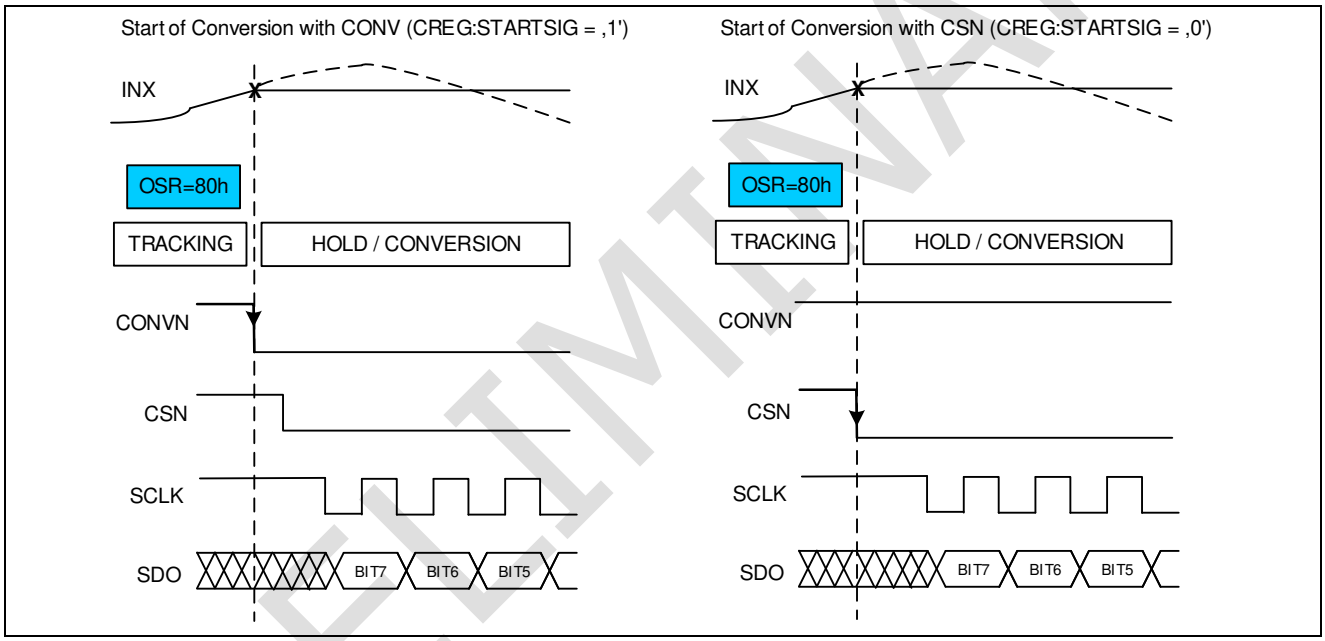


Figure 5: start of conversion with CONV or CSN



The accuracy of the AD conversion is determined by different effects. The duration of the tracking phase (t_{TRACK}) is very important for the accuracy of the current-to-digital conversion result and should not be shorter than specified. To achieve the best possible accuracy, the SPI clock f_{SCLK} should be not higher than 10MHz and the time t_{CSNS} should be at least 2.5 µs. If the AS89020 is used with a power supply under 2.9 V, it is recommended that CREG: SETVB bit is set to ‚1b' to achieve the full accuracy of ADC.

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5.6 Input amplifier

The input amplifier has a low-pass characteristic. The bandwidth of amplifiers depends on the selected gain via the registers SW_RX (see Table 3). Therefore the bandwidth has a significant influence of value which is sampled and converted. The bandwidth determines the settling time t_{SET} which is required from the input amplifier to provide a stable signal for an accuracy of 12 bits at its output. The time t_{SET} can be estimated with following formula.

$$t_{SET} \sim \frac{9}{2 * \pi * f3dB}$$

t_{SET}: settling time to achieve 12 bit accuracy
f3dB: Bandwidth of input amplifier (see Table 3)

Table 5 shows the values for the settling time t_{SET} for the individual gain stages. These values are calculated with the minimal bandwidth of input amplifier.

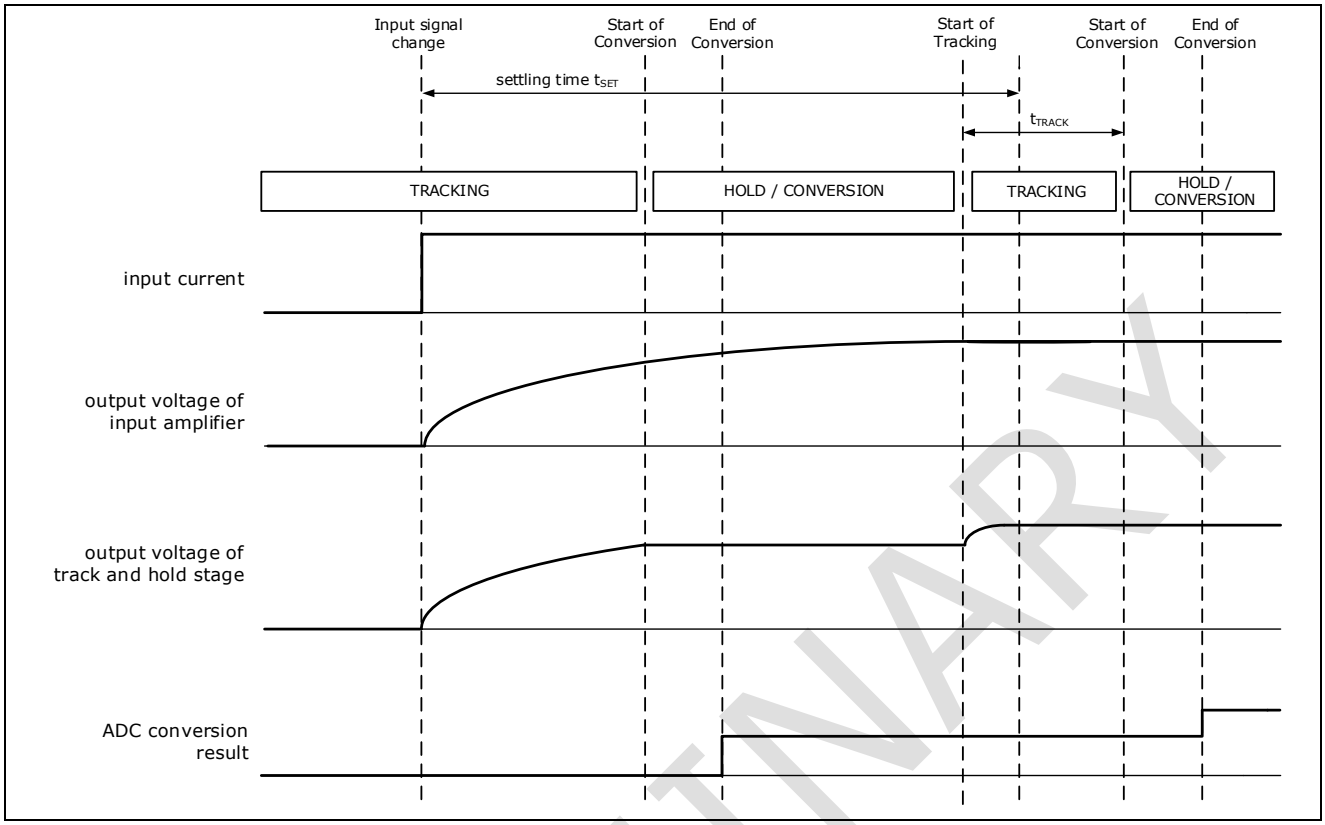
Table 5: settling time t_{SET}

STAGE (see Table 11)	MIN. BANDWIDTH		SETTLING TIME t_{SET}	
0	170	kHz	8.4	µs
1	100	kHz	14.3	µs
2	50	kHz	28.6	µs
3	40	kHz	35.8	µs
4	25	kHz	57.3	µs
5	15	kHz	95.5	µs
6	12	kHz	119.4	µs
7	8	kHz	179.0	µs
8	4	kHz	358.1	µs
9	2	kHz	716.2	µs
10-15	1.2	kHz	1193.7	µs
16-20	20	kHz	71.6	µs
21	12	kHz	119.4	µs
22	10	kHz	143.2	µs
23	6	kHz	238.7	µs
24	3	kHz	477.5	µs

Figure 6 shows the effect of settling time t_{SET} on the conversion result. For the AD conversion the actual value is sampled from output of the input amplifier by track and hold circuit. The conversion result always corresponds to the low-pass characteristic of the input amplifier. This is especially taken into account when the sample taken inside the settling time t_{SET} or frequency of the input signal is close to the bandwidth of input amplifier. The AD conversion takes place at an accuracy of 12 Bits, regardless of the bandwidth of input amplifier.

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Figure 6: Influence of settling time to conversion result



This example shows: The ADC result after first conversion is lower than result after second conversion. This is why the settling time is not reached at start of first conversion.

5.7 Temperature Compensation

The implemented transimpedance resistors of the channel's input amplifiers have a temperature coefficient (TCR) with a typical value of -4300 ppm/K. However, the AS89020 integrates a temperature compensation circuit, so that the temperature dependence of the transimpedance resistance is eliminated. Furthermore the overall ADC gain is internally controlled, so that the absolute accuracy can be achieved. If the internal temperature compensation is disabled (CREG: TCOMPENA = ,0b'), the overall behavior of the device is no longer temperature independent. Normally, the AS89020 should be used with enabled temperature compensation (CREG: TCOMPENA = ,1b').

However, the temperature dependence of the reference current source at REXT (generating I(REXT)) is not compensated and therefore the temperature coefficient of the external resistor R_{EXT} of 200 kΩ directly affects the ADC accuracy.

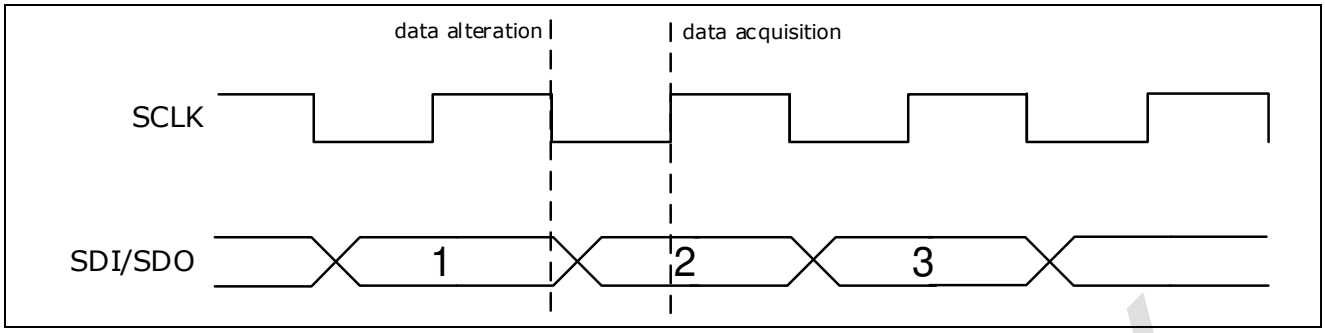
5.8 SPI – Interface & Communication

The digital interface of the AS89020 consists of a bidirectional four wire SPI for programming the registers and for transferring the conversion data to the microcontroller.

The SPI interface is used for the connection of the AS89020 to the system's SPI bus. The SPI clock SCLK is low active and stays high while the AS89020 is in idle state. The data is changed at the time of the falling clock edge and will be accepted at the time of the rising clock edge.

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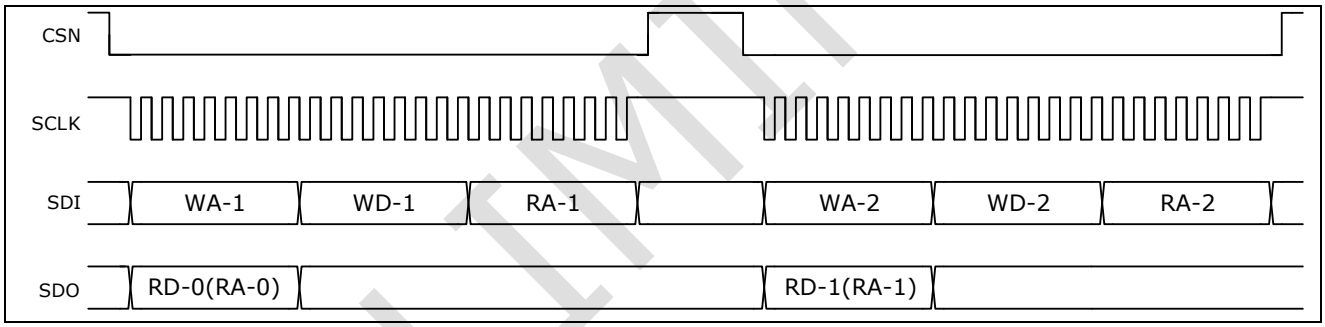
Figure 7: SPI Transfer Mode



The data transfer starts at first with the MSB (bit 7) and ends with LSB (bit 0). During the transfer of at least 8 bit the signal CSN must be at low level. The signal CSN is allowed to be set back to the high level between full bytes, if more than one byte of data will be transferred.

In the configuration state (OSR:DOS = ‚010b') the data transfer must always be performed with exactly 3 data bytes. The SPI transfer fails in case of a violation and any further communication also fails. The write address (WA) has to be 6.5 sent as the first byte, the second byte contains the data which is to be written (WD) and the third byte is the read address (RA) which is to be read in the next transmission cycle. The first data byte at SDO always contains the data (RD) of the address which has been selected by the read address (RA) of the previous transmission cycle (see Figure 8).

Figure 8: Configuration State – Example of the SPI Data Transfer Cycle

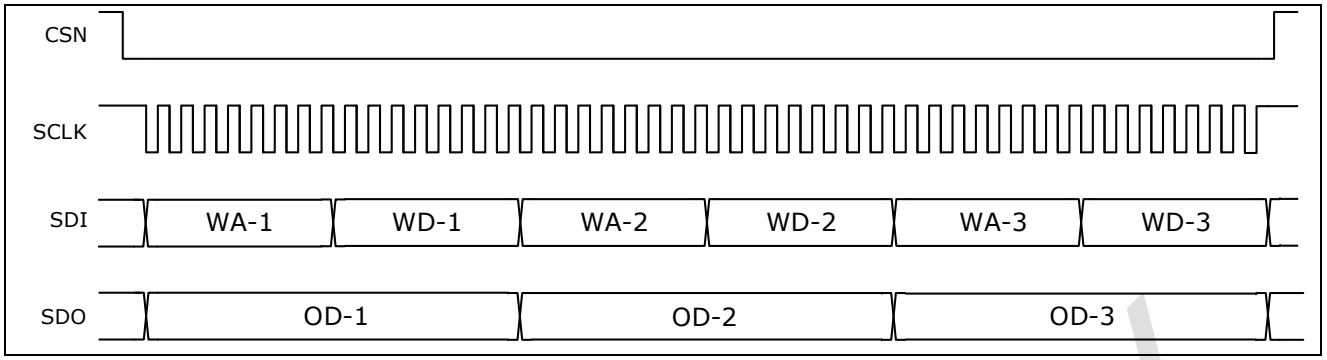


Writing OSR:DOS = ‚011b' causes the change to measurement state.

In the measurement state the read address is not required, so per transfer cycle only 2 data bytes must be transferred via SDI. The first byte contains the write address and the second byte the write data. Usually the OSR register should be written. The write address (WA) is ‚00h' and the write data (WD) for no operation or no change is ‚00h'. If a new tracking will be started, the write data (WA must be set to ‚80h'. The returned data (on SDO) in the measurement state are the output data (OD) of the AD conversion. Figure 9 shows an example of three transfer cycles within the measurement state. However, it is recommended to pause at least one clock cycle between each transfer of two bytes for a better accuracy of the AD conversion. The read out order of the conversion result registers will be defined by the Register CH_ORDER (see chapter 0).

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Figure 9: Measurement State – Example of the SPI Data Transfer Cycle



A return from measurement state to configuration state via programming OSR (OSR:DOS = ‚010b') always resets all control registers to their default value except the register OSR itself.

6 DESCRIPTION OF REGISTERS

6.1 Control Register Bank

Table 6 shows an overview of the internal registers which can be accessed via SPI-interface. The Operational State Register OSR is the only register, which can be written in both states - configuration and measurement state, but it cannot be read. Reading of an inexistent or only writable register always returns the value ‚00h'. Table 7 shows the addressable register space of the AS89020.

Table 6: Register Access Overview

ADDRESS [HEX]	ACCESS IN CONFIGURATION STATE		ACCESS IN MEASUREMENT STATE	
	WRITE	READ	WRITE	READ
00	OSR	–	OSR	
01	–		–	
02	–	AGEN	–	
03	–		–	
04	–		–	
05	–		–	
06	CREG		–	
07	SW_R0		–	
08	SW_R1		–	
09	SW_R2		–	
0A	SW_R3		–	
0B	CH_PD		–	
0C	CH_ORDER		–	
0D	–		–	
0E	–		–	
0F	–		–	

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Table 7: Addressable Register Space

ADDRESS [HEX]	ACCESS[7]	NAME	NO. OF SIGNIFICANT BITS	DEFAULT [HEX]	DESCRIPTION
00	wo	OSR	8	02	operational state register
01	–	–	–	–	reserved
02	ro	AGEN	8	40	API generation
03	–	–	–	–	reserved
04	–	–	–	–	reserved
05	–	–	–	–	reserved
06	rw	CREG	8	A0	configuration register
07	rw	SW_R0	6	01	transimpedance of channel 0
08	rw	SW_R1	6	01	transimpedance of channel 1
09	rw	SW_R2	6	01	transimpedance of channel 2
0A	rw	SW_R3	6	01	transimpedance of channel 3
0B	rw	CH_PD	4	0	channel Power Down
0C	rw	CH_ ORDER	8	1B	channel order for the conversion
0D	–	–	–	–	reserved
0E	–	–	–	–	reserved
0F	–	–	–	–	reserved

6.2 Operational State Register – OSR

The write-only register OSR controls the device operational state (DOS), the general Power Down mode (PD) and the tracking behavior (TRACK) of the AS89020 according to Table 8. This register can be written at any time, independently of the actual operational state. Please note, reading this register always returns the value ‚00h' because the register is write-only.

Table 8: Register OSR – Address 00h

OPERATIONAL STATE REGISTER OSR	NAME	VALUE [B]	AFFECTED OPERATIONAL STATE
		0[8]	sample input signal or start the AD conversion (active only in measurement state)
		1	track input signal and stop AD conversion (active only in measurement state)
		0[8]	nominal operation, no Power Down mode
		1	activate Power Down mode
bit 5 to 3	-	-	reserved

[7] ro – read-only, wo – write-only, rw – read-write, reading register with access write-only results in ‚00h'

[8] Default after power-on-reset.

OPERATIONAL STATE REGISTER OSR	NAME	VALUE [B]	AFFECTED OPERATIONAL STATE
bit 2 to 0	DOS (Device Operational State)	000	NOP (no operation)
		001	reserved
		010[8]	operational state: configuration
		011	operational state: measurement
		1XX	reserved

The bits OSR:DOS switch the operational state of the device between configuration and measurement. The configuration state enables the access to the control register bank (Table 7). In this state no measurement can be performed. The measurements can only be performed in the measurement state. In this state any access to the control register bank (except OSR) is not possible. The control registers will be reset to their default values when the operational state is switched back to the configuration state.

The start of the measurement is controlled by the setting of the bit OSR:TRACK, which is only evaluated in the measurement state.

The Power Down mode is controlled by the setting of the OSR:PD. The Power Down mode takes effect in both operational states. The active Power Down state in measurement state can be used between two consecutive measurements. The start-up time $t_{SUPDOFF}$ is to be considered before the new conversion can be started.

6.3 API Generation Register – AGEN

The value of this read-only register indicates the generation of the control register bank. The register's value changes whenever any formal modification is introduced to the control register bank. This case indicates that the Application Programming Interface (API) has been changed.

Table 9: Register AGEN – Address 02h

AGEN	Name	Value [b]	Description
bit 7 to 4	DEVID	0100	device ID number; the value ‚0100b' is reserved for AS89020 devices
Bit 3 to 0	MUT	0000	version number of control register bank

6.4 Configuration Register – CREG

The register CREG configured the main characteristics of AS89020.

Table 10: Register CREG - Address 06h

CREG	NAME	VALUE [B]	DESCRIPTION
		0	disable the temperature compensation
		1[9]	enable the temperature compensation
		0[9]	no offset signal will be generated at all inputs INX
		1	generates offset signal of ‚63dec' for all inputs INX
		0	input current direction is out of the inputs INX – common anode photodiodes (see Figure 15 (b))

[9] Default after power-on-reset

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CREG	NAME	VALUE [B]	DESCRIPTION
		1[9]	input current direction is into the inputs INX – common cathode photodiodes (see Figure 15 (a))
		0[9]	the falling edge of the signal CSN captures the sample of the input signals at all INX
		1	the falling edge of the signal CONVN captures the sample of the input signals at all INX
		0[9]	set for a supply voltage > 2.9 V
		1	set for a supply voltage <= 2.9 V
bit 2-0		000[10]	reserved; these bits must be set to ‚000b' otherwise the operation of the AS89020 fails

For better understanding of the proper use of CREG:TCOMPENA please see chapter 5.7.

The bit CREG:OFFGEN enables an internal offset generation for the input currents of all INX and for their conversion results. It helps to measure very low (e.g. zero) input currents even in presence of a negative leakage current at the inputs INX, which would normally lead to an underflow. The conversion result under ideal conditions (no device offsets and no leakage currents) would lead to a decimal value of 63 (‚3Fh'). This must be considered for the conversion result under real conditions.

The bit CREG:DIR must be set depending on which direction the input current flows of all inputs INX.

For the proper use of the bit CREG:STARTSIG please see chapter 6.4 .

The bit CREG:SETVB is very important to concerning the power supply range of the AS89020, which is used.

6.5 Transimpedance Register – SW_RX

The transimpedance of each channel can be chosen by setting the register SW_RX, where X stands for the channel number 0…3, so every channel comes with its own register. The bits SW_RX[3:0] support a binary subdivision of the transimpedance for each channel. Using additional bit SW_RX[4] some intermediate stages of a few more transimpedance values can be chosen.

The bit SW_RX[5] is for a special purpose. If SW_RX[5] is set to '1b', the input of the transimpedance amplifier will disconnected from the appropriate input pin (IN[x]). So the leftover offset of the internal chip could be measured. The offset value depends on the settings for the transimpedance defined by SW_RX[4:].

During the configuration of the transimpedance via SPI the leading bits SW_RX[7:6] should be ‚00b'.

Table 11: Registers SW_RX (X = 0…3) – Addresses 07h, 08h, 09h and 0Ah

STAGE	SW_RX[4] [B]	SW_RX[3:0] [HEX]	TRANSIMPEDANCE [MΩ]	ADC REFERENCE CURRENT (FSR)	
0	0	0	0.1	12 µA	$6 \cdot 2^{1}$ µA
1[10]	0	1	0.2	6 µA	$6 \cdot 2^{0}$ µA
2	0	2	0.4	3 µA	$6 \cdot 2^{-1}$ µA
3	0	3	0.8	1.5 µA	$6 \cdot 2^{-2}$ µA
4	0	4	1.6	750 nA	$6 \cdot 2^{-3}$ µA

[10] Default after power-on-reset.

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STAGE	SW_RX[4] [B]	SW_RX[3:0] [HEX]	TRANSIMPEDANCE [MΩ]	ADC REFERENCE CURRENT (FSR)	
5	0	5	3.2	375 nA	$6 \cdot 2^{-4}$ µA
6	0	6	6.4	187.5 nA	$6 \cdot 2^{-5}$ µA
7	0	7	12.8	93.75 nA	$6 \cdot 2^{-6}$ µA
8	0	8	25.6	46.875 nA	$6 \cdot 2^{-7}$ µA
9	0	9	51.2	23.4375 nA	$6 \cdot 2^{-8}$ µA
10-15	0	A, B, C, D, E, F	102.4	11.71875 nA	$6 \cdot 2^{-9}$ µA
16-20	1	0, 1, 2, 3, 4	2.4	500 nA	$4 \cdot 2^{-3}$ µA
21	1	5	4.8	250 nA	$4 \cdot 2^{-4}$ µA
22	1	6	9.6	125 nA	$4 \cdot 2^{-5}$ µA
23	1	7	19.2	62.5 nA	$4 \cdot 2^{-6}$ µA
24	1	8	38.4	31.25 nA	$4 \cdot 2^{-7}$ µA
25-31	1	9, A, B, C, D, E, F	76.8	15.625 nA	$4 \cdot 2^{-8}$ µA

6.6 Channel Power Down Register – CH_PD

The Power Down setting for each transimpedance amplifier channel separately or their combination can be programmed in register CH_PD as shown in Table 12. It is valid as long as the bit OSR:PD = ‚0b' and the pin PDN = VDD.

A Power Down for the whole device can be activated by setting bit OSR:PD to ‚1b' or PDN = VDD, which overrides the channel Power Down settings via register CH_PD (see also chapter 5.3).

Table 12: Register CH_PD – Address 0Bh

CH_PD	NAME	VALUE [B]	DESCRIPTION
bit 7 to 4		0000[11]	reserved
		0000[11]	all channels active
		XXX1	Power Down mode for channel 0
		XX1X	Power Down mode for channel 1
		X1XX	Power Down mode for channel 2
		1XXX	Power Down mode for channel 3

[11] Default after power-on-reset

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6.7 Channel Order Register – CH_ORDER

The conversion and read out order of the four channels after every sampling can be programmed freely by register CH_ORDER. Every channel address must be present one time.

Table 13: Register CH_ORDER – Address 0Ch

CH_ORDER	Name	Value [b]	Description
bit 7-6	1st	xx	address of channel to be converted and read 1st (default 00)
bit 5-4	2nd	xx	address of channel to be converted and read 2nd (default 01)
bit 3-2	3rd	xx	address of channel to be converted and read 3rd (default 10)
bit 1-0	4th	xx	address of channel to be converted and read 4th (default 11)

As an example for an order to read out channel 3, 2, 0 and 1 register CH_ORDER has to be set with the value ‚11100001b'.

6.8 Channel Output Data Format

The channel conversion result is always 2 bytes long and contains some status information (4 MSB) and the 12 bit value of the ADC (see Table 14).

Table 14: Channel Output Data Format

Channel (Output) Data	Name	Description
bit 15–14	CHANNEL	return of channel address (‚00b' for IN0 until ‚11b' for IN3)
bit 13	STARTSIG	shows the actually used sample signal returns ‚0' for CSN and ‚1' for CONVN
bit 12	TR_ON	active only if STARTSIG = ‚1' returns a ‚1' if the CONVN sample signal came before the start of conversion by CSN
bit 11–0	ADC	12 bit result of the AD conversion (bit 11 = MSB)

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7 EXAMPLES OF COMMUNICATION VIA SPI

After a power-up, the device is in the default configuration state. The user can now set up the device for the application by writing control register. Success of the configuration can be proven by reading the control register.

Before a measurement can be started, the device must change its state to the measurement state. The last three bits of OSR:DOS must be loaded with ‚011b'. Now a conversion can be started, it will start accordingly to the falling edge of signal CSN or CONVN after tracking the input signals.

In order to change configuration settings the user has to switch back to the configuration state first.

Some examples of usual SPI communication sequences are shown in the following figures.

a.) Example of Configuration SPI sequences

First of all it is possible to enable the tracking phase (OSR:TRACK = ‚1b')
To show a register read process, the address ‚02h' is chosen (AGEN).

	S	WA	WD	RA	X
SDI	**S**	**00h**	**80h**	**02h**	**X**
SDO	**S**	**XXh**	**XXh**	**XXh**	**X**

During sending the three SDI bytes three SDO bytes are received. In this case these SDO bytes are of no relevance.

In the next cycle the first received byte on SDO is ‚02h'. The following 2 byte are meaningless. The first transmitted 2 bytes on SDI are always for a "register write" cycle. In the example only a read (SDO) is relevant. No register write should occur, since this the write address (WA) is ‚01h' (not defined write register). The write data (WD) in the second byte is meaningless. Since no additional register should be read, the read address (RA) in byte 3 is also meaningless.

	S	WA	WD	RA	X
SDI	**S**	**01h**	**XXh**	**XXh**	**X**
SDO	**S**	**02h**	**XXh**	**XXh**	**X**

b.) Example of Changing to Measurement State

To proceed the AS89020 switches to the measurement state the OSR:DOS is set to ‚03h'. OSR:TRACK is set to ‚1b' to keep tracking active. After all OSR is set to ‚83h'. The read address of third byte at SDI is meaningless, because of the format change to two bytes during measurement state (see chapter 5.8).

	S	WA	WD	RA	X
SDI	**S**	**00h**	**83h**	**XXh**	**X**
SDO	**S**	**XXh**	**XXh**	**XXh**	**X**

The three SDO bytes are of no relevance.

c.) Example of Measurement SPI sequences

After the last transferred byte at SDI (3rd byte of example b), the next falling edge of the chip select signal CSN stops the tracking and samples the input signals of all 4 channels. The clock signal SCLK starts the conversion and also immediately the read out of conversion result byte-by-byte. At the same time the input stream at SDI for write address WA and write data WD could be for the register OSR with no operation or no change (WA = ‚00h' and WD = ‚00h'). In order to start a new tracking cycle the last data byte WD should be ‚80h'.

	S	WA	WD	WA	WD	WA	WD	WA	WD	X
SDI	**S**	**00h**	**00h**	**00h**	**00h**	**00h**	**00h**	**00h**	**80h**	**X**
SDO	**S**	**CH0[15:0]**		**CH1[15:0]**		**CH2[15:0]**		**CH3[15:0]**		**X**

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Activate or Deactivate Power Down Mode within the Measurement State
Within the measurement state the Power Down mode can be activated and subsequently deactivated by the following frames.

Activate Power Down Mode:

	S	WA	WD	X
SDI	**S**	**00h**	**40h**	**X**
SDO	**S**	**XXXXh**		**X**

Deactivate Power Down Mode and start Tracking within the Measurement State:

Figure 10: Example of Switching from Measurement State to Configuration State

	S	WA	WD	X
SDI	**S**	**00h**	**80h**	**X**
SDO	**S**	**XXXXh**		**X**

If a new configuration should be set, the device has to change its state back to configuration by writing ‚010b' into the three lowest bits of OSR:DOS (see Table 8). During this action all control registers (except OSR itself) will reset to their default values. A new configuration cycle can be started now.

	S	WA	WD	X
SDI	**S**	**00h**	**02h**	**X**
SDO	**S**	**XXXXh**		**X**

8 PACKAGE

8.1 Shape & Dimensions

Figure 11: Shape for Package

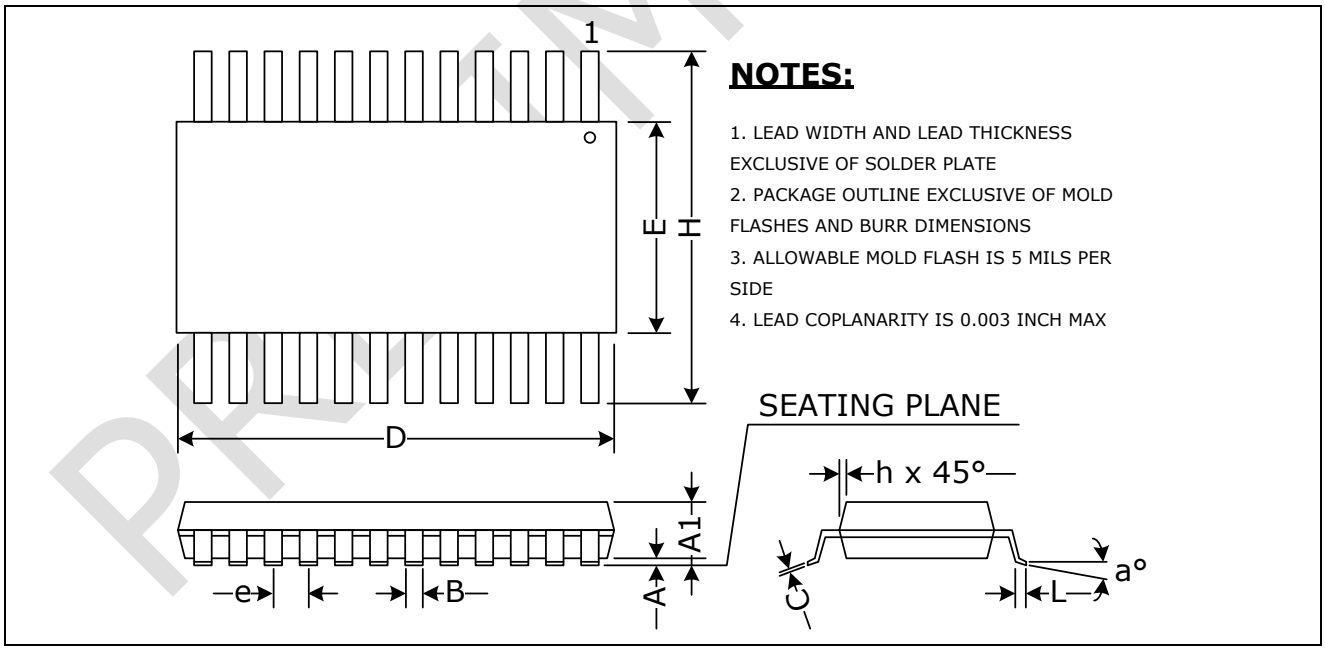


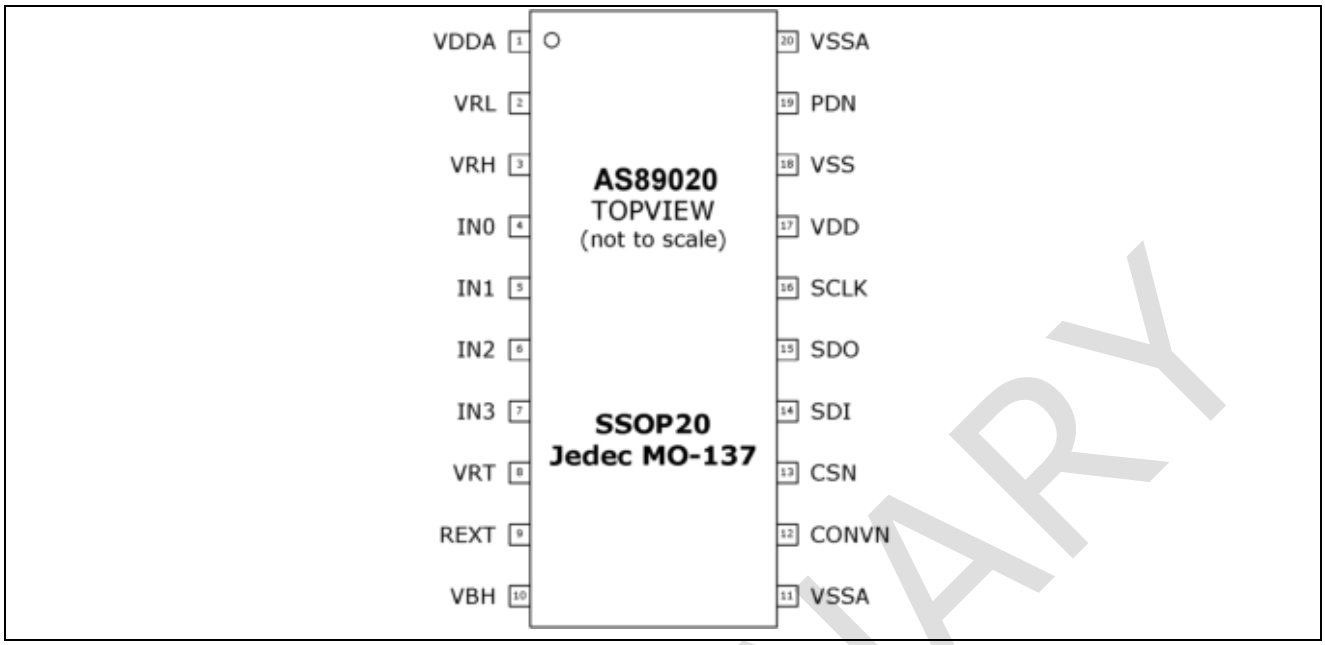
Table 15: Dimensions for Package (Dimensions are given in Inches, BSC = Basic Spacing between Centers)

TYP	PACKAGE	A	A1	B	C	D	E	e	H	h	L	a°
AS89020	SSOP20 JEDEC MO-137	0.060 – 0.068	0.004 – 0.008	0.009 – 0.012	0.007 – 0.010	0.337 – 0.344	0.150 – 0.157	0.025 BSC	0.230 – 0.244	0.010 – 0.016	0.016	0° – 8°

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8.2 Pin Configuration

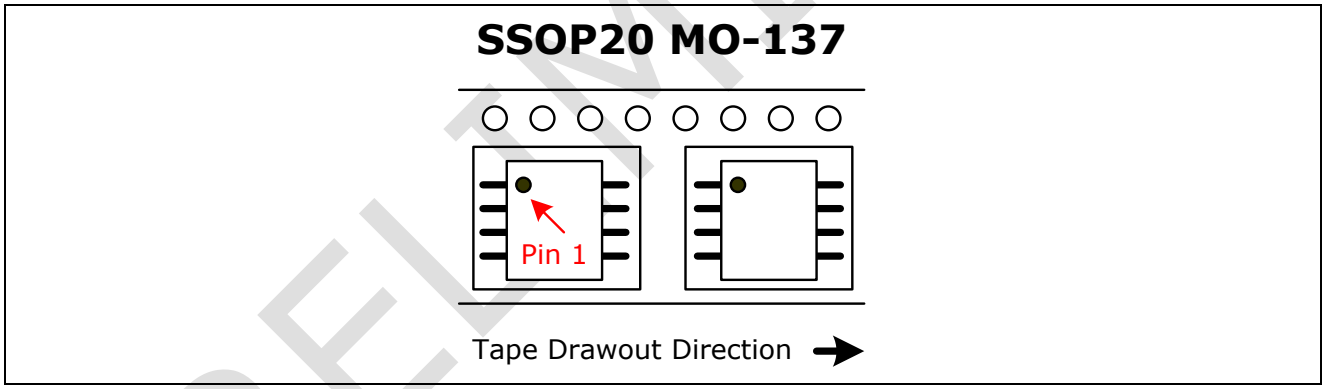
Figure 12: Pin Configuration



8.3 Packing Information

Standard packing is tape and reel or tube. Otherwise it has to be discussed with our sales team.

Figure 13: Standard packing



8.4 Soldering Information

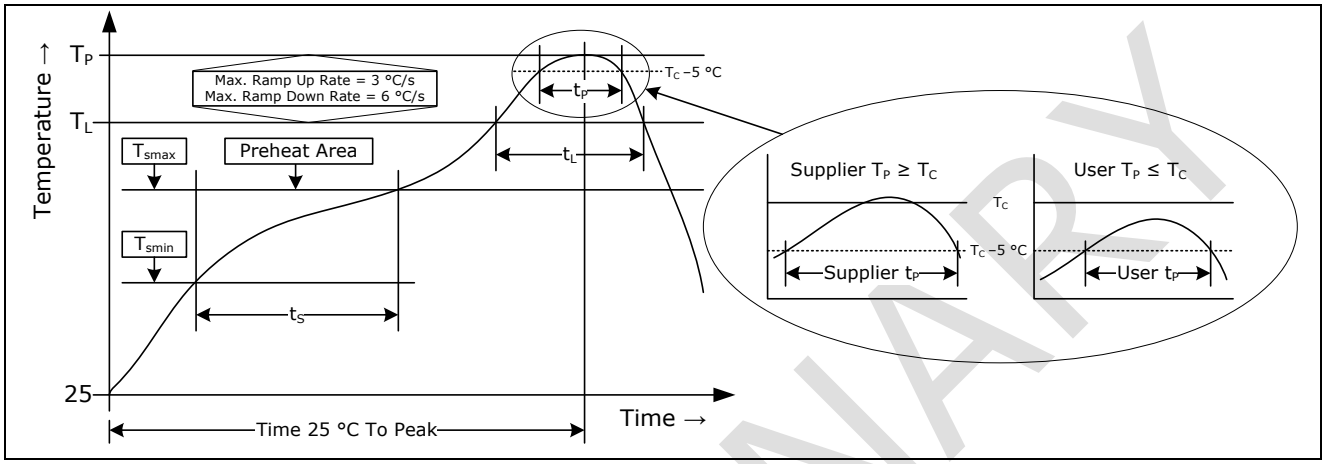
Table 16: Profile features according JEDEC

	IPC/JEDEC J-STD-020D.1 (Pb-Free)	RECOMMENDED DATA
Time [s] from 150°C to 200°C (preheat)	60 – 120	100
Average ramp-up rate [°C/s] (200°C to peak temperature)	max. 3.0	0.5 – 1.0
Liquid's temperature [°C] Time [s] above liquid's (217°C)	217 60 – 150	217 110
T_P Peak package body temperature [°C]	max. 260	≤ 260
Time [s] within 5°C of the classification temperature T_C	min. 30	35 – 45

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	IPC/JEDEC J-STD-020D.1 (Pb-Free)	RECOMMENDED DATA
Average ramp-down rate [°C/s] (Peak temperature to 200°C)	max. 6.0	3.0
Time [s] from 25°C to peak temperature	max. 480	350

Figure 14: recommend soldering profile

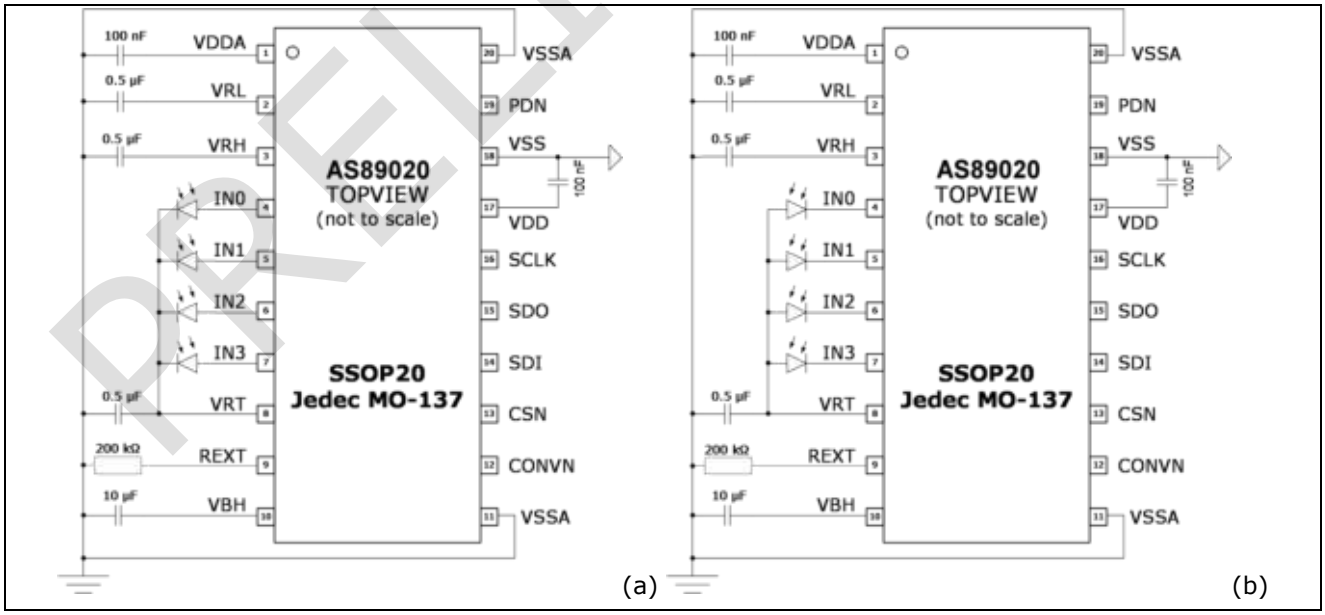


Do not to exceed the recommended values. For further information see JEDEC J-STD-020D.1.

9 APPLICATION NOTES

Figure 15 shows typical connections of external devices to the AS89020. If digital and analog grounds are routed separately onto the printed circuit board, they should be connected together near the device.

Figure 15: Typical Connection Circuitry – (a) Common Cathode Photodiode Array (CREG:DIR = ‚1b'), (b) Common Anode Photodiode Array (CREG:DIR = ‚0b')

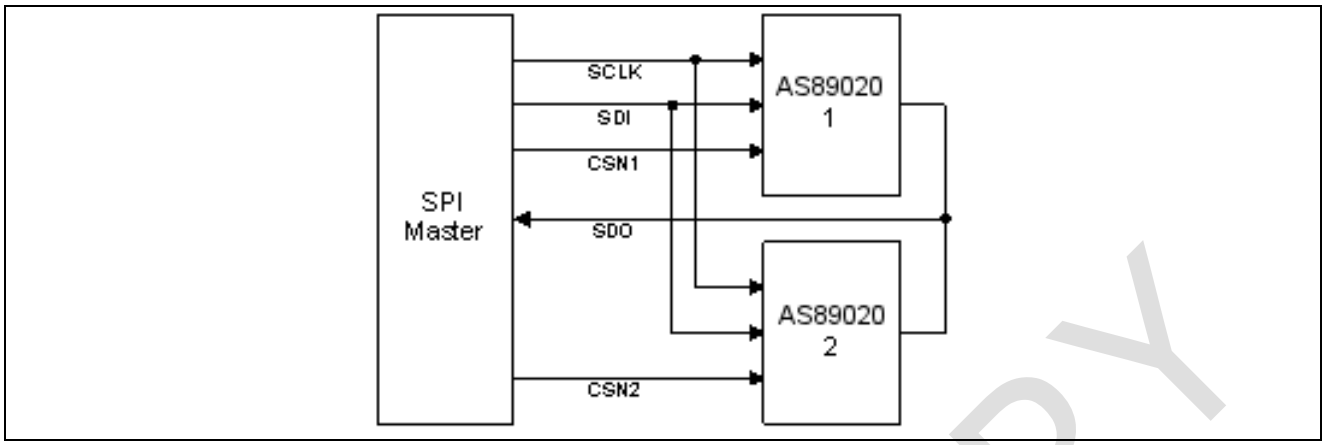


Please make sure that all specified components within your application circuit operate according to their working range and to the parameters in the data sheet. For example, photodiode sensor (input current) and voltage regulators (workspace load current, separated analog and digital or decoupled power supplies based on a common regulator) need special treatment to avoid noise or deviations during operation.

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Figure 16 shows the SPI interconnection of two AS89020 in principle.

Figure 16: Symbolic Interconnection of two AS89020



10 NOTES FOR PCB LAYOUT

The connections to the inputs IN0…IN3 of the AS89020 have to be protected against any kind of electromagnetic coupling and have to be guarded with VRT potential to avoid leakage currents. Without guarding layers at the inputs the isolation resistance of the PCB gives leakage currents with equivalent values like the sensor currents

The analog supply for AS89020 must be placed as close as possible to the converter. The connection between the analog and digital ground should be beneath (LP level) and/or near the AS89020 (Pins 18 & 20).

Digital signals and circuit lines with high current loads must not be used directly beneath and next to the photodiode sensor as well as the AS89020.

The AS89020 converter operates internally with minimal currents (pAmps). Therefore, protection measures need to be performed to shield the IC against EMC stress or external interferences.

The connections between the photodiode sensor (anode and cathode) and the AS89020 should be as short as possible (< 10 mm) and without interlayer connections.

Photodiode sensor, AS89020 and its REXT should be placed on the same PCB side. The signal VRT (common cathode or common anode) should have the same cross-section as the four sensor connectors.

Around signal lines a conductor connected with VRT should be created. One level below the signals a VRT potential area should be created that extends only to the analog inputs and the signal lines.

PRELIMINARY

ORDERING INFORMATION

NAME	Status	PACKAGE	Article
AS89020	Series	SSOP20	305040004

PRELIMINARY

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PRELIMINARY

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