

Description

The Abracon ASEMP series is a programmable MEMS oscillator, with a continuous operating power supply ranging from 2.25V to 3.6V. This series features low power consumption, a wide frequency range, excellent phase noise, tight stabilities, and short lead times for industrial, consumer, and other applications. The ASEMP series comes in a 3.2 x 2.5 mm compact package with CMOS, HCSL, LVDS, or LVPECL output logic.



Features

- Low Power Consumption for high-speed communication
- Exceptional Stability Over Temp. at -40 to +85°C, ± 10 ppm
- Extended Operating Temperature at -55 to +125°C, ± 25 ppm
- MIL-STD-883 shock and vibration compliant
- Durable QFN Plastic Compact Packaging
- Enable or Disable Tri-state function
- Low jitter (Period jitter RMS and Phase jitter RMS)
- High power supply noise reduction, -50dBc
- [REACH/RoHS II Compliant](#) | [MSL Level 1](#)

Applications

- Storage Area Networks (SATA, SAS, Fiber Channel)
- Passive Optical Networks (EPON, 10G-EPON, GPON, 10G-PON)
- Ethernet (1G, 10GBASE-T, KR/LR/SR, FCoE)
- PCI Express
- Display port

Key Electrical Specifications - Continuous Vdd: 2.5V - 0.25V to 3.3V + 0.3V

Parameters		Min.	Typ.	Max.	Units	Notes
Frequency Range	CMOS	2.3000		170.0000	MHz	-20 ~ +70°C -40 ~ +85°C
	CMOS	3.3000		170.0000		-40 ~ +105°C -55 ~ +125°C
	LVPECL	2.3000		460.0000		-20 ~ +70°C -40 ~ +85°C -40 ~ +105°C
	LVDS	2.3000		460.0000		-20 ~ +70°C -40 ~ +85°C -40 ~ +105°C
	HCSL	2.3000		460.0000		-20 ~ +70°C -40 ~ +85°C -40 ~ +105°C
Operating Temperature		-20		+70	°C	See options
Storage Temperature		-55		+150	°C	
Overall Frequency Stability [Note 1]		-50		+50	ppm	See options
Supply Voltage (Vdd)		+2.25		+3.6	V	
Startup Time				5	ms	
Enable Time				20	ns	STD (Tri-state)

Key Electrical Specifications Cont. - CMOS, LVPECL, LVDS, and HCSL

Parameters	Min.	Typ.	Max.	Unit	Notes
Disable Time			5	ns	
Disable Current		20	22	mA	STD (Tri-state)
Tri-state Function (Enable/Disable)	"1" ($V_{IH} \geq 0.75 \cdot V_{DD}$) or Open: Oscillation "0" ($V_{IL} < 0.25 \cdot V_{DD}$): Hi Z			V	40k Ω pull-up resistor embedded
Aging	-5.0		+5.0	ppm	First year

Note 1: Includes post reflow frequency accuracy, temperature stability, load pulling and power supply variation.

Key Electrical Specifications - CMOS

Parameters		Min.	Typ.	Max.	Units	Notes
Supply Current (I _{DD})			31	35	mA	CL=15pF, 125MHZ
Output Logic Level	V _{OH}	0.9*V _{DD}			V	I=±6mA
	V _{OL}			0.1*V _{DD}	V	
Rise Time	T _r		1.1	2.0	ns	CL=15pF 20% to 80%
Fall Time	T _f		1.3	2.0	ns	
Duty Cycle		45		55	%	
Integrated Phase Jitter (J _{PH})			0.30	2	ps	200kHz ~ 20MHz@125MHz
			0.38	2		100kHz ~ 20MHz@125MHz
			1.70	2		12kHz ~ 20MHz@125MHz
Period Jitter RMS (J _{PER})			3.0		ps	

Key Electrical Specifications - LVPECL

Parameters		Min.	Typ.	Max.	Units	Notes
Supply Current (I _{dd})			56.5	58	mA	RL= 50Ω
Output Logic Level	V _{OH}	V _{dd} -1.08			V	RL= 50Ω
	V _{OL}			V _{dd} -1.55	V	
Peak to Peak Output Swing (V _{pp})			800		mV	Single ended
Rise Time:	T _r		250		ps	RL=50Ω , CL=0pF 20% to 80%
Fall Time:	T _f		250			
Duty Cycle		48		52	%	Differential
Integrated Phase Jitter (J _{PH})			0.25	2	ps	200kHz~20MHz@156.25MHz
			0.38	2		100kHz~20MHz@156.25MHz
			1.70	2		12kHz ~ 20MHz@156.25MHz
Period Jitter RMS (J _{PER})			2.5		ps	

Key Electrical Specifications - LVDS

Parameters		Min.	Typ.	Max.	Units	Notes
Supply Current (I _{dd})			29	32	mA	RL= 100Ω
Output Offset Voltage (ΔV _{OS})		1.125		1.4	V	RL= 100Ω differential
Delta Offset Voltage (ΔV _{OS})				50	mV	
Peak to Peak Output Swing (V _{pp})			350		mV	Single ended
Rise Time:	T _r		200		ps	RL=50Ω , CL=2pF 20% to 80%
Fall Time:	T _f		200			
Duty Cycle		48		52	%	Differential
Integrated Phase Jitter (J _{PH})			0.28	2	ps	200kHz~20MHz@156.25MHz
			0.40	2		100kHz~20MHz@156.25MHz
			1.70	2		12kHz ~ 20MHz@156.25MHz
Period Jitter RMS (J _{PER})			2.5		ps	

Key Electrical Specifications - HCSL

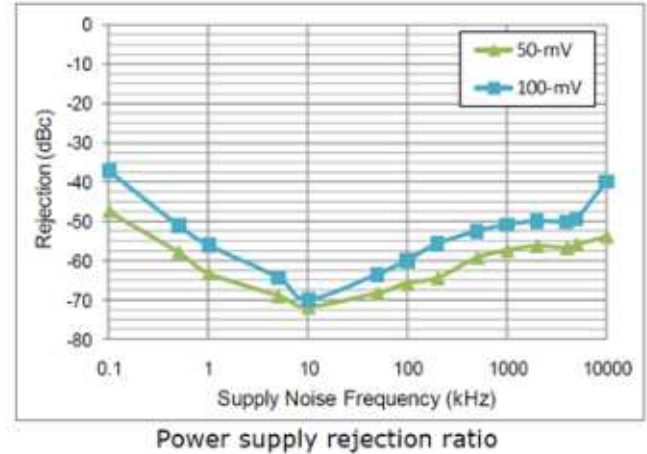
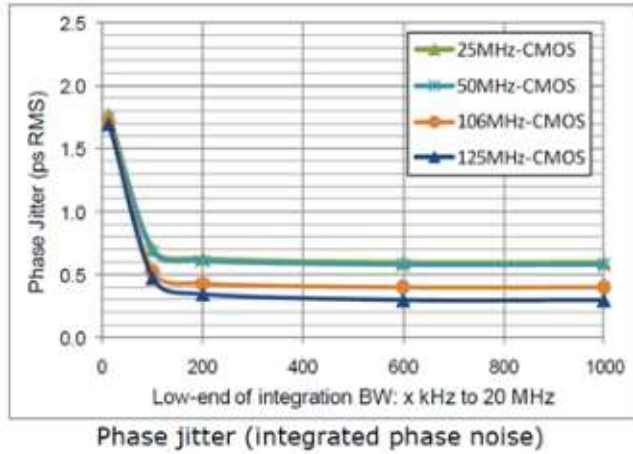
Parameters		Min.	Typ.	Max.	Units	Notes
Supply Current (I _{dd})			40	42	mA	RL= 50Ω
Output Logic Level	V _{OH}	0.725			V	RL= 50Ω
	V _{OL}			0.1	V	
Peak to Peak Output Swing (V _{pp})			750		mV	Single ended
Rise Time:	Tr	200		400	ps	RL=50Ω , CL=2pF 20% to 80%
Fall Time:	Tf	200		400		
Duty Cycle		48		52	%	Differential
Integrated Phase Jitter (J _{PH})			0.25	2	ps	200kHz ~ 20MHz@156.25MHz
			0.37	2		100kHz ~ 20MHz@156.25MHz
			1.70	2		12kHz ~ 20MHz@156.25MHz
Period Jitter RMS (J _{PER})			2.5		ps	

Absolute Maximum Ratings

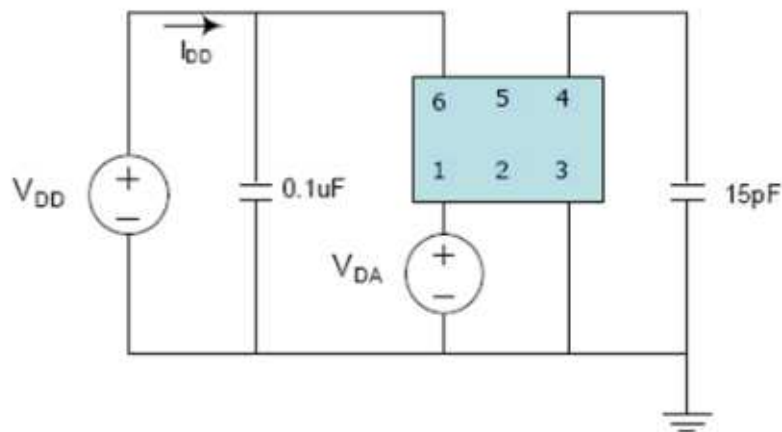
Item	Min.	Max.	Units
Supply Voltage	-0.3	+4.0	V
Input Voltage	-0.3	V _{dd} +0.3	V
Junction Temp.		+150	°C
Storage Temp.	-55	+150	°C
Soldering Temp.		+260	°C
ESD			
HBM		4,000	V
MM		400	
CDM		1,500	

Key Nominal Performance Parameters (Unless specified otherwise: $T=25^{\circ}\text{C}$, $V_{DD}=3.3\text{V}$)

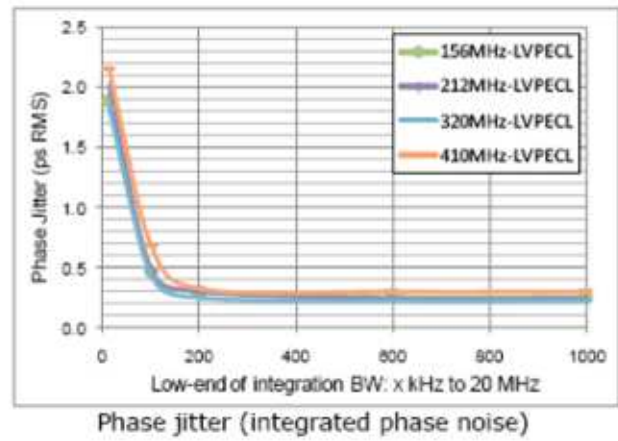
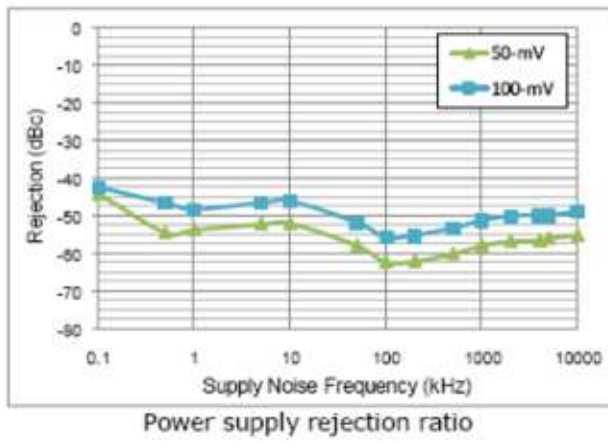
CMOS OUTPUT



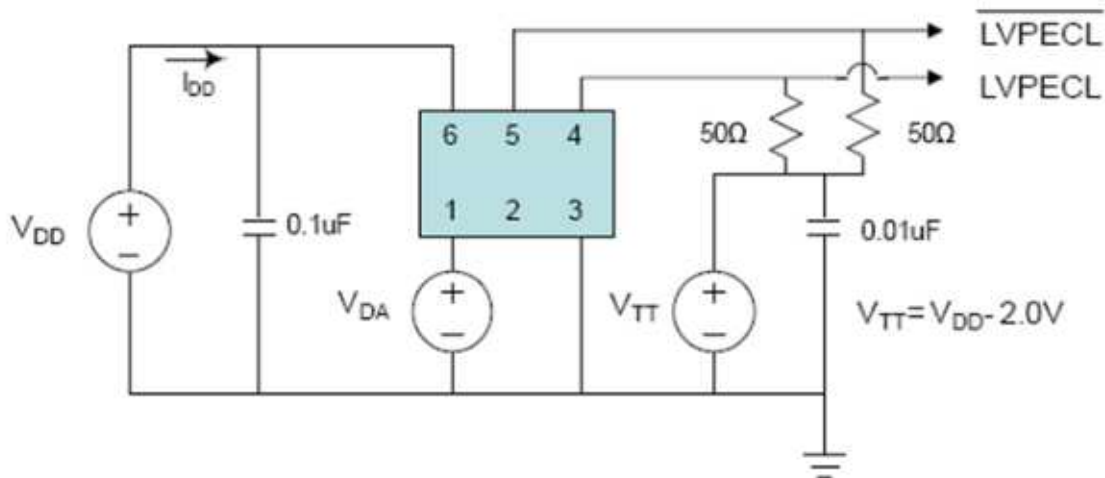
Test Circuit



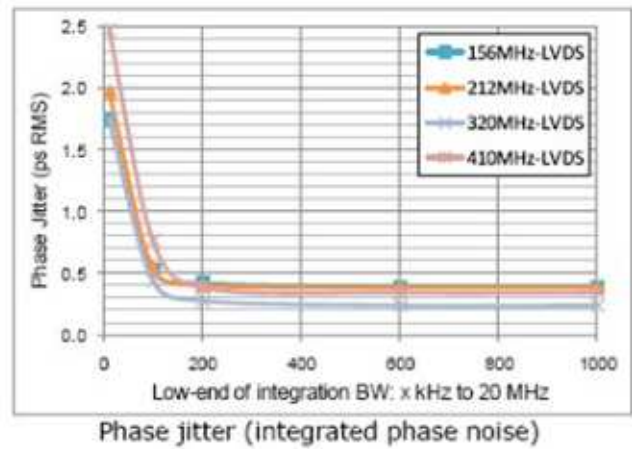
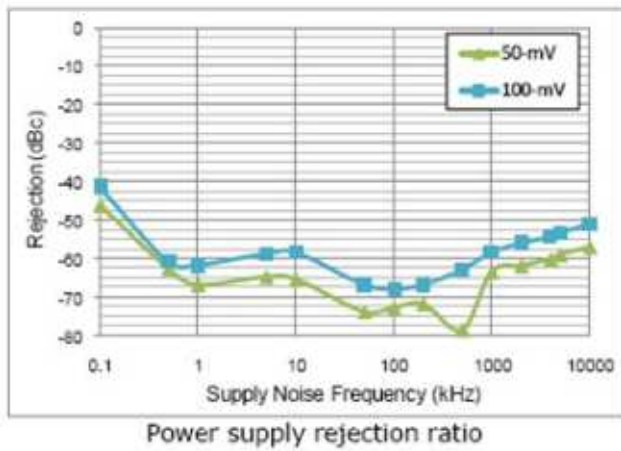
LVPECL OUTPUT



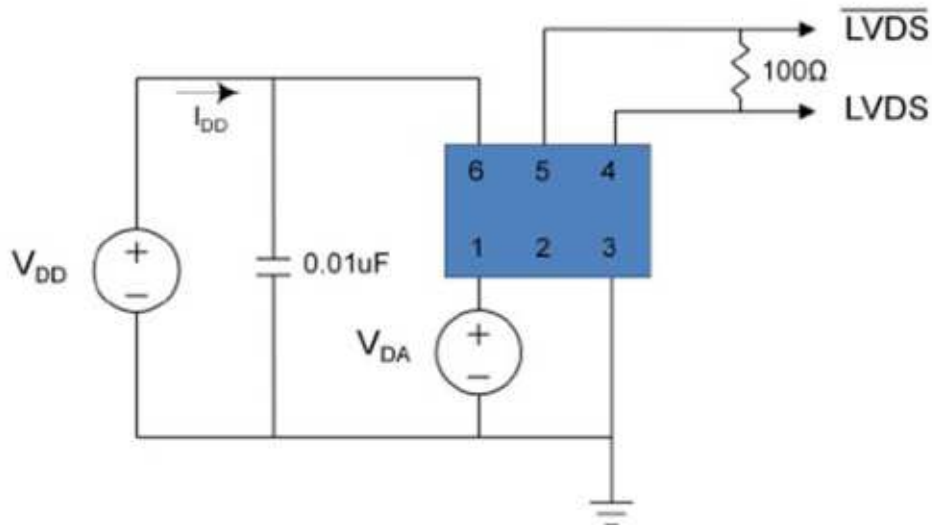
Test Circuit



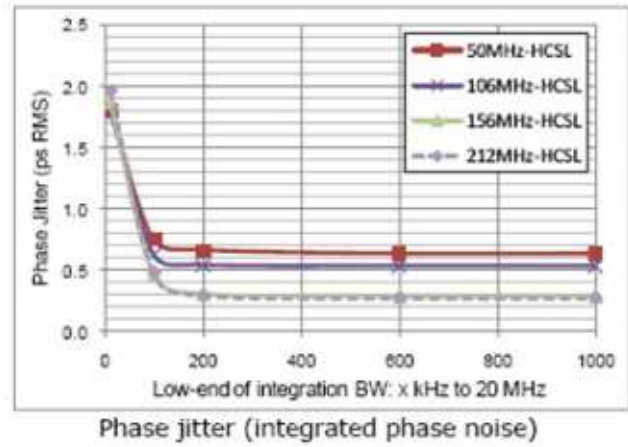
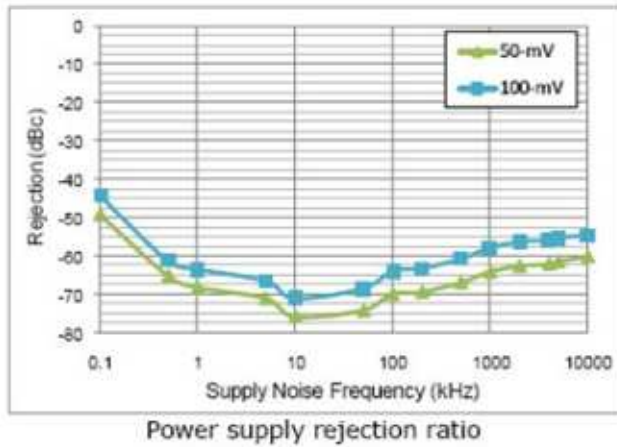
LVDS OUTPUT



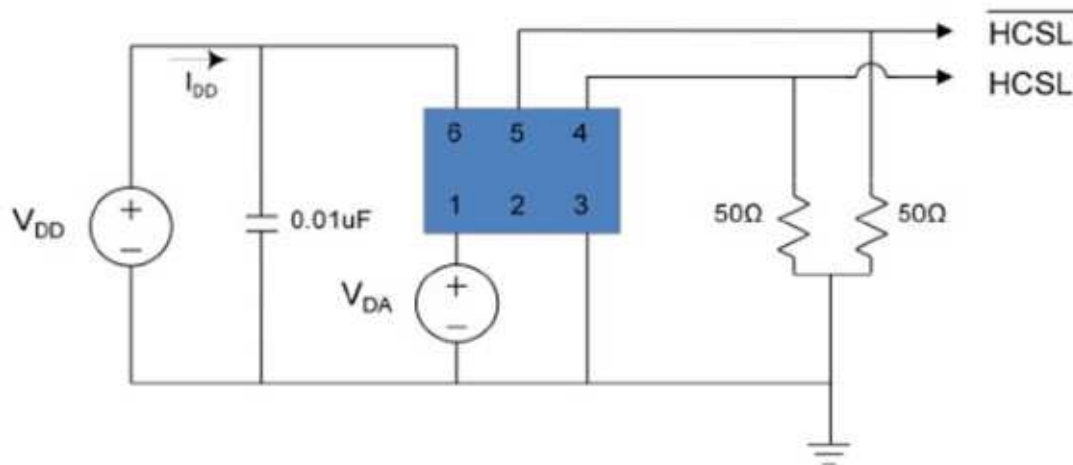
Test Circuit



HCSL OUTPUT



Test Circuit



Options and Part Identification (left blank if standard)

ASEMP - MHz - - -

Output Type
C : CMOS
LP : LVPECL
LV : LVDS
HC : HCSL

Frequency in MHz
e.g. 14.3181 MHz (Maximum 4 digits after decimal)

Operating Temp.
Blank: -20°C ~ +70°C
L: -40°C ~ +85°C
X: -40°C ~ +105°C
Z*: -55°C ~ +125°C

Overall Freq. Stability
Blank: ±50ppm
Y: ±10ppm*
R: ±25 ppm

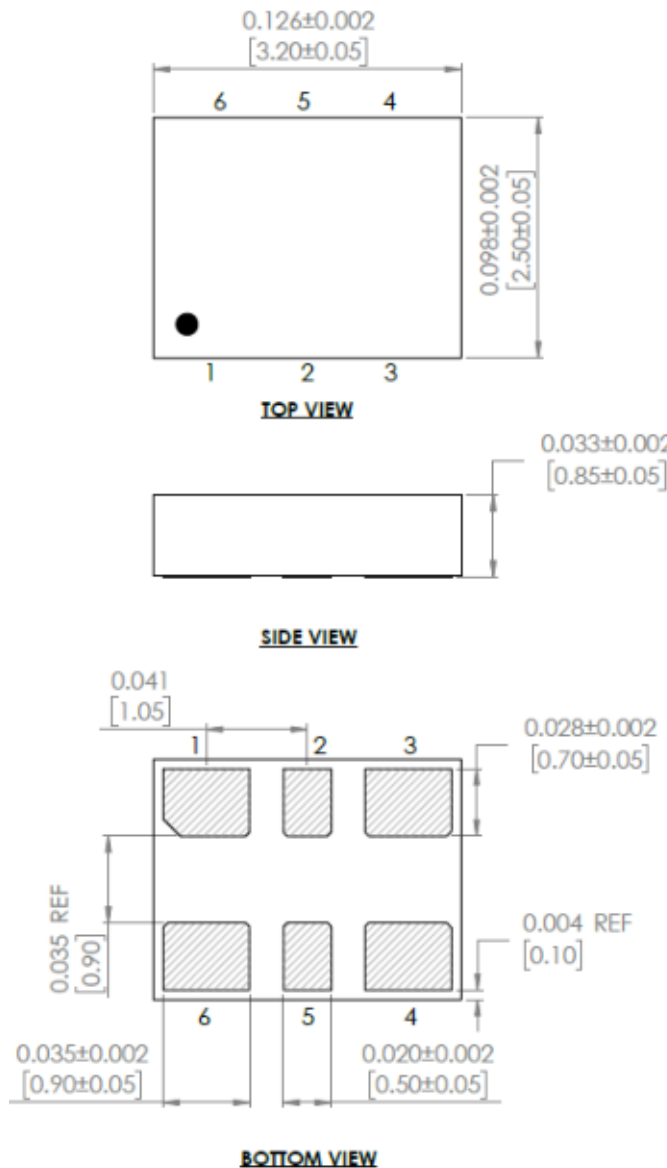
Tri-state (Pin 1)
Blank: Tri-state

Packaging
Blank: Bulk
T: Tape & Reel (1kpcs / reel)

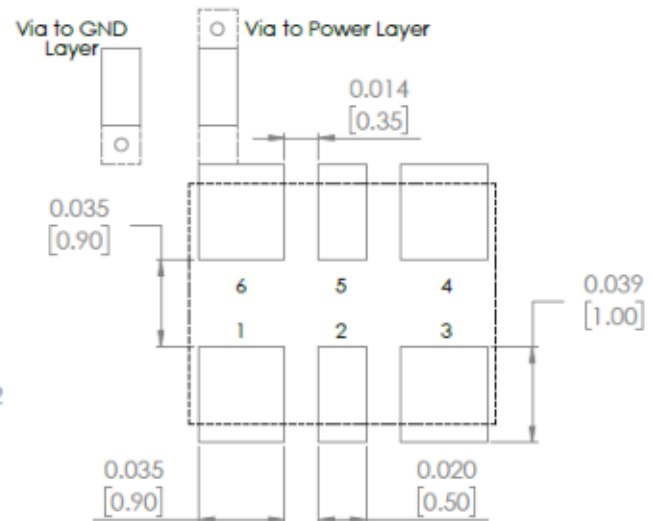
* Temp option L, X or -20°C ~ +70°C, only

** CMOS output only

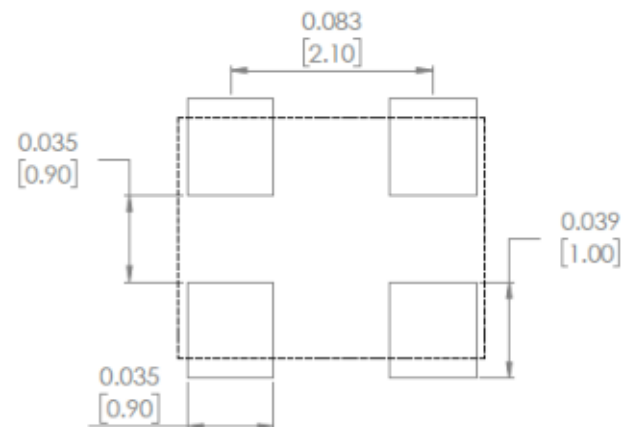
Mechanical Dimensions



Recommended Land Pattern FOR LVPECL, LVDS, HCSL



Recommended Land Pattern FOR CMOS



Note: Recommended using an approximately 0.01uF bypass capacitor between pin 6 and 3.

Dimensions: Inches[mm]

Pin #	Function
1	Tri-State
2	NC
3	GND
4	Output
5	NC (CMOS) Output (LVPECL, LVDS, HCSL)
6	Vdd

Reflow Profile [JEDEC J-STD-020]

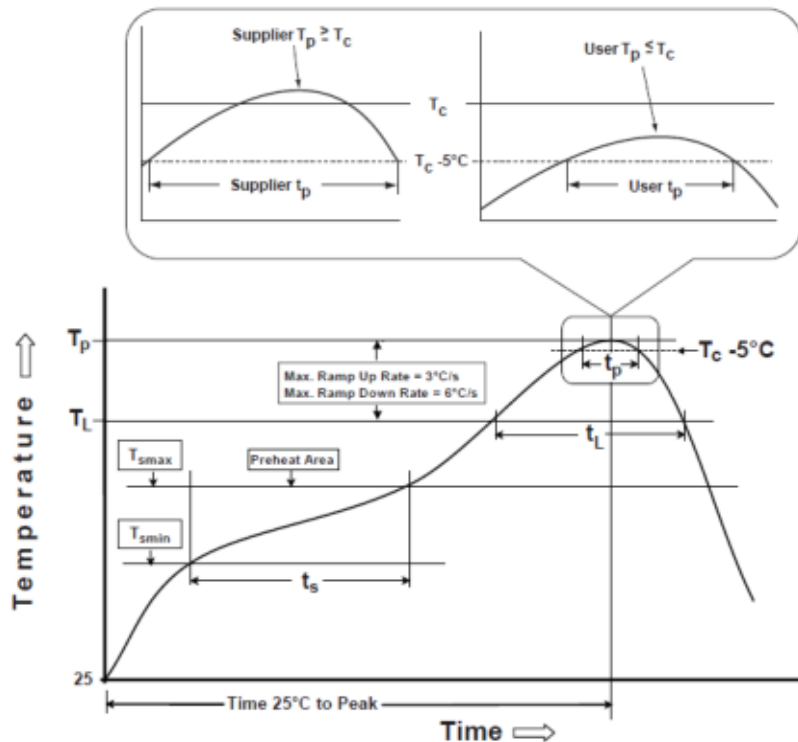


Table 1

SnPb Eutectic Process Classification Temperatures (T_c)		
Package Thickness	Volume mm^3 <350	Volume mm^3 ≥ 350
<2.5 mm	235 $^\circ\text{C}$	220 $^\circ\text{C}$
≥ 2.5 mm	220 $^\circ\text{C}$	220 $^\circ\text{C}$

Table 2

Pb-Free Process Classification Temperatures (T_c)			
Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 $^\circ\text{C}$	260 $^\circ\text{C}$	260 $^\circ\text{C}$
1.6 mm - 2.5 mm	260 $^\circ\text{C}$	250 $^\circ\text{C}$	245 $^\circ\text{C}$
>2.5 mm	250 $^\circ\text{C}$	245 $^\circ\text{C}$	245 $^\circ\text{C}$

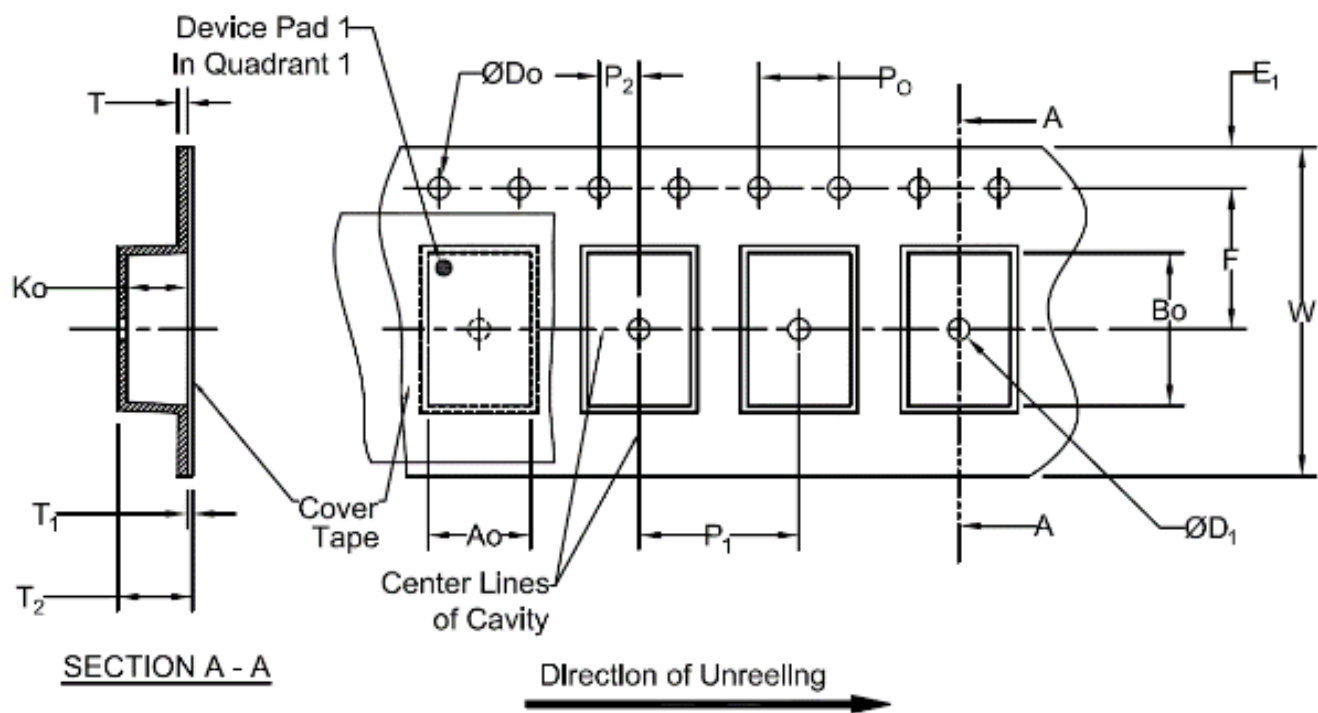
Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat / soak		
Temperature minimum (T_{smin})	100 $^\circ\text{C}$	150 $^\circ\text{C}$
Temperature maximum (T_{smax})	150 $^\circ\text{C}$	200 $^\circ\text{C}$
Time (T_{smin} to T_{smax}) (t_s)	60 - 120 sec.	60 - 120 sec.
Average ramp-up rate (T_{smax} to T_p)	3 $^\circ\text{C/sec. max}$	3 $^\circ\text{C/sec. max}$
Liquidous temperature (T_L)	183 $^\circ\text{C}$	217 $^\circ\text{C}$
Time at liquidous (t_L)	60 - 150 sec.	60 - 150 sec.
Peak package body temperature (T_p)*	see Table 1	see Table 2
Time (t_p)** within 5°C of the specified classification temperature (T_c)	20 sec.	30 sec.
Ramp-down rate (T_p to T_{smax})	6 $^\circ\text{C/sec. max}$	6 $^\circ\text{C/sec. max}$
Time 25 $^\circ\text{C}$ to peak temperature	6 min. max	8 min. max
Reflow cycles	2 max	2 max

*Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.

**Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

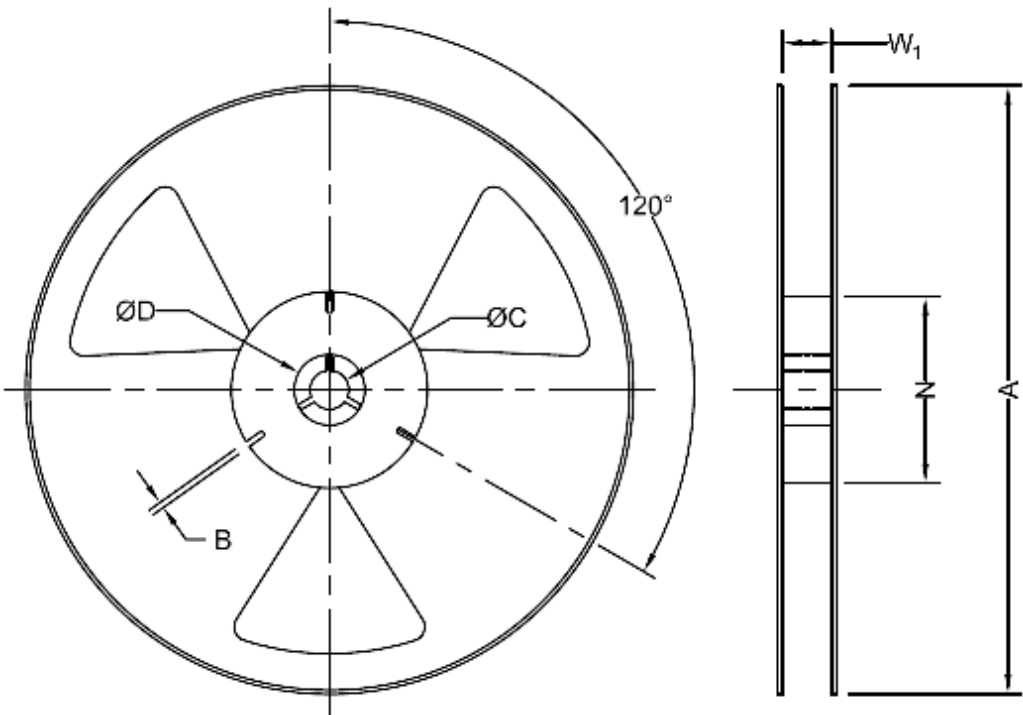
Packaging

T: 1,000pcs/reel (D=180mm)



Tape Specifications (mm)							
Width	Ao	Bo	Do	D ₁ (Min)	E ₁	F	Ko
12mm	*	*	1.5+0.1/-0.0	1.0	1.75±0.1	5.5±0.05	*
Width	P1	P2	P0	T (Max)	T1 (Max)	T2 (Max)	W (Max)
12mm	4.0±0.1	2.0±0.05	4.0±0.1	0.6	0.1	6.5	12.3
*Note: Compliant to EIA-481							

Dimensions: mm



Reel Specifications (mm)							
Width	Qty/Reel	A (Nom)	B (Min)	C (Min)	D (Min)	N (Min)	*W ₁
12mm	1000	178	1.5	13.0+0.5/-0.2	20.2	50	12.4+2.0/-0.0
*Note: Measured at Hub							

Dimensions: mm