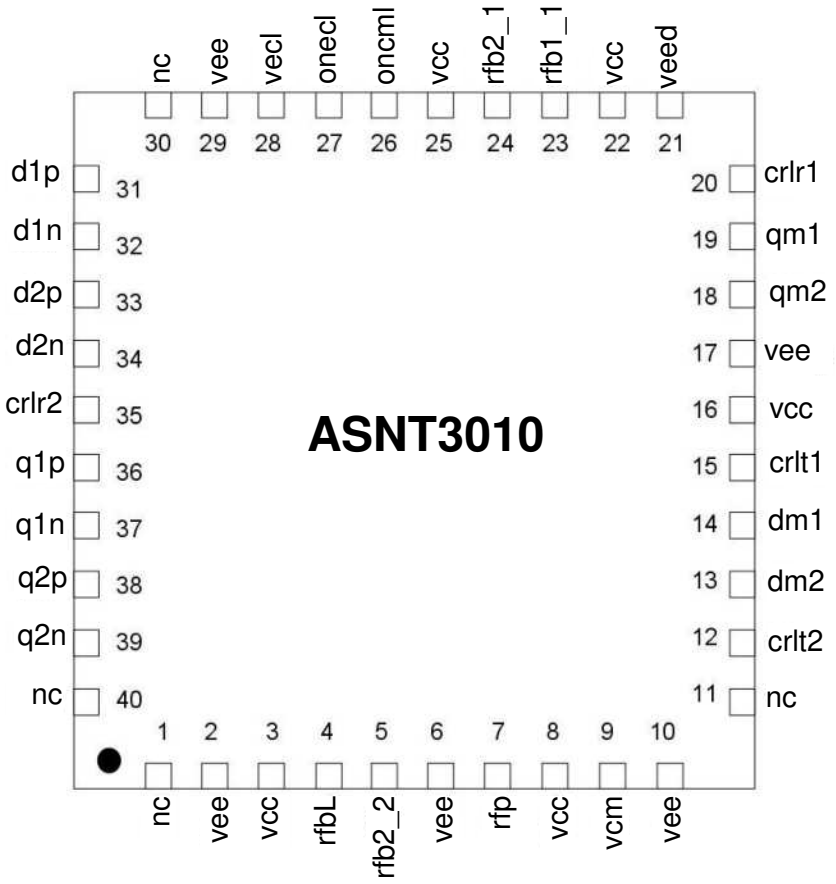
ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Drive Suite 112, Torrance, CA 90505

Offices: 310-530-9400 / Fax: 310-530-9402
www.adsantec.com

ASNT3010-PQB
DC-2*Gbps* LVDS/CMOS/LVDS Converter and Signal Splitter

- 2-channel LVDS-to-CMOS converter (Receiver) and 2-channel CMOS-to-LVDS converter (Transmitter)
- Optional signal splitter function with selectable inversion
- Optional DS (Data/Strobe) encoding/decoding for compatibility with Space Wire Standard
- Programmable LVDS/CML/ECL Receiver input interface
- True LVDS Transmitter output interface
- Flexible selection of enabling and operational modes of the channels
- High-impedance states of disabled CMOS outputs
- Single +3.3*V* power supply
- Industrial temperature range
- Power consumption: 115*mW* with all 4 channels enabled
- Standard MLF/QFN 40-pin package



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DESCRIPTION

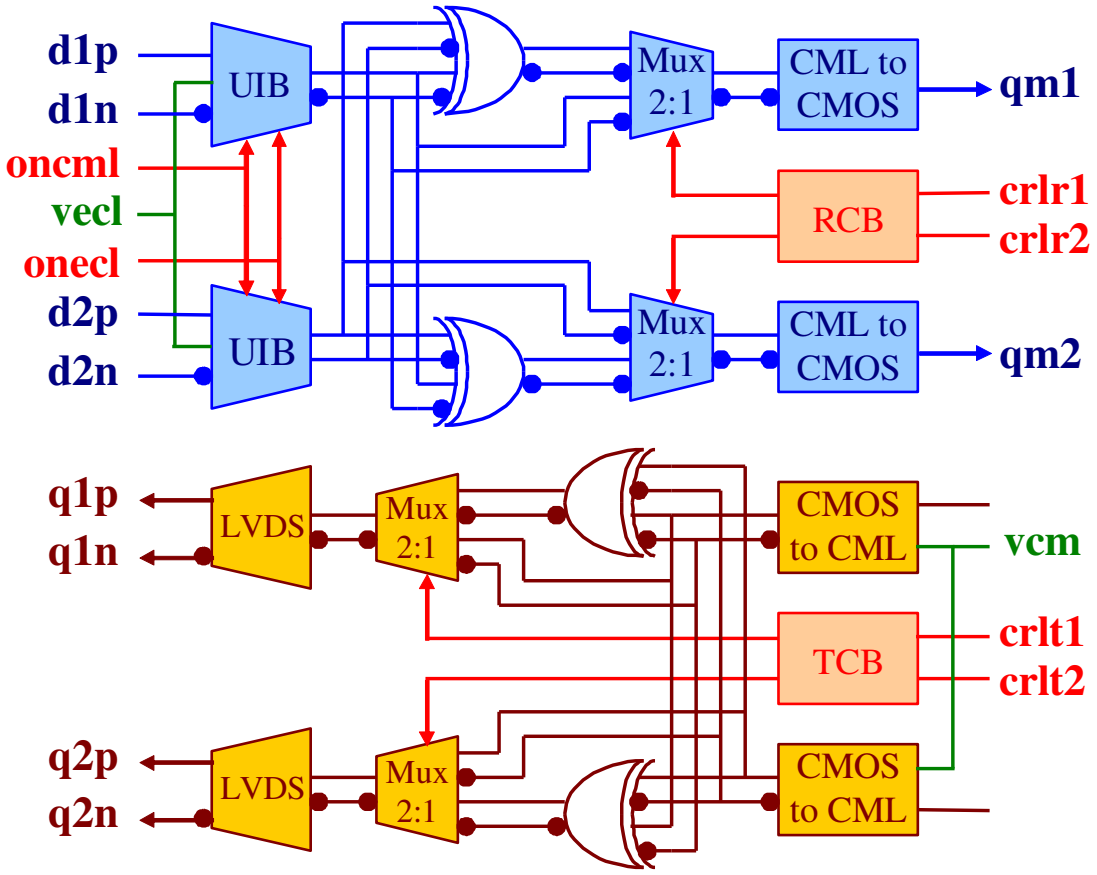


Fig. 1. Functional Block Diagram

ASNT3010-PQB is a bi-directional 4-channel digital interface converter. The part shown in Fig. 1 includes two individual receiver channels with programmable LVDS/CML/ECL differential inputs d1p/d1n, d2p/d2n, and CMOS outputs qm1, qm2; as well as two individual transmitter channels with CMOS inputs dm1, dm2 and LVDS differential outputs q1p/q1n, q2p/q2n.

All channels can be independently enabled or disabled by control signals crlr1, crlr2, crlt1, crlt2. When a receiver channel is disabled, the corresponding CMOS output drivers are set to a high impedance (high-Z) state. The individual receiver or transmitter channels can be combined into a corresponding Space Wire receiver or transmitter with an optional data/strobe (DS) encoding or decoding respectively. The assignment of the data and strobe, or data and clock signals to the individual channels is user-selectable.

Dual transmitter and/or receiver channels can be used for splitting one of the input signals into two exact copies at the two corresponding outputs. The signal at the second output can be inverted using the second input as a selector (a differential DC signal must be applied to the LVDS input). Detailed instructions for using this operational mode are available on request.

The converter operates from a single +3.3*V* power supply. The device is characterized for operation from −25°C to 125°C of junction temperature.

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Universal IB

The proprietary Universal Input Buffer (UIB) is designed to support one of three interfaces: LVDS, CML, or ECL. The type of interface is defined by two CMOS control signals oncml and onecl as shown in Table 1. In the ECL mode, it is required that the pin vecl is terminated to the specified voltage.

Table 1. LS Input Interface Selection

oncml	onecl	Interface type	Internal termination	vecl, *V*
vee (default)	vee (default)	LVDS	100*Ohm* differential	not used
vee	vcc	ECL	50*Ohm* SE to vecl	vcc-2.0
vcc	vee	CML	50*Ohm* SE to vcc	not used
vcc	vcc	Not allowed		

In the LVDS mode, the buffer exceeds the requirements of standards IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995. UIB is designed to accept differential signals with amplitudes above 60*mV* peak-to-peak, DC common mode voltage variation between the negative (vee) and positive (vcc) supply rails, and AC common mode noise with a frequency up to 5*MHz* and voltage levels ranging from 0 to 2.4*V*. It can also receive single-ended signals with swings above 60*mV*p-p and threshold voltages between vee and vcc.

CML-to-CMOS Converter

The CML-to-CMOS converter represents the output buffer of the receiver. It includes a signal converter based on a current mirror architecture and an output CMOS driver. The block operates at a data rate up to 2*Gbps*.

CMOS-to-CML Converter

The input CMOS-to-CML converter represents the input buffer of the transmitter. It is designed as a standard CML buffer with additional resistive dividers required for handling rail-to-rail CMOS signals.

LVDS Output Buffer

The proprietary LVDS output buffer utilizes NPN HBTs that are available in standard BiCMOS technologies. It accepts internal CML signals and converts them into output LVDS signals. The buffer utilizes a special architecture that ensures operation at data rates up to 2*Gbps* with a low power consumption level of 19*mW*. The buffer satisfies all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995.

Internal Data Processing Circuitry

The internal parts of all 4 channels include an XOR and multiplexer 2:1 CML cells. When activated, the XOR performs the DS encoding or decoding required by the Space Wire protocol, while the multiplexer operates as a selector of either the channel's input signal or the XOR-processed signals. The corresponding control signals are generated by the receiver or transmitter control blocks (RCB or TCB) from the 3-state external control signals.

Each channel can function as an independent converter, as well as a data/strobe or clock/strobe Space Wire encoder/decoder in accordance with Table 2 or Table 3. In the second mode, the device can also

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perform the 1-to-2 data splitting operation. The notations Out1, Out2, In1, and In2 in the tables represent the logic states of the corresponding outputs and inputs, either differential or single-ended.

Table 2. Receiver Operational Modes

Mode	crlr1	crlr2	Channel 1 out (qm1)	Channel 2 out (qm2)
2 channels	vee	vee	High-Z	High-Z
2 channels	vee	N/C (Default)	High-Z	Out2=In2
2 channels	vee	vcc	High-Z	Out2=In2
2 channels	N/C (Default)	vee	Out1=In1	High-Z
2 channels	N/C (Default)	N/C (Default)	Out1=In1	Out2=In2
SW or splitter	N/C (Default)	vcc	Out1=In1	Out2=XOR(In1, In2), or Out2=(+/-)In1 if In2=”0”/”1”
2 channels	vcc	vee	Out1=In1	High-Z
SW or splitter	vcc	N/C (Default)	Out1=XOR(In1, In2), or Out1=(+/-)In2 if In1=”0”/”1”	Out2=In2
2 channels	vcc	vcc	Out1=In1	Out2=In2

Table 3. Transmitter Operational Modes

Mode	crlt1	crlt2	Channel 1 outs (q1p/q1n)	Channel 2 outs (q2p/q2n)
2 channels	vee	vee	Equal undefined levels	Equal undefined levels
2 channels	vee	N/C (Default)	Equal undefined levels	Out2=In2
2 channels	vee	vcc	Equal undefined levels	Out2=In2
2 channels	N/C (Default)	vee	Out1=In1	Equal undefined levels
2 channels	N/C (Default)	N/C (Default)	Out1=In1	Out2=In2
SW or splitter	N/C (Default)	vcc	Out1=In1	Out2=XOR(In1, In2), or Out2=(+/-)In1 if In2=”0”/”1”
2 channels	vcc	vee	Out1=In1	Equal undefined levels
SW or splitter	vcc	N/C (Default)	Out1=XOR(In1, In2), or Out1=(+/-)In2 if In1=”0”/”1”	Out2=In2
2 channels	vcc	vcc	Out1=In1	Out2=In2

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 4 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vee).

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Table 4. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vcc)		3.6	*V*
Power Consumption		130	*mW*
CMOS Input Voltage Swing		vcc-vee	*V*
LVDS Input Voltage Swing (Diff.)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

Name	Number	Type	DESCRIPTION
vcc	3,8,16,22,25	PS	Positive power supply
vee	2,6,10,17,29	PS	Negative power supply (analog ground)
veed	21	PS	Negative power supply (digital ground)
vecl	28	PS	ECL input termination voltage
nc	1,11,30,40	-	Floating package pins
rfbL	4	Control	Internal reference voltages. Used only in test operational modes. **For normal operation must be left not connected.**
rfb2_2	5	Control	
rfb2_1	24	Control	
rfb1_1	23	Control	
rfp	7	Control	
crlt2	12	Control	Transmitter channel 2 activation control signal
crlt1	15	Control	Transmitter channel 1 activation control signal
crlr1	20	Control	Receiver channel 1 activation control signal
oncml	26	Control	Activation of the input CML termination mode
onecl	27	Control	Activation of the input ECL termination mode
crlr2	35	Control	Receiver channel 2 activation control signal
vcm	9	DC voltage	CMOS input threshold voltage, default=(vcc+vee)/2
dm2	13	Input	Transmitter channel 2 SE CMOS input
dm1	14	Input	Transmitter channel 1 SE CMOS input
qm2	18	Output	Receiver channel 2 SE CMOS output
qm1	19	Output	Receiver channel 1 SE CMOS output
d1p	31	Input	Receiver channel 1 LVDS direct input
d1n	32	Input	Receiver channel 1 LVDS inverted input
d2p	33	Input	Receiver channel 2 LVDS direct input
d2n	34	Input	Receiver channel 2 LVDS inverted input
q1p	36	Output	Transmitter channel 1 LVDS direct output
q1n	37	Output	Transmitter channel 1 LVDS inverted output
q2p	38	Output	Transmitter channel 2 LVDS direct output
q2n	39	Output	Transmitter channel 2 LVDS inverted output

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vcc	3.14	3.3	3.47	*V*	±5%
vee		0.0		*V*	LVDS ground
veed		0.0		*V*	CMOS ground
vecl		vcc-2.0		*V*	ECL input termination
*I*vcc		35		*mA*	All channels enabled
Power consumption		7.0		*mW*	1 Receiver channel, DC
		20.0		*mW*	1 Transmitter channel
		115.0		*mW*	All channels enabled
Junction temperature	-25	50	125	*°C*	
LVDS Inputs (d1p/d1n, d2p/d2n)					
Data Rate	0.0		2.0	*Gbps*	
DC common mode voltage	vee		vcc	*V*	DC voltage
AC common mode voltage	vee		2.4	*V*	AC signal <5*MHz*
Sensitivity		60		*mV*	
CMOS Inputs (dm1, dm2)					
Data Rate	0.0		1.0	*Gbps*	
Logic “1” level	vcc -0.4			*V*	
Logic “0” level			0.4	*V*	
LVDS Outputs (q1p/q1n, q2p/q2n)					
Voltage Swing		320		*mV*	Each SE output
CM voltage	1.2		1.25	*V*	
Impedance	77		122	*Ohm*	DC test
	45		115	*Ohm*	AC test (0-2*Gbps*)
Total current	5.2		5.7	*mA*	From vcc
Output current	17		27	*mA*	Shorted to vee
	4.5		7.0	*mA*	Shorted together
Rise/Fall Times		TBD		*pS*	20%-80%
CMOS Outputs (qm1, qm2)					
Logic “1” level	vcc -0.2			*V*	
Logic “0” level			0.2	*V*	
Rise/Fall Times		TBD			20%-to-80%
Duty Cycle	45%	50%	55%		
CMOS Control Inputs (crlr1, crlr2, crlt1, crlt2)					
Logic “1” level	vcc -0.4			*V*	
Logic “0” level			0.4	*V*	

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PACKAGE INFORMATION

The chip die is housed in a standard 40-pin QFN package shown in Fig. 2. It is recommended that the center heat slug located on the back side of the package is soldered to the vee plain that is ground for the positive supply.

The part's identification label is ASNT3010-PQB. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

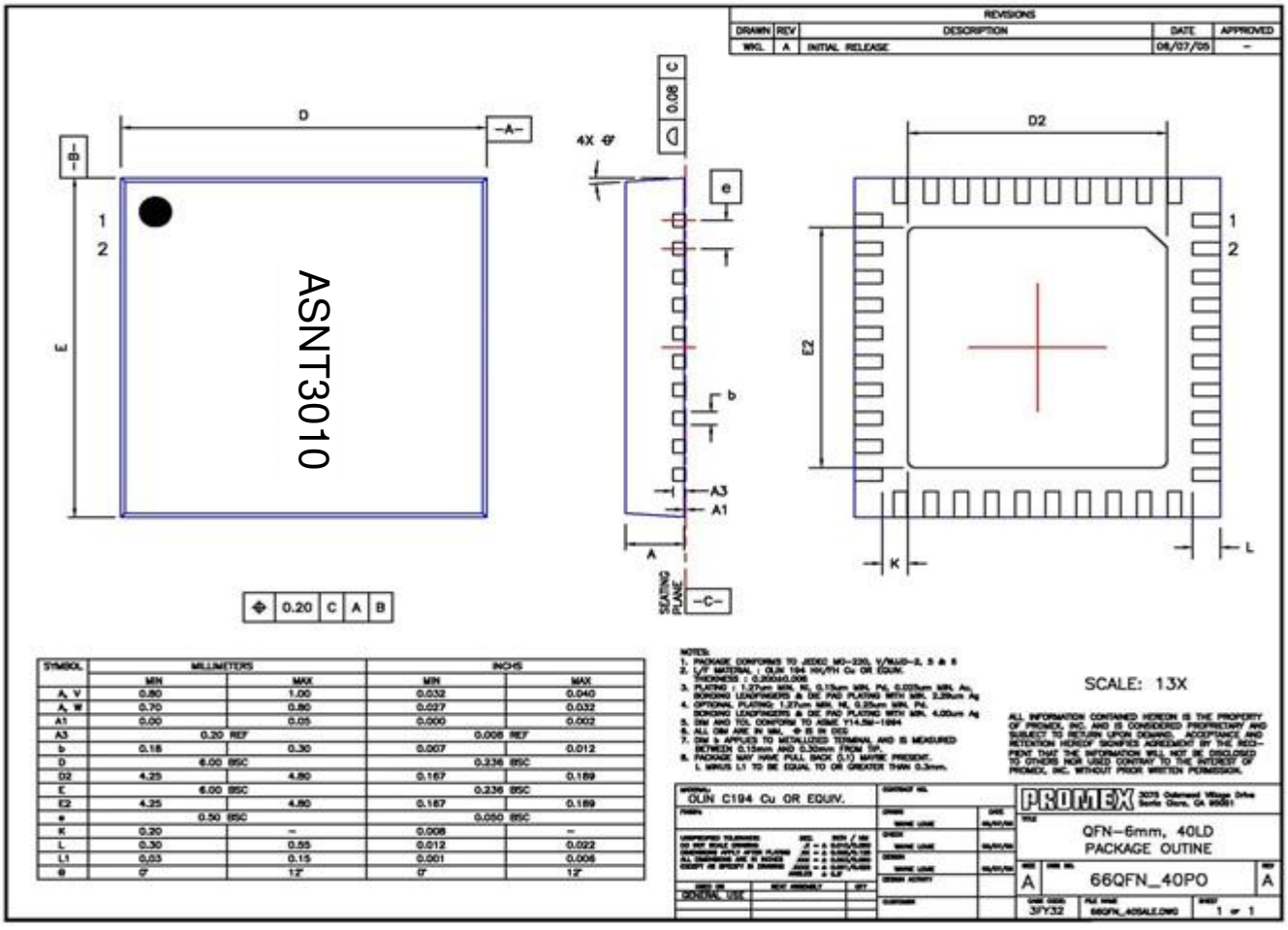


Fig. 2. QFN 40-Pin Package Drawing (All Dimensions in mm)

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REVISION HISTORY

Revision	Date	Changes
6.1.2	02-2020	Updated Package Information
6.0.2	07-2019	Updated Letterhead
6.0.1	03-2013	Revised title Revised description Added pin out diagram Corrected block diagram Revised Operational Modes tables Added absolute maximum ratings Revised electrical characteristics Revised package information Added package mechanical drawing Added revision history Updated format
5.0	09-2009	Revised electrical characteristics
4.0	02-2008	Revised electrical characteristics section Revised packaging information section
3.0	06-2007	Revised electrical characteristics section
2.0	04-2007	Revised terminal functions section
1.0	01-2007	First release