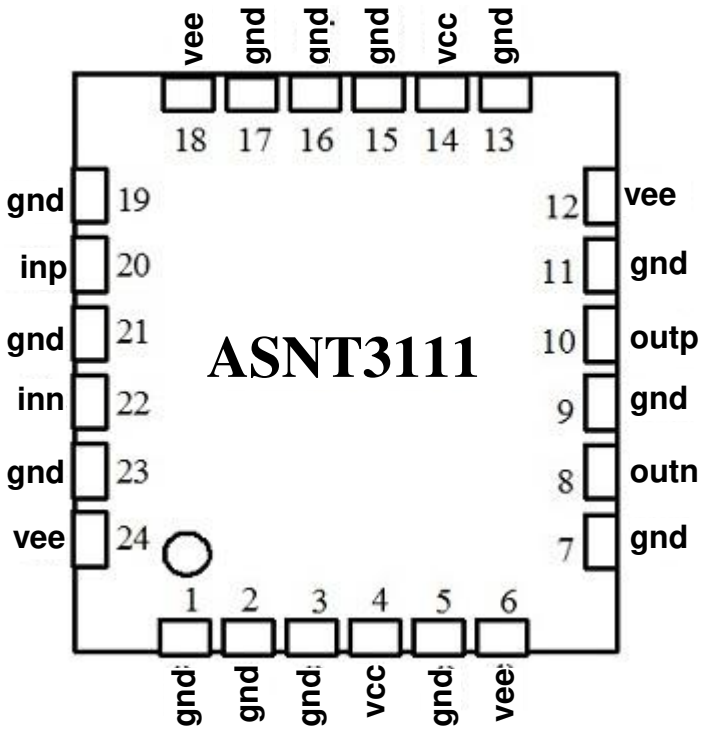
ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Drive Suite 112, Torrance, CA 90505

Offices: 310-530-9400 / Fax: 310-530-9402
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ASNT3111-PQC
DC-20*Gbps* Single-Channel CML-to-PCML Level Shifter

- High-speed broadband digital signal level up-shifter
- Fully differential input CML interface with on-chip single-ended 50*Ohm* termination to ground
- Fully differential output PCML interface with on-chip single-ended 50*Ohm* termination to the positive supply rail
- Exhibits low jitter and limited temperature variation over industrial temperature range
- Fabricated in SiGe for high performance, yield, and reliability
- Power consumption: 260*mW*
- Standard 24-pin QFN package



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DESCRIPTION

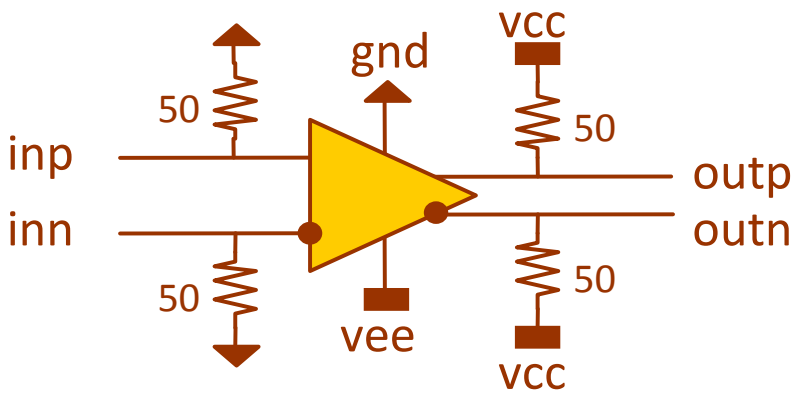


Fig. 1. Functional Block Diagram

The ASNT3111-PQC SiGe IC shown in Fig. 1 provides a voltage shift for high-speed data and clock CML signals from the levels associated with negative power supplies to the levels associated with positive power supplies.

The part's inputs support the CML logic interface with on chip 50*Ohm* termination to gnd and may be used differentially, AC/DC coupled, single-ended, or in any combination. In the first mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the second mode, the input termination provides the required common mode voltage automatically. The part's outputs support the PCML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination. The differential DC signaling is recommended for optimal performance.

Fig. 2 and Fig. 3 below demonstrate the chip's simulated performance.

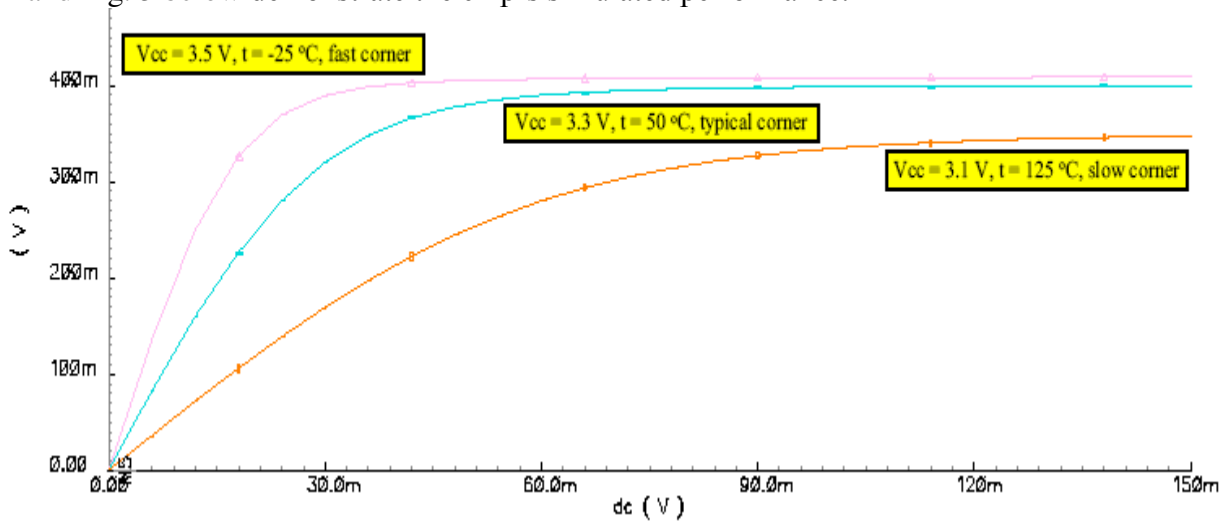


Fig. 2. Simulated DC Transfer Function

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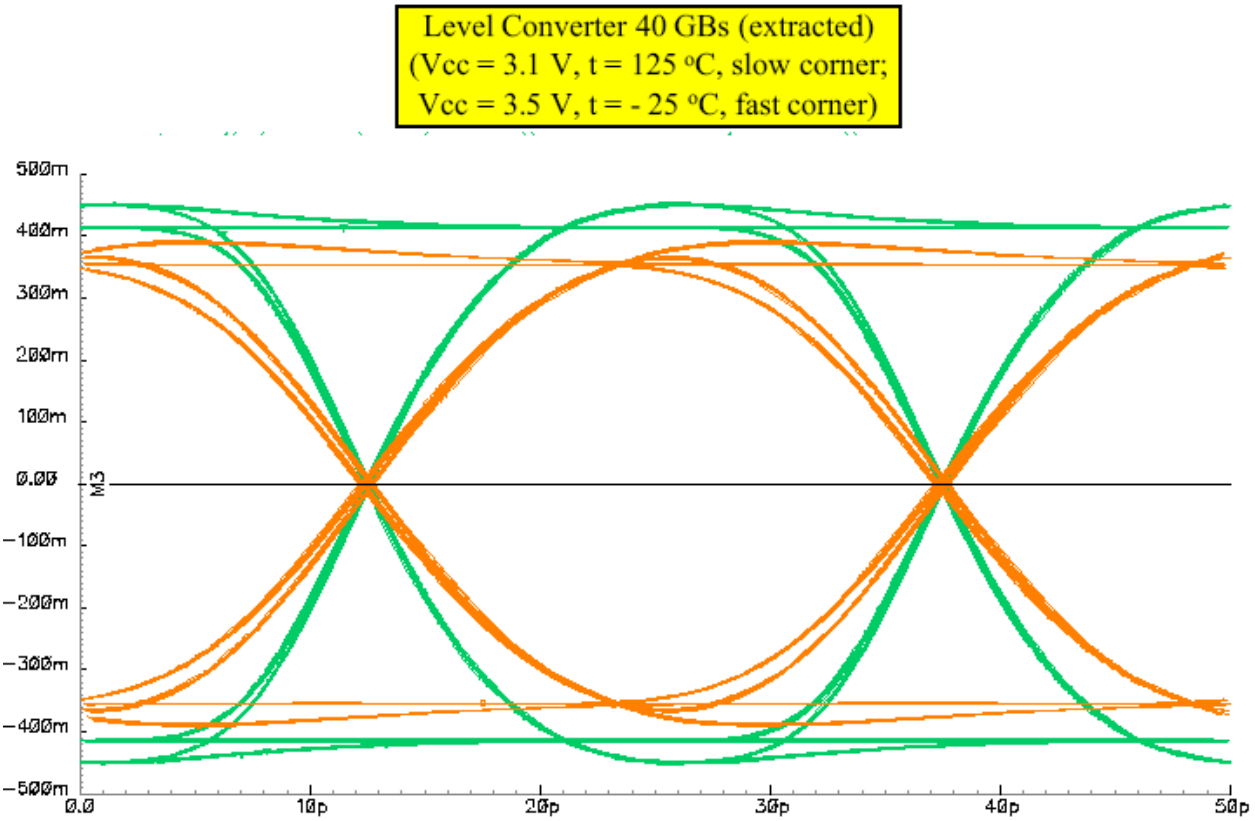


Fig. 3. 40Gbps Simulated Output Eye Diagrams at Different Conditions

POWER SUPPLY CONFIGURATION

The chip operates from two independent power supplies related to gnd: negative vee=-3.3*V* and positive vcc=+3.3*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Negative Supply Voltage (vee)		-3.6	*V*
Positive Supply Voltage (vcc)		+3.6	*V*
Power Consumption		0.29	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Storage Temperature	-40	+100	*°C*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

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TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
inp	20	CML input	Differential inputs with internal SE 50*Ohm* termination to gnd
inn	22		
outp	10	PCML output	Differential outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc
outn	8		

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply (+3.3*V*)	4, 14
gnd	External ground (0*V*)	1, 2, 3, 5, 7, 9, 11, 13, 15, 16, 17, 19, 21, 23
vee	Negative power supply (-3.3*V*)	6, 12, 18, 24

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
gnd		0.0		*V*	External ground
vcc	3.1	3.3	3.5	*V*	±6%
*I*gnd		42		*mA*	
*I*vcc		18		*mA*	
Power consumption		260		*mW*	
Junction temperature	-25	50	125	*°C*	
HS Input Data (inp/inn)					
Data rate	DC		20	*Gbps*	
Swing	0.05		1.0	*V*	Differential or SE, p-p
CM Voltage Level	gnd-0.8		gnd	*V*	Must match for both inputs
HS Output Data (outp/outn)					
Data rate	DC		20	*Gbps*	
Logic “1” level		vcc		*V*	
Logic “0” level		vcc-0.4		*V*	With external 50*Ohm* DC termination
Rise/Fall times		14		*ps*	20%-80%
Additive Jitter			<1	*ps*	Peak-to-peak

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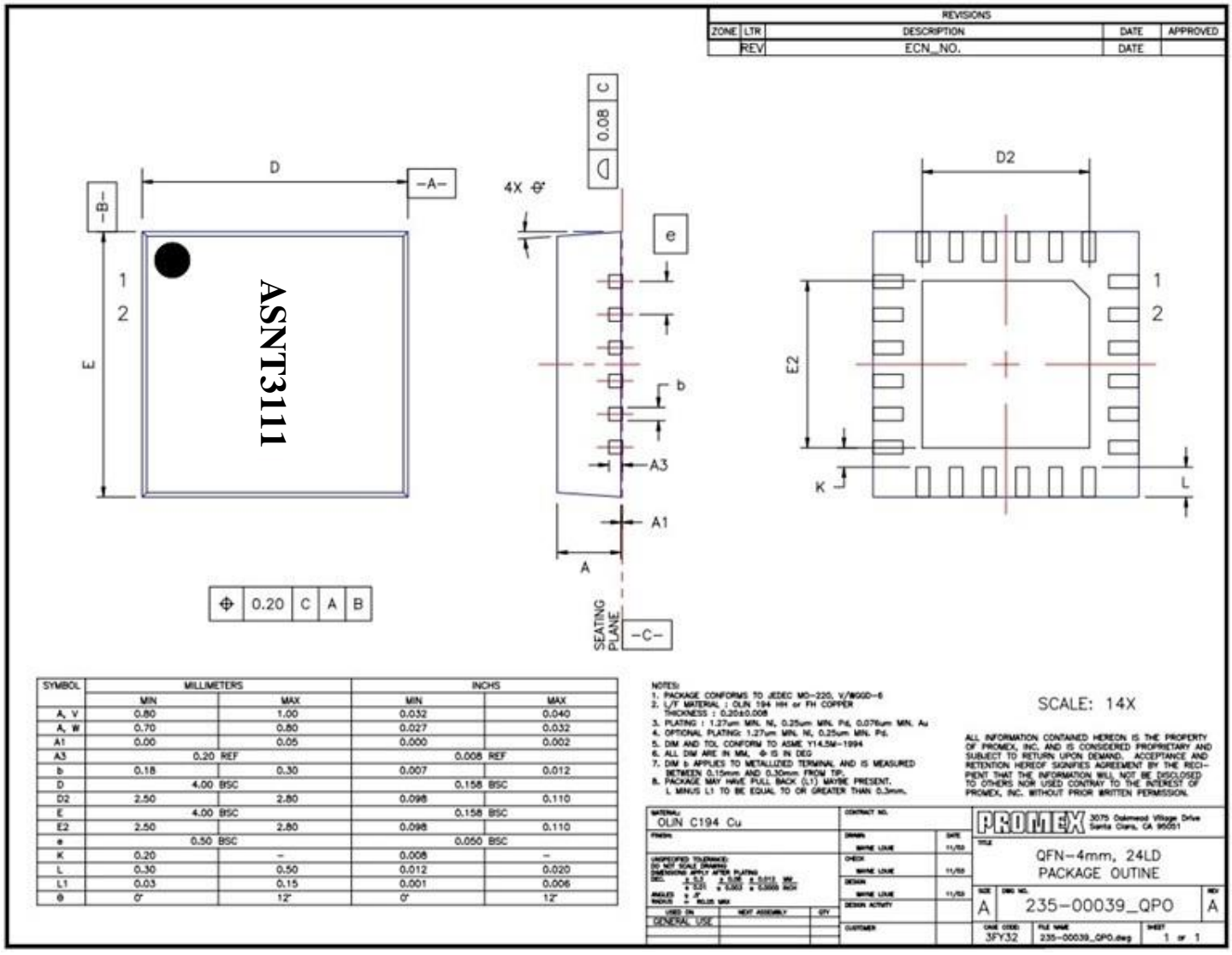
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PACKAGE INFORMATION

The chip die is housed in a standard 24-pin QFN package shown in Fig. 4. It is recommended that the center heat slug located on the back side of the package is soldered to the vee plain, which is ground for the positive supply or power for the negative supply. It will help dissipate heat generated by the chip during operation.

The part's identification label is ASNT3111-PQC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.



SYMBOL	MILLIMETERS		INCHS	
	MIN	MAX	MIN	MAX
A, V	0.80	1.00	0.032	0.040
A, W	0.70	0.80	0.027	0.032
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	4.00 BSC		0.158 BSC	
D2	2.50	2.80	0.098	0.110
E	4.00 BSC		0.158 BSC	
E2	2.50	2.80	0.098	0.110
e	0.50 BSC		0.050 BSC	
K	0.20	–	0.008	–
L	0.30	0.50	0.012	0.020
L1	0.03	0.15	0.001	0.006
θ	0°	12°	0°	12°

Fig. 4. QFN 24-Pin Package Drawing (All Dimensions in mm)

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REVISION HISTORY

Revision	Date	Changes
2.2.2	02-2020	Updated Package Information
2.1.2	07-2019	Updated Letterhead
2.1.1	11-2016	Corrected input CM Voltage Level
2.0.1	03-2013	Corrected title Updated description Added pin out diagram Added power supply configuration section Added absolute maximum ratings section Revised electrical characteristics Revised package information section Added package mechanical drawing
1.1.1	01-2013	Revised electrical characteristics section Revised package information section
1.0	11-2011	First release