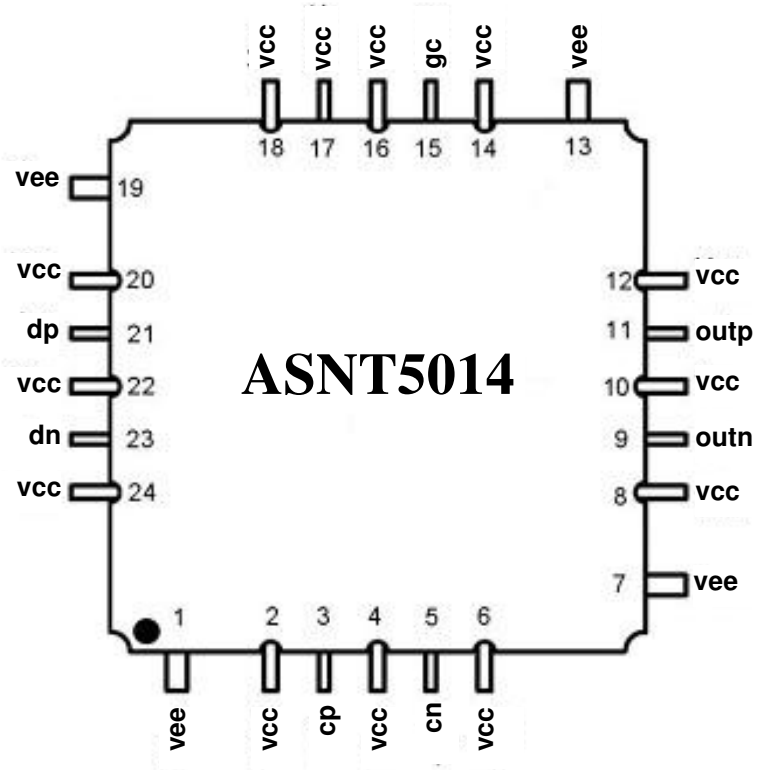
ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Drive Suite 112, Torrance, CA 90505

Offices: 310-530-9400 / Fax: 310-530-9402
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ASNT5014-KMC
DC-25*Gbps* D-Type Flip-Flop

- High speed broadband D-Type Flip-Flip for data retiming with full rate clock and single-ended output amplitude control
- Exhibits low jitter and limited temperature variation over industrial temperature range
- 6.5*ps* set-up/hold time capability
- 87% clock phase margin for retiming of data input eye
- Fully differential CML input interfaces
- Fully differential CML output interface with amplitude control
- Single +3.3*V* or -3.3*V* power supply
- Power consumption: 725*mW*
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 24-pin package



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DESCRIPTION

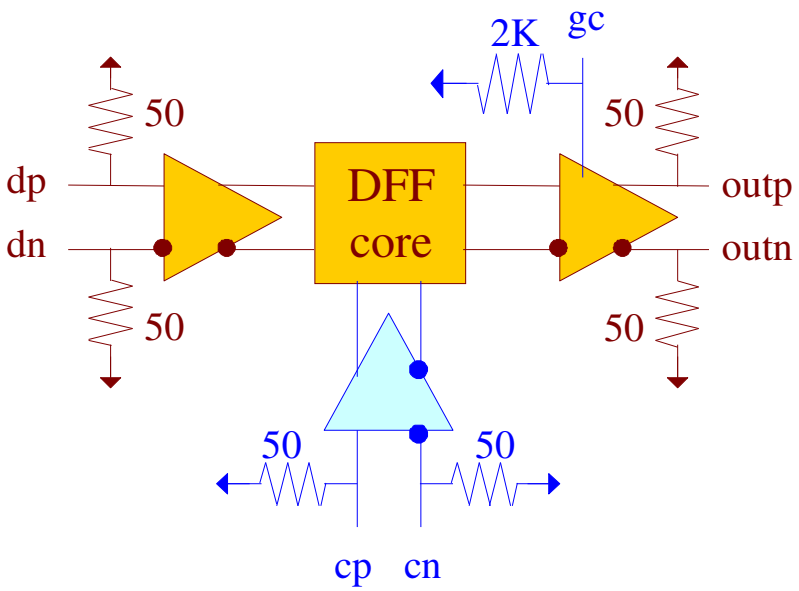


Fig. 1. Functional Block Diagram

The temperature stable ASNT5014-KMC SiGe IC provides broadband data retiming functionality and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can sample a high-speed data signal dp/dn with a full-rate external clock cp/cn to create a full-rate retimed NRZ data output outp/outn with its output signal amplitude controlled by gc.

The part's I/O's support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = 0.0*V* = ground and vee = −3.3*V*), or positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

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All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power Consumption		0.80	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*°C*
Storage Temperature	-40	+100	*°C*
Operational Humidity	10	98	%
Storage Humidity	10	98	%

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
dp	21	CML input	Differential data inputs with internal SE 50*Ohm* termination to vcc.
dn	23		
cp	3	CML input	Differential clock inputs with internal SE 50*Ohm* termination to vcc.
cp	5		
outp	11	CML output	Differential data outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc.
outn	9		
gc	15	CML input	Single-ended output amplitude control signal with internal 2K*Ohm* termination to vcc.

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply. (+3.3*V* or 0)	2, 4, 6, 8, 10, 12, 14, 16, 17, 18, 20, 22, 24
vee	Negative power supply. (0*V* or -3.3*V*)	1, 7, 13, 19

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee		220		*mA*	
Power consumption		725		*mW*	
Junction temperature	-40	25	125	*°C*	
HS Input Data (dp/dn)					
Frequency	DC		25	*Gbps*	
Swing	0.05		0.8	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
HS Input Clock (cp/cn)					
Frequency	DC		25	*GHz*	
Swing	0.05		0.8	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
Clock Phase Margin	85	87	89	*%*	
HS Output Data (outp/outn)					
Frequency	DC		25	*Gbps*	
Logic "1" level		vcc		*V*	
Logic "0" level	vcc-1.0		vcc	*V*	With external 50*Ohm* DC termination. Controlled by gc signal
Rise/Fall times			18	*ps*	20%-80%
Output Jitter			5	*ps*	Peak-to-peak
Gain Control (gc)					
Control voltage	vcc-1.0		vcc	*V*	Single-ended

PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFP package shown in Fig. 2. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT5014-KMC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

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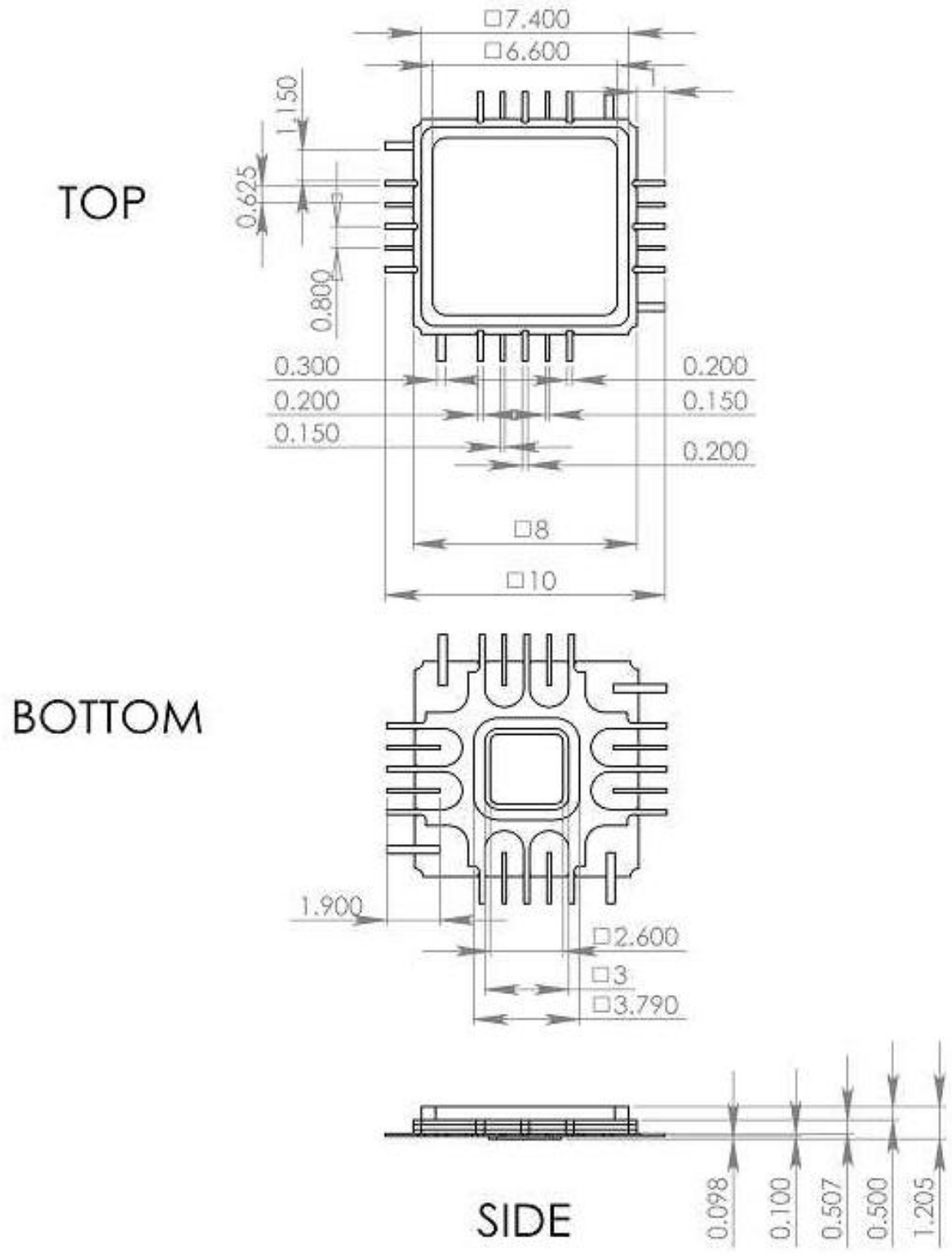


Fig. 2. CQFP 24-Pin Package Drawing (All Dimensions in mm)

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REVISION HISTORY

Revision	Date	Changes
3.1.2	05-2020	Updated Package Information
3.0.2	07-2019	Updated Letterhead
3.0.1	02-2013	Revised title Added package pin out drawing Revised functional block diagram Revised description Added power supply configuration Added absolute maximum ratings Revised terminal functions Revised electrical characteristics Added package information and mechanical drawing Format correction
2.0	03-2009	Revised electrical characteristics
1.0	02-2008	First release