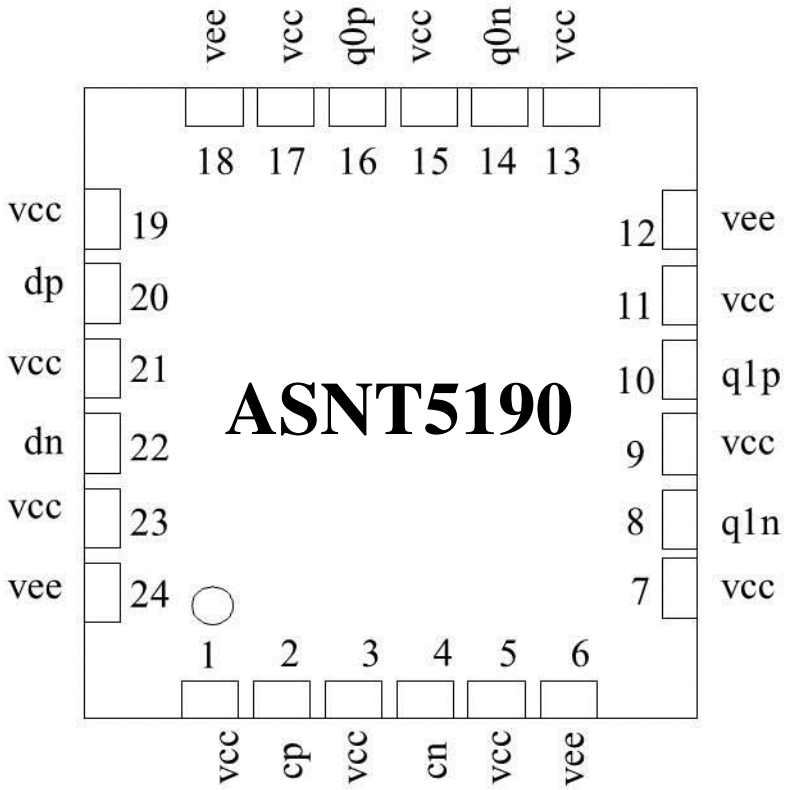
ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Drive Suite 112, Torrance, CA 90505

Offices: 310-530-9400 / Fax: 310-530-9402
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ASNT5190-PQC
DC-36*Gbps* Broadband Digital 1:2 Demultiplexer

- High speed broadband 1:2 Demultiplexer
- Exhibits low jitter and limited temperature variation over industrial temperature range
- Ideal for high speed proof-of-concept prototyping
- Fully differential CML input interfaces
- Fully differential CML output interface with 400*mV* single-ended swing
- Single +3.3*V* or -3.3*V* power supply
- Power consumption: 495*mW*
- Fabricated in SiGe for high performance, yield, and reliability
- Standard MLF/QFN 24-pin package



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DESCRIPTION

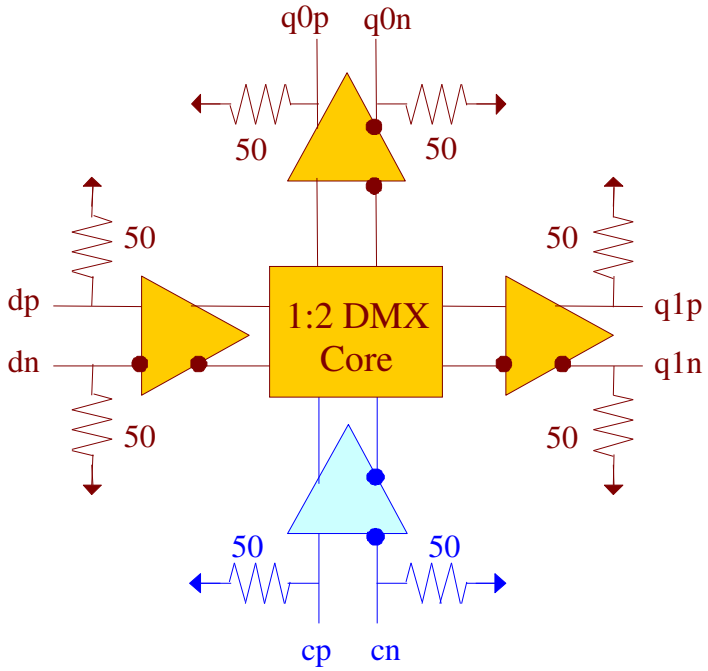


Fig. 1. Functional Block Diagram

The temperature stable ASNT5190-PQC SiGe IC can be utilized as a high speed 1:2 demultiplexer, and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can receive a high speed differential data input signal dp/dn and effectively demultiplex it into two high speed differential data output signals q0p/q0n and q1p/q1n by using a high speed differential clock input signal cp/cn.

The part's I/O's support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = 0.0*V* = ground and vee = −3.3*V*), or positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

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All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power Consumption		0.65	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	%
Storage Humidity	10	98	%

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
dp	20	CML input	Differential data input signals with internal 50*Ohm* termination to vcc
dn	22		
q0p	16	CML output	Differential data output signals with internal 50*Ohm* termination to vcc
q0n	14		
q1p	10	CML output	Differential data output signals with internal 50*Ohm* termination to vcc
q1n	8		
cp	2	CML input	Differential clock input signals with internal 50*Ohm* termination to vcc
cn	4		
Supply and Termination Voltages			
Name	**Description**		**Pin Number**
vcc	Positive power supply (+3.3*V* or 0)		1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23
vee	Negative power supply (0*V* or -3.3*V*)		6, 12, 18, 24

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee	120	150	180	*mA*	
Power consumption	370	495	630	*mW*	
Junction temperature	-40	25	125	*°C*	
HS Input Data (dp/dn)					
Data rate	DC		36	*Gbps*	
Swing	0.05		1.0	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
HS Input Clock (cp/cn)					
Frequency	DC		18	*GHz*	
Swing	0.05		1.0	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
Duty cycle	45	50	55	*%*	
HS Output Data (q0p/q0n, q1p/q1n)					
Data rate	DC		18	*Gbps*	
Logic “1” level		vcc		*V*	
Logic “0” level		vcc-0.4		*V*	With external 50*Ohm* DC termination
Rise/Fall times	14	18	22	*ps*	20%-80%
Output Jitter			1	*ps*	Peak-to-peak

PACKAGE INFORMATION

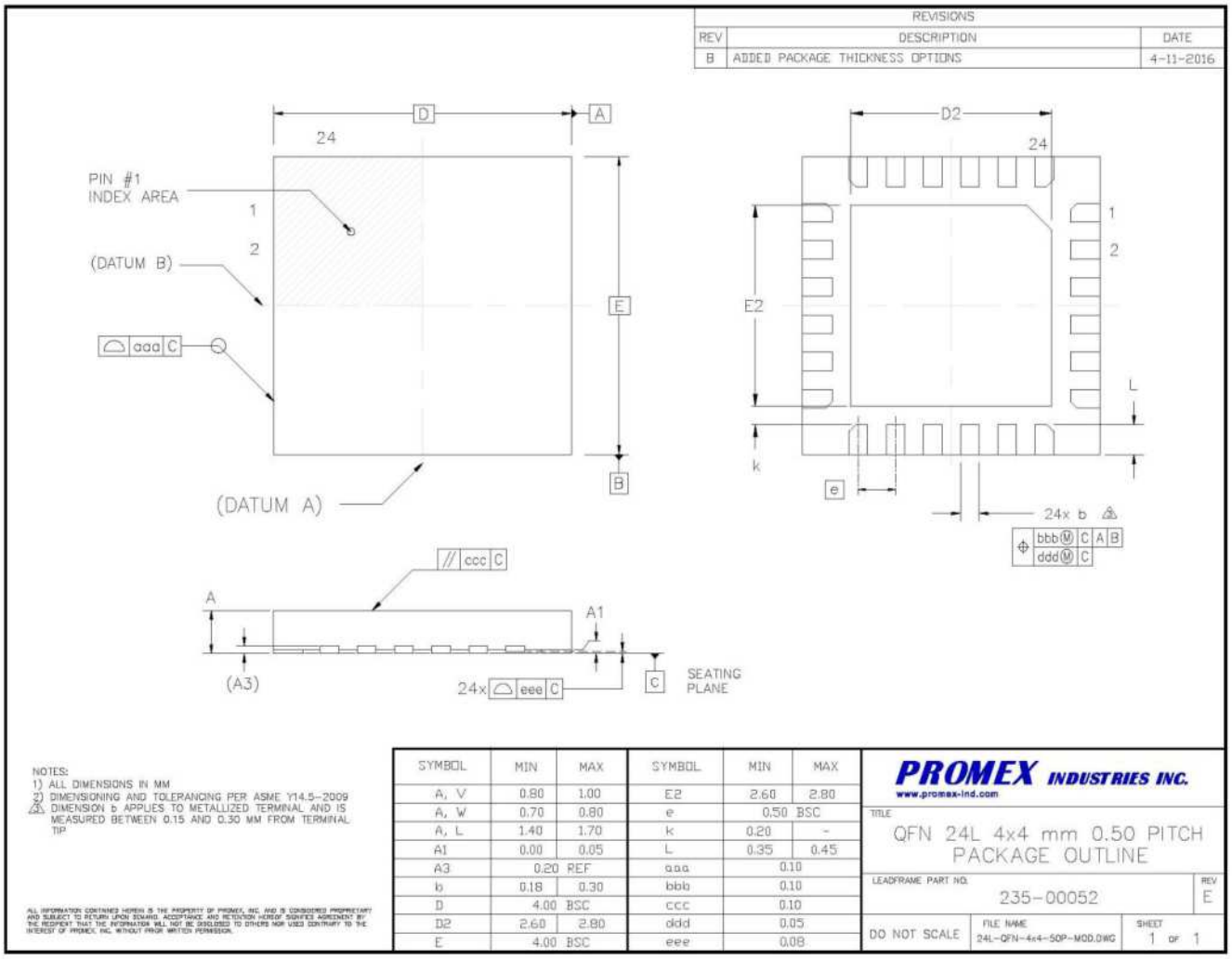
The chip die is housed in a standard 24-pin QFN package shown in Fig. 2. It is recommended that the center heat slug located on the back side of the package is soldered to the vee plain that is ground for the positive supply or power for the negative supply.

The part’s identification label is ASNT5190-PQC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package’s manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

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SYMBOL	MIN	MAX	SYMBOL	MIN	MAX
A, V	0.80	1.00	E2	2.60	2.80
A, W	0.70	0.80	e	0.50 BSC	
A, L	1.40	1.70	k	0.20	-
A1	0.00	0.05	L	0.35	0.45
A3	0.20 REF		aaa	0.10	
b	0.18	0.30	bbb	0.10	
D	4.00 BSC		ccc	0.10	
D2	2.60	2.80	ddd	0.05	
E	4.00 BSC		eee	0.08	

Fig. 2. QFN 24-Pin Package Drawing (All Dimensions in mm)

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REVISION HISTORY

Revision	Date	Changes
1.1.2	01-2020	Updated Package Information
1.0.2	07-2019	Updated Letterhead
1.0.1	11-2017	First release