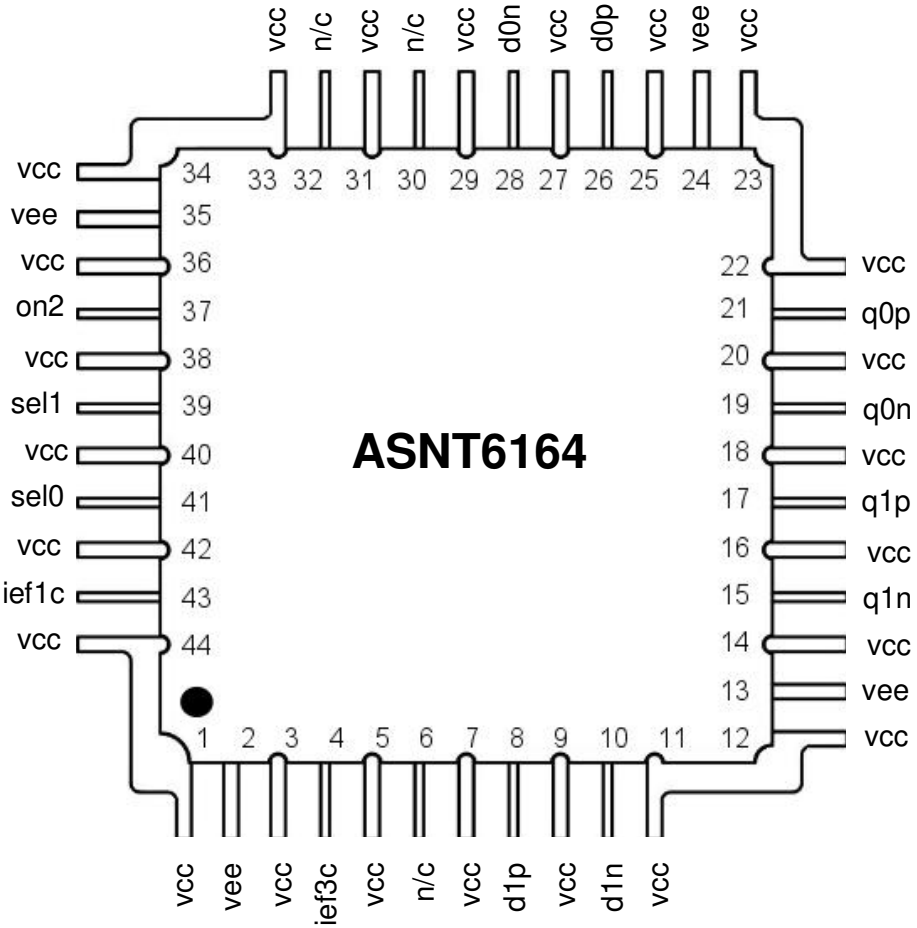
ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Dr., Ste #112, Torrance, CA 90505

Office: (310) 530-9400 Fax: (310) 530-9402
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ASNT6164-KMM
DC-32*GHz* Linear Non-Blocking Cross-Switch 2x2

- DC to 32*GHz* broadband operation
- Two differential CML-type input ports and two differential CML-type output ports
- Temperature-stabilized differential gain of approximately 0*dB*
- 1*dB* compression point of 0*dBm*
- DC-to-1*GHz* broadband channel selector ports
- Optional two-channel mixer/adder setting available
- Low jitter and limited temperature variation over industrial temperature range
- Single +3.6*V* or -3.6*V* power supply
- Power consumption: 1400*mW*
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 44-pin package



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DESCRIPTION

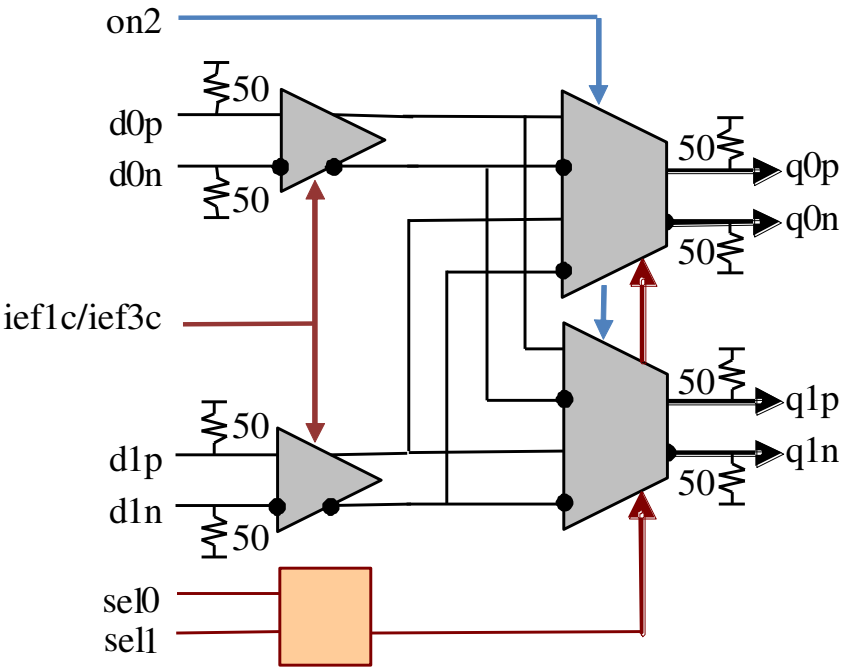


Fig. 1. Functional Block Diagram

The temperature stable ASNT6164-KMM linear non-blocking cross-switch 2x2 is intended for use in high-speed systems. The IC shown in Fig. 1 can deliver two different broad-band analog differential signals d0p/d0n and d1p/d1n to two differential outputs q0p/q0n and q1p/q1n with a nominal gain of 0*dB*. It can also be used as a two-channel analog mixer/adder of signals d0p/d0n and d1p/d1n. Two low-speed analog current controls Ief1c and Ief3c are available for bandwidth and peaking adjustments. Both controls are very similar and change peaking of the part's frequency response at high frequencies (above 20*GHz*). Ief1c has a higher impact on the frequency response and also improves linearity at low control voltages. A relatively flat frequency response can be achieved at lower control voltages but it may be not the best setting for the signal eye.

The assignment of inputs to outputs is performed through the external high-speed ports sel1 and sel2 that can be referenced to either vcc or vee. The assignment logic is shown in Table 1. When the low-speed single-ended control port on2 is set to vcc, it switches the circuit into mixer/adder mode with both inputs active at the same time.

Table 1. Channel Selection

on2	sel1	sel0	Input connected to q0	Input connected to q1	Comments
0	0	0	d0	d0	
0	0	1	d1	d0	
0	1	0	d0	d1	
0	1	1	d1	d1	default state
1	*	*	d0+d1	d0+d1	

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The part's I/O's support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination. In DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in the ELECTRICAL CHARACTERISTICS. In AC-coupling mode, the input termination provides the required common mode voltage automatically.

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = 0.0*V* = ground and vee = −3.6*V*), or positive supply (vcc = +3.6*V* and vee = 0.0*V* = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground.

Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0*V* = ground.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 2 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-4	*V*
Power supply current		320	*mA*
Input Voltage	vcc-1.2	vcc-0.6	*V*
RF Input Voltage Swing (SE)		0.6	*V*
Analog control voltages	vee	vcc	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	%
Storage Humidity	10	98	%

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TERMINAL FUNCTION

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-speed Signals			
d0p	26	CML - type	Differential high speed data inputs with internal SE 67*Ohm* termination to vcc and SE 50*Ohm* termination to virtual ground
d0n	28		
d1p	8	CML - type	
d1n	10		
q0p	21	CML - type	Differential high speed data outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc
q0n	19		
q1p	17	CML - type	
q1n	15		
Control Signals			
sel0	41	SE	High-speed input with selectable logic levels, (active: high; default: low). For the selection logic see Table 1
sel1	39	SE	
ief1c	43	Analog Control	Analog current control with internal 64*KOhm* termination to vcc and 72*KOhm* termination to vee.
ief3c	4		
on2	37	CMOS	Low-speed high-impedance input (active: high, mixer/adder mode; default: low, 1-of-2 selector mode;)

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply rail	1, 3, 5, 7, 9, 11, 12, 14, 16, 18, 20, 22, 23, 25, 27, 29, 31, 33, 34, 36, 38, 40, 42, 44
vee	Negative power supply rail	2, 13, 24, 35
n/c	Not connected pins	6, 30, 32

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.4	-3.6	-3.8	*V*	±5.5%
vcc		0.0		*V*	External ground
*I*vee		400		*mA*	In Selector Mode
		600		*mA*	In Mixer/Adder Mode
Power consumption		1400		*mW*	In Selector Mode
		2100		*mW*	In Mixer/Adder Mode
Junction temperature	-25	50	125	*°C*	
Input Analog (d0p/d0n, d1p/d1n)					
Bandwidth	DC		32	*GHz*	-3*dB*
Common mode level		vcc		*mV*	
Voltage swing, pk-pk	0		400	*mV*	Single-ended, with unused input not connected or AC terminated
	0		800	*mV*	Differential
S11		-35		*dB*	at 3*GHz*
		-16		*dB*	at 10*GHz*
		-11		*dB*	at 20*GHz*
		-9		*dB*	at 25*GHz*
Current Control Signals (ief1c/ief3c)					
Control range	vee+0.95		vee+1.95	*V*	
Default voltage level		vee+1.9		*V*	at ±3.6*V* supply
Output Analog (q0p/q0n, q1p/q1n)					
Bandwidth	DC		32	*GHz*	-3*dB*
Common mode level		vcc-0.55		*V*	With external 50*Ohm* DC termination to vcc
Small Signal Differential Gain	-1.5	0.0	+1.5	*dB*	up to 25*GHz*
Output referred 1*dB* Compression Point		1		*dBm*	Single-Ended, 20*GHz*
THD		0.6		%	at 1*GHz*
		0.7		%	at 10*GHz*
		2		%	at 25*GHz*
		3.5		%	at 35*GHz*
Low-Speed Control (on2)					
High logic level		vcc		*V*	Mixer/Adder Mode
Low logic level		vee		*V*	1-of-2 Selector Mode
High-Speed Control (sel0, sel1)					
Bandwidth		1		*GHz*	
High logic level		vcc		*V*	See Table 1
Low logic level		vee		*V*	See Table 1
Input current			20	*uA*	sink or source

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PACKAGE INFORMATION

The chip die is housed in a custom 44-pin CQFP package shown in Fig. 2. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

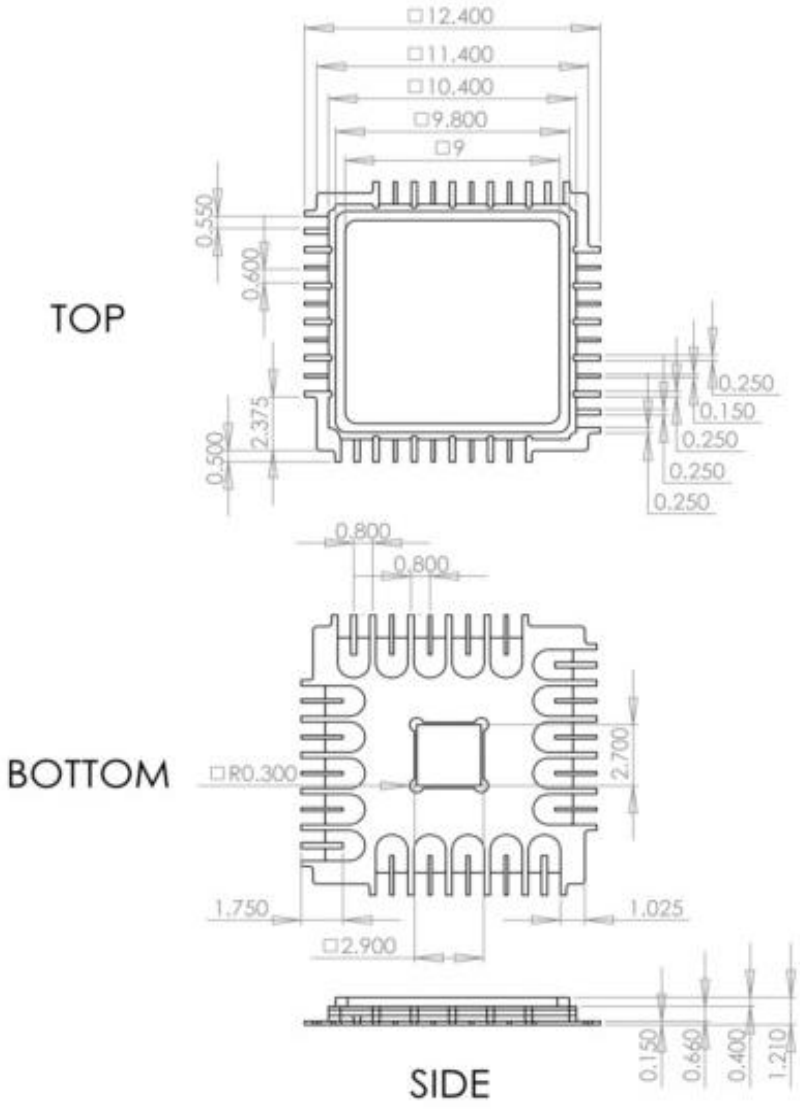


Fig. 2. CQFP 44-Pin Package Drawing (All Dimensions in mm)

The part's identification label is ASNT6164-KMM. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 digits after the underscore represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

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REVISION HISTORY

Revision	Date	Changes
1.2.2	01-2020	Updated Package Information
1.1.2	11-2019	Corrected range of analog controls Added description of analog controls Added maximum values of analog control voltages
1.0.2	10-2019	Corrected default states in Table 1
0.2.2	08-2019	Corrected Terminal Functions table
0.1.2	08-2019	Corrected bandwidth Corrected pinout drawing
0.0.2	08-2019	Updated letterhead
0.0.1	01-2019	Preliminary release