ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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ADSANTEC 32.5*Gb/s* Pre-Emphasis
Advanced Driver/Amplifier with USB Control Interface

- Four pre-emphasis taps with software controlled weight and inversion
- Adjustable data output amplitude and eye quality
- Output data eye cross point adjustment
- Optional main clock frequency ×2 multiplier
- Main clock duty cycle indicators located before and after the multiplier
- Opposite and parallel adjustment of the main clock and data delays
- Alternate clock input
- Differential CML input/output data, and clock interfaces
- Selectable main or additional clock at the output with adjustable amplitude
- Duty cycle adjustment on clock input
- GUI software interfaces with onboard USB
- DLL is provided for control with example python code



Fig. 1. PreEmphasis Front Panel

Description

The ADSANTEC Pre-Emphasis unit can be used for test applications, design verification, and R&D environments. The device incorporates the advanced programmable driver amplifier shown in Fig. 1 with built-in four-tap pre-emphasis, external control circuitry in an integrated instrument box with power supplies, and USB computer interface. All connectors are female SMA except the Data Output pair, which is 2.92 mm (type K). All device I/O's are CML.

The ADA contains both digital and analog controls to set signed tap weights for the four delayed copies of the input signal (set apart one clock from each other by a shift register), which are then summed to produce the output signal. Other features include a limiting amplifier for the input clock, input clock doubler, duty cycle, peaking and amplitude controls.

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The back panel of the instrument is shown in Fig 2. The power ON/OFF switch turns the instrument on and off, and it combines with an LED to indicate the instrument is powered ON. The +5V DC power supply (included) connects to the male barrel jack. The USB-B connector (with connectivity indicator) allows connection to a computer for controlling the instrument through a Windows GUI. Alternatively the unit can be controlled through a DLL. An example python code is provided as one way to use the DLL to control the unit. Matlab, Java, and many more programs can use the DLL. See the user guide for more details.



Fig. 2. Rear Panel

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Data Input

Data In can be used single-ended or differentially.

Data Output

Data Out has a data rate up to 32.5*Gbps* with controllable eye crossing level, peaking, duty cycle, and amplitude control from 0*V* to 2.5*V* differentially.

Clock I/O's

Clock In is normally a half-rate clock input. A full-rate clock can be used for data rates below 17*Gbps* by not using the internal clock doubler. Can be used single-ended or differentially.

Clock Out has adjustable amplitude, and peaking controls. Clock Out is meant as a debugging output and is not a usable clock.

Terminal Functions

TERMINAL		DESCRIPTION
Name	**Type**	
High-Speed I/O's		
Clock In	CML input	Female SMA connector; differential clock input; AC coupled with internal 50*Ohm* termination; requires a 50*Ohm* source impedance
Clock Out	CML output	Female SMA connector; single-ended clock output; DC coupled with internal 50*Ohm* termination; requires external 50*Ohm* termination
Data Out +	CML output	Female 2.92*mm* connector; single-ended direct data output; DC coupled with internal 50*Ohm* termination. Requires external 50*Ohm* termination.
Data Out -	CML output	Female 2.92*mm* connector; single-ended inverted data output; DC coupled with internal 50*Ohm* termination; requires external 50*Ohm* termination.
Data In +	CML input	Female SMA connector; single-ended direct data input DC coupled with internal 50*Ohm* termination. Requires external 50*Ohm* termination.
Data In -	CML input	Female SMA connector; single-ended direct data input; DC coupled with internal 50*Ohm* termination; requires external 50*Ohm* termination.

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Mechanical Dimensions

PARAMETER	TYP	UNIT	COMMENTS
Length	125	*mm*	
Width	108	*mm*	
Height	59	*mm*	

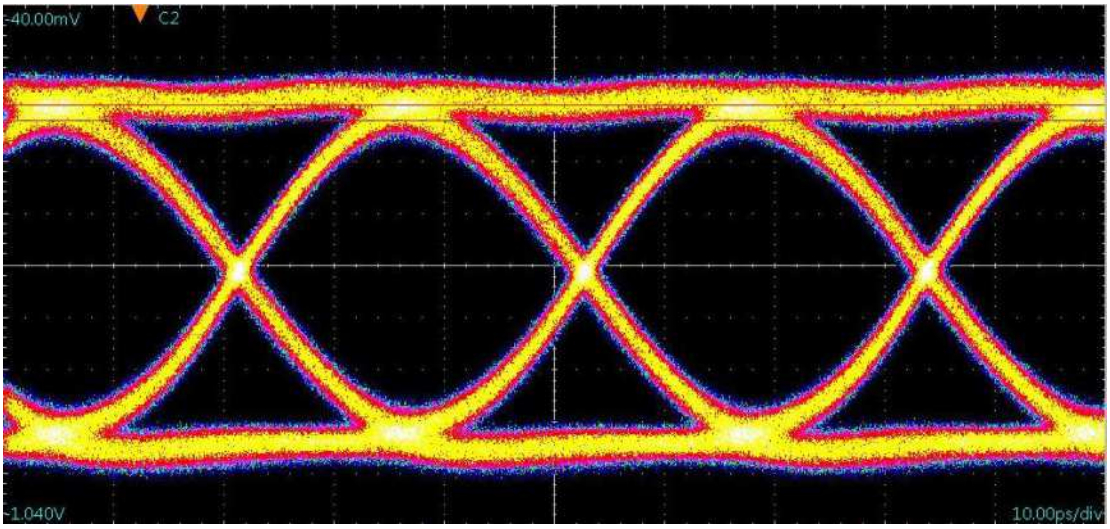


Fig. 3. 1-Tap Output Eye Diagram at 32Gb/s Data Rate

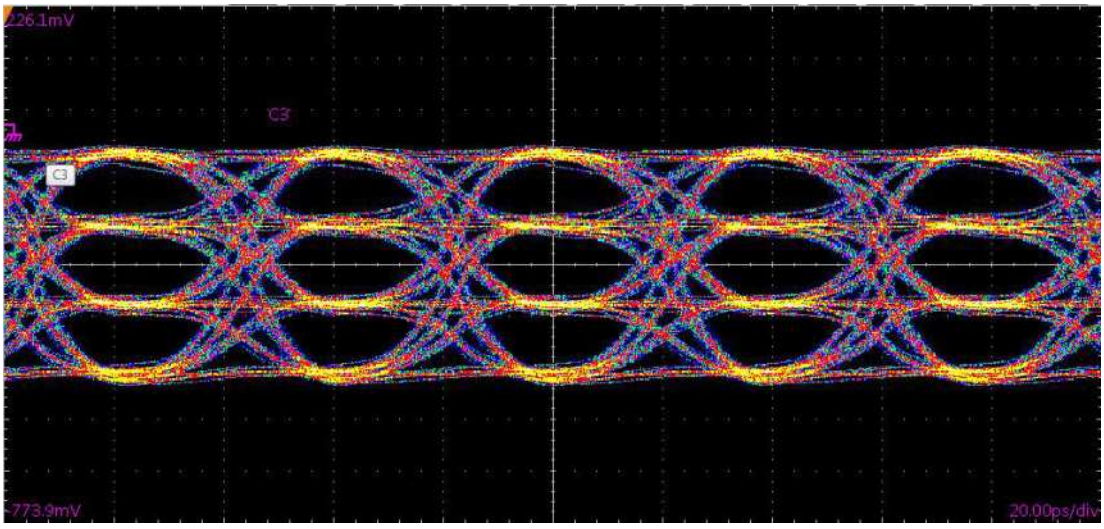


Fig. 4. PAM4 Output Eye Diagram at 25.8Gb/s (51.6Gbaud/s) Data Rate

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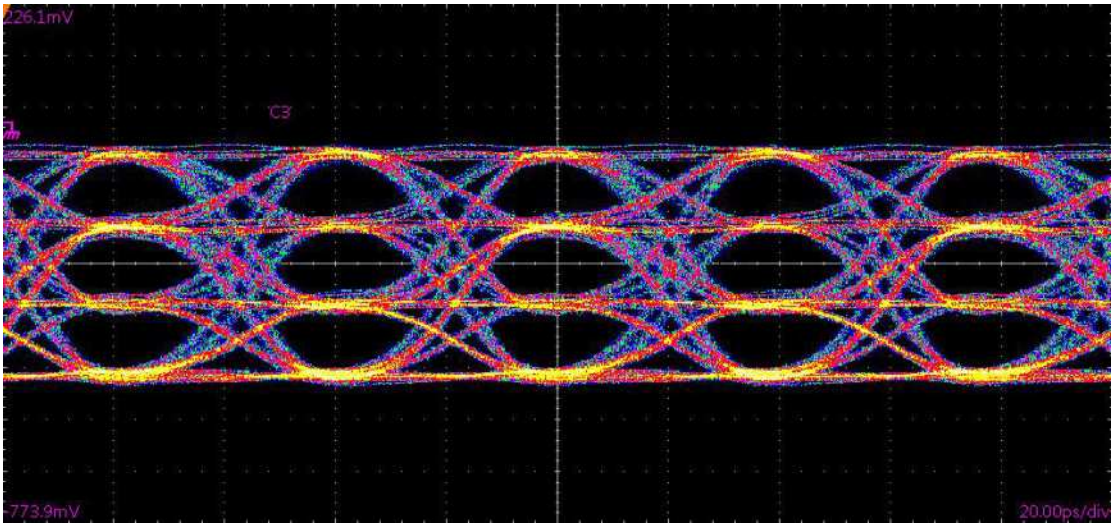


Fig. 5. PAM4 Output Eye Diagram at 28Gb/s (56Gbaud/s) Data Rate

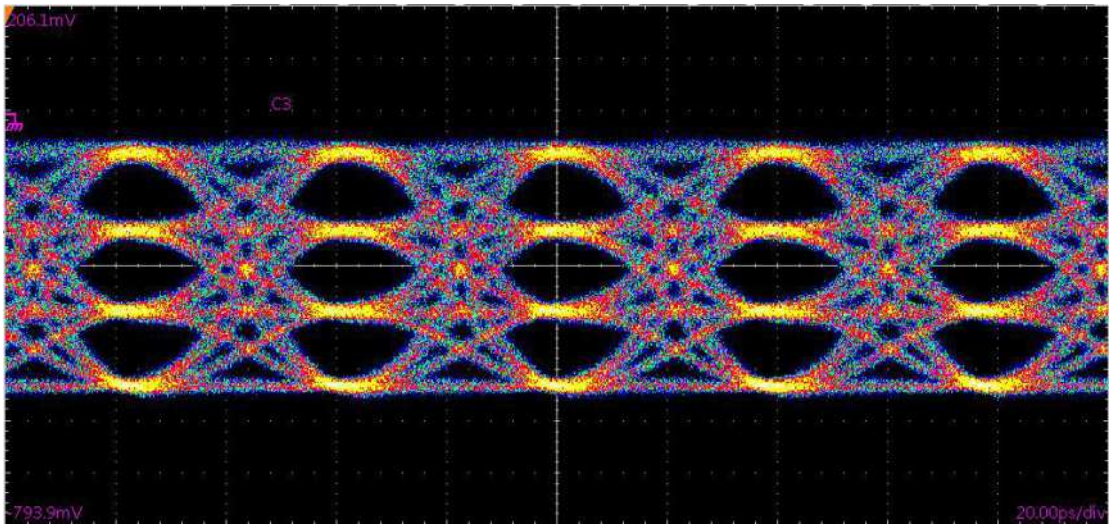


Fig. 6. PAM4 Output Eye Diagram at 32Gb/s (64Gbaud/s) Data Rate

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Electrical Characteristics

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Clock In					
Single-ended Swing	100	200	500	mV_{PP}	
Frequency	0.5		4.0	*GHz*	Full rate clock for data rates from 1 to 8Gbps
	4.0		8.125	*GHz*	Half rate clock for data rates from 8 to 16.25Gbps
Delay Adjustment range	+/- 30			*ps*	
Data In					
Single-ended Swing	100	200	500	mV_{PP}	Single-Ended
Data Rate	1		32.5	*Gbps*	
Clock Out					
Differential Swing	1060		1840	mV_{PP}	1.0-17*GHz*
	320		800	mV_{PP}	18-32*GHz*
Frequency	1		32	*GHz*	
Rise/Fall times	TBD			*ps*	
Data Out					
Data Rate	1.0		32.5	*Gbps*	
Differential Swing	0		2500	mV_{PP}	Adjustable
Rise/Fall times	12	13	14	*ps*	20% - 80%

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Revision History

Revision	Date	Changes
1.3.2	07-2019	Updated Letterhead
1.3.1	11-2017	Added PAM4 eye diagrams Gbaud rate Updated Electrical Characteristics
1.2.1	03-2017	Added PAM4 eye diagrams
1.1.1	07-2016	Added DLL capability Added Terminal Functions Updated Electrical Characteristics Removed some figures to standardize document
1.0.1	11-2014	Initial release