ASVMP series

Plastic SMD MEMs Clock Oscillator

Description

The Abracon ASVMP series is a programmable MEMS oscillator, with a continuous operating power supply ranging from 2.25V to 3.6V. This series features low power consumption, a wide frequency range, excellent phase noise, tight stabilities, and short lead times for industrial, consumer, and other applications. The ASVMP series comes in a 7.0 x 5.0 mm compact package with CMOS, HCSL, LVDS, or LVPECL output logic.



Features

- Low Power Consumption for high-speed communication
- Exceptional Stability Over Temp. at -40 to +85°C, ±10ppm
- Extended Operating Temperature at -55 to +125°C, ±25ppm
- MIL-STD-883 shock and vibration compliant
- Durable QFN Plastic Compact Packaging
- Enable or Disable Tri-state function
- Low jitter (Period jitter RMS and Phase jitter RMS)
- High power supply noise reduction, -50dBc
- REACH/RoHS II Compliant | MSL Level 1

Applications

- Storage Area Networks (SATA, SAS, Fiber Channel)
- Passive Optical Networks (EPON, 10G-EPON, GPON, 10G-PON)
- Ethernet (1G, 10GBASE-T,/KR/LR/SR, FCoE)
- PCI Express
- Display port

Key Electrical Specifications – Continuous Vdd: 2.5V - 0.25V to 3.3V + 0.3V

Parameters		Min.	Typ.	Max.	Units	Notes
Frequency Range	CMOS	2.3000		170.0000	MHz	-20 ~ +70°C -40 ~ +85°C
	CMOS	3.3000		170.0000		-40 ~ +105°C -55 ~ +125°C
	LVPECL	2.3000		460.0000		-20 ~ +70°C -40 ~ +85°C -40 ~ +105°C
	LVDS	2.3000		460.0000		-20 ~ +70°C -40 ~ +85°C -40 ~ +105°C
	HCSL	2.3000		460.0000		-20 ~ +70°C -40 ~ +85°C -40 ~ +105°C
Operating Temperature		-20		+70	°C	See options
Storage Temperature		-55		+150	°C	
Overall Frequency Stability [Note 1]		-50		+50	ppm	See options
Supply Voltage (Vdd)		+2.25		+3.6	V	
Startup Time				5	ms	
Enable Time				20	ns	STD (Tri-state)

Key Electrical Specifications Cont. - CMOS, LVPECL, LVDS, and HCSL

Parameters	Min.	Typ.	Max.	Units	Notes
Disable Time			5	ns	
Disable Current		20	22	mA	STD (Tri-state)
Tri-state Function (Enable/Disable)	"1" (VIH≥0.75*Vdd) or Open: Oscillation "0" (VIL<0.25*Vdd): Hi Z			V	40kΩ pull-up resistor embedded
Aging	-5.0		+5.0	ppm	First year

Note 1: Includes post reflow frequency accuracy, temperature stability, load pulling and power supply variation.

Key Electrical Specifications CMOS

Parameters		Min.	Typ.	Max.	Units	Notes
Supply current (Idd)			31	35	mA	CL=15pF, 125MHz
Output Logic Level	V_{OH}	0.9*Vdd			V	I=±6mA
	V_{OL}			0.1*Vdd	V	
Rise Time	Tr		1.1	2.0	ns	CL=15pF 20% to 80%
Fall Time	Tf		1.3	2.0	ns	
Duty Cycle		45		55	%	
Integrated phase Jitter (J_{PH})			0.30	2	ps	200kHz~20MHz@125MHz
			0.38	2		100kHz~20MHz@125MHz
			1.70	2		12kHz ~ 20MHz@125MHz
Period Jitter RMS (J_{PER})			3.0		ps	

Key Electrical Specifications- LVPECL

Parameters		Min.	Typ.	Max.	Units	Notes
Supply Current (I_{dd})			56.5	58	mA	RL=50Ω
Output Logic Level	V_{OH}	V_{dd}-1.08			V	RL=50Ω
	V_{OL}			Vdd-1.55	V	
Peak to Peak Output Swing			800		mV	Single ended
Rise Time	Tr		250		ps	RL=50Ω, CL=0pF 20% to 80%
Fall Time	Tf		250			
Duty Cycle			48	52	%	Differential
Integrated phase Jitter (J_{PH})			0.25	2	ps	200kHz~20MHz@156.25MHz
			0.38	2		100kHz~20MHz@156.25MHz
			1.70	2		12kHz ~ 20MHz@156.25MHz
Period Jitter RMS (J_{PER})			2.5		ps	

Key Electrical Specifications LVDS

Parameters		Min.	Typ.	Max.	Units	Notes
Supply current (Idd)			29	32	mA	RL=100Ω
Output Offset Voltage (Vos)		1.125		1.4	V	RL=100Ω differential
Delta Offset Voltage (ΔVos)				50	mV	
Peak to Peak Output Swing (Vpp)			350		mV	Single ended
Rise Time	Tr		200		ps	RL=50Ω, CL=2pF 20% to 80%
Fall Time	Tf		200			
Duty Cycle		48		52	%	Differential
Integrated phase Jitter (J_{PH})			0.28	2	ps	200kHz~20MHz@156.25MHz
			0.40	2		100kHz~20MHz@156.25MHz
			1.70	2		12kHz ~ 20MHz@156.25MHz
Period Jitter RMS (J_{PER})			2.5		ps	

Key Electrical Specifications HCSL

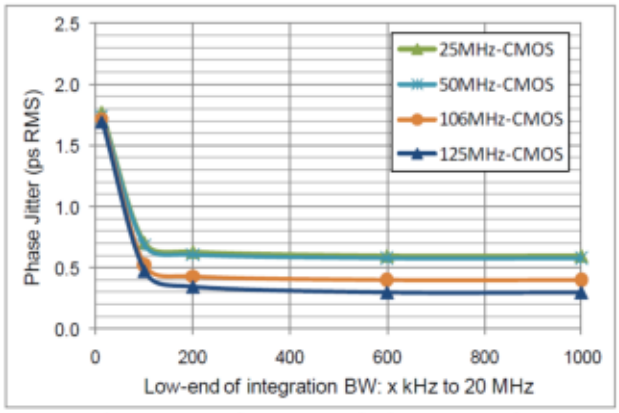
Parameters		Min.	Typ.	Max.	Units	Notes
Supply Current (Idd)			40	42	mA	RL=50Ω
Output Logic Level	V_{OH}	0.725			V	RL=50Ω
	V_{OL}			0.1	V	
Peak to Peak Output Swing (Vpp)			750		mV	Single ended
Rise Time	Tr	200		400	ps	RL=50Ω, CL=2pF 20% to 80%
Fall Time	Tf	200		400		
Duty Cycle		48		52	%	Differential
Integrated Phase Jitter (J_{PH})			0.25	2	ps	200kHz ~ 20MHz@156.25MHz
			0.37	2		100kHz ~ 20MHz@156.25MHz
			1.70	2		12kHz ~ 20MHz@156.25MHz
Period Jitter RMS (J_{PER})			2.5		ps	

Absolute Maximum Ratings

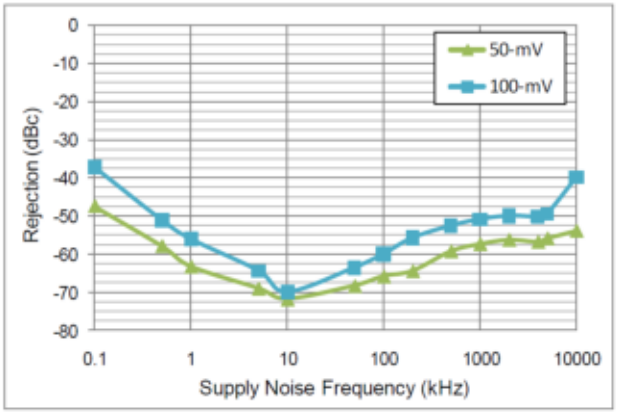
Item	Min.	Max.	Units
Supply voltage	-0.3	+4.0	V
Input voltage	-0.3	Vdd+0.3	V
Junction Temp.		+150	°C
Storage Temp.	-55	+150	°C
Soldering Temp.		+260	°C
ESD HBM MM CDM		 4,000 400 1,500	V

Nominal Performance Parameters (Unless specified otherwise: T=25° C, VDD=3.3 V)

CMOS OUTPUT

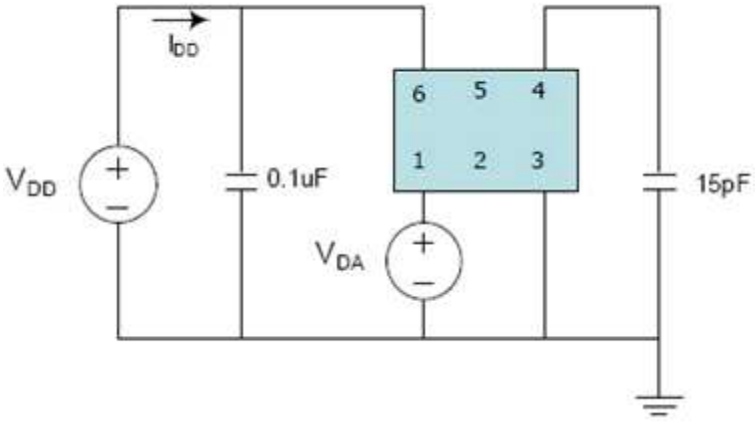


Phase jitter (integrated phase noise)

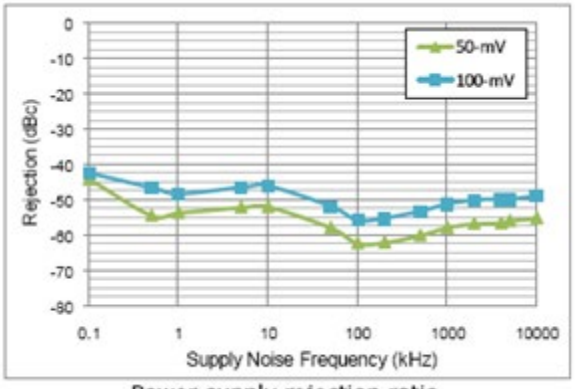


Power supply rejection ratio

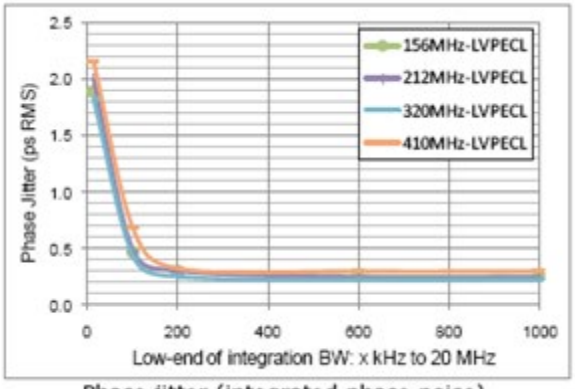
Test Circuit



LVPECL OUTPUT

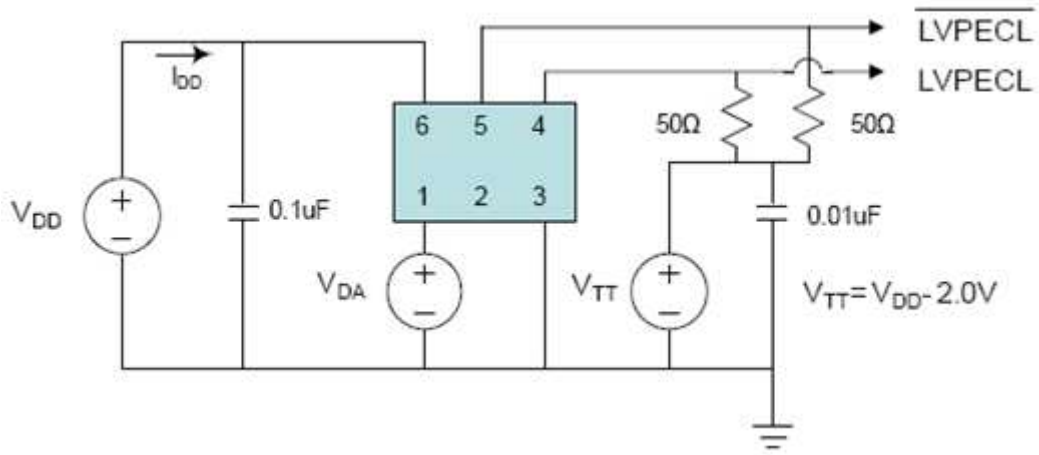


Power supply rejection ratio

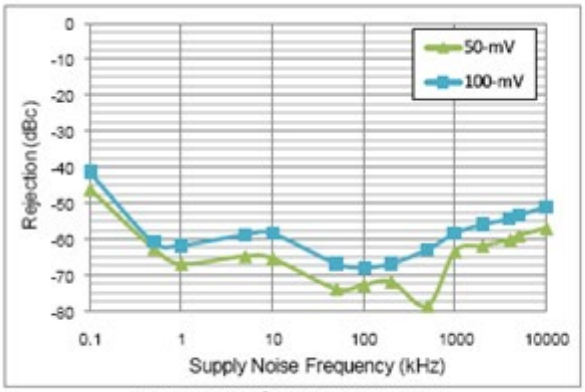


Phase jitter (integrated phase noise)

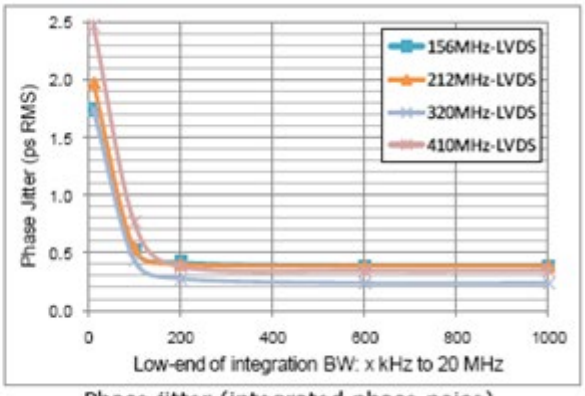
Test Circuit



LVDS OUTPUT

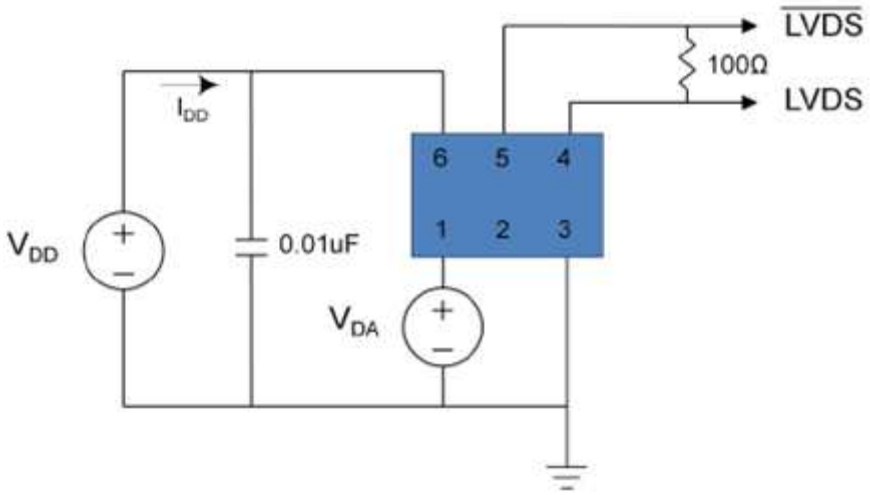


Power supply rejection ratio

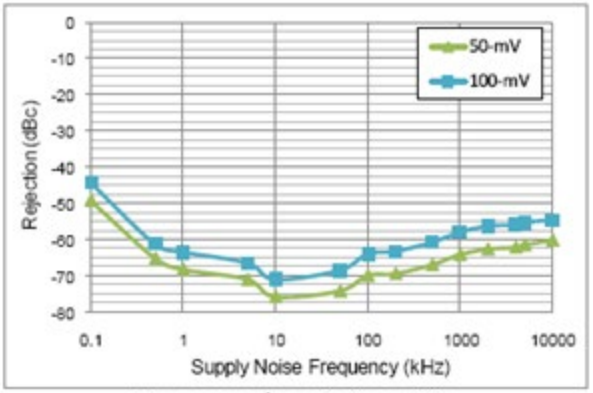


Phase jitter (integrated phase noise)

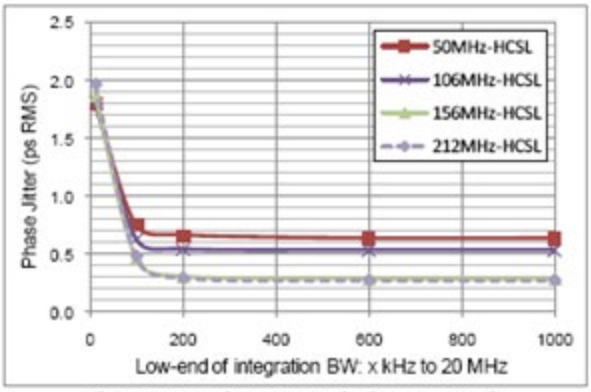
Test Circuit



HCSL OUTPUT

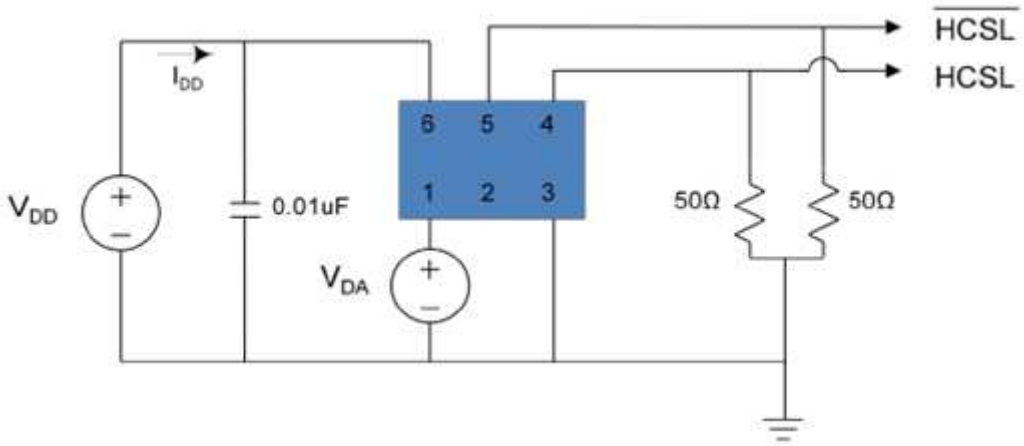


Power supply rejection ratio

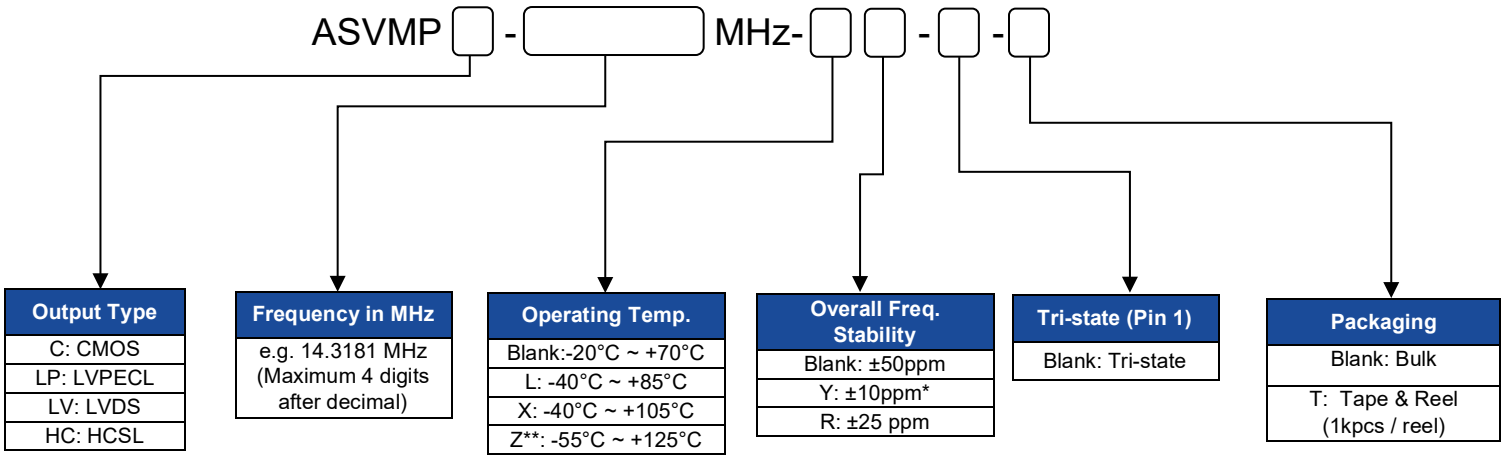


Phase jitter (integrated phase noise)

Test Circuit



Option and Part Identification (left blank if standard)



Output Type
C: CMOS
LP: LVPECL
LV: LVDS
HC: HCSL

Frequency in MHz
e.g. 14.3181 MHz (Maximum 4 digits after decimal)

Operating Temp.
Blank:-20°C ~ +70°C
L: -40°C ~ +85°C
X: -40°C ~ +105°C
Z**: -55°C ~ +125°C

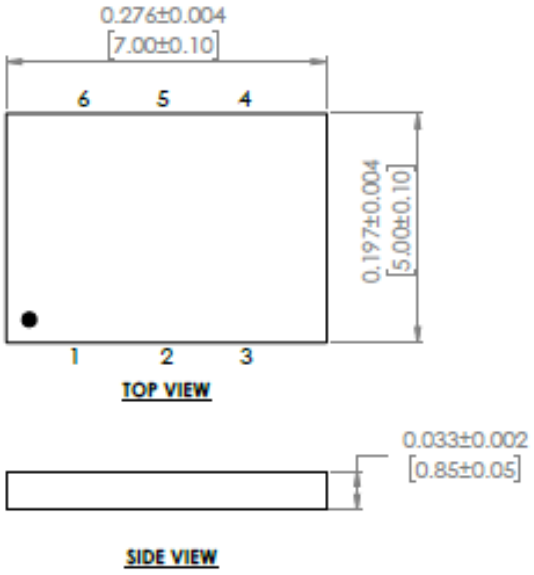
Overall Freq. Stability
Blank: ±50ppm
Y: ±10ppm*
R: ±25 ppm

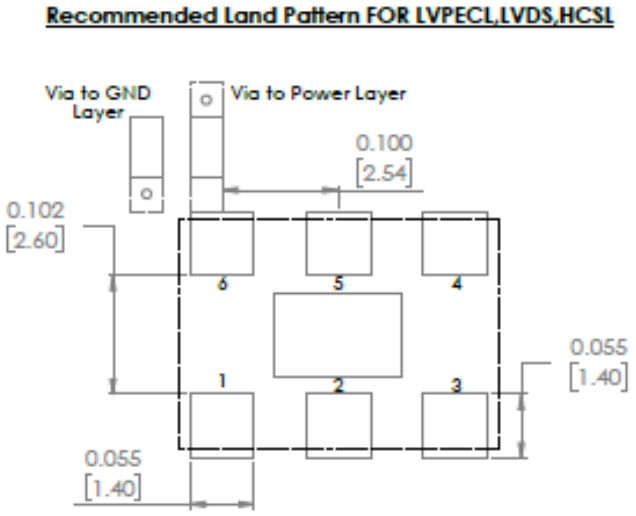
Tri-state (Pin 1)
Blank: Tri-state

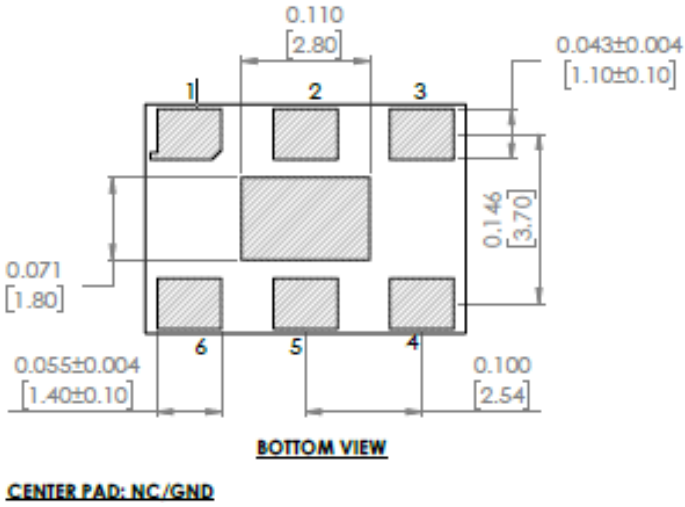
Packaging
Blank: Bulk
T: Tape & Reel (1kpcs / reel)

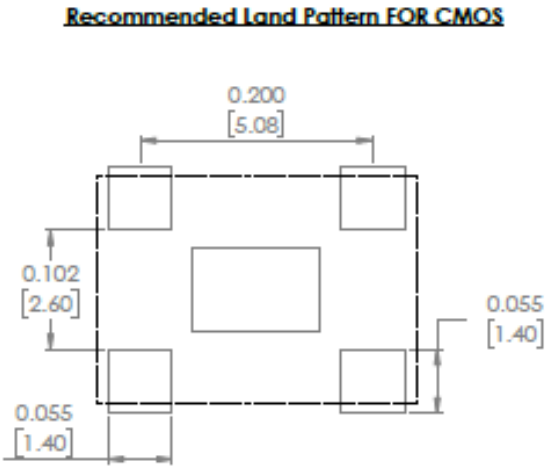
* Temp option L, X or -20°C ~ +70°C, only
** CMOS output only

Mechanical Dimensions









Note: Recommended using an approximately 0.01µF bypass capacitor between PIN 6 and PIN 3

Dimensions: Inches[mm]

Pin #	Function
1	Tri-State
2	NC
3	GND
4	Output
5	NC (CMOS) Output (LVPECL, LVDS, HCSL)
6	Vdd

Reflow Profile [JEDEC J-STD-020]

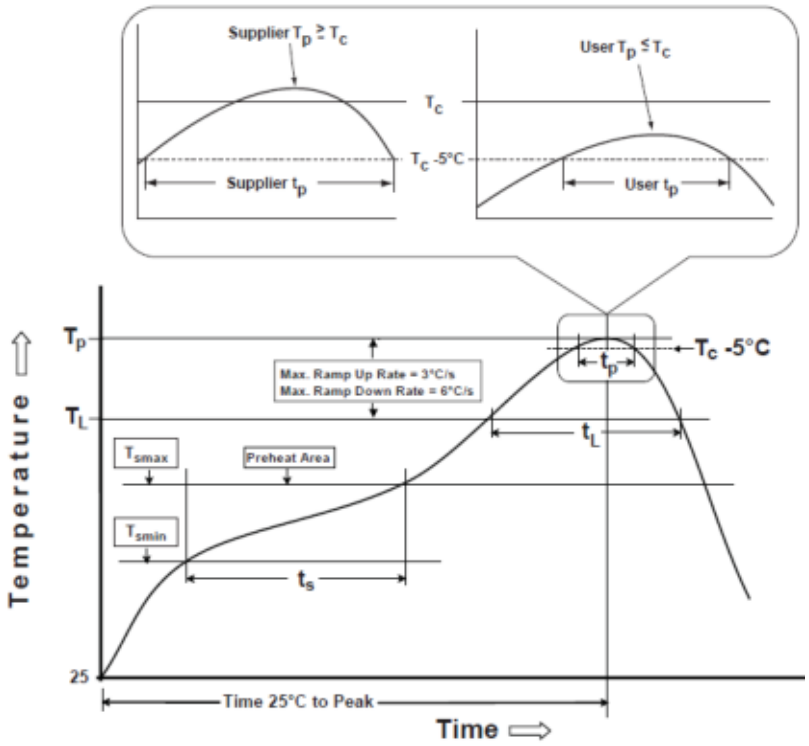


Table 1

SnPb Eutectic Process Classification Temperatures (T_c)		
Package Thickness	**Volume mm³ <350**	**Volume mm³ ≥350**
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2

Pb-Free Process Classification Temperatures (T_c)			
Package Thickness	**Volume mm³ <350**	**Volume mm³ 350-2000**	**Volume mm³ >2000**
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

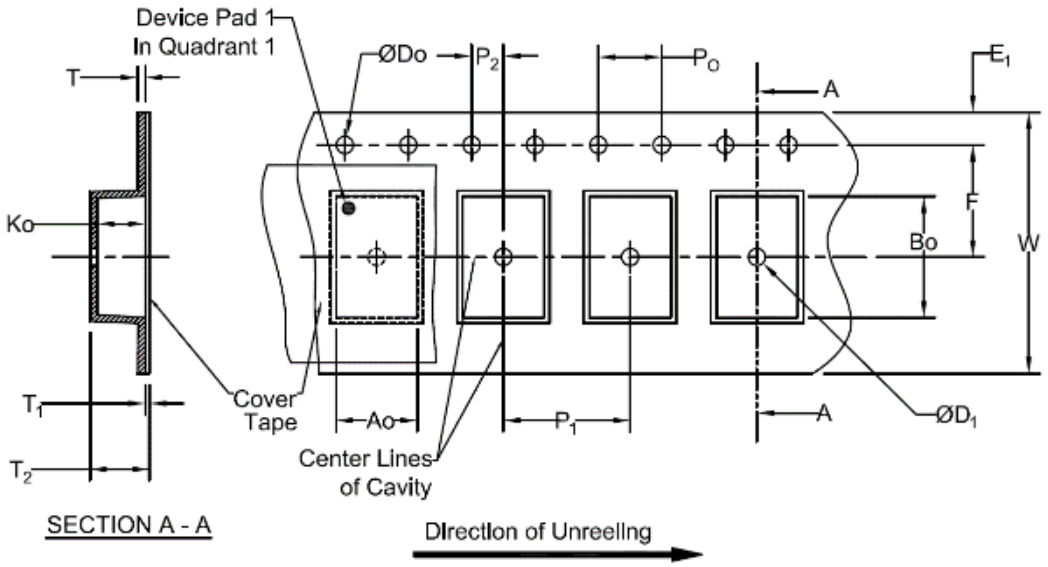
Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat / soak		
Temperature minimum (T_{smin})	100°C	150°C
Temperature maximum (T_{smax})	150°C	200°C
Time (T_{smin} to T_{smax}) (t_s)	60 - 120 sec.	60 - 120 sec.
Average ramp-up rate (T_{smax} to T_P)	3°C/sec. max	3°C/sec. max
Liquidous temperature (T_L)	183°C	217°C
Time at liquidous (t_L)	60 - 150 sec.	60 - 150 sec.
Peak package body temperature (T_P)*	**see Table 1**	**see Table 2**
Time (t_p)** within 5°C of the specified classification temperature (T_C)	20 sec.	30 sec.
Ramp-down rate (T_p to T_{smax})	6°C/sec. max	6°C/sec. max
Time 25°C to peak temperature	6 min. max	8 min. max
Reflow cycles	2 max	2 max

*Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.

**Tolerance for time at peak profile temperature (t_p) is defined as supplier minimum and a user maximum.

Packaging

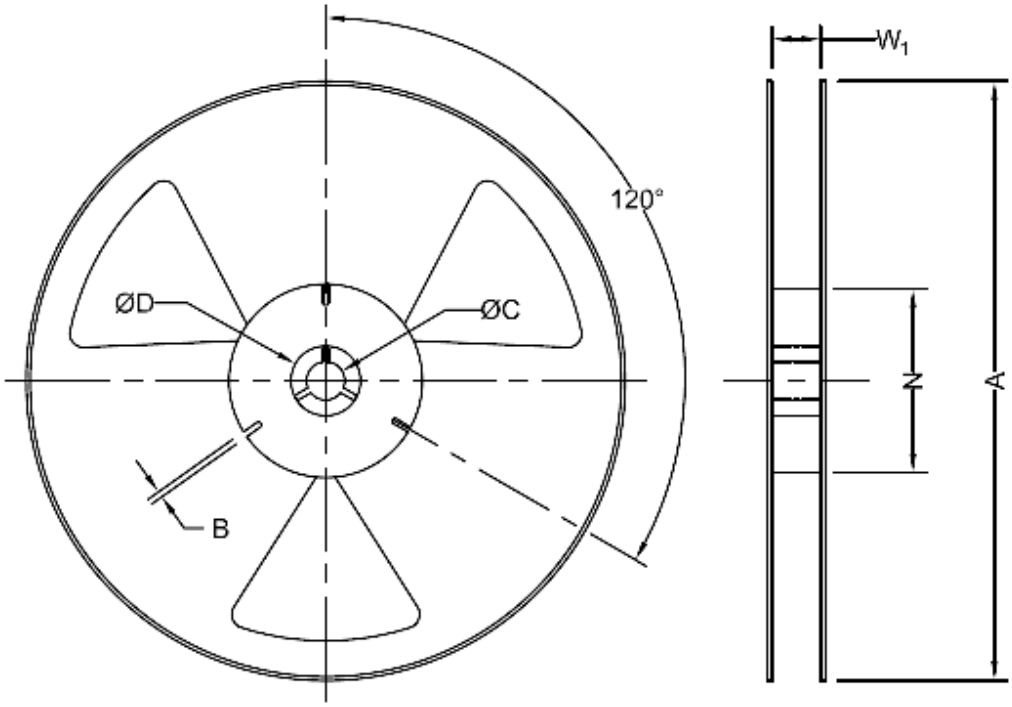
T: 1,000pcs/reel (D=180mm)



Tape Specifications (mm)							
Width	Ao	Bo	Do	D_1 (Min)	E_1	F	Ko
16mm	*	*	1.5+0.1/-0.0	1.0	1.75±0.1	7.5±0.10	*
Width	P1	P2	P0	T (Max)	T1 (Max)	T2 (Max)	W (Max)
16mm	8.0±0.1	2.0±0.1	4.0±0.1	0.6	0.1	8.0	16.3

***Note: Compliant to EIA-481**

Dimensions: mm



Reel Specifications (mm)							
Width	Qty/Reel	A (Nom)	B (Min)	C (Min)	D (Min)	N (Min)	*W_1
16mm	1000	178	1.5	13.0+0.5/-0.2	20.2	50	16.4+2.0/-0.0

***Note: Measured at Hub**

Dimension: mm