Features

- Fast Read Access Time – 70 ns
- Dual Voltage Range Operation
  - Unregulated Battery Power Supply Range, 2.7V to 3.6V or Standard 5V ±10% Supply Range
- Pin Compatible with JEDEC Standard AT27C512R
- Low Power CMOS Operation
  - 20 µA Max (Less than 1 µA Typical) Standby for V_{CC} = 3.6V
  - 29 mW Max Active at 5 MHz for V_{CC} = 3.6V
- JEDEC Standard Surface Mount Packages
  - 32-lead PLCC
  - 28-lead SOIC
  - 28-lead TSOP
- High Reliability CMOS Technology
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid Programming Algorithm – 100 µs/Byte (Typical)
- CMOS and TTL Compatible Inputs and Outputs
  - JEDEC Standard for LVTTL and LVBO
- Integrated Product Identification Code
- Industrial Temperature Range
- Green (Pb/Halide-free) Packaging Option

512K (64K x 8) Unregulated Battery-Voltage High-Speed OTP EPROM

AT27BV512

1. Description

The AT27BV512 is a high-performance, low-power, low-voltage 524,288-bit one-time programmable read-only memory (OTP EPROM) organized as 64K by 8 bits. It requires only one supply in the range of 2.7 to 3.6V in normal read mode operation, making it ideal for fast, portable systems using either regulated or unregulated battery power.

Atmel's innovative design techniques provide fast speeds that rival 5V parts while keeping the low power consumption of a 3V supply. At V_{CC} = 2.7V, any byte can be accessed in less than 70 ns. With a typical power consumption of only 18 mW at 5 MHz and V_{CC} = 3V, the AT27BV512 consumes less than one fifth the power of a standard 5V EPROM.

Standby mode supply current is typically less than 1 µA at 3V. The AT27BV512 simplifies system design and stretches battery lifetime even further by eliminating the need for power supply regulation.

The AT27BV512 is available in industry-standard JEDEC-approved one-time programmable (OTP) plastic PLCC, SOIC, and TSOP packages. All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

The AT27BV512 operating with V_{CC} at 3.0V produces TTL level outputs that are compatible with standard TTL logic devices operating at V_{CC} = 5.0V. At V_{CC} = 2.7V, the part is compatible with JEDEC approved low voltage battery operation (LVBO) interface specifications. The device is also capable of standard 5-volt operation making it ideally suited for dual supply range systems or card products that are pluggable in both 3-volt and 5-volt hosts.

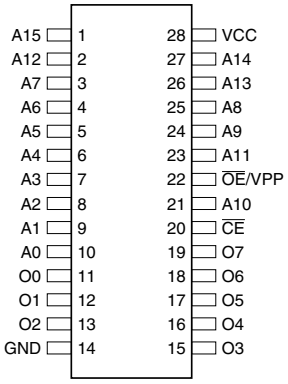
0602E–EPROM–12/07

Atmel's AT27BV512 has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry-standard programming equipment to select the proper programming algorithms and voltages. The AT27BV512 programs exactly the same way as a standard 5V AT27C512R and uses the same programming equipment.

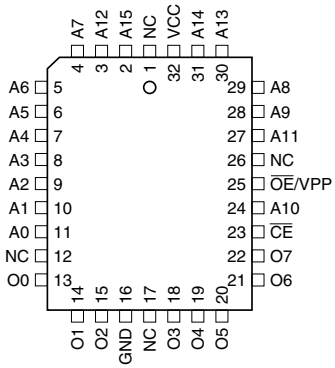
2. Pin Configurations

Pin Name	Function
A0 - A15	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$/VPP	Output Enable/Program Supply
NC	No Connect

2.1 28-lead SOIC Top View

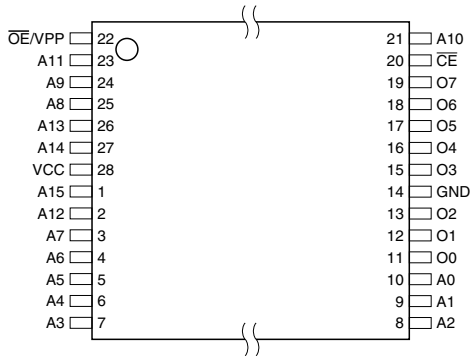


2.2 32-lead PLCC Top View



Note: PLCC package pins 1 and 17 are Don't Connect.

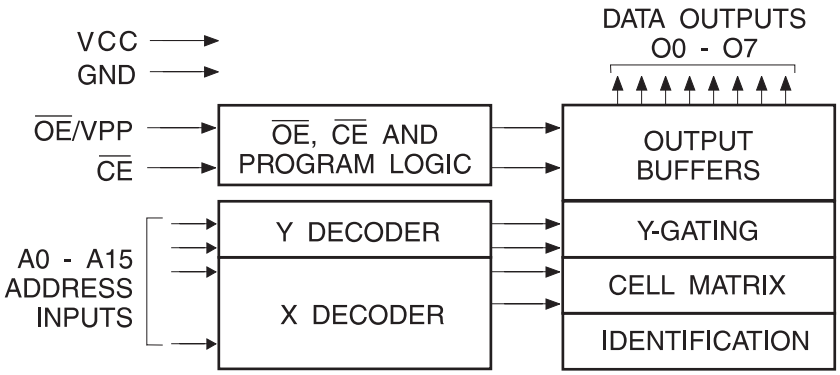
2.3 28-lead TSOP (Type 1) Top View



3. System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed datasheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

4. Block Diagram



5. Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Notes: 1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0V for pulses of less than 20 ns.

6. Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}/V_{PP}$	Ai	V_{CC}	Outputs
Read[2]	V_{IL}	V_{IL}	Ai	V_{CC}	D_{OUT}
Output Disable[2]	V_{IL}	V_{IH}	X[1]	V_{CC}	High Z
Standby[2]	V_{IH}	X	X	V_{CC}	High Z
Rapid Program[3]	V_{IL}	V_{PP}	Ai	V_{CC}	D_{IN}
PGM Verify[3]	V_{IL}	V_{IL}	Ai	V_{CC}	D_{OUT}
PGM Inhibit[3]	V_{IH}	V_{PP}	X	V_{CC}	High Z
Product Identification[3][5]	V_{IL}	V_{IL}	A9 = V_H[4] A0 = V_{IH} or V_{IL} A1 - A15 = V_{IL}	V_{CC}	Identification Code

Notes:
1. X can be V_{IL} or V_{IH}.
2. Read, output disable, and standby modes require, 2.7V ≤V_{CC} ≤3.6V, or 4.5V ≤V_{CC} ≤5.5V.
3. Refer to Programming Characteristics. Programming modes require V_{CC} = 6.5V.
4. V_H = 12.0 ±0.5V.
5. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

7. DC and AC Operating Conditions for Read Operation

	AT27BV512-70
Operating Temperature (Case)	-40°C - 85°C
V_{CC} Power Supply	2.7V to 3.6V
	5V ±10%

8. DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
V_{CC} = 2.7V to 3.6V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		20	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		100	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}, V_{CC} = 3.6V		8	mA
V_{IL}	Input Low Voltage	V_{CC} = 3.0 to 3.6V	-0.6	0.8	V
		V_{CC} = 2.7 to 3.6V	-0.6	0.2 x V_{CC}	V
V_{IH}	Input High Voltage	V_{CC} = 3.0 to 3.6V	2.0	V_{CC} + 0.5	V
		V_{CC} = 2.7 to 3.6V	0.7 x V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA		0.4	V
		I_{OL} = 100 µA		0.2	V
		I_{OL} = 20 µA		0.1	V
V_{OH}	Output High Voltage	I_{OH} = -2.0 mA	2.4		V
		I_{OH} = -100 µA	V_{CC} - 0.2		V
		I_{OH} = -20 µA	V_{CC} - 0.1		V
V_{CC} = 4.5V to 5.5V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ±0.3V		100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		20	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

Notes: 1. V_{CC} must be applied simultaneously with or before $\overline{OE}/V_{PP}$, and removed simultaneously with or after $\overline{OE}/V_{PP}$.

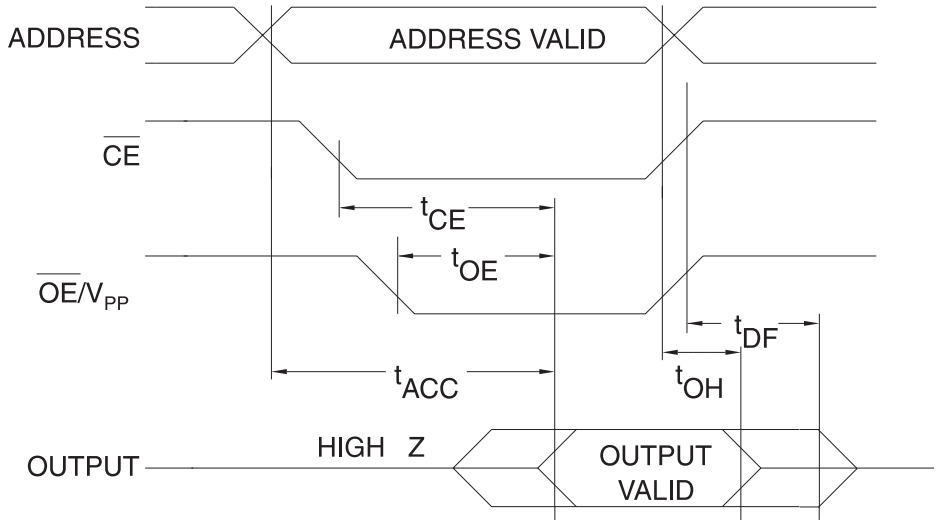
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

9. AC Characteristics for Read Operation

V_{CC} = 2.7V to 3.6V and 4.5V to 5.5V

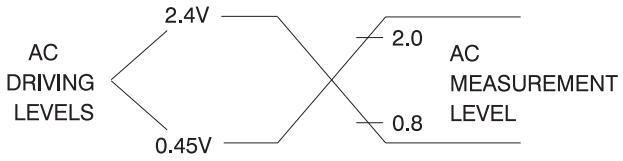
Symbol	Parameter	Condition	AT27BV512-70		Units
			Min	Max	
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}/V_{PP}$ = V_{IL}		70	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}/V_{PP}$ = V_{IL}		70	ns
t_{OE} (2)(3)	$\overline{OE}/V_{PP}$ to Output Delay	$\overline{CE}$ = V_{IL}		50	ns
t_{DF} (4)(5)	$\overline{OE}/V_{PP}$ or $\overline{CE}$ High to Output Float, Whichever Occurred First			40	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$, Whichever Occurred First		0		ns

10. AC Waveforms for Read Operation (1)



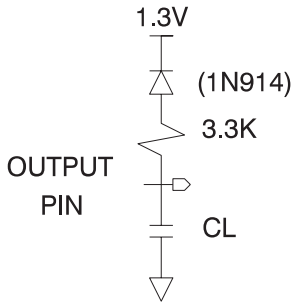
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}/V_{PP}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}/V_{PP}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.
6. When reading a AT27BV256, a 0.1 µF capacitor is required across V_{CC} and ground to suppress spurious voltage transients.

11. Input Test Waveform and Measurement Level



t_R, t_F < 20 ns (10% to 90%)

12. Output Test Load



Note: CL = 100 pF
including jig capacitance.

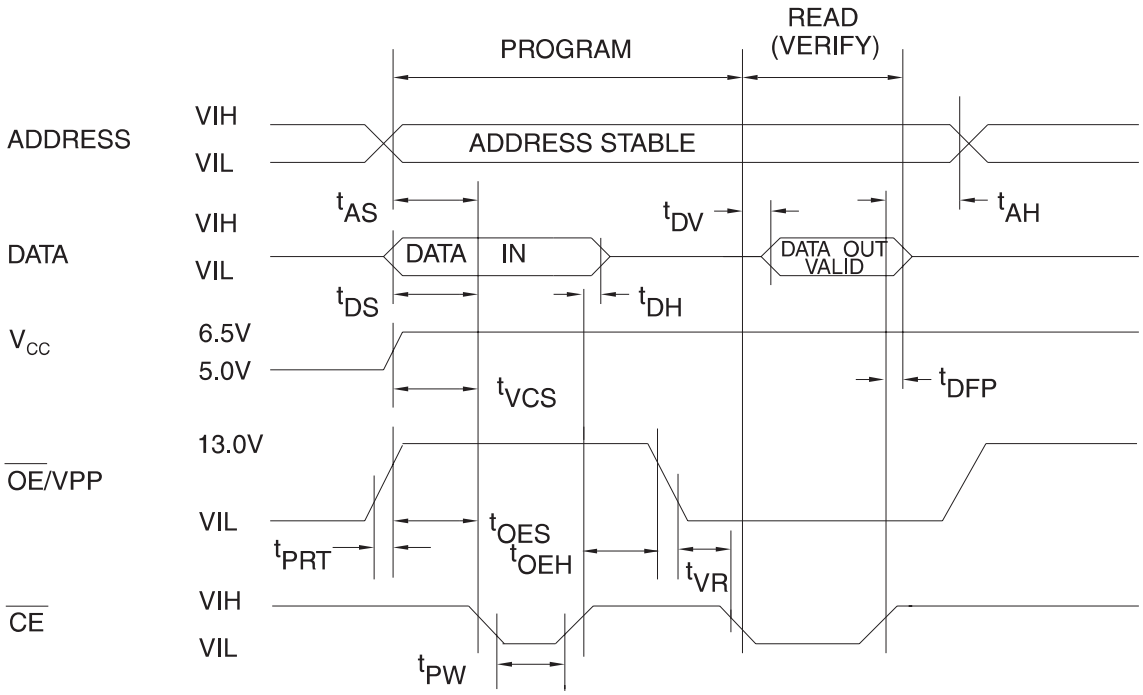
13. Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

14. Programming Waveforms[1]



Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27BV512, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

15. DC Programming Characteristics

T_A = 25 ±5°C, V_{CC} = 6.5 ±0.25V, $\overline{OE}/V_{PP}$ = 13.0 ±0.25V

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			25	mA
I_{PP2}	$\overline{OE}/V_{PP}$ Current	$\overline{CE} = V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

16. AC Programming Characteristics

T_A = 25 ±5°C, V_{CC} = 6.5 ±0.25V, $\overline{OE}/V_{PP}$ = 13.0 ±0.25V

Symbol	Parameter	Test Conditions[1]	Limits		Units
			Min	Max	
t_{AS}	Address Setup Time	Input Rise and Fall Times: (10% to 90) 20 ns Input Pulse Levels: 0.45V to 2.4V Input Timing Reference Level: 0.8V to 2.0V Output Timing Reference Level: 0.8V to 2.0V	2		µs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time		2		µs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{CE}$ High to Output Float Delay[2]		0	130	ns
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width[3]		95	105	µs
t_{DV}	Data Valid from $\overline{CE}$[2]			1	µs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2		µs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50		ns

Notes:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven – see timing diagram.
3. Program Pulse width tolerance is 100 µsec ±5%.

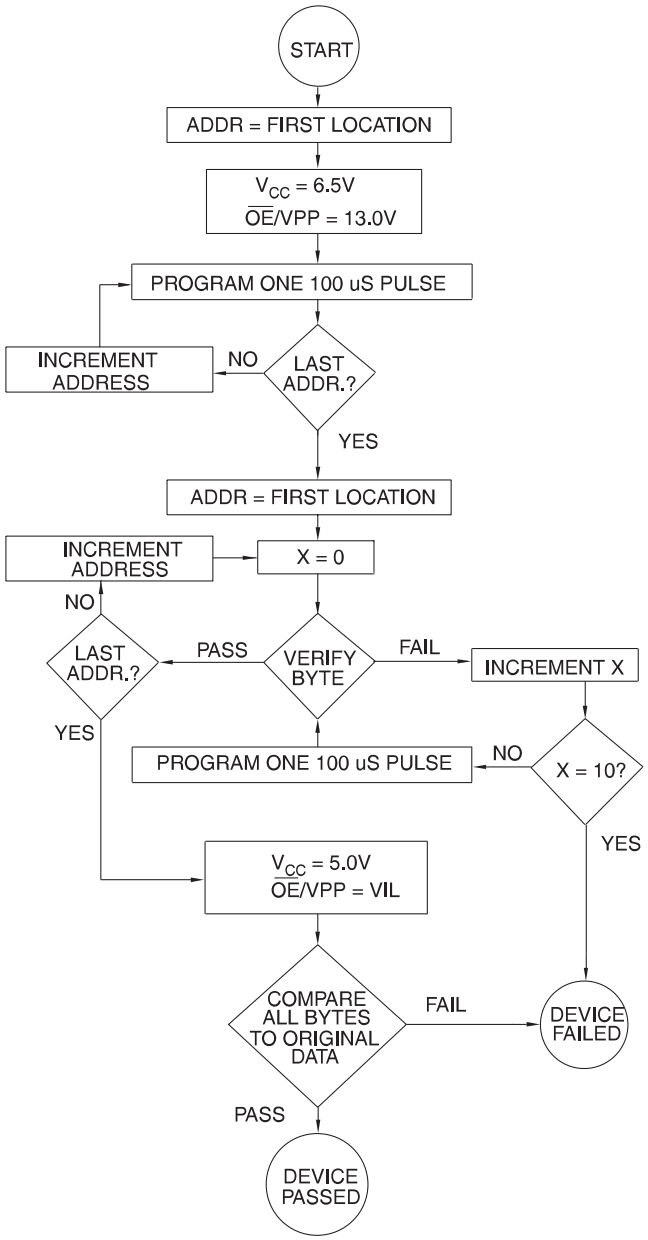
17. Atmel's AT27BV512 Integrated Product Identification Code[1]

Codes	Pins									Hex Data
	A0	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	1	0	1	0D

Note: 1. The AT27BV512 has the same Product Identification Code as the AT27C512R. Both are programming compatible.

18. Rapid Programming Algorithm

A 100 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and $\overline{OE}/V_{PP}$ is raised to 13.0V. Each address is first programmed with one 100 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. $\overline{OE}/V_{PP}$ is then lowered to V_{IL} and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



19. Ordering Information

19.1 Standard Package

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	8	0.02	AT27BV512-70JI AT27BV512-70RI AT27BV512-70TI	32J 28R(1) 28T	Industrial (-40°C to 85°C)

Note: Not recommended for new designs. Use Green package option.

19.2 Green Package Option (Pb/Halide-free)

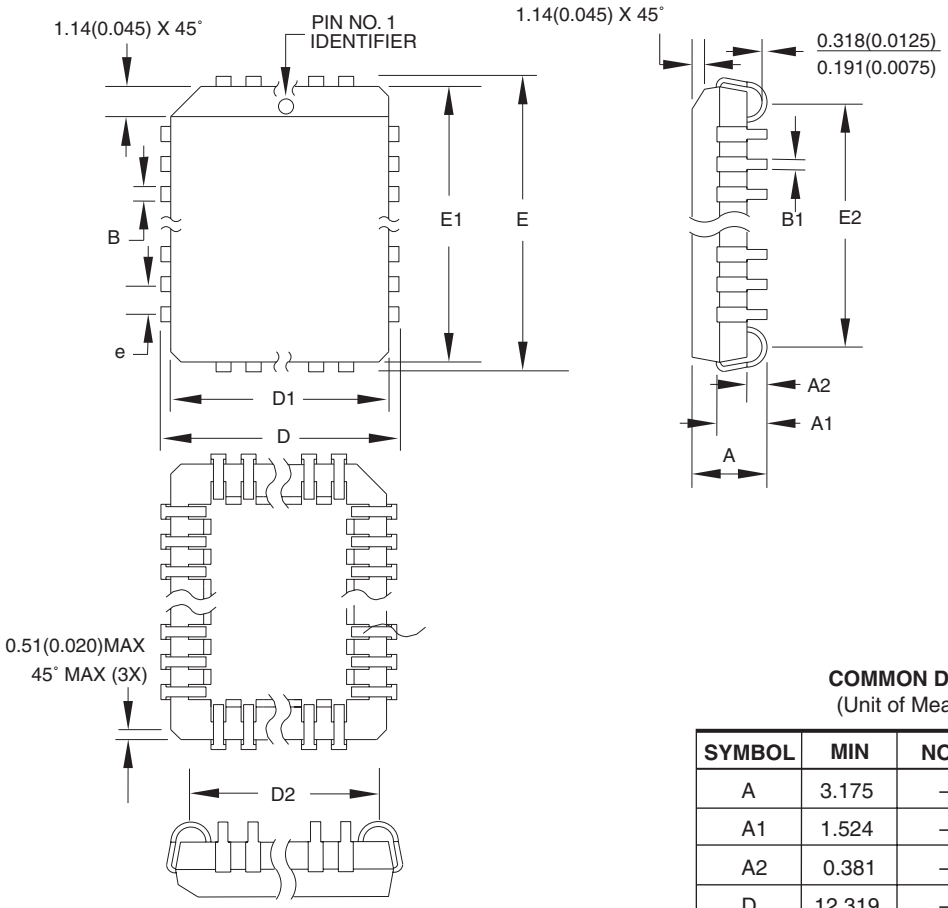
t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	8	0.02	AT27BV512-70JU AT27BV512-70RU AT27BV512-70TU	32J 28R(1) 28T	Industrial (-40°C to 85°C)

Note: 1. The 28-pin SOIC package is not recommended for new designs.

Package Type	
32J	32-lead, Plastic J-leaded Chip Carrier (PLCC)
28R	28-lead, 0.330" Wide, Plastic Gull Wing Small Package (SOIC)
28T	28-lead, Plastic Thin Small Outline Package (TSOP)

20. Packaging Information

20.1 32J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

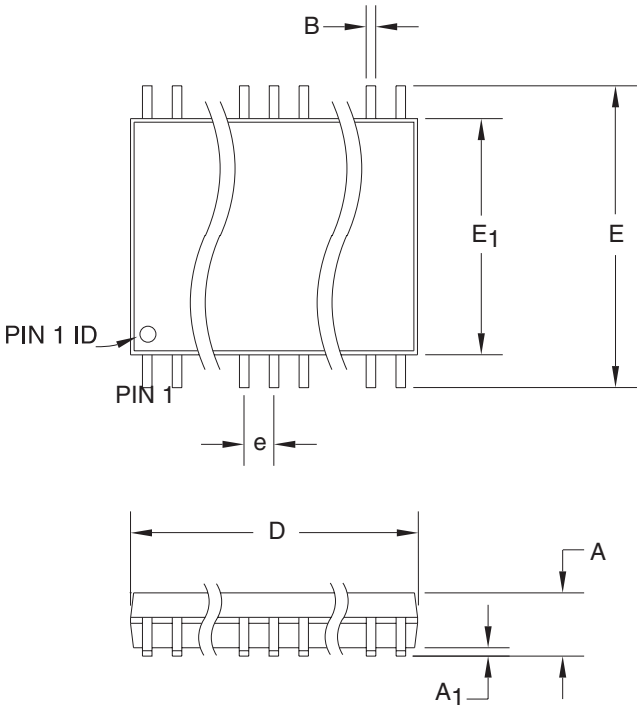
SYMBOL	MIN	NOM	MAX	NOTE
A	3.175	–	3.556	
A1	1.524	–	2.413	
A2	0.381	–	–	
D	12.319	–	12.573	
D1	11.354	–	11.506	Note 2
D2	9.906	–	10.922	
E	14.859	–	15.113	
E1	13.894	–	14.046	Note 2
E2	12.471	–	13.487	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-016, Variation AE.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32J**, 32-lead, Plastic J-leaded Chip Carrier (PLCC)	32J	B

20.2 28R – SOIC



COMMON DIMENSIONS
(Unit of Measure = mm)

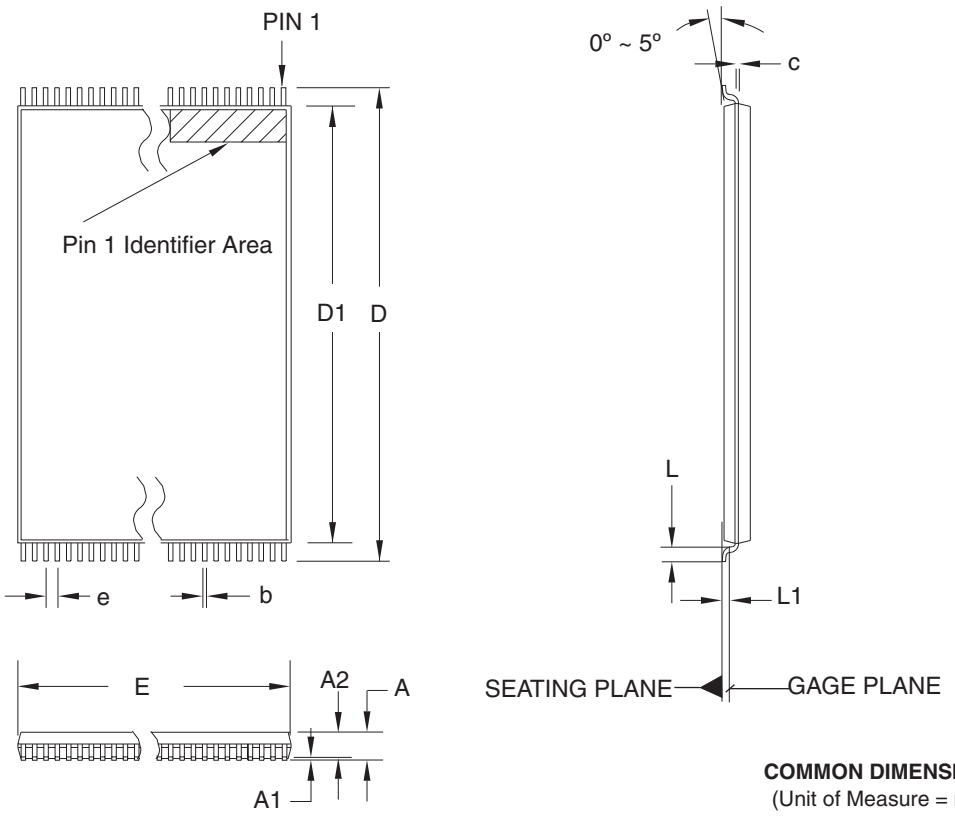
SYMBOL	MIN	NOM	MAX	NOTE
A	2.39	–	2.79	
A1	0.050	–	0.356	
D	18.00	–	18.50	Note 1
E	11.70	–	12.50	
E1	8.59	–	8.79	Note 1
B	0.356	–	0.508	
C	0.203	–	0.305	
L	0.94	–	1.27	
e	1.27 TYP			

Note: 1. Dimensions D and E1 do not include mold Flash or protrusion. Mold Flash or protrusion shall not exceed 0.25 mm (0.010").

5/18/2004

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**28R,** 28-lead, 0.330" Body Width, Plastic Gull Wing Small Outline (SOIC)	28R	C

20.3 28T – TSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.90	1.00	1.05	
D	13.20	13.40	13.60	
D1	11.70	11.80	11.90	Note 2
E	7.90	8.00	8.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.55 BASIC			

Notes:
1. This package conforms to JEDEC reference MO-183.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

12/06/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**28T**, 28-lead (8 x 13.4 mm) Plastic Thin Small Outline Package, Type I (TSOP)	28T	C

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
eprom@atmel.com

Sales Contact
www.atmel.com/contacts

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