Features

- **Fast Read Access Time - 70 ns**
- **Low Power CMOS Operation**
  - **100 µA max. Standby**
  - **30 mA max. Active at 5 MHz**
- **JEDEC Standard Packages**
  - **32-Lead 600-mil PDIP**
  - **32-Lead 450-mil SOIC (SOP)**
  - **32-Lead PLCC**
  - **32-Lead TSOP**
- **5V ± 10% Supply**
- **High Reliability CMOS Technology**
  - **2000V ESD Protection**
  - **200 mA Latchup Immunity**
- **Rapid™ Programming Algorithm - 100 µs/byte (typical)**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Commercial and Industrial Temperature Ranges**

4-Megabit (512K x 8) OTP EPROM

AT27C040

Description

The AT27C040 chip is a low-power, high-performance, 4,194,304-bit one-time programmable read only memory (OTP EPROM) organized as 512K by 8 bits. The AT27C040 requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 70 ns, eliminating the need for speed reducing WAIT states on high-performance microprocessor systems.

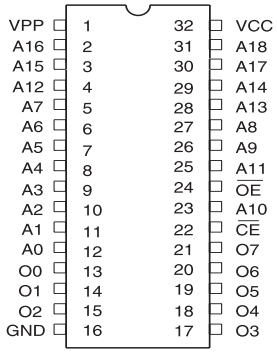
Atmel's scaled CMOS technology provides low active power consumption, and fast programming. Power consumption is typically 8 mA in active mode and less than 10 µA in standby mode.

(continued)

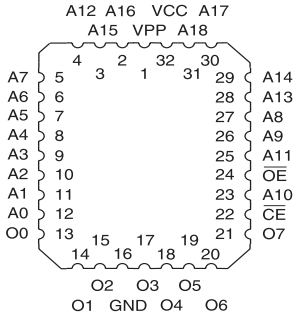
Pin Configurations

Pin Name	Function
A0 - A18	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable

PDIP, SOIC Top View



PLCC Top View



TSOP Top View



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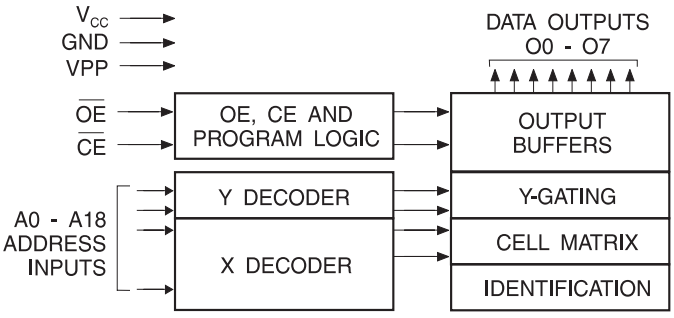
The AT27C040 is available in a choice of industry standard JEDEC-approved one-time programmable (OTP) plastic PDIP, PLCC, SOIC (SOP), and TSOP packages. The device features two-line control ($\overline{CE}$, $\overline{OE}$) to eliminate bus contention in high-speed systems.

Atmel's AT27C040 has additional features to ensure high quality and efficient production use. The Rapid™Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Switching Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Operating Modes

Mode/Pin	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	Ai	X(1)	D_{OUT}
Output Disable	X	V_{IH}	X	X	High Z
Standby	V_{IH}	X	X	X	High Z
Rapid Program(2)	V_{IL}	V_{IH}	Ai	V_{PP}	D_{IN}
PGM Verify	X	V_{IL}	Ai	V_{PP}	D_{OUT}
PGM Inhibit	V_{IH}	V_{IH}	X	V_{PP}	High Z
Product Identification(4)	V_{IL}	V_{IL}	A9 = V_H(3) A0 = V_{IH} or V_{IL} A1 - A18 = V_{IL}	X	Identification Code

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to Programming Characteristics
3. $V_H = 12.0 \pm 0.5V$.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identificaton byte and high (V_{IH}) to select the Device Code byte.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V (1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V (1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V (1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Conditions for Read Operation

		AT27C040			
		-70	-90	-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

DC and Operating Characteristics for Read Operation

Symbol	Paramter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1}(2)	V_{PP}(1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC1}(1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		30	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

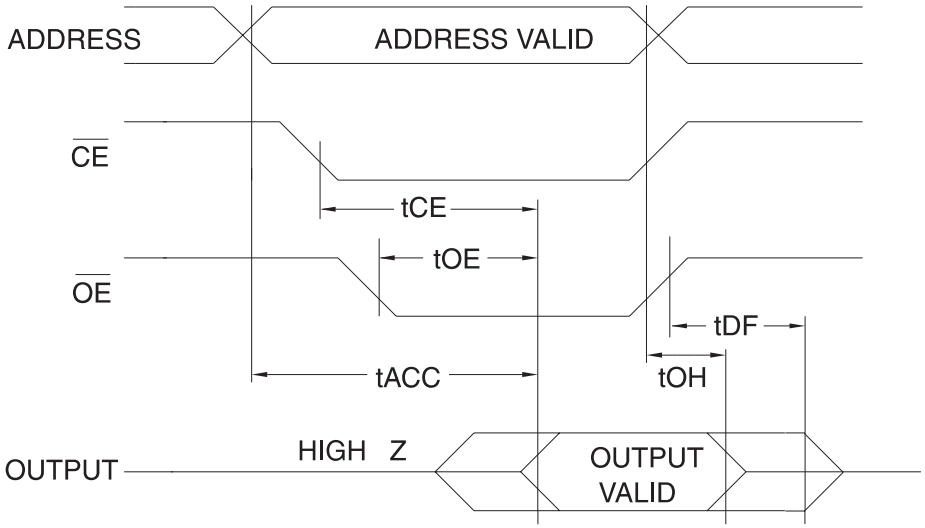
Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

AC Characteristics for Read Operation

			AT27C040								
			-70		-90		-12		-15		
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC}(3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		70		90		120		150	ns
t_{CE}(2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		70		90		120		150	ns
t_{OE}(2)(3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		30		35		35		40	ns
t_{DF}(4)(5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			20		20		30		30	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		0		0		0		0		ns

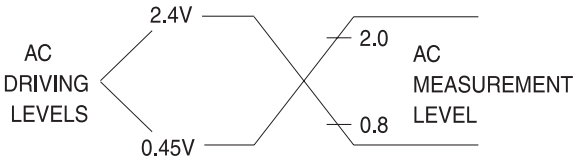
Note: 2, 3, 4, 5 - see AC Waveforms for Read Operation

AC Waveforms for Read Operation[1]

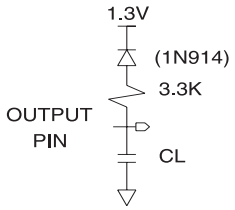


Notes:
1. Tiiming measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



Output Test Load



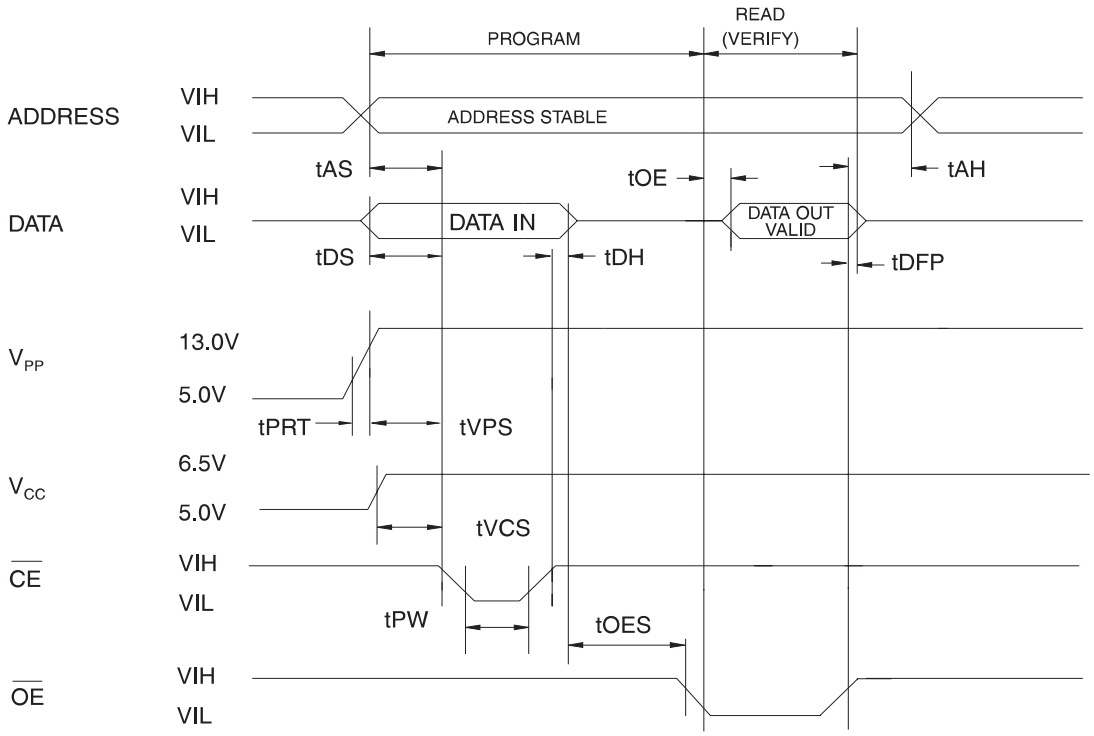
Pin Capacitance

(f = 1 MHz, T = 25°C)[1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms[1]



Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C040 a 0.1 µF capacitor is required across V_{PP} and ground to supress spurious voltage transients.

DC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.7	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			40	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE} = V_{IL}$		20	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25V$, $V_{PP} = 13.0 \pm 0.25V$

Symbol	Parameter	Test Conditions[1]	Limits		Units
			Min	Max	
t_{AS}	Address Setup Time	Input Rise and Fall Times (10% to 90%) 20ns Input Pulse Levels 0.45V to 2.4V Input Timing Reference Level 0.8V to 2.0V Output Timing Reference Level 0.8V to 2.0V	2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay[2]		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width[3]		95	105	µs
t_{OE}	Data Valid from $\overline{OE}$[2]			150	ns
t_{PRT}	V_{PP} Pulse Rise Time During Programming		50		ns

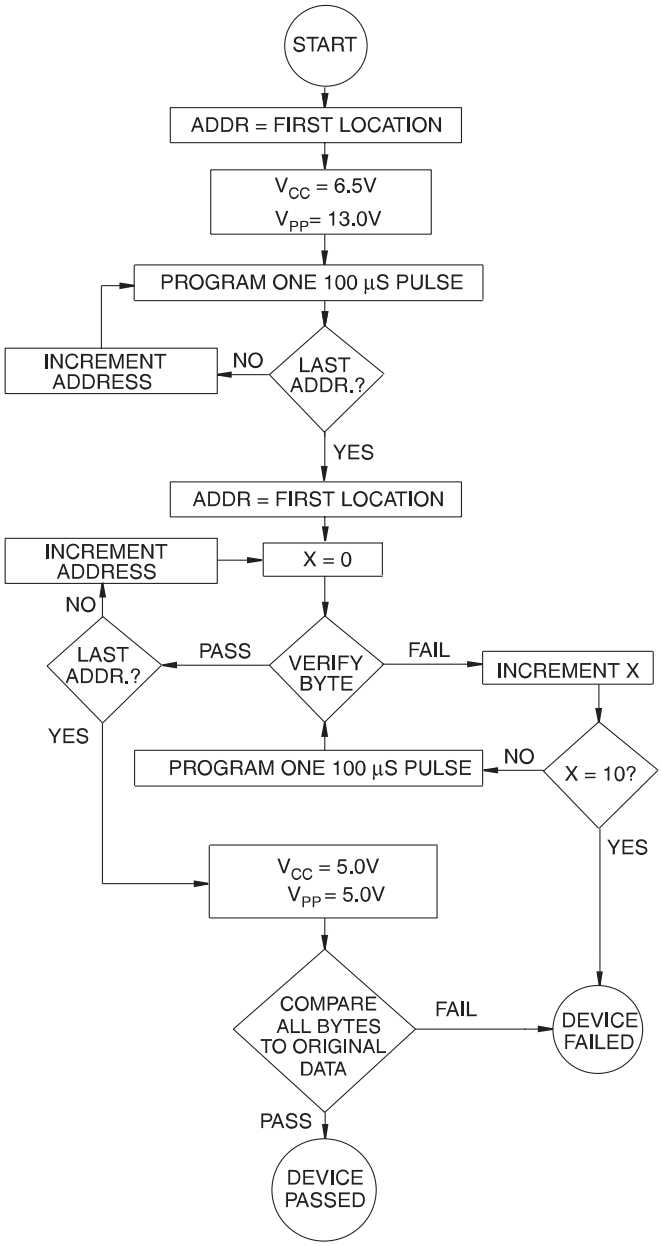
Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

Atmel's 27C040 Integrated Product Identification Code

Codes	Pins									Hex Data
	A0	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	0	1	1	0B

Rapid Programming Algorithm

A 100 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	30	0.1	AT27C040-70JC	32J	Commercial
			AT27C040-70PC	32P6	(0°C to 70°C)
			AT27C040-70RC	32R	
			AT27C040-70TC	32T	
	30	0.1	AT27C040-70JI	32J	Industrial
			AT27C040-70PI	32P6	(-40°C to 85°C)
			AT27C040-70RI	32R	
			AT27C040-70TI	32T	
90	30	0.1	AT27C040-90JC	32J	Commercial
			AT27C040-90PC	32P6	(0°C to 70°C)
			AT27C040-90RC	32R	
			AT27C040-90TC	32T	
	30	0.1	AT27C040-90JI	32J	Industrial
			AT27C040-90PI	32P6	(-40°C to 85°C)
			AT27C040-90RI	32R	
			AT27C040-90TI	32T	
120	30	0.1	AT27C040-12JC	32J	Commercial
			AT27C040-12PC	32P6	(0°C to 70°C)
			AT27C040-12RC	32R	
			AT27C040-12TC	32T	
	30	0.1	AT27C040-12JI	32J	Industrial
			AT27C040-12PI	32P6	(-40°C to 85°C)
			AT27C040-12RI	32R	
			AT27C040-12TI	32T	
150	30	0.1	AT27C040-15JC	32J	Commercial
			AT27C040-15PC	32P6	(0°C to 70°C)
			AT27C040-15RC	32R	
			AT27C040-15TC	32T	
	30	0.1	AT27C040-15JI	32J	Industrial
			AT27C040-15PI	32P6	(-40°C to 85°C)
			AT27C040-15RI	32R	
			AT27C040-15TI	32T	

Package Type	
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
32P6	32-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32R	32-Lead, 0.450" Wide, Plastic Gull Wing Small Outline (SOIC)
32T	32-Lead, Plastic Thin Small Outline Package (TSOP)