Features

- Single 2.7 - 3.6V Supply
- RapidS™ Serial Interface: 40 MHz Maximum Clock Frequency (SPI Modes 0 and 3 Compatible for Frequencies Up to 33 MHz)
- Page Program
  - 8192 Pages (528 Bytes/Page)
- Automated Erase Operations
  - Page Erase 528 Bytes
  - Block Erase 4,224 Bytes
- Two 528-byte SRAM Data Buffers – Allows Receiving of Data while Reprogramming the Flash Array
- Continuous Read Capability through Entire Array
  - Ideal for Code Shadowing Applications
- Low-power Dissipation
  - 10 mA Active Read Current Typical
  - 6 µA Standby Current Typical
- Hardware and Software Data Protection Features
  - Individual Sector Locking
- Security: 128-byte Security Register
  - 64-byte User Programmable Space
  - Unique 64-byte Device Identifier
- JEDEC Standard Manufacturer and Device ID Read
- 100,000 Program/Erase Cycles per Page Minimum
- Data Retention – 20 years
- Commercial and Industrial Temperature Ranges
- Green (Pb/Halide-free/RoHS Compliant) Packaging Options

1. Description

The AT45DB321C is an SPI compatible, serial-interface Flash memory ideally suited for a wide variety of digital voice-, image-, program code- and data-storage applications. The AT45DB321C supports a 4-wire serial interface known as RapidS for applications requiring very high speed operations.

Its 34,603,008 bits of memory are organized as 8192 pages of 528 bytes each. In addition to the 33-megabit main memory, the AT45DB321C also contains two SRAM buffers of 528 bytes each.

The buffers allow the receiving of data while a page in the main page Memory is being reprogrammed, as well as writing a continuous data stream. EEPROM emulation (bit or byte alterability) is easily handled with a self-contained three step read-modify-write operation. Unlike conventional Flash memories that are accessed randomly with multiple address lines and a parallel interface, the DataFlash uses a RapidS serial interface to sequentially access its data. The simple sequential access dramatically reduces active pin count, facilitates hardware layout, increases system reliability, minimizes switching noise, and reduces package size. The device is optimized for use in many commercial and industrial applications where high-density, low-pin count, low-voltage and low-power are essential. The device operates at clock frequencies up to 40 MHz with a typical active read current consumption of 10 mA.

32-megabit 2.7 volt DataFlash®

AT45DB321C

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3387M–DFLASH–2/08

To allow for simple in-system reprogrammability, the AT45DB321C does not require high input voltages for programming. The device operates from a single power supply, 2.7V to 3.6V, for both the program and read operations. The AT45DB321C is enabled through the chip select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK).

All programming and erase cycles are self-timed.

2. Pin Configurations and Packages

Table 2-1. Pin Configurations

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Clock
SI	Serial Input
SO	Serial Output
$\overline{WP}$	Hardware Page Write Protect Pin
$\overline{RESET}$	Chip Reset
RDY/$\overline{BUSY}$	Ready/Busy

Figure 2-1. TSOP Top View – Type 1

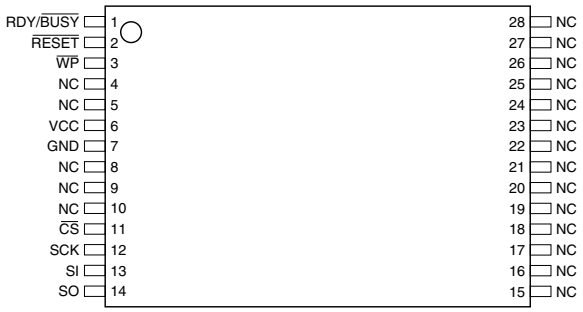


Figure 2-2. CBGA Top View through Package

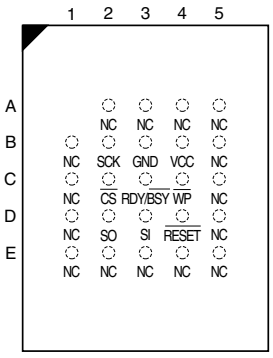


Figure 2-3. SOIC Top View

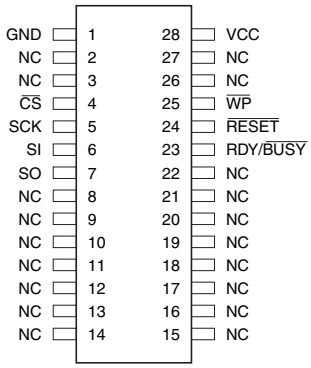


Figure 2-4. DataFlash Card[1] Top View through Package

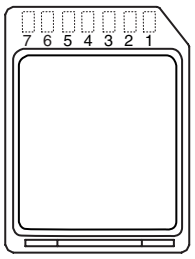
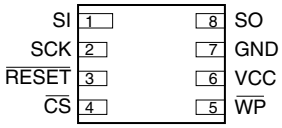
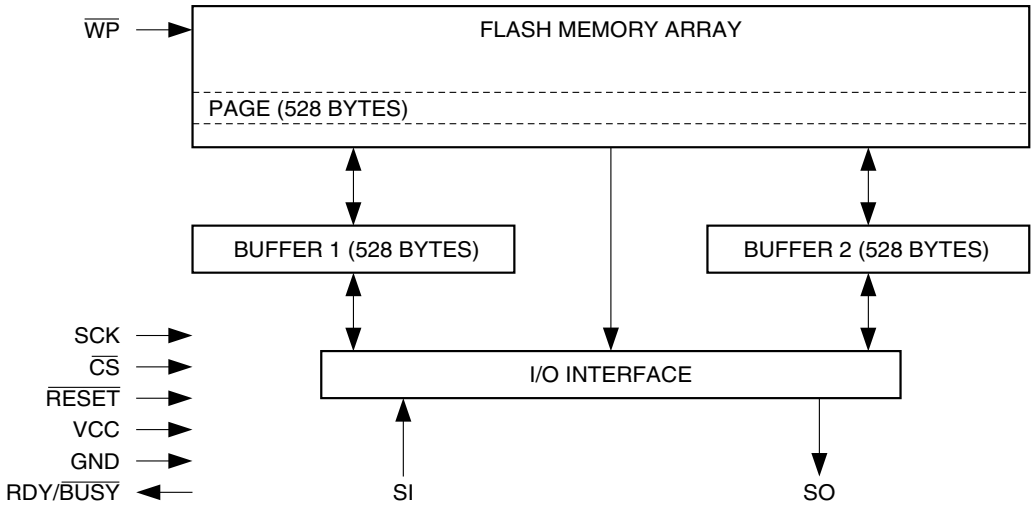


Figure 2-5. CASON – Top View through Package



Note: 1. See AT45DCB004C Datasheet

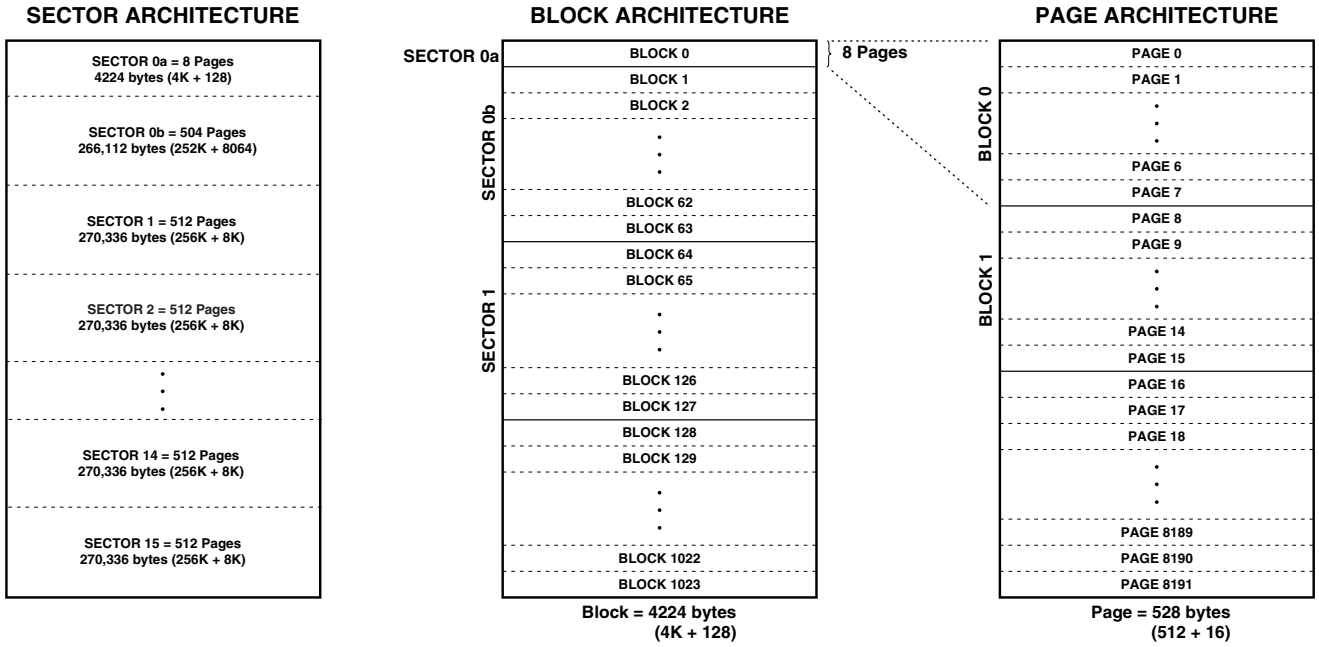
3. Block Diagram



4. Memory Array

To provide optimal flexibility, the memory array of the AT45DB321C is divided into three levels of granularity comprising of sectors, blocks, and pages. The “Memory Architecture Diagram” illustrates the breakdown of each level and details the number of pages per sector and block. All program operations to the DataFlash occur on a page by page basis. The erase operations can be performed at the block or page level.

Figure 4-1. Memory Architecture Diagram



5. Device Operation

The device operation is controlled by instructions from the host processor. The list of instructions and their associated opcodes are contained in Tables 1 through 4. A valid instruction starts with the falling edge of $\overline{CS}$ followed by the appropriate 8-bit opcode and the desired buffer or main memory address location. While the $\overline{CS}$ pin is low, toggling the SCK pin controls the loading of the opcode and the desired buffer or main memory address location through the SI (serial input) pin. All instructions, addresses, and data are transferred with the most significant bit (MSB) first.

Buffer addressing is referenced in the datasheet using the terminology BFA9-BFA0 to denote the 10 address bits required to designate a byte address within a buffer. Main memory addressing is referenced using the terminology PA12-PA0 and BA9-BA0, where PA12-PA0 denotes the 13 address bits required to designate a page address and BA9-BA0 denotes the 10 address bits required to designate a byte address within the page.

5.1 Read Commands

By specifying the appropriate opcode, data can be read from the main memory or from either one of the two SRAM data buffers. The DataFlash supports RapidS protocol for Mode 0 and Mode 3. Please refer to the “Detailed Bit-level Read Timing” diagrams in this datasheet for details on the clock cycle sequences for each mode.

5.1.1 Continuous Array Read

By supplying an initial starting address for the main memory array, the Continuous Array Read command can be utilized to sequentially read a continuous stream of data from the device by simply providing a clock signal; no additional addressing information or control signals need to be provided. The DataFlash incorporates an internal address counter that will automatically increment on every clock cycle, allowing one continuous read operation without the need of additional address sequences. To perform a continuous read, an opcode of E8H must be clocked into the device. The opcode is followed by three address bytes (which comprises 24-bit page and byte address sequence) and 32 don’t care clock cycles. The first bit of the 24-bit address sequence is reserved for upward and downward compatibility to larger and smaller density devices (see the notes under Section 13.6 on page 25. The next 13 bits (PA12-PA0) of the 24-bit address sequence specify which page of the main memory array to read, and the last 10 bits (BA9-BA0) of the 24-bit address sequence specify the starting byte address within the page. The 32 don’t care clock cycles that follow the four address bytes are needed to initialize the read operation. Following the don’t care clock cycles, additional clock pulses on the SCK pin will result in data being output on the SO (serial output) pin.

The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the don’t care bytes, and the reading of data. When the end of a page in main memory is reached during a Continuous Array Read, the device will continue reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device will continue reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays will be incurred when wrapping around from the end of the array to the beginning of the array.

A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tristate the output pin (SO). The maximum SCK frequency allowable for the Continuous Array Read is defined by the f_{CAR} specification. The Continuous Array Read bypasses both data buffers and leaves the contents of the buffers unchanged.

5.1.2 Main Memory Page Read

A main memory page read allows the user to read data directly from any one of the 8192 pages in the main memory, bypassing both of the data buffers and leaving the contents of the buffers unchanged. To start a page read, an opcode of D2H must be clocked into the device. The opcode is followed by three address bytes (which comprise 24-bit page and byte address sequence) and 32 don't care clock cycles. The first bit of the 24-bit address sequence is a reserved bit, the next 13 bits (PA12-PA0) of the 24-bit address sequence specify the page in main memory to be read, and the last 10 bits (BA9-BA0) of the 24-bit address sequence specify the starting byte address within that page. The 32 don't care clock cycles that follow the three address bytes are sent to initialize the read operation. Following the don't care bytes, additional pulses on SCK result in data being output on the SO (serial output) pin. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the don't care bytes, and the reading of data. When the end of a page in main memory is reached, the device will continue reading back at the beginning of the same page. A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tristate the output pin (SO). The maximum SCK frequency allowable for the Main Memory Page Read is defined by the f_{SCK} specification. The Main Memory Page Read bypasses both data buffers and leaves the contents of the buffers unchanged.

5.1.3 Buffer Read

Data can be read from either one of the two buffers, using different opcodes to specify which buffer to read from. An opcode of D4H is used to read data from buffer 1, and an opcode of D6H is used to read data from buffer 2. To perform a buffer read, the opcode must be clocked into the device followed by three address bytes comprised of 14 don't care bits and 10 buffer address bits (BFA9-BFA0). Following the three address bytes, an additional don't care byte must be clocked in to initialize the read operation. Since the buffer size is 528 bytes, 10 buffer address bits are required to specify the first byte of data to be read from the buffer. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the don't care bytes, and the reading of data. When the end of a buffer is reached, the device will continue reading back at the beginning of the buffer. A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tristate the output pin (SO).

5.2 Program and Erase Commands

5.2.1 Buffer Write

Data can be clocked in from the SI pin into either buffer 1 or buffer 2. To load data into either buffer, a 1-byte opcode, 84H for buffer 1 or 87H for buffer 2, must be clocked into the device, followed by three address bytes comprised of 14 don't care bits and 10 buffer address bits (BFA9-BFA0). The 10 buffer address bits specify the first byte in the buffer to be written. After the last address byte has been clocked into the device, data can then be clocked in on subsequent clock cycles. If the end of the data buffer is reached, the device will wrap around back to the beginning of the buffer. Data will continue to be loaded into the buffer until a low-to-high transition is detected on the $\overline{CS}$ pin.

5.2.2 Buffer to Main Memory Page Program with Built-in Erase:

Data written into either buffer 1 or buffer 2 can be programmed into the main memory. To start the operation, an 8-bit opcode, 83H for buffer 1 or 86H for buffer 2, must be clocked into the device followed by three address bytes consisting of one reserved bit, 13 page address bits (PA12-PA0) that specify the page in the main memory to be written and 10 don't care bits. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will first erase the selected page in main memory (the erased state is a logic 1) and then program the data stored in the buffer into the specified page in main memory. Both the erase and the programming of the page are internally self-timed and should take place in a maximum time of t_{EP}. During this time, the status register and the RDY/$\overline{BUSY}$ pin will indicate that the part is busy.

5.2.3 Buffer to Main Memory Page Program without Built-in Erase

A previously-erased page within main memory can be programmed with the contents of either buffer 1 or buffer 2. To start the operation, an 8-bit opcode, 88H for buffer 1 or 89H for buffer 2, must be clocked into the device followed by three address bytes consisting of one reserved bit, 13 page address bits (PA12-PA0) that specify the page in the main memory to be written and 10 don't care bits. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will program the data stored in the buffer into the specified page in the main memory. It is necessary that the page in main memory that is being programmed has been previously erased using one of the erase commands (Page Erase or Block Erase). The programming of the page is internally self-timed and should take place in a maximum time of t_P. During this time, the status register and the RDY/$\overline{BUSY}$ pin will indicate that the part is busy.

5.2.4 Page Erase

The Page Erase command can be used to individually erase any page in the main memory array allowing the Buffer to Main Memory Page Program without Built-in Erase command to be utilized at a later time. To perform a page erase, an opcode of 81H must be loaded into the device, followed by three address bytes comprised of one reserved bit, 13 page address bits (PA12-PA0) that specify the page in the main memory to be erased and 10 don't care bits. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will erase the selected page (the erased state is a logic 1). The erase operation is internally self-timed and should take place in a maximum time of t_{PE}. During this time, the status register and the RDY/$\overline{BUSY}$ pin will indicate that the part is busy.

5.2.5 Block Erase

A block of eight pages can be erased at one time. This command is useful when large amounts of data has to be written into the device. This will avoid using multiple Page Erase Commands. To perform a block erase, an opcode of 50H must be loaded into the device, followed by three address bytes comprised of one reserved bit, 10 page address bits (PA12-PA3) and 13 don't care bits. The 10 page address bits are used to specify which block of eight pages is to be erased. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will erase the selected block of eight pages. The erase operation is internally self-timed and should take place in a maximum time of t_{BE}. During this time, the status register and the RDY/$\overline{BUSY}$ pin will indicate that the part is busy.

Table 5-1. Block Erase Addressing

PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	Block
0	0	0	0	0	0	0	0	0	0	X	X	X	0
0	0	0	0	0	0	0	0	0	1	X	X	X	1
0	0	0	0	0	0	0	0	1	0	X	X	X	2
0	0	0	0	0	0	0	0	1	1	X	X	X	3
•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	0	0	X	X	X	1020
1	1	1	1	1	1	1	1	0	1	X	X	X	1021
1	1	1	1	1	1	1	1	1	0	X	X	X	1022
1	1	1	1	1	1	1	1	1	1	X	X	X	1023

5.2.6 Main Memory Page Program Through Buffer

This operation is a combination of the Buffer Write and Buffer to Main Memory Page Program with Built-in Erase operations. Data is first clocked into buffer 1 or buffer 2 from the input pin (SI) and then programmed into a specified page in the main memory. To initiate the operation, an 8-bit opcode, 82H for buffer 1 or 85H for buffer 2, must first be clocked into the device, followed by three address bytes. The address bytes are comprised of one reserved bit, 13 page address bits (PA12-PA0) that select the page in the main memory where data is to be written, and 10 buffer address bits (BFA9-BFA0) that select the first byte in the buffer to be written. After all address bytes are clocked in, the part will take data from the input pins and store it in the specified data buffer. If the end of the buffer is reached, the device will wrap around back to the beginning of the buffer. When there is a low-to-high transition on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into that memory page. Both the erase and the programming of the page are internally self-timed and should take place in a maximum time of t_{EP}. During this time, the status register and the RDY/$\overline{BUSY}$ pin will indicate that the part is busy.

5.3 Additional Commands

5.3.1 Main Memory Page to Buffer Transfer

A page of data can be transferred from the main memory to either buffer 1 or buffer 2. To start the operation, a 1-byte opcode, 53H for buffer 1 and 55H for buffer 2, must be clocked into the device, followed by three address bytes comprised of one reserved bit, 13 page address bits (PA12- PA0), which specify the page in main memory that is to be transferred, and 10 don't care bits. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode and the address bytes from the input pin (SI). The transfer of the page of data from the main memory to the buffer will begin when the $\overline{CS}$ pin transitions from a low to a high state. During the transfer of a page of data (t_{XFR}), the status register can be read to determine whether the transfer has been completed or not.

5.3.2 Main Memory Page to Buffer Compare

A page of data in main memory can be compared to the data in buffer 1 or buffer 2. To initiate the operation, an 8-bit opcode, 60H for buffer 1 and 61H for buffer 2, must be followed by 24 address bits consisting of one reserved bit, 13 address bits (PA12 - PA0) which specify the page in the main memory that is to be compared to the buffer, and ten don't care bits. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode, the address bits, and the don't care bits from the SI pin. On the low-to-high transition of the $\overline{CS}$ pin, the 528 bytes in the selected main memory page will be compared with the 528 bytes in buffer 1 or buffer 2. During this time (t_{XFR}), the status register will indicate that the part is busy. On completion of the compare operation, bit 6 of the status register is updated with the result of the compare.

5.3.3 Auto Page Rewrite

This mode is only needed if multiple bytes within a page or multiple pages of data are modified in a random fashion. This mode is a combination of two operations: Main Memory Page to Buffer Transfer and Buffer to Main Memory Page Program with Built-in Erase. A page of data is first transferred from the main memory to buffer 1 or buffer 2, and then the same data (from buffer 1 or buffer 2) is programmed back into its original page of main memory. To start the rewrite operation, a 1-byte opcode, 58H for buffer 1 or 59H for buffer 2, must be clocked into the device, followed by three address bytes comprised of one reserved bit, 13 page address bits (PA12-PA0) that specify the page in main memory to be rewritten and 10 don't care bits. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will first transfer data from the page in main memory to a buffer and then program the data from the buffer back into same page of main memory. The operation is internally self-timed and should take place in a maximum time of t_{EP}. During this time, the status register and the RDY/$\overline{BUSY}$ pin will indicate that the part is busy.

If a sector is programmed or reprogrammed sequentially page by page, then the programming algorithm shown in Figure 15-1 on page 31 is recommended. Otherwise, if multiple bytes in a page or several pages are programmed randomly in a sector, then the programming algorithm shown in Figure 15-2 on page 32 is recommended. Each page within a sector must be updated/rewritten at least once within every 10,000 cumulative page erase/program operations in that sector.

5.3.4 Status Register Read

The status register can be used to determine the device's ready/busy status, the result of a Main Memory Page to Buffer Compare operation, or whether the sector protection has been enabled. To read the status register, an opcode of D7H must be loaded into the device. After the opcode and optional dummy byte is clocked in, the 1-byte status register will be clocked out on the output pin (SO), starting with the next clock cycle. For applications over 25 MHz, the opcode must be always followed with a dummy (don't care) byte. The data in the status register, starting with the MSB (bit 7), will be clocked out on the SO pin during the next eight clock cycles.

The most-significant bits of the status register will contain device information, while the remaining least-significant bit is reversed for future use and will have undefined value. After the one byte of the status register has been clocked out, the sequence will repeat itself (as long as $\overline{CS}$ remains low and SCK is being toggled). The data in the status register is constantly updated, so each repeating sequence will output new data.

Ready/busy status is indicated using bit 7 of the status register. If bit 7 is a 1, then the device is not busy and is ready to accept the next command. If bit 7 is a 0, then the device is in a busy state. There are many operations that can cause the device to be in a busy state: Main Memory Page to Buffer Transfer, Buffer to Main Memory Page Program with Built-in Erase, Buffer to

Main Memory Page Program without Built-in Erase, Page Erase, Block Erase, Main Memory Page Program, and Auto Page Rewrite.

Bit 1 in the Status Register is used to provide information to the user whether or not the sector protection has been enabled or disabled, either by software-controlled method or hardware-controlled method. A logic 1 indicates that sector protection has been enabled and logic 0 indicates that sector protection has been disabled.

The device density is indicated using bits 5, 4, 3, and 2 of the status register. For the AT45DB321C, the four bits are 1,1, 0, 1. The decimal value of these four binary bits does not equate to the device density; the four bits represent a combinational code relating to differing densities of DataFlash devices. The device density is not the same as the density code indicated in the JEDEC device ID information. The device density is provided only for backward compatibility.

The result of the most recent Main Memory Page to Buffer Compare operation is indicated using bit 6 of the status register. If bit 6 is a 0, then the data in the main memory page matches the data in the buffer. If bit 6 is a 1, then at least one bit of the data in the main memory page does not match the data in the buffer.

Table 5-2. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RDY/$\overline{\text{BUSY}}$	COMP	1	1	0	1	Protect	X

6. Sector Protection

Two protection methods, hardware and software controlled, are provided. The selection of which sectors to be protected/unprotected from program and erase operations is defined in the Sector Protection Register.

6.1 Software Sector Protection

Sectors specified for protection in the Sector Protection Register can be protected from program and erase operations by issuing the Enable Sector Protection command. To enable the sector protection using the software controlled method, the $\overline{\text{CS}}$ pin must first be asserted as it would be with any other command. Once the $\overline{\text{CS}}$ pin has been asserted, the appropriate 4-byte command sequence must be clocked in via the input pin (SI). After the last bit of the command sequence has been clocked in, the $\overline{\text{CS}}$ pin must be deasserted after which the sector protection will be enabled.

Command	Byte 1	Byte 2	Byte 3	Byte 4
Enable Sector Protection	3DH	2AH	7FH	A9H
Disable Sector Protection	3DH	2AH	7FH	9AH
Read Sector Protection Register	32H	00H	00H	00H

To disable the sector protection using the software controlled method, the $\overline{\text{CS}}$ pin must first be asserted as it would be with any other command. Once the $\overline{\text{CS}}$ pin has been asserted, the appropriate 4-byte sequence for the Disable Sector Protection command must be clocked in via the input pin (SI). After the last bit of the command sequence has been clocked in, the $\overline{\text{CS}}$ pin must be deasserted after which the sector protection will be disabled. The Disable Sector Protection command is ignored while the $\overline{\text{WP}}$ pin is asserted.

Software Sector Protection is useful in applications in which the $\overline{WP}$ pin is not or cannot be controlled by a host processor. In such instances, the $\overline{WP}$ pin may be left floating (the $\overline{WP}$ pin is pulled high internally) and sector protection can be controlled using the software commands.

If the device is power cycled, then the Software Sector Protection will be disabled. Once the device is powered up, the Enable Sector Protection command should be reissued if sector protection is desired and if the $\overline{WP}$ pin is not used. The $\overline{RESET}$ pin has no effect on the Software Sector Protection.

6.2 Hardware Sector Protection

Sectors specified for protection in Sector Protection Register can be protected from program and erase operations by utilizing the Write Protection ($\overline{WP}$) pin. The protection can be enabled by asserting the $\overline{WP}$ pin and keeping the pin in its asserted state. Any sector specified for protection cannot be erased or reprogrammed as long as the $\overline{WP}$ pin is asserted. The protection can be disabled by deasserting the $\overline{WP}$ pin high. A filter is provided on the $\overline{WP}$ pin to help protect against spurious noise on the $\overline{WP}$ pin. Hardware Sector Protection will provide continuous protection, based on the contents of the Sector Protection Register, in an application where $\overline{WP}$ is always driven low. Please read "Write Protect (WP)" on page 15 for more information.

6.3 Sector Protection Register

Sector Protection Register is a nonvolatile register that contains 16 bytes of data, as shown below:

Sector Number	0 (0a, 0b)	1 to 15
Protected	See Below	FFH
Unprotected		00H

Table 6-1. Sector 0 (0a, 0b):

	0a (Page 0-7)	0b (Page 8-511)			
	Bit 6, 7	Bit 4, 5	Bit 2, 3	Bit 0, 1	Data Value
Sectors 0a, 0b Unprotected	00	00	00	00	00H
Protect Sector 0a (Page 0-7)	11	00	00	00	C0H
Protect Sector 0b (Page 8-511)	00	11	11	00	3CH
Protect Sectors 0a, 0b (Page 0-511)	11	11	11	00	FCH

Note: 1. Default value for devices shipped from Atmel is 00H.

6.3.1 Erasing the Sector Protection Register

To erase the Sector Protection Register, the $\overline{CS}$ pin must first be asserted. Once the $\overline{CS}$ pin has been asserted, the 4-byte erase command sequence must be clocked in via the SI (serial input) pin. After the last bit of the command sequence has been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed erase cycle (t_{PE}). The Ready/Busy status will indicate that the device is busy during the erase cycle. The erased state of each bit (of a byte) in the Sector Protection Register indicates that the corresponding sector is flagged for protection. The $\overline{RESET}$ pin is disabled during this erase cycle to prevent incomplete erasure of the Sector Protection Register.

Command	Byte 1	Byte 2	Byte 3	Byte 4
Erase Sector Protection Register	3DH	2AH	7FH	CFH

6.3.2 Programming the Sector Protection Register

To program the Sector Protection Register, the $\overline{CS}$ pin must first be asserted. Once the $\overline{CS}$ pin has been asserted, the 4-byte command sequence must be clocked in via the SI (serial input) pin. After the last bit of the command sequence has been clocked in, the data for the contents of the Sector Protection Register must be clocked in. The first byte corresponds to sector 0 (0a, 0b), the second byte corresponds to Sector 1 and the last byte (byte 16) corresponds to Sector 15. After the last bit of data has been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed program cycle (t_P). The Ready/Busy status will indicate that the device is busy during the program cycle. The $\overline{RESET}$ pin is disabled during this program cycle to prevent incomplete programming of the sector protection register.

Command	Byte 1	Byte 2	Byte 3	Byte 4
Program Sector Protection Register	3DH	2AH	7FH	FCH

6.3.3 Reading the Sector Protection Register

To read the Sector Protection Register, the $\overline{CS}$ pin must first be asserted. Once the $\overline{CS}$ pin has been asserted, a 4-byte command sequence 32H, 00H, 00H, 00H and 32 don't care clock cycles must be clocked in via the SI (serial input) pin. The 32 don't care clock cycles are required to initialize the read operation. After the 32 don't care clock cycles, any additional clock pulses on the SCK pin will result in data being output on the SO (serial output) pin. The read will begin with Byte_1 of the Sector Protection Register for Sector_0, followed with Byte_2 for Sector_1. The read operation will continue until Byte_16 for Sector_15 is read. Once the last byte is read a low-to-high transition on the $\overline{CS}$ pin is required to terminate the read operation.

Command	Byte 1	Byte 2	Byte 3	Byte 4
Read Sector Protection Register	32H	00H	00H	00H

Note: Next generation devices of the "D" family will not require the 32 don't care clock cycles.

6.3.4 Various Aspects About the Sector Protection Register

Due to the sharing of the internal circuitry, the contents of the buffer 1 will get modified during the erase and programming of Sector Protection Register. If the device is powered down during erasing or programming the sector protection register, then the contents of the Sector Protection Register cannot be guaranteed. The Sector Protection Register can be erased or reprogrammed with the sector protection enabled or disabled. Being able to reprogram the Sector Protection Register with the sector protection enabled allows the user to temporarily disable the sector protection to an individual sector rather than disabling the sector protection completely.

The Sector Protection Register is subject to the same endurance characteristics as the main memory array. Users are encouraged to carefully evaluate the number of times the Sector Protection Register will be modified during the course of the applications' life cycle. If the application requires that the Sector Protection Register be modified more than the specified endurance of the DataFlash because the application needs to temporarily unprotect individual sectors (sector protection remains enabled while the Sector Protection Register is reprogrammed), then the application will need to limit this practice. Instead, a combination of temporarily unprotecting individual sectors along with disabling sector protection completely will need to be implemented by the application to ensure that the endurance limits of the device are not exceeded.

7. Manufacturer and Device ID Read

This instruction conforms to the JEDEC standard and allows the user to read the Manufacturer ID, Device ID, and Extended Device Information. A 1-byte opcode, 9FH, must be clocked into the device while the $\overline{CS}$ pin is low. After the opcode is clocked in, the Manufacturer ID, 2 bytes of Device ID and Extended Device Information will be clocked out on the SO pin. The fourth byte of the sequence output is the Extended Device Information String Length byte. This byte is used to signify how many bytes of Extended Device Information will be output.

7.1 Manufacturer and Device ID Information

7.1.1 Byte 1 – Manufacturer ID

Hex Value	JEDEC Assigned Code							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1FH	0	0	0	1	1	1	1	1

Manufacturer ID	1FH = Atmel

7.1.2 Byte 2 – Device ID (Part 1)

Hex Value	Family Code			Density Code				
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
27H	0	0	1	0	0	1	1	1

Family Code	001 = DataFlash
Density Code	00111 = 32-Mbit

7.1.3 Byte 3 – Device ID (Part 2)

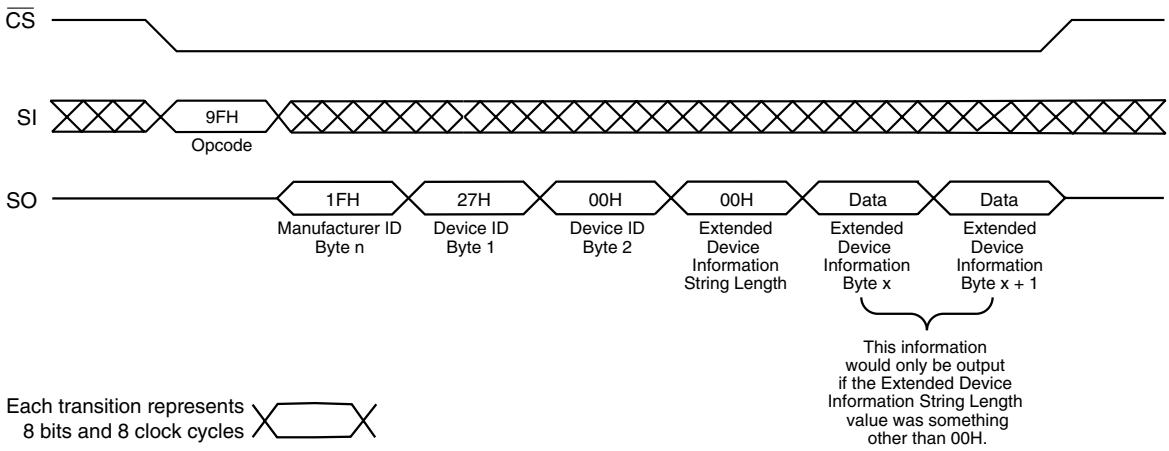
Hex Value	MLC Code			Product Version Code				
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	0	0	0	0	0	0	0	0

MLC Code	000 = 1-bit/Cell Technology
Product Version	00000 = Initial Version

7.1.4 Byte 4 – Extended Device Information String Length

Hex Value	Byte Count							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	0	0	0	0	0	0	0	0

Byte Count	00H = 0 Bytes of Information



Note: Based on JEDEC publication 106 (JEP106), Manufacturer ID data can be comprised of any number of bytes. Some manufacturers may have Manufacturer ID codes that are two, three or even four bytes long with the first byte(s) in the sequence being 7FH. A system should detect code 7FH as a “Continuation Code” and continue to read Manufacturer ID bytes. The first non-7FH byte would signify the last byte of Manufacturer ID data. For Atmel (and some other manufacturers), the Manufacturer ID data is comprised of only one byte.

7.2 Security Register

The AT45DB321C contains a specialized register that can be used for security purposes in system design. The Security Register is a unique 128-byte register that is divided into two portions. The first 64 bytes (byte 0 to byte 63) of this page are allocated as a one-time user programmable space. Once these 64 bytes have been programmed, they should not be reprogrammed. The remaining 64 bytes of this page (byte 64 to byte 127) are factory programmed by Atmel and will contain a unique number for each device. The factory programmed data is fixed and cannot be changed.

The Security Register can be read by clocking in a 4-byte sequence 77H, 00H, 00H, 00H to the device followed by 32 don't care clock cycles. See the opcode Table 9-4 on page 20.

Note: Next generation devices of the "D" family will not require the 32 don't care clock cycles.

To program the first 64 bytes of the Security Register, a two step sequence must be used. The first step requires that the user loads the desired data into Buffer 1 by using the Buffer 1 Write operation (opcode 84H – "Buffer Write" on page 5). The user should specify the starting buffer address as location zero and should write a full 64 bytes of information into the buffer. Otherwise, the first 64 bytes of the buffer may contain data that was previously stored in the buffer. It is not necessary to fill the remaining 464 bytes (byte locations 64 through 527) of the buffer with data. After the Buffer 1 Write operation has been completed, the Security Register can be subsequently programmed by reselecting the device and clocking in opcode 9AH into the device followed by three don't care bytes (24 clock cycles). After the final don't care clock cycle has been completed, a low-to-high transition on the $\overline{CS}$ pin will cause the device to initiate an internally self-timed program operation in which the contents of Buffer 1 will be programmed into the Security Register. Only the first 64 bytes of data in Buffer 1 will be programmed into the Security Register; the remaining 464 bytes of the buffer will be ignored. The Security Register program operation should take place in a maximum time of t_P.

7.3 Operation Mode Summary

The modes described can be separated into two groups – modes that make use of the Flash memory array (Group A) and modes that do not make use of the Flash memory array (Group B).

Group A modes consist of:

1. Main Memory Page Read
2. Continuous Array Read
3. Main Memory Page to Buffer 1 (or 2) Transfer
4. Main Memory Page to Buffer 1 (or 2) Compare
5. Buffer 1 (or 2) to Main Memory Page Program with Built-in Erase
6. Buffer 1 (or 2) to Main Memory Page Program without Built-in Erase
7. Main Memory Page Program through Buffer 1 (or 2)
8. Page Erase
9. Block Erase
10. Auto Page Rewrite

Group B modes consist of:

1. Buffer 1 (or 2) Read
2. Buffer 1 (or 2) Write
3. Status Register Read
4. Manufacturer and Device ID Read

If a Group A mode is in progress (not fully completed), then another mode in Group A should not be started. However, during this time in which a Group A mode is in progress, modes in Group B can be started, except the first two Group A commands (Memory Array Read Commands).

This gives the DataFlash the ability to virtually accommodate a continuous data stream. While data is being programmed into main memory from buffer 1, data can be loaded into buffer 2 (or vice versa). See application note AN-4 (“Using Atmel’s Serial DataFlash”) for more details.

7.4 Pin Descriptions

7.4.1 Serial Input (SI)

The SI pin is an input-only pin and is used to shift data serially into the device. The SI pin is used for all data input, including opcodes and address sequences.

7.4.2 Serial Output (SO)

The SO pin is an output-only pin and is used to shift data serially out from the device.

7.4.3 Serial Clock (SCK)

The SCK pin is an input-only pin and is used to control the flow of data to and from the DataFlash. Data is always clocked into the device on the rising edge of SCK and clocked out of the device on the falling edge of SCK.

7.4.4 Chip Select ($\overline{CS}$)

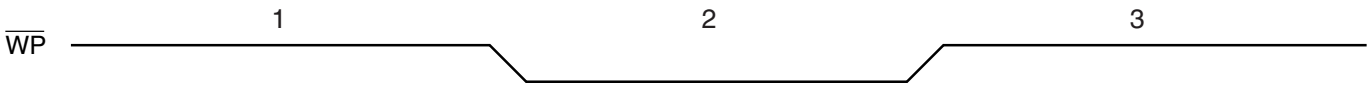
The DataFlash is selected when the $\overline{CS}$ pin is low. When the device is not selected, data will not be accepted on the input pin (SI), and the output pin (SO) will remain in a high impedance state. A high-to-low transition on the $\overline{CS}$ pin is required to start an operation, and a low-to-high transition on the $\overline{CS}$ pin is required to end an operation or to start an internally self-timed operation.

7.4.5 Write Protect ($\overline{WP}$)

The $\overline{WP}$ pin is used to control the Hardware Sector Protection. Hardware Sector Protection is enabled by asserting the $\overline{WP}$ pin and keeping the pin in it’s asserted state. Disabling Hardware Sector Protection is accomplished by simply deasserting the $\overline{WP}$ pin. The $\overline{WP}$ pin will override the software controlled sector protection method but only for protecting the sectors. For example, if the sectors were not previously protected by the Enable Sector Protection command, then simply asserting the $\overline{WP}$ pin for the minimum specified time (t_{WPE}) would enable the sector protection. When the $\overline{WP}$ pin is deasserted; however, the sector protection would no longer be enabled as long as the Enable Sector Protection command was not issued while the $\overline{WP}$ pin was asserted. If the Enable Sector Protection command was issued before or while the $\overline{WP}$ pin was asserted, then simply deasserting the $\overline{WP}$ pin would not disable the sector protection. In this case, the Disable Sector Protection command would need to be issued while the $\overline{WP}$ pin is deasserted to disable the sector protection. The Disable Sector Protection command is also ignored whenever the $\overline{WP}$ pin is asserted.

To ensure backwards compatibility with previous generations of DataFlash, the function of the $\overline{WP}$ pin has not changed. Therefore, when the $\overline{WP}$ pin is asserted, certain sectors in the memory array will be protected, and when the $\overline{WP}$ pin is deasserted, the memory array will be unprotected provided the Enable Sector Protection command hasn’t been issued. New devices are shipped from Atmel with the contents of the Sector Protection Register pre-programmed with “00H” (unprotect). The user can reprogram the Sector Protection Register to change which sectors will be protected by the $\overline{WP}$ pin.

The table below details the sector protection status for various scenarios of the $\overline{WP}$ pin, the Enable Sector Protection command, and the Disable Sector Protection command.



Time Period	$\overline{WP}$ Pin	Enable Sector Protection Command	Disable Sector Protection Command	Sector Protection Status
1	High	Command Not Issued Previously	x	Disabled
	High	Command Issued	–	Enabled
	High	–	Command Issued	Disabled
2	Low	x	x	Enabled
3	High	Command Issued during Period 1 or 2	Not Issued Yet	Enabled
	High	–	Command Issued	Disabled
	High	Issue Command	–	Enabled

7.4.6 $\overline{RESET}$

A low state on the reset pin ($\overline{RESET}$) will terminate the operation in progress and reset the internal state machine to an idle state. The device will remain in the reset condition as long as a low level is present on the $\overline{RESET}$ pin. Normal operation can resume once the $\overline{RESET}$ pin is brought back to a high level.

The device incorporates an internal power-on reset circuit, so there are no restrictions on the $\overline{RESET}$ pin during power-on sequences. The $\overline{RESET}$ pin is also internally pulled high; therefore, in low pin count applications, connection of the $\overline{RESET}$ pin is not necessary if this pin and feature will not be utilized. However, it is recommended that the $\overline{RESET}$ pin be driven high externally whenever possible.

7.4.7 READY/$\overline{BUSY}$

This open drain output pin will be driven low when the device is busy in an internally self-timed operation. This pin, which is normally in a high state (through an external pull-up resistor), will be pulled low during programming/erase operations, and page-to-buffer transfers.

The busy status indicates that the Flash memory array and one of the buffers cannot be accessed; read and write operations to the other buffer can still be performed. During Page Erase and Block Erase, read and write operations can be performed to both buffers.

8. Power-on/Reset State

When power is first applied to the device, or when recovering from a reset condition, the device will default to Mode 3. In addition, the output pin (SO) will be in a high impedance state, and a high-to-low transition on the $\overline{CS}$ pin will be required to start a valid instruction. The mode (Mode 3 or Mode 0) will be automatically selected on every falling edge of $\overline{CS}$ by sampling the inactive clock state. After power is applied and V_{CC} is at the minimum datasheet value, the system should wait 20 ms before an operational mode (DataFlash) is started.

9. System Considerations

The RapidS serial interface is controlled by the serial clock SCK, serial input SI and chip select $\overline{CS}$ pins. These signals must rise and fall monotonically and be free from noise. Excessive noise or ringing on these pins can be misinterpreted as multiple edges and cause improper operation of the device. The PC board traces must be kept to a minimum distance or appropriately terminated to ensure proper operation. If necessary, decoupling capacitors can be added on these pins to provide filtering against noise glitches.

As system complexity continues to increase, voltage regulation is becoming more important. A key element of any voltage regulation scheme is its current sourcing capability. Like all Flash memories, the peak current for DataFlash occur during the programming and erase operation. The regulator needs to supply this peak current requirement. An under specified regulator can cause current starvation. Besides increasing system noise, current starvation during programming or erase can lead to improper operation and possible data corruption.

For applications that require random modifications of data within a sector, please refer to “Auto Page Rewrite” on page 8.

Atmel C generation DataFlash utilizes a sophisticated adaptive algorithm during erase and programming to maximize the endurance over the life of the device. The algorithm uses a verification mechanism to check if the memory cells have been erased or programmed successfully. If the memory cells were not erased or programmed completely, the algorithm erases or programs the memory cells again. The process will continue until the device is erased or programmed successfully.

In order to optimize the erase and programming time, fixed timing should not be used. Instead, the RDY/$\overline{BUSY}$ bit of the status register or the RDY/$\overline{BUSY}$ pin should be monitored.

Table 9-1. Read Commands

Command	SCK Mode	Opcode
Continuous Array Read	RapidS Mode 0 or 3	E8H
	Inactive Clock Polarity Low or High	68H
Main Memory Page Read	RapidS Mode 0 or 3	D2H
	Inactive Clock Polarity Low or High	52H
Buffer 1 Read	RapidS Mode 0 or 3	D4H
	Inactive Clock Polarity Low or High	54H
Buffer 2 Read	RapidS Mode 0 or 3	D6H
	Inactive Clock Polarity Low or High	56H
Status Register Read	RapidS Mode 0 or 3	D7H
	Inactive Clock Polarity Low or High	57H
Manufacturer and Device ID	RapidS Mode 0 or 3	9FH

Note: 1. Legacy Opcodes 52H, 54H, 56H, 57H, and 68H are still supported for reasons of backward compatibility only and are not recommended for new designs. The inactive clock polarity high or low modes will not be supported in the future products.

Table 9-2. Program and Erase Commands

Command	SCK Mode	Opcode
Buffer 1 Write	Mode 0, Mode 3	84H
Buffer 2 Write	Mode 0, Mode 3	87H
Buffer 1 to Main Memory Page Program with Built-in Erase	Mode 0, Mode 3	83H
Buffer 2 to Main Memory Page Program with Built-in Erase	Mode 0, Mode 3	86H
Buffer 1 to Main Memory Page Program without Built-in Erase	Mode 0, Mode 3	88H
Buffer 2 to Main Memory Page Program without Built-in Erase	Mode 0, Mode 3	89H
Page Erase	Mode 0, Mode 3	81H
Block Erase	Mode 0, Mode 3	50H
Main Memory Page Program Through Buffer 1	Mode 0, Mode 3	82H
Main Memory Page Program Through Buffer 2	Mode 0, Mode 3	85H

Table 9-3. Additional Commands

Command	SCK Mode	Opcode
Main Memory Page to Buffer 1 Transfer	Mode 0, Mode 3	53H
Main Memory Page to Buffer 2 Transfer	Mode 0, Mode 3	55H
Main Memory Page to Buffer 1 Compare	Mode 0, Mode 3	60H
Main Memory Page to Buffer 2 Compare	Mode 0, Mode 3	61H
Auto Page Rewrite Through Buffer 1[1]	Mode 0, Mode 3	58H
Auto Page Rewrite Through Buffer 2[1]	Mode 0, Mode 3	59H
Security Register Program[2]	Mode 0, Mode 3	9AH
Security Register Read	Mode 0, Mode 3	77H

Notes: 1. This command should be used for applications requiring a high number of random page writes within a sector. See "Auto Page Rewrite" on page 8.

2. The Security Register Program command utilizes data stored in Buffer 1. Therefore, this command must be used in conjunction with the Buffer 1 write command. See "Security Register" on page 14 for details.

Table 9-4. Detailed Bit-level Addressing Sequence

Opcode	Opcode	Address Byte								Address Byte								Address Byte								Additional Don't Care Bytes Required
		Reserved	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	BA9	BA8	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0	
50H	0 1 0 1 0 0 0 0	r	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	x	x	x	N/A
52H	0 1 0 1 0 0 1 0	r	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	4 Bytes
53H	0 1 0 1 0 0 1 1	r	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	N/A
54H	0 1 0 1 0 1 0 0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	B	1 Byte
55H	0 1 0 1 0 1 0 1	r	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	N/A
56H	0 1 0 1 0 1 1 0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	B	1 Byte
57H	0 1 0 1 0 1 1 1	N/A								N/A								N/A								N/A
58H	0 1 0 1 1 0 0 0	r	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	N/A
59H	0 1 0 1 1 0 0 1	r	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	N/A
60H	0 1 1 0 0 0 0 0	r	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	N/A
61H	0 1 1 0 0 0 0 1	r	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	N/A
68H	0 1 1 0 1 0 0 0	r	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	4 Bytes
77H	0 1 1 1 0 1 1 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4
81H	1 0 0 0 0 0 0 1	r	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	N/A
82H	1 0 0 0 0 0 1 0	r	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	N/A
83H	1 0 0 0 0 0 1 1	r	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	N/A
84H	1 0 0 0 0 1 0 0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	B	N/A
85H	1 0 0 0 0 1 0 1	r	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	N/A
86H	1 0 0 0 0 1 1 0	r	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	N/A
87H	1 0 0 0 0 1 1 1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	B	N/A
88H	1 0 0 0 1 0 0 0	r	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	N/A
89H	1 0 0 0 1 0 0 1	r	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	N/A
9AH	1 0 0 1 1 0 1 0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	N/A
9FH	1 0 0 1 1 1 1 1	N/A								N/A								N/A								N/A
D2H	1 1 0 1 0 0 1 0	r	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	4
D4H	1 1 0 1 0 1 0 0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	B	1
D6H	1 1 0 1 0 1 1 0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	B	1
D7H	1 1 0 1 0 1 1 1	N/A								N/A								N/A								1/0
E8H	1 1 1 0 1 0 0 0	r	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	4

Note: r = Reserved Bit, P = Page Address Bit, B = Byte/Buffer Address Bit, x = Don't Care

10. Electrical Specifications

Table 10-1. Absolute Maximum Ratings*

Temperature under Bias	-55° C to +125° C
Storage Temperature	-65° C to +150° C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 10-2. DC and AC Operating Range

		AT45DB321C
Operating Temperature (Case)	Com.	0° C to 70° C
	Ind.	-40° C to 85° C
V_{CC} Power Supply[1]		2.7V to 3.6V

Note: 1. After power is applied and V_{CC} is at the minimum specified datasheet value, the system should wait 20 ms before an operational mode is started.

Table 10-3. DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{SB}[1]	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		6	15	µA
I_{CC1}[2][3]	Active Current, Read Operation, Serial Interface	f = 20 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		10	15	mA
I_{CC2}	Active Current, Program Operation, Page Program	V_{CC} = 3.6V		35	50	mA
I_{CC3}	Active Current, Page Erase Operation	V_{CC} = 3.6V		30	40	mA
I_{CC4}	Active Current, Block Erase Operation	V_{CC} = 3.6V		30	40	mA
I_{LI}	Input Load Current	V_{IN} = CMOS levels			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = CMOS levels			1	µA
V_{IL}	Input Low Voltage				V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7			V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 2.7V			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CC} - 0.2V			V

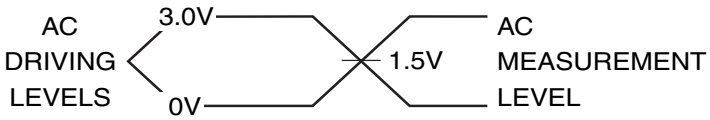
Notes: 1. I_{SB} maximum specification limit is tested at 3.3V and 70° C.
2. I_{CC1} during a buffer read is 30 mA maximum.
3. I_{CC1} changes typically by 300 µA per 1 MHz change in clock frequency.
4. All inputs are 5 volts tolerant.

Table 10-4. AC Characteristics – Serial Interface

Symbol	Parameter	Min	Typ	Max	Units
f_{SCK} (1)	SCK Frequency			40	MHz
f_{CAR} (1)	SCK Frequency for Continuous Array Read			40	MHz
t_{WH}	SCK High Time	10			ns
t_{WL}	SCK Low Time	10			ns
t_{CS}	Minimum $\overline{CS}$ High Time	250			ns
t_{CSS}	$\overline{CS}$ Setup Time	100			ns
t_{CSH}	$\overline{CS}$ Hold Time	250			ns
t_{CSB}	$\overline{CS}$ High to RDY/$\overline{BUSY}$ Low			150	ns
t_{SU}	Data In Setup Time	3			ns
t_H	Data In Hold Time	6			ns
t_{HO}	Output Hold Time	0			ns
t_{DIS}	Output Disable Time			10	ns
t_V	Output Valid			12	ns
t_{XFR}	Page to Buffer Transfer/Compare Time			350	µs
t_{EP} (2)(3)	Page Erase and Programming Time		16	50	ms
t_P (2)(3)	Page Programming Time		8	15	ms
t_{PE} (2)(3)	Page Erase Time		8	35	ms
t_{BE} (2)(3)	Block Erase Time		20	100	ms
t_{RST}	$\overline{RESET}$ Pulse Width	10			µs
t_{REC}	$\overline{RESET}$ Recovery Time			1	µs
t_{WPE}	$\overline{WP}$ Low to Protection Enabled	1			µs
t_{WPD}	$\overline{WP}$ High to Protection Disabled			1	µs

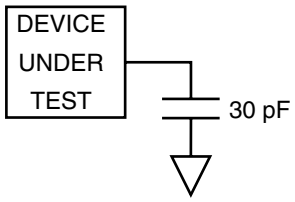
Note:
1. Maximum specified frequency for SPI compatibility is 33 MHz.
2. The device uses an adaptive algorithm during program and erase operations. Use the RDY/$\overline{BUSY}$ bit of the status register or the RDY/$\overline{BUSY}$ pin to determine whether the program or erase operation has completed. Fixed timing should not be used.
3. Value are based on device characterization, not 100% tested in production.

11. Input Test Waveforms and Measurement Levels



t_R, t_F < 2 ns (10% to 90%)

12. Output Test Load

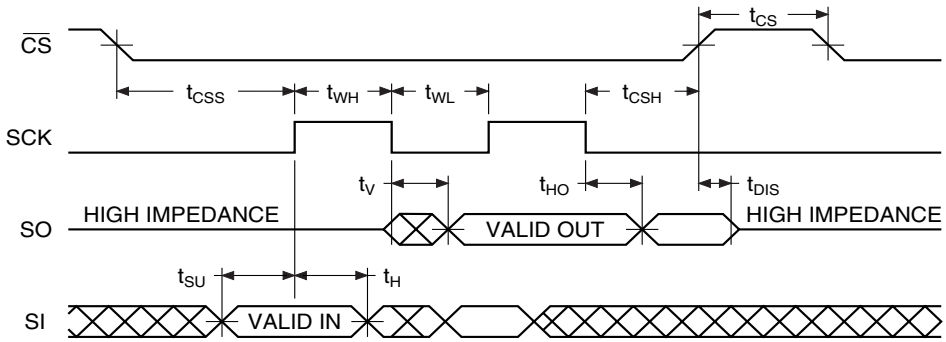


13. AC Waveforms

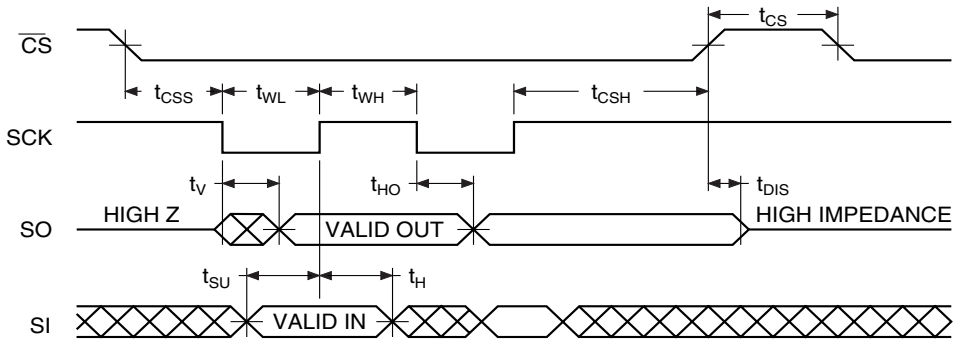
Four different timing waveforms are shown below. Waveform 1 shows the SCK signal being low when $\overline{CS}$ makes a high-to-low transition, and waveform 2 shows the SCK signal being high when $\overline{CS}$ makes a high-to-low transition. In both cases, output SO becomes valid while the SCK signal is still low (SCK low time is specified as t_{WL}). Timing waveforms 1 and 2 conform to RapidS serial interface but for frequencies up to 33 MHz and are compatible with SPI Mode 0 and SPI Mode 3 respectively. Waveforms 1 and 2 are also compatible with inactive clock polarity low and inactive clock polarity high, since the maximum specified frequency in that case is 33 MHz.

Waveform 3 and waveform 4 illustrate general timing diagram for RapidS serial interface. These are similar to waveform 1 and waveform 2, except that output SO is not restricted to become valid during the t_{WL} period. These timing waveforms are valid over the full frequency range (maximum frequency = 40 MHz) of the RapidS serial case.

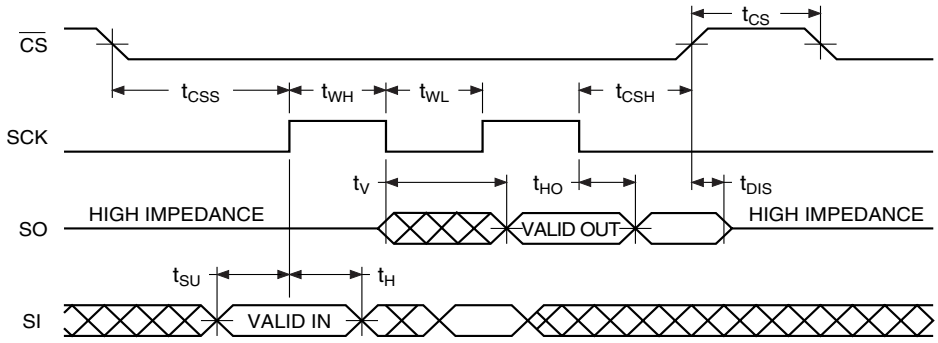
13.1 Waveform 1 – SPI Mode 0 Compatible (for Frequencies up to 33 MHz)



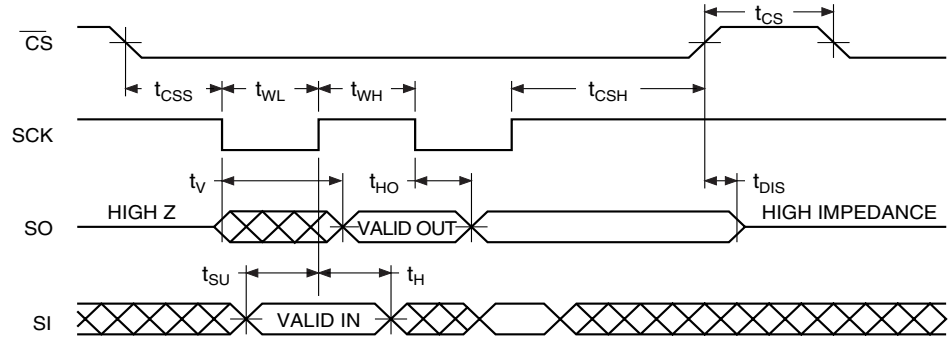
13.2 Waveform 2 – SPI Mode 3 Compatible (for Frequencies up to 33 MHz)



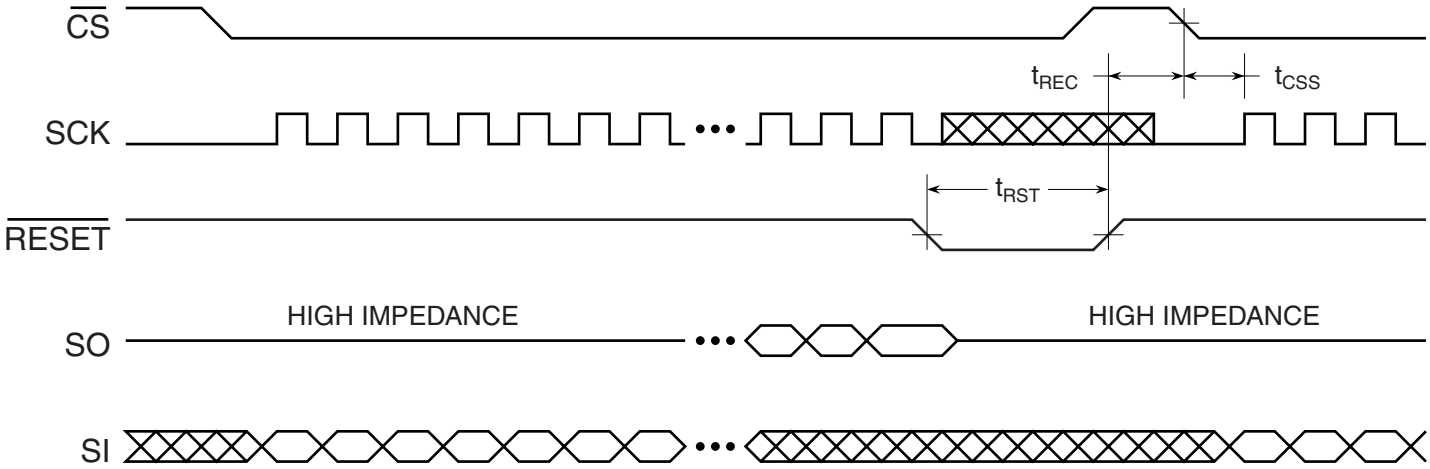
13.3 Waveform 3 – RapidS Mode 0 (for all Frequencies)



13.4 Waveform 4 – RapidS Mode 3 (for all Frequencies)

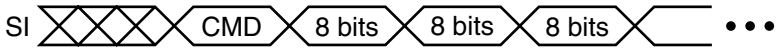


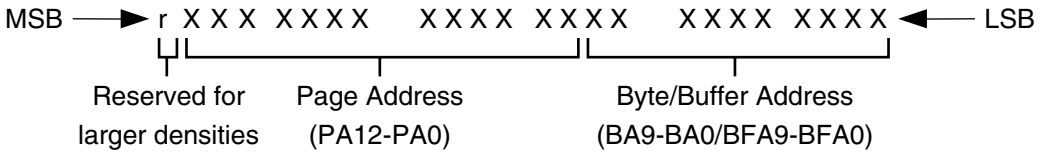
13.5 Reset Timing



Note: The $\overline{CS}$ signal should be in the high state before the $\overline{RESET}$ signal is deasserted.

13.6 Command Sequence for Read/Write Operations (except Status Register Read)

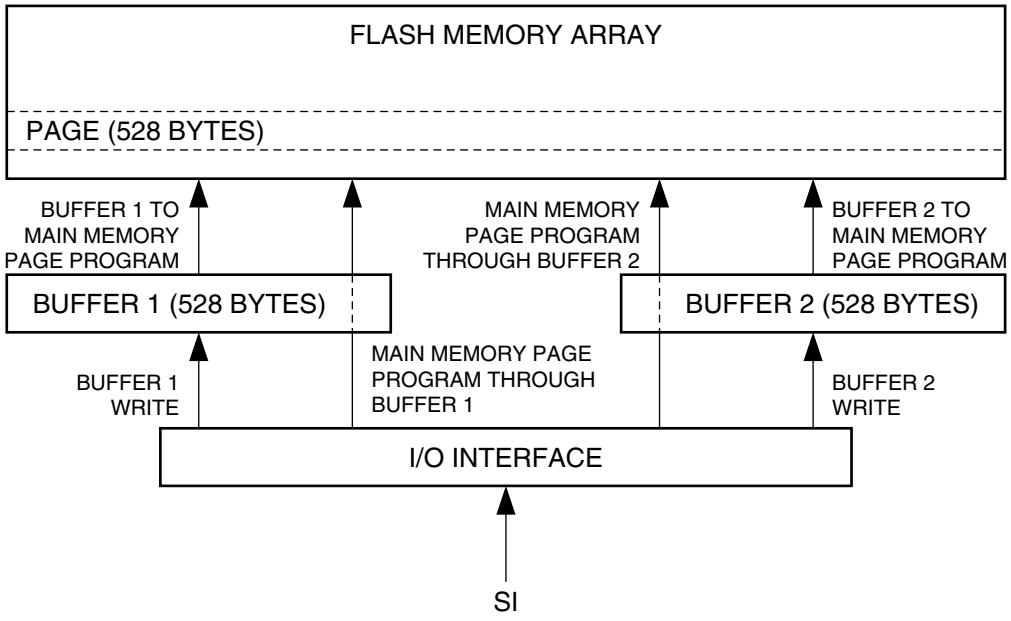




Notes:
1. "r" designates bits reserved for larger densities.
2. It is recommended that "r" be a logical "0" for densities of 32M bits or smaller.
3. For densities larger than 32M bits, the "r" bit becomes the most significant Page Address bit for the appropriate density.

14. Write Operations

The following block diagram and waveforms illustrate the various write sequences available.



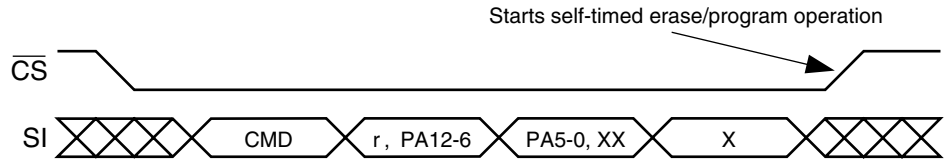
14.1 Main Memory Page Program through Buffers



14.2 Buffer Write



14.3 Buffer to Main Memory Page Program (Data from Buffer Programmed into Flash Page)



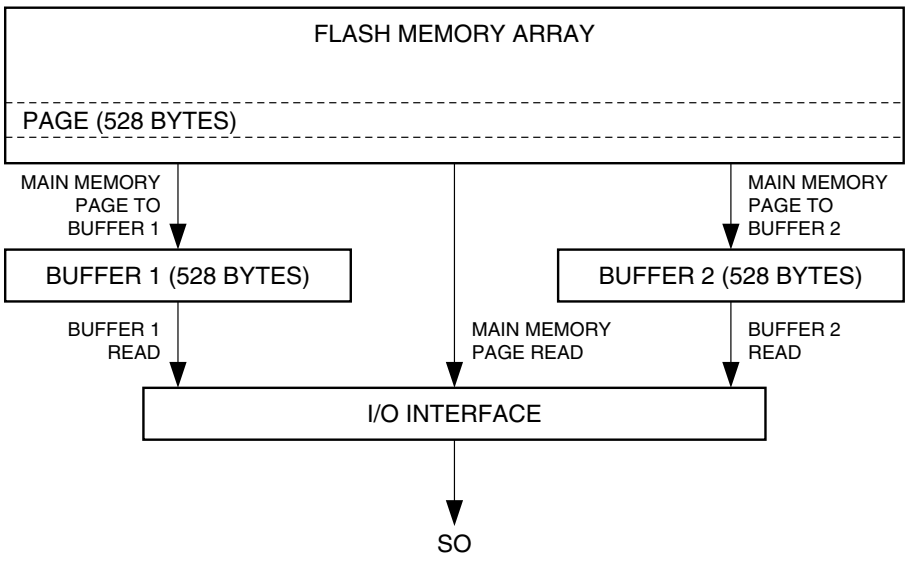
Each transition represents 8 bits and 8 clock cycles



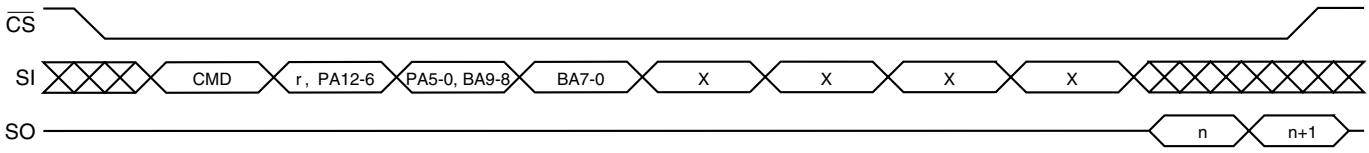
n = 1st byte write
n+1 = 2nd byte write

15. Read Operations

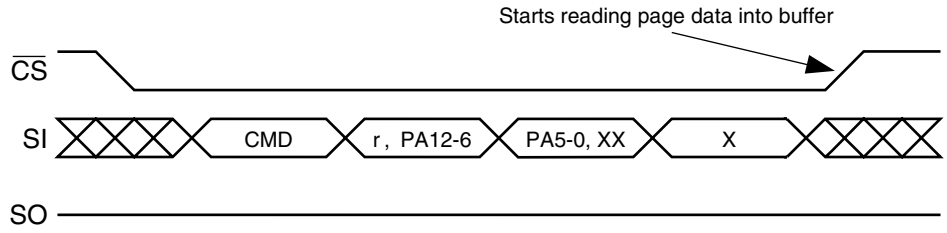
The following block diagram and waveforms illustrate the various read sequences available.



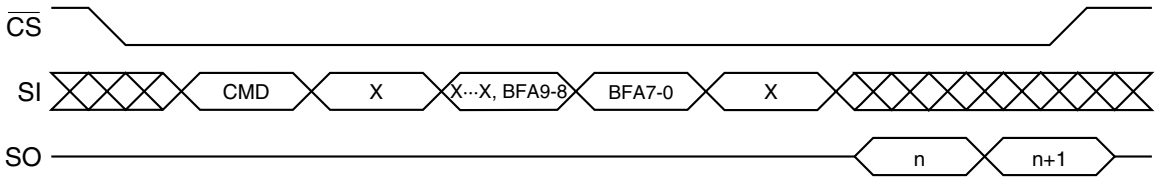
15.1 Main Memory Page Read



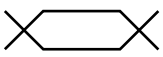
15.2 Main Memory Page to Buffer Transfer (Data from Flash Page Read into Buffer)



15.3 Buffer Read



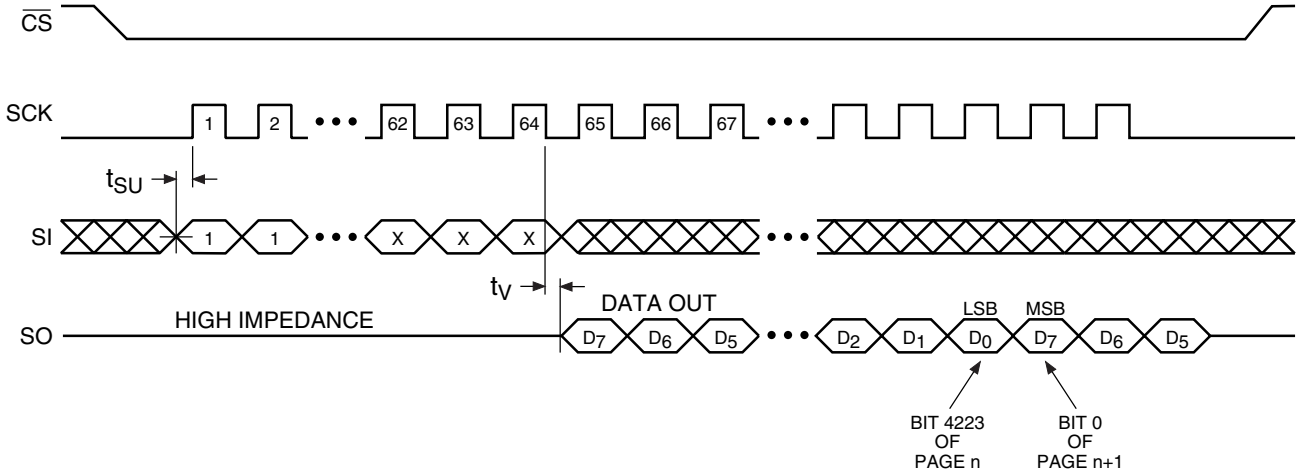
Each transition represents 8 bits and 8 clock cycles



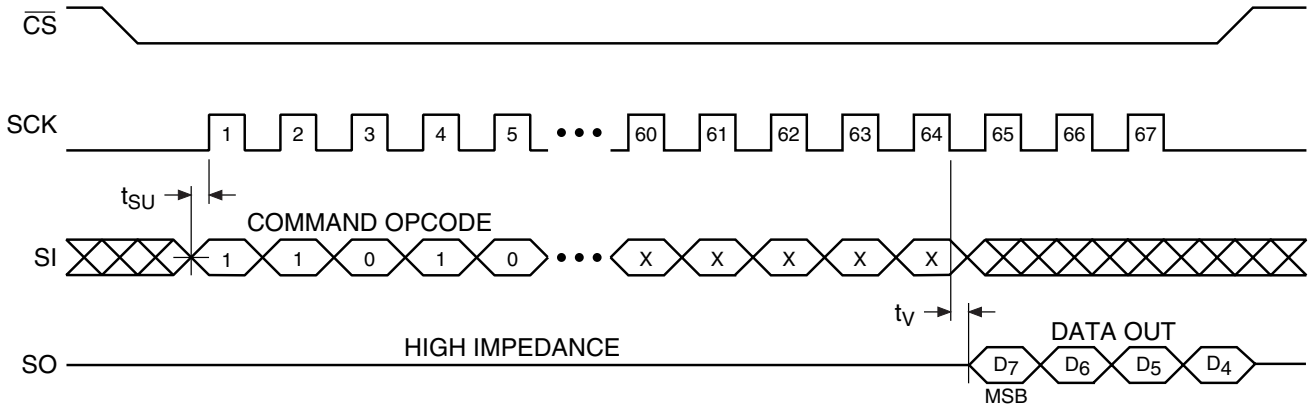
n = 1st byte read
n+1 = 2nd byte read

15.4 Detailed Bit-level Read Timing – RapidS Serial Interface Mode 0

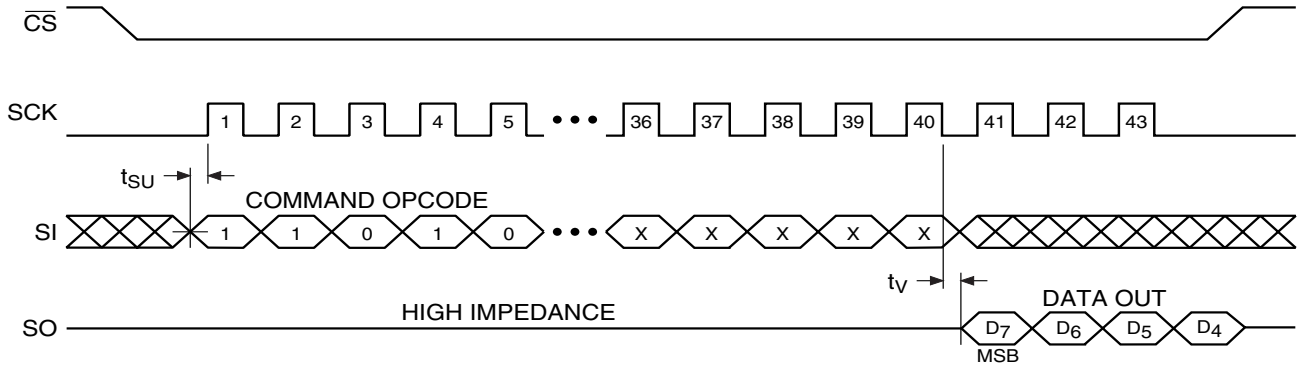
15.4.1 Continuous Array Read (Opcode: E8H)



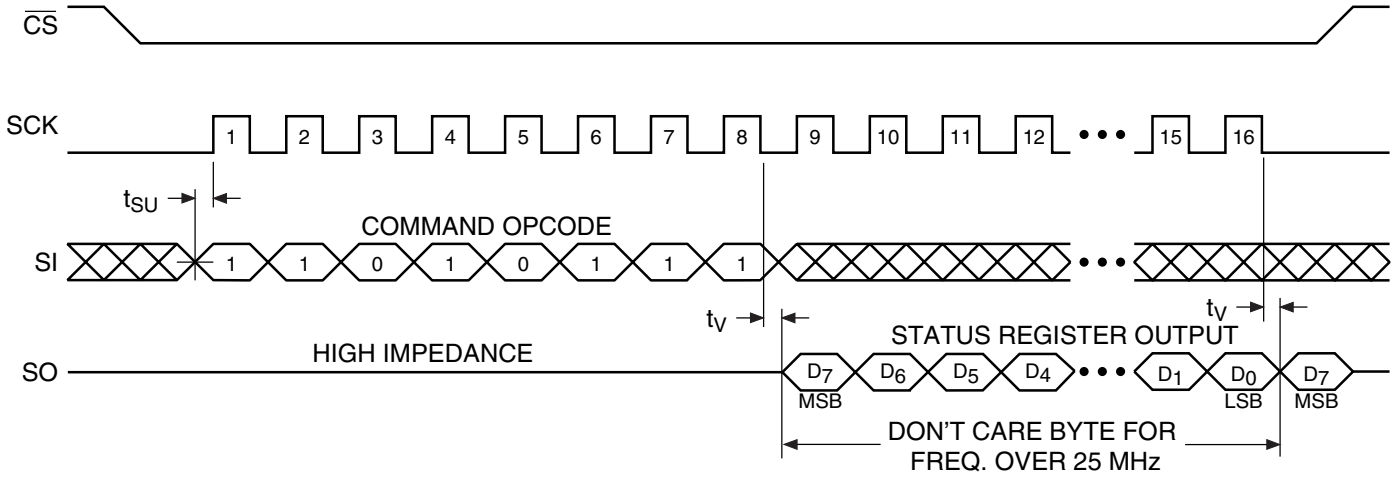
15.4.2 Main Memory Page Read (Opcode: D2H)



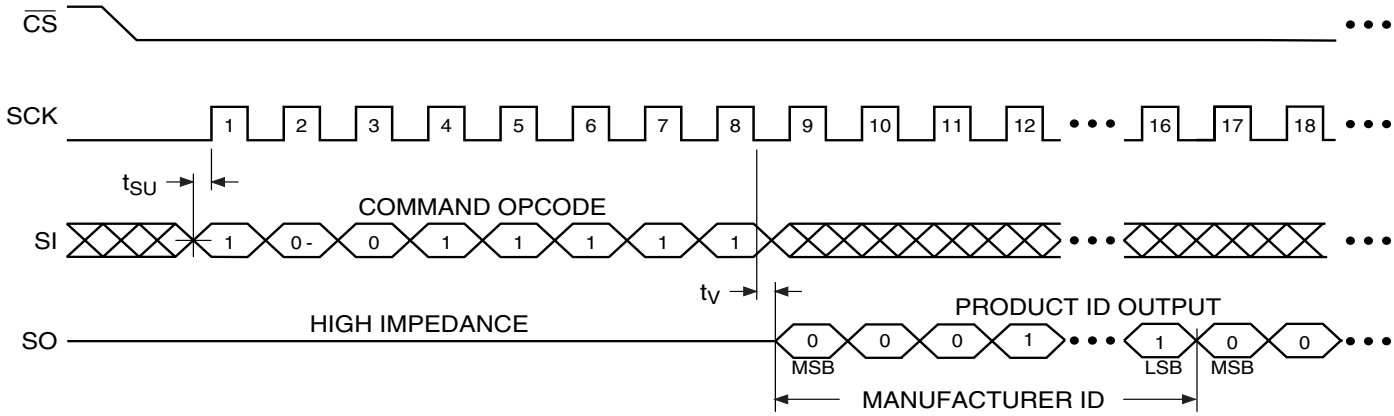
15.4.3 Buffer Read (Opcode: D4H or D6H)



15.4.4 Status Register Read (Opcode: D7H)

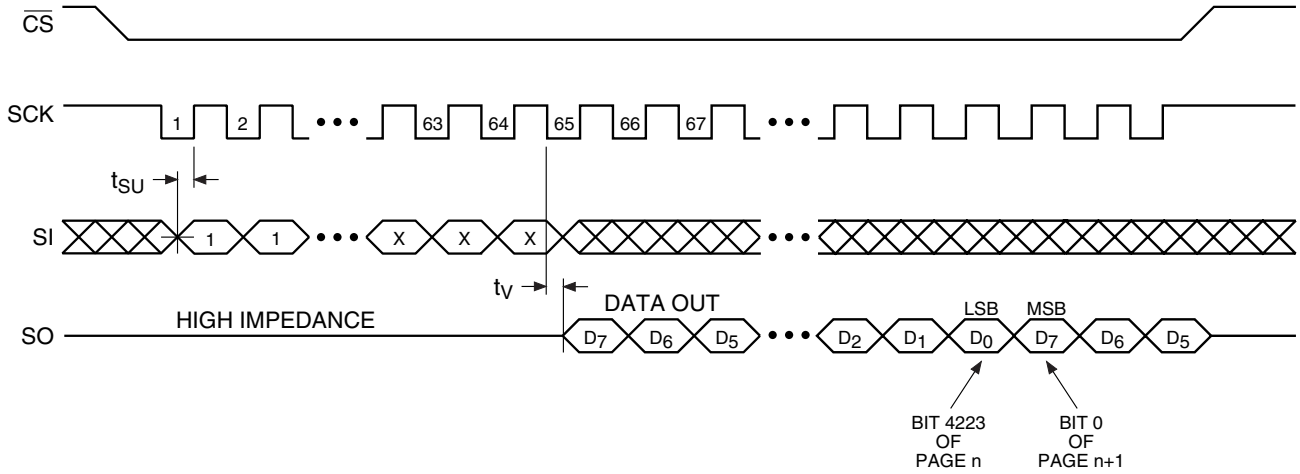


15.4.5 Manufacturer and Device ID Read (Opcode: 9FH)

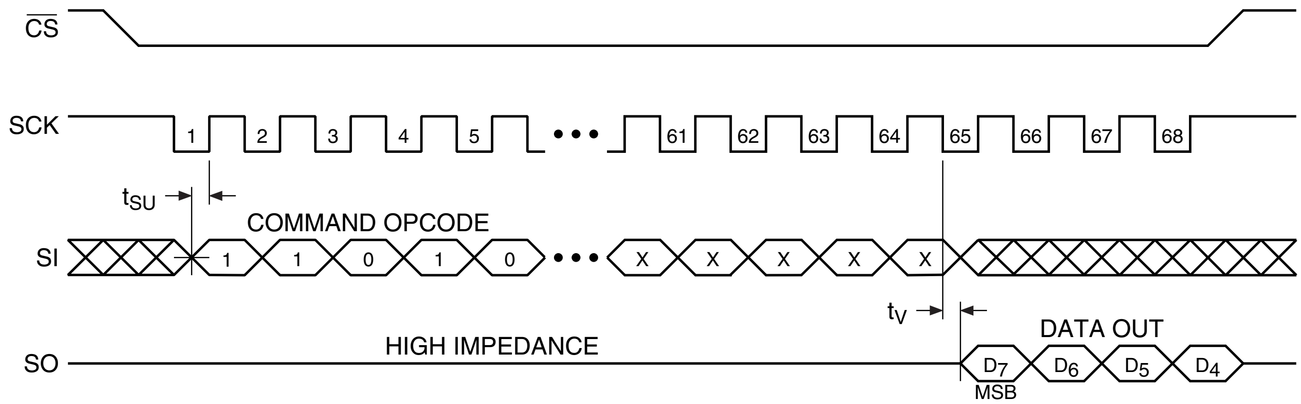


15.5 Detailed Bit-level Read Timing – RapidS Serial Interface Mode 3

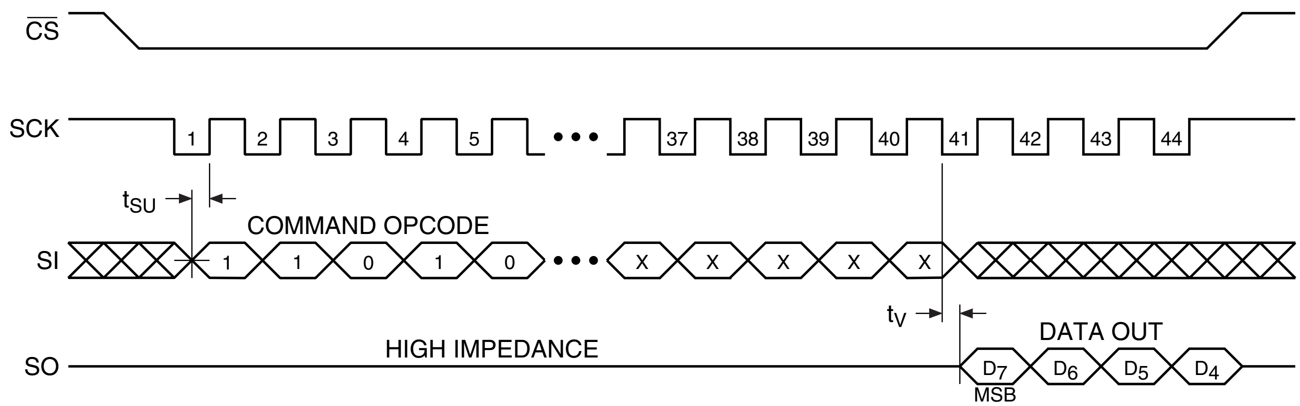
15.5.1 Continuous Array Read (Opcode: E8H)



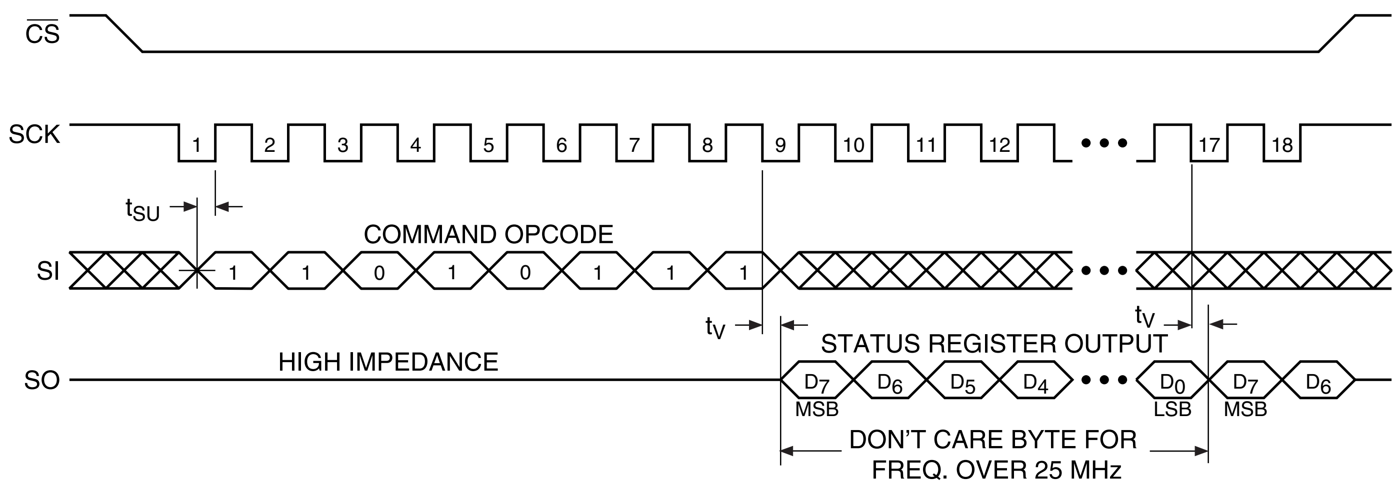
15.5.2 Main Memory Page Read (Opcode: D2H)



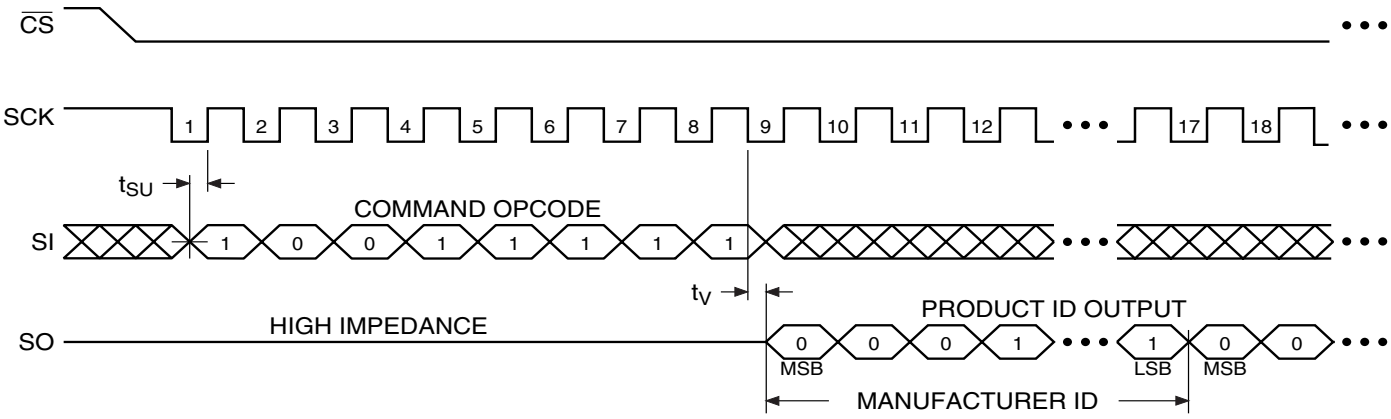
15.5.3 Buffer Read (Opcode: D4H or D6H)



15.5.4 Status Register Read (Opcode: D7H)

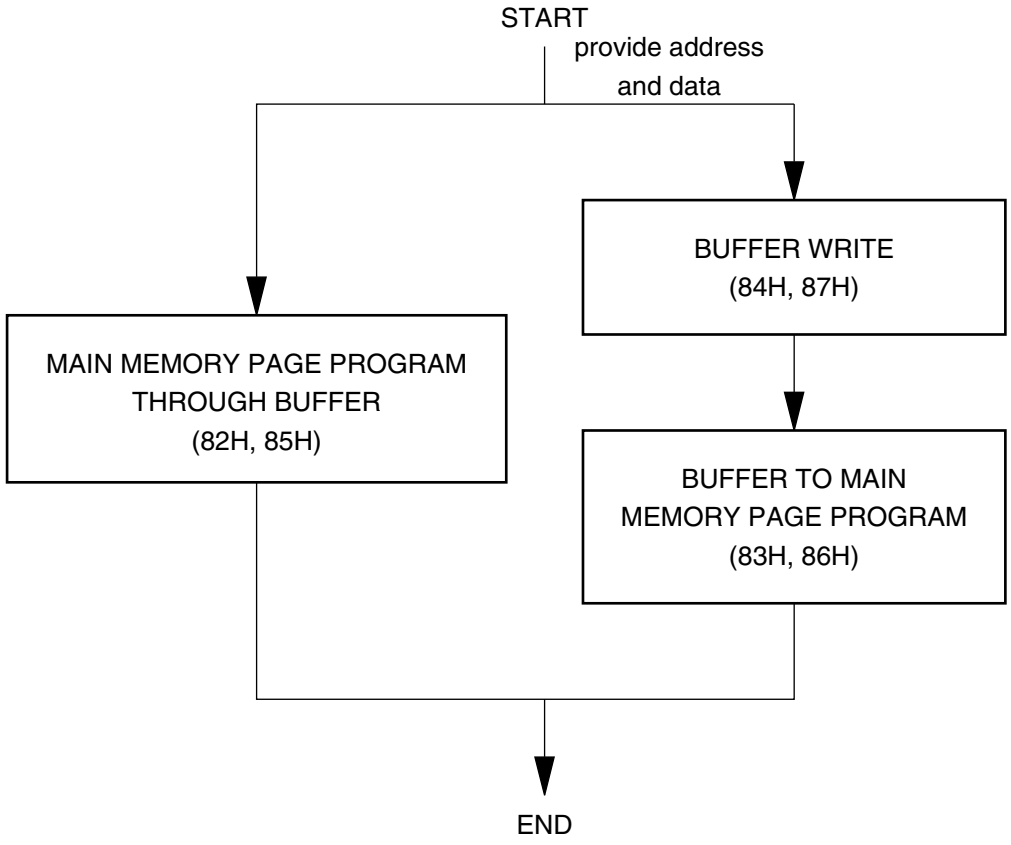


15.5.5 Manufacturer and Device ID Read (Opcode: 9FH)



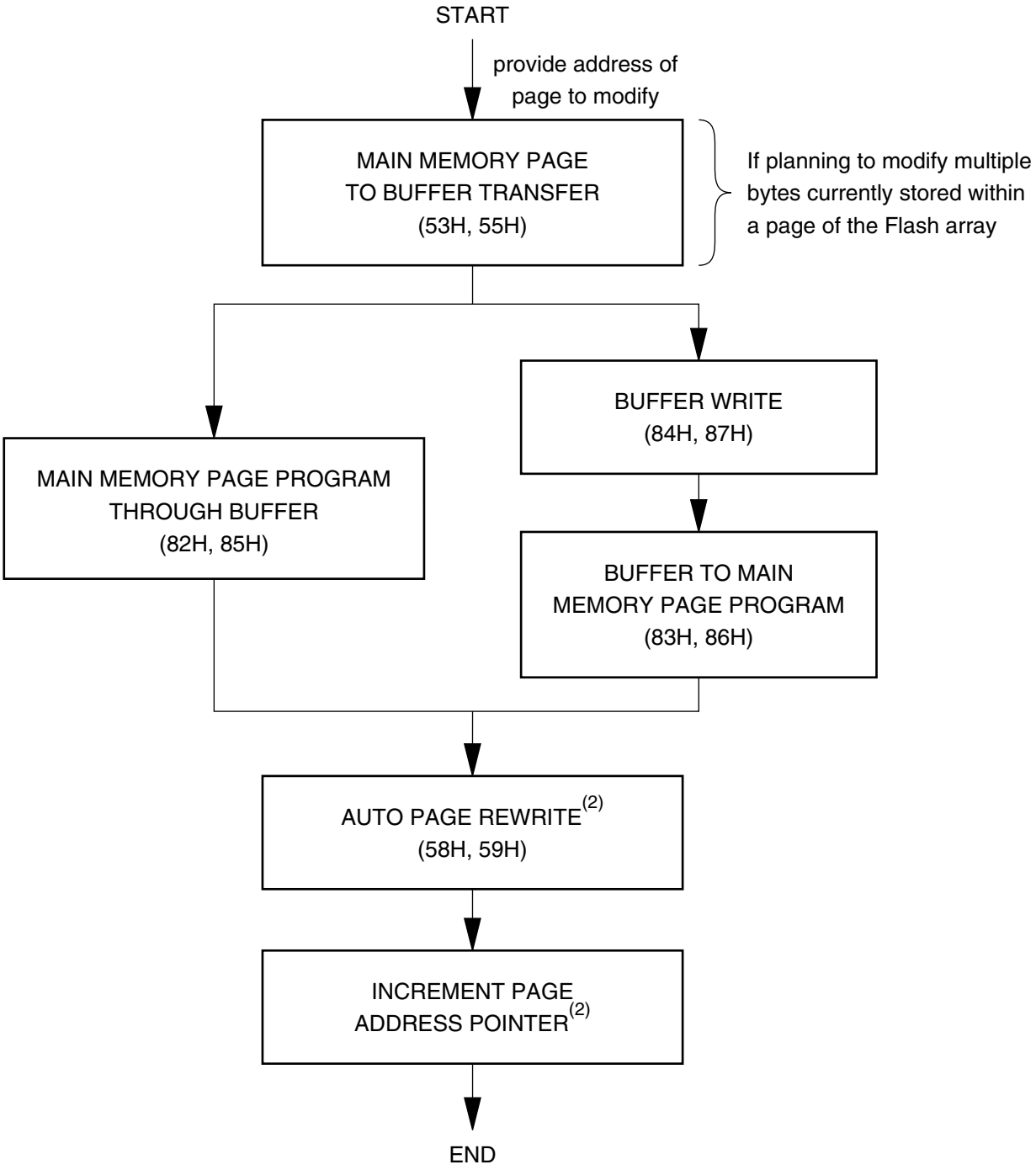
15.6 Auto Page Rewrite Flowchart

Figure 15-1. Algorithm for Programming or Reprogramming of the Entire Array Sequentially



Notes:
1. This type of algorithm is used for applications in which the entire array is programmed sequentially, filling the array page-by-page.
2. A page can be written using either a Main Memory Page Program operation or a Buffer Write operation followed by a Buffer to Main Memory Page Program operation.
3. The algorithm above shows the programming of a single page. The algorithm will be repeated sequentially for each page within the entire array.

Figure 15-2. Algorithm for Randomly Modifying Data



Notes:
1. To preserve data integrity, each page of a DataFlash sector must be updated/rewritten at least once within every 10,000 cumulative page erase and program operations.
2. A Page Address Pointer must be maintained to indicate which page is to be rewritten. The Auto Page Rewrite command must use the address specified by the Page Address Pointer.
3. Other algorithms can be used to rewrite portions of the Flash array. Low-power applications may choose to wait until 10,000 cumulative page erase and program operations have accumulated before rewriting all pages of the sector. See application note AN-4 (“Using Atmel’s Serial DataFlash”) for more details.

16. Sector Addressing

PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2 - PA0	Sector
0	0	0	0	0	0	0	0	0	0	X	0a
0	0	0	0	X	X	X	X	X	X	X	0b
0	0	0	1	X	X	X	X	X	X	X	1
0	0	1	0	X	X	X	X	X	X	X	2
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
1	1	0	0	X	X	X	X	X	X	X	12
1	1	0	1	X	X	X	X	X	X	X	13
1	1	1	0	X	X	X	X	X	X	X	14
1	1	1	1	X	X	X	X	X	X	X	15

17. Ordering Information

f_{SCK} (MHz)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
40	15	0.015	AT45DB321C-CC AT45DB321C-CNC AT45DB321C-TC	24C3 8CN3 28T	Commercial (0° C to 70° C)
40	15	0.015	AT45DB321C-CI AT45DB321C-TI	24C3 28T	Industrial (-40° C to 85° C)

18. Green Package Options (Pb /Halide-free/RoHS Compliant)

f_{SCK} (MHz)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
40	15	0.015	AT45DB321C-CU AT45DB321C-CNU AT45DB321C-TU	24C3 8CN3 28T	Industrial (-40° C to 85° C)

19. Legacy Package Options[1]

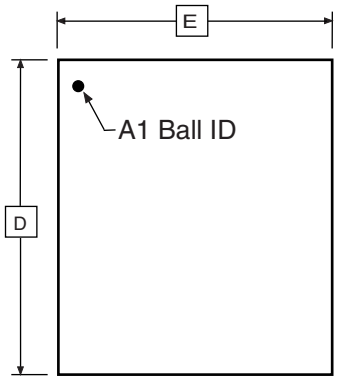
f_{SCK} (MHz)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
40	15	0.015	AT45DB321C-RC	28R	Commercial (0° C to 70° C)
40	15	0.015	AT45DB321C-RU	28R	Industrial (-40° C to 85° C)

Note: 1. Not recommended for new designs.

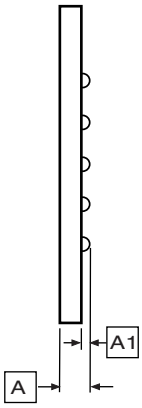
Package Type	
24C3	24-ball (5 x 5 Array), 1.0 mm Pitch, 6 x 8 x 1.2 mm, Plastic Chip-scale Ball Grid Array (CBGA)
8CN3	8-pad (6 mm x 8 mm) Chip Array Small Outline No Lead Package (CASON)
28T	28-lead, Plastic Thin Small Outline Package (TSOP)
28R	28-lead, 0.330” Wide, Plastic Gull Wing Small Outline Package (SOIC)

20. Packaging Information

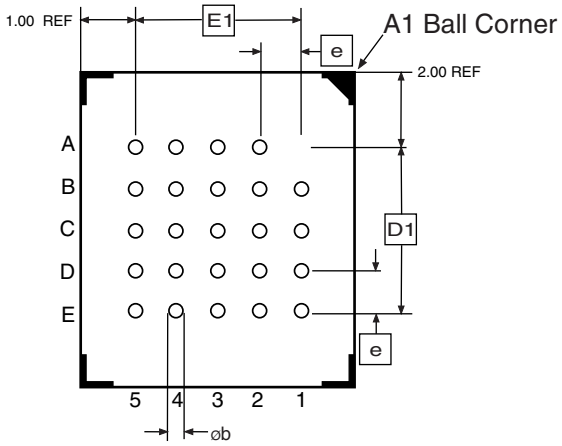
20.1 24C3 – CBGA



Top View



Side View



Bottom View

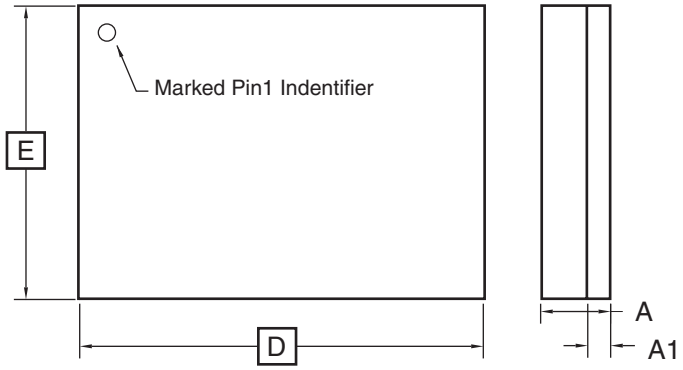
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
E	5.90	6.00	6.10	
E1		4.0 TYP		
D	7.90	8.00	8.10	
D1		4.0 TYP		
A	–	–	1.20	
A1	0.25	–	–	
e		1.00 BSC		
b		0.40 TYP		

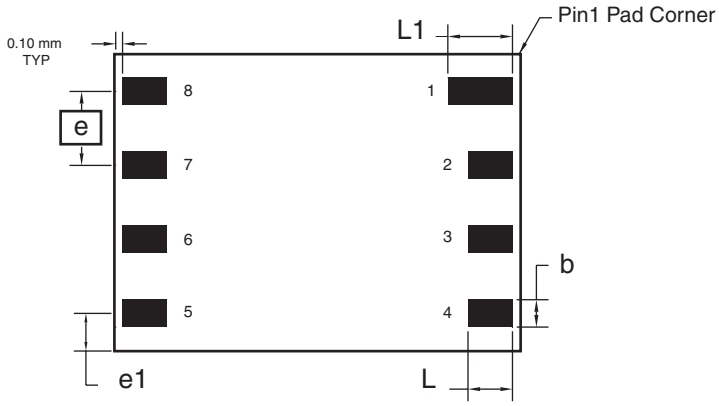
9/10/04

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**24C3**, 24-ball (5 x 5 Array), 1.0 mm Pitch, 6 x 8 x 1.20 mm, Chip-scale Ball Grid Array Package (CBGA)	24C3	A

20.2 8CN3 – CASON



Top View **Side View**



Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

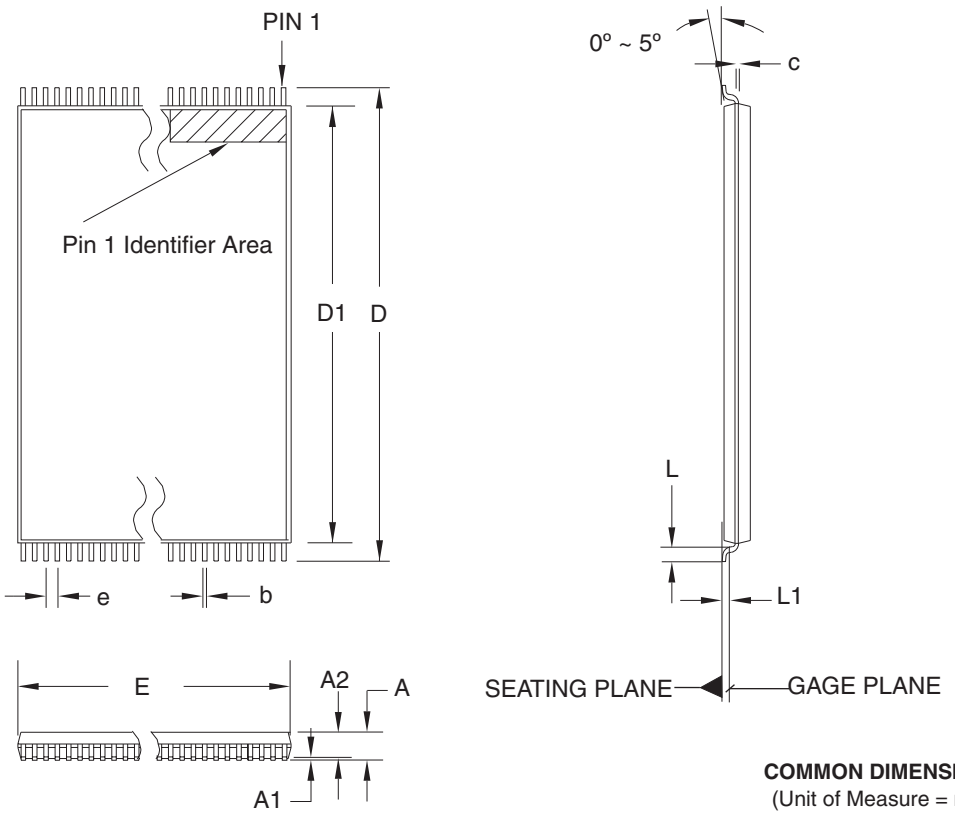
SYMBOL	MIN	NOM	MAX	NOTE
A			1.0	
A1	0.17	0.21	0.25	
b		0.41 TYP		4
D	7.90	8.00	8.10	
E	5.90	6.00	6.10	
e		1.27 BSC		
e1		1.095 REF		
L		0.67 TYP		4
L1	0.92	0.97	1.02	4

Notes:
1. All dimensions and tolerance conform to ASME Y 14.5M, 1994.
2. The surface finish of the package shall be EDM Charmille #24-27.
3. Unless otherwise specified tolerance: Decimal ±0.05, Angular ±2°.
4. Metal Pad Dimensions.

7/10/03

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8CN3,** 8-pad (6 x 8 x 1.0 mm Body), Lead Pitch 1.27 mm, Chip Array Small Outline No Lead Package (CASON)	8CN3	B

20.3 28T – TSOP, Type I



COMMON DIMENSIONS
(Unit of Measure = mm)

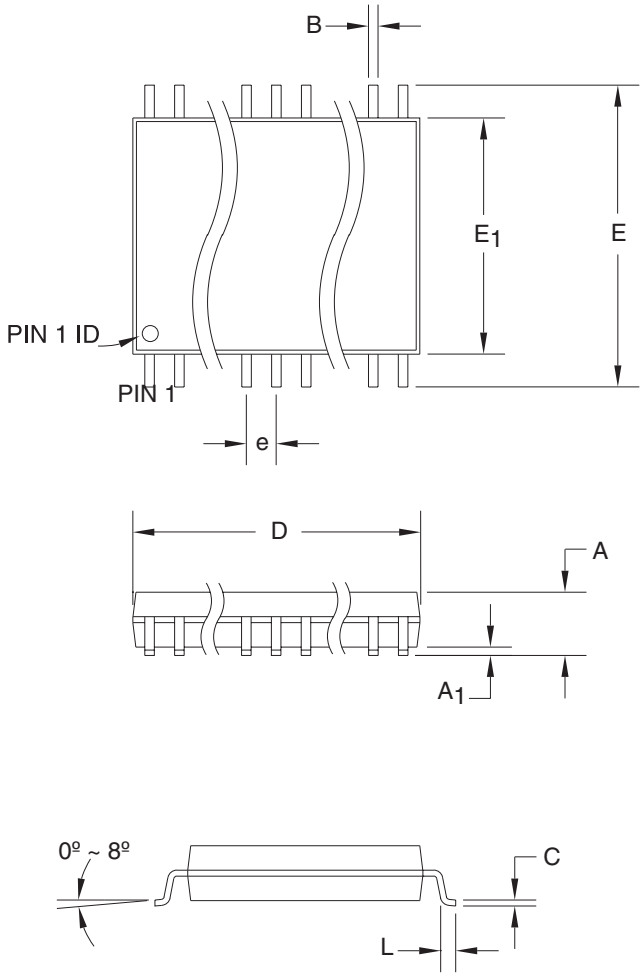
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.90	1.00	1.05	
D	13.20	13.40	13.60	
D1	11.70	11.80	11.90	Note 2
E	7.90	8.00	8.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.55 BASIC			

Notes:
1. This package conforms to JEDEC reference MO-183.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

12/06/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**28T**, 28-lead (8 x 13.4 mm) Plastic Thin Small Outline Package, Type I (TSOP)	28T	C

20.4 28R – SOIC



Note: 1. Dimensions D and E1 do not include mold Flash or protrusion. Mold Flash or protrusion shall not exceed 0.25 mm (0.010").

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	2.39	–	2.79	
A1	0.050	–	0.356	
D	18.00	–	18.50	Note 1
E	11.70	–	12.50	
E1	8.59	–	8.79	Note 1
B	0.356	–	0.508	
C	0.203	–	0.305	
L	0.94	–	1.27	
e	1.27 TYP			

5/18/2004

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**28R,** 28-lead, 0.330" Body Width, Plastic Gull Wing Small Outline (SOIC)	28R	C

21. Revision History

Revision Level – Release Date	History
L – June 2006	Added 28-lead SOIC pinout diagram on page 2.
M – February 2008	Moved to Mature Products.

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