Atmel AT45DB321D

32Mb, 2.5V or 2.7V Atmel DataFlash

DATASHEET

Features

- Single 2.5V - 3.6V or 2.7V - 3.6V supply
- Atmel® RapidS™ serial interface: 66MHz maximum clock frequency
  - SPI compatible modes 0 and 3
- User configurable page size
  - 512 bytes per page
  - 528 bytes per page
  - Page size can be factory preconfigured for 512 bytes
- Page program operation
  - Intelligent programming operation
  - 8,192 pages (512/528 bytes/page) main memory
- Flexible erase options
  - Page erase (512 bytes)
  - Block erase (4KB)
  - Sector erase (64KB)
  - Chip erase (32Mb)
- Two SRAM data buffers (512/528 bytes)
  - Allows receiving data while reprogramming the flash array
- Continuous read capability through entire array
  - Ideal for code shadowing applications
- Low power dissipation
  - 7mA active read current ,typical
  - 25µA standby current, typical
  - 15µA deep power down, typical
- Hardware and software data protection features
  - Individual sector
- Sector lockdown for secure code and data storage
  - Individual sector
- Security: 128-byte security register
  - 64-byte user programmable space
  - Unique 64-byte device identifier
- JEDEC standard manufacturer and device ID read
- 100,000 program/erase cycles per page, minimum
- Data retention: 20 years
- Industrial temperature range
- Green (Pb/halide-free/RoHS compliant) packaging options

1. Description

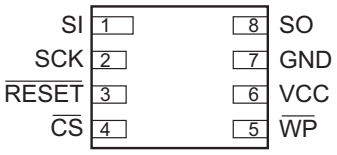
The Atmel AT45DB321D is a 2.5V or 2.7V, serial interface, sequential access flash memory ideally suited for a wide variety of digital voice-, image-, program code-, and data-storage applications. The AT45DB321D supports the Atmel RapidS serial interface for applications requiring very high speed operations. The RapidS serial interface is SPI compatible for frequencies up to 66MHz. The 34,603,008-bits of memory are organized as 8,192 pages of 512 bytes or 528 bytes each. In addition to the main memory, the AT45DB321D also contains two SRAM buffers of 512/528 bytes each. These buffers allow the receiving of data while a page in the main memory is being reprogrammed, as well as the writing of a continuous data stream. EEPROM (electrically erasable and programmable read-only memory) emulation (bit or byte alterability) is easily handled with a self-contained, three-step read-modify-write operation. Unlike conventional flash memories, which are accessed randomly with multiple address lines and a parallel interface, Atmel DataFlash® devices use a RapidS serial interface to sequentially access its data. The simple sequential access dramatically reduces active pin count, facilitates hardware layout, increases system reliability, minimizes switching noise, and reduces package size. The device is optimized for use in many commercial and industrial applications where high density, low pin count, low voltage and low power are essential.

To allow for simple, in-system reprogrammability, the AT45DB321D does not require high input voltages for programming. The device operates from a single power supply, 2.7V to 3.6V, for both the program and read operations. The AT45DB321D is enabled through the chip select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of the serial input (SI), serial output (SO), and serial clock (SCK) lines.

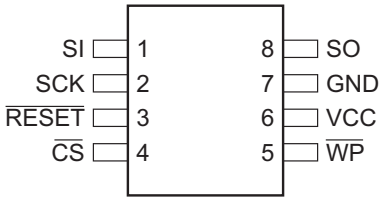
All programming and erase cycles are self timed.

Figure 1-1. Pin configurations and pinouts.

MLF[1] (VDFN)
Top View

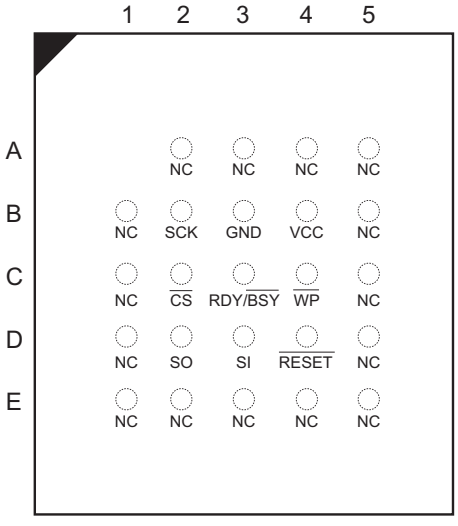


SOIC
Top View

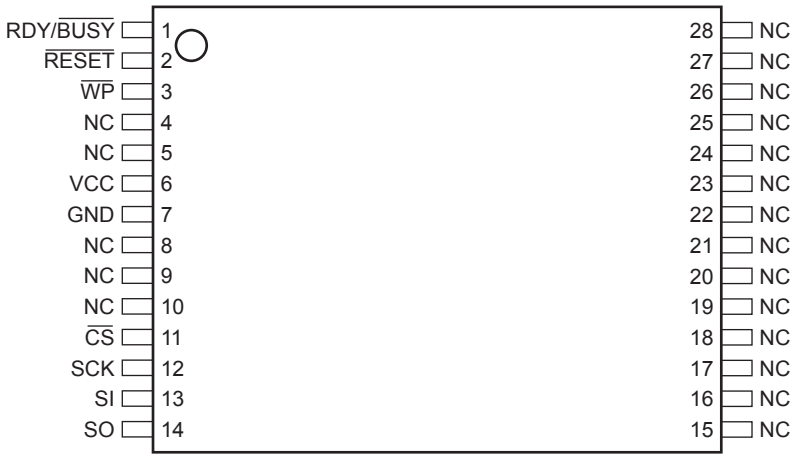


Note: 1. The metal pad on the bottom of the MLF package is floating. This pad can be a “No Connect” or connected to GND.

BGA Package Ball-out
Top View



TSOP: Type 1
Top View

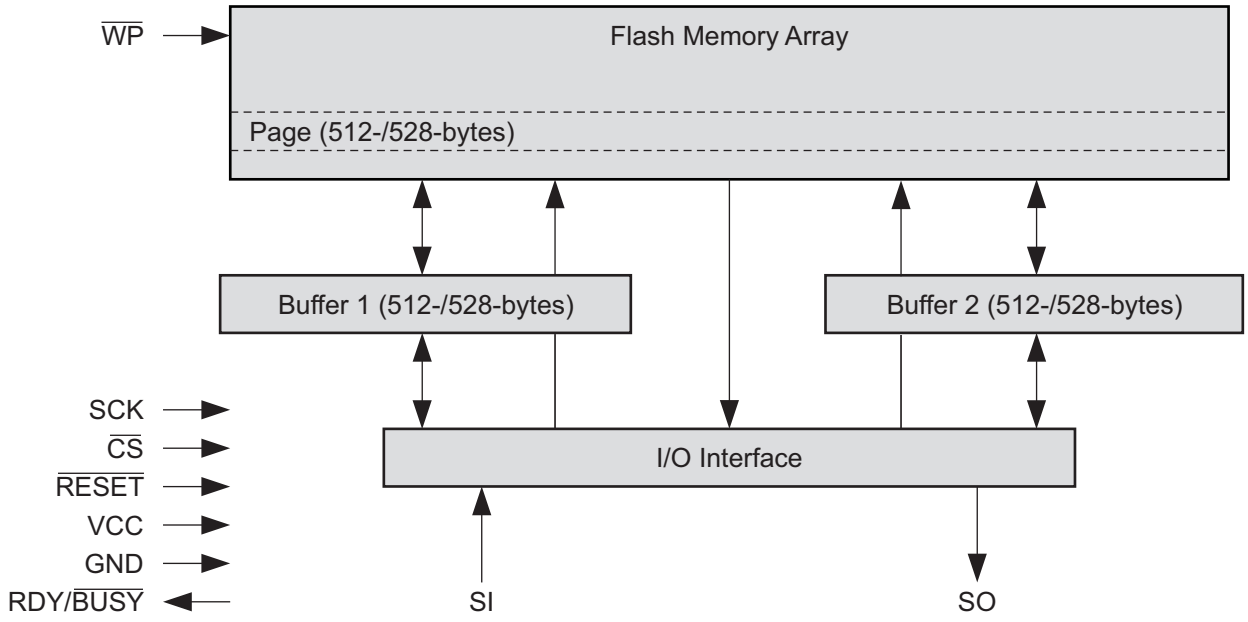


Note: TSOP package is not recommended for new designs. Future die shrinks will support 8-pin packages only.

Table 1-1. Pin Configurations

Symbol	Name and Function	Asserted State	Type
$\overline{CS}$	**Chip Select:** Asserting the $\overline{CS}$ pin selects the device. When the $\overline{CS}$ pin is deasserted, the device will be deselected and normally be placed in the standby mode (not deep power-down mode), and the output pin (SO) will be in a high-impedance state. When the device is deselected, data will not be accepted on the input pin (SI). A high-to-low transition on the $\overline{CS}$ pin is required to start an operation, and a low-to-high transition is required to end an operation. When ending an internally self-timed operation such as a program or erase cycle, the device will not enter the standby mode until the completion of the operation.	Low	Input
SCK	**Serial Clock:** This pin is used to provide a clock to the device, and is used to control the flow of data to and from the device. Command, address, and input data present on the SI pin are always latched on the rising edge of SCK, while output data on the SO pin are always clocked out on the falling edge of SCK.	–	Input
SI	**Serial Input:** The SI pin is used to shift data into the device. The SI pin is used for all data input, including command and address sequences. Data on the SI pin are always latched on the rising edge of SCK.	–	Input
SO	**Serial Output:** The SO pin is used to shift data out from the device. Data on the SO pin are always clocked out on the falling edge of SCK.	–	Output
$\overline{WP}$	**Write Protect:** When the $\overline{WP}$ pin is asserted, all sectors specified for protection by the sector protection register will be protected against program and erase operations, regardless of whether the enable sector protection command has been issued or not. The $\overline{WP}$ pin functions independently of the software controlled protection method. After the $\overline{WP}$ pin goes low, the content of the sector protection register cannot be modified. If a program or erase command is issued to the device while the $\overline{WP}$ pin is asserted, the device will simply ignore the command and perform no operation. The device will return to the idle state once the $\overline{CS}$ pin has been deasserted. The enable sector protection command and sector lockdown command, however, will be recognized by the device when the $\overline{WP}$ pin is asserted. The $\overline{WP}$ pin is internally pulled high, and may be left floating if hardware controlled protection will not be used. However, it is recommended that the $\overline{WP}$ pin also be externally connected to V_{CC} whenever possible.	Low	Input
RESET	**Reset:** A low state on the reset pin ($\overline{RESET}$) will terminate the operation in progress and reset the internal state machine to an idle state. The device will remain in the reset condition as long as a low level is present on the $\overline{RESET}$ pin. Normal operation can resume once the $\overline{RESET}$ pin is brought back to a high level. The device incorporates an internal power-on reset circuit, and so there are no restrictions on the $\overline{RESET}$ pin during power-on sequences. If this pin and feature are not utilized, it is recommended that the $\overline{RESET}$ pin be driven high externally.	Low	Input
RDY/$\overline{BUSY}$	**Ready/Busy:** This open drain output pin will be driven low when the device is busy in an internally self-timed operation. This pin, which is normally in a high state (through an external pull-up resistor), will be pulled low during programming/erase operations, compare operations, and page-to-buffer transfers. The busy status indicates that the flash memory array and one of the buffers cannot be accessed; read and write operations to the other buffer can still be performed.	–	Output
V_{CC}	**Device Power Supply:** The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.	–	Power
GND	**Ground:** The ground reference for the power supply. GND should be connected to the system ground.	–	Ground

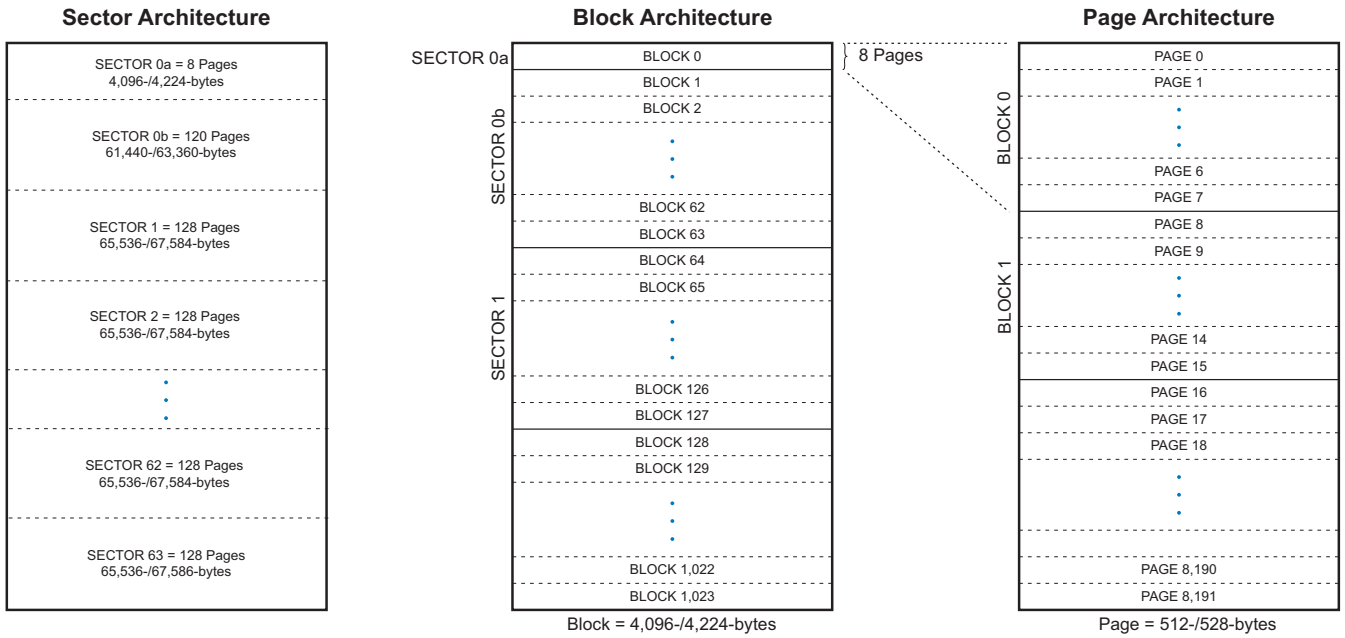
Figure 1-2. Block Diagram



2. Memory Array

To provide optimal flexibility, the AT45DB321D memory array is divided into three levels of granularity comprising sectors, blocks, and pages. The "Memory Architecture Diagram" illustrates the breakdown of each level, and details the number of pages per sector and block. All program operations to the DataFlash device occur on a page-by-page basis. The erase operations can be performed at the chip, sector, block, or page level.

Figure 2-1. Memory Architecture Diagram



3. Device Operation

The device operation is controlled by instructions from the host processor. The list of instructions and their associated opcodes are contained in Table 13-1 on page 24 through Table 13-7 on page 27. A valid instruction starts with the falling edge of $\overline{CS}$, followed by the appropriate 8-bit opcode and the desired buffer or main memory address location. While the $\overline{CS}$ pin is low, toggling the SCK pin controls the loading of the opcode and the desired buffer or main memory address location through the SI (serial input) pin. All instructions, addresses, and data are transferred with the most-significant bit (msb) first.

Buffer addressing for the standard DataFlash page size (528 bytes) is referenced in the datasheet using the terminology BFA9 - BFA0 to denote the ten address bits required to designate a byte address within a buffer. Main memory addressing is referenced using the terminology PA12 - PA0 and BA9 - BA0, where PA12 - PA0 denotes the 13 address bits required to designate a page address and BA9 - BA0 denotes the ten address bits required to designate a byte address within the page.

For a “power of two” binary page size (512 bytes), the buffer addressing is referenced in the datasheet using the conventional terminology BFA8 - BFA0 to denote the nine address bits required to designate a byte address within a buffer. Main memory addressing is referenced using the terminology A21 - A0, where A21 - A9 denotes the 13 address bits required to designate a page address and A8 - A0 denotes the nine address bits required to designate a byte address within a page.

4. Read Commands

By specifying the appropriate opcode, data can be read from the main memory or from either one of the two SRAM data buffers. The DataFlash device supports RapidS protocols for Mode 0 and Mode 3. Please refer to Section 22., Detailed Bit-level Read Waveform – Atmel RapidS Serial Interface Mode 0/Mode 3 diagrams in this datasheet for details on the clock cycle sequences for each mode.

4.1 Continuous Array Read (Legacy Command: E8H): Up to 66MHz

By supplying an initial starting address for the main memory array, the continuous array read command can be utilized to sequentially read a continuous stream of data from the device by simply providing a clock signal; no additional addressing information or control signals need to be provided. The DataFlash device incorporates an internal address counter that will automatically increment on every clock cycle, allowing one continuous read operation without the need of additional address sequences. To perform a continuous read from the standard DataFlash page size (528 bytes), an opcode of E8H must be clocked into the device, followed by three address bytes (which comprise the 24-bit page and byte address sequence) and four “don’t care” bytes. The first 13 bits (PA12 - PA0) of the 23-bit address sequence specify which page of the main memory array to read, and the last 10 bits (BA9 - BA0) of the 23-bit address sequence specify the starting byte address within the page. To perform a continuous read from the binary page size (512-bytes), the opcode (E8H) must be clocked into the device followed by three address bytes and four don’t care bytes. The first 13 bits (A21 - A9) of the 22-bit sequence specify which page of the main memory array to read, and the last 9 bits (A8 - A0) of the 22-bit address sequence specify the starting byte address within the page. The don’t care bytes that follow the address bytes are needed to initialize the read operation. Following the don’t care bytes, additional clock pulses on the SCK pin will result in data being output on the SO (serial output) pin.

The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the don’t care bytes, and the reading of data. When the end of a page in main memory is reached during a continuous array read, the device will continue reading at the beginning of the next page, with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device will continue reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays will be incurred when wrapping around from the end of the array to the beginning of the array.

A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pin (SO). The maximum SCK frequency allowable for the continuous array read is defined by the f_{CAR1} specification. The continuous array read bypasses both data buffers and leaves the contents of the buffers unchanged.

4.2 Continuous Array Read (High Frequency Mode: 0BH): Up to 66MHz

This command can be used with the serial interface to read the main memory array sequentially in high-speed mode for any clock frequency up to the maximum specified by f_{CAR1}. To perform a continuous read array with the page size set to 528 bytes, $\overline{CS}$ must first be asserted, and then a 0BH opcode must be clocked into the device, followed by three address bytes and a dummy byte. The first 13 bits (PA12 - PA0) of the 23-bit address sequence specify which page of the main memory array to read, and the last 10 bits (BA9 - BA0) of the 23-bit address sequence specify the starting byte address within the page. To perform a continuous read with the page size set to 512 bytes, the 0BH opcode must be clocked into the device, followed by three address bytes (A21 - A0) and a dummy byte. Following the dummy byte, additional clock pulses on the SCK pin will result in data being output on the SO (serial output) pin.

The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, and the reading of data. When the end of a page in the main memory is reached during a continuous array read, the device will continue reading at the beginning of the next page, with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device will continue reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays will be incurred when wrapping around from the end of the array to the beginning of the array. A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pin (SO). The maximum SCK frequency allowable for the continuous array read is defined by the f_{CAR1} specification. The continuous array read bypasses both data buffers and leaves the contents of the buffers unchanged.

4.3 Continuous Array Read (Low Frequency Mode: 03H): Up to 33MHz

This command can be used with the serial interface to read the main memory array sequentially without a dummy byte up to the maximum frequency specified by f_{CAR2}. To perform a continuous read array with the page size set to 528 bytes, the $\overline{CS}$ must first be asserted, and then a 03H opcode must be clocked into the device, followed by three address bytes (which comprise the 24-bit page and byte address sequence). The first 13 bits (PA12 - PA0) of the 23-bit address sequence specify which page of the main memory array to read, and the last 10 bits (BA9 - BA0) of the 23-bit address sequence specify the starting byte address within the page. To perform a continuous read with the page size set to 512 bytes, the 03H opcode must be clocked into the device, followed by three address bytes (A21 - A0). Following the address bytes, additional clock pulses on the SCK pin will result in data being output on the SO (serial output) pin.

The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, and the reading of data. When the end of a page in the main memory is reached during a continuous array read, the device will continue reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device will continue reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays will be incurred when wrapping around from the end of the array to the beginning of the array. A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pin (SO). The continuous array read bypasses both data buffers and leaves the contents of the buffers unchanged.

4.4 Main Memory Page Read

A main memory page read allows the user to read data directly from any one of the 8,192 pages in the main memory, bypassing both of the data buffers and leaving the contents of the buffers unchanged. To start a page read from the standard DataFlash page size (528 bytes), an opcode of D2H must be clocked into the device, followed by three address bytes (which comprise the 24-bit page and byte address sequence) and four don't care bytes. The first 13 bits (PA12 - PA0) of the 23-bit address sequence specify the page in main memory to be read, and the last 10 bits (BA9 - BA0) of the 23-bit address sequence specify the starting byte address within that page. To start a page read from the binary page size (512 bytes), the D2H opcode must be clocked into the device, followed by three address bytes and four don't care bytes. The first 13 bits (A21 - A9) of the 22-bit sequence specify which page of the main memory array to read, and the last 9 bits (A8 - A0) of the 22-bit address sequence specify the starting byte address within the page. The don't care bytes that follow the address bytes are sent to initialize the read operation. Following the don't care bytes, additional pulses on SCK result in data being output on the SO (serial output) pin. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the don't care bytes, and the reading of data. When the end of a page in main memory is reached, the device will continue reading back at the beginning of the same page. A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pin (SO). The maximum SCK frequency allowable for the main memory page read is defined by the f_{SCK} specification. The main memory page read bypasses both data buffers and leaves the contents of the buffers unchanged.

4.5 Buffer Read

The SRAM data buffers can be accessed independently of the main memory array, and utilizing the buffer read command allows data to be sequentially read directly from the buffers. Four opcodes, D4H or D1H for buffer 1 and D6H or D3H for buffer 2, can be used for the buffer read command. The use of each opcode depends on the maximum SCK frequency that will be used to read data from the buffer. The D4H and D6H opcodes can be used at any SCK frequency, up to the maximum specified by f_{CAR1}. The D1H and D3H opcodes can be used for lower frequency read operations, up to the maximum specified by f_{CAR2}.

To perform a buffer read from the standard DataFlash buffer (528 bytes), the opcode must be clocked into the device, followed by three address bytes comprised of 14 don't care bits and 10 buffer address bits (BFA9 - BFA0). To perform a buffer read from the binary buffer (512 bytes), the opcode must be clocked into the device, followed by three address bytes comprised of 15 don't care bits and 9 buffer address bits (BFA8 - BFA0). Following the address bytes, one don't care byte must be clocked in to initialize the read operation. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the don't care byte, and the reading of data. When the end of a buffer is reached, the device will continue reading back at the beginning of the buffer. A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pin (SO).

5. Program and Erase Commands

5.1 Buffer Write

Data can be clocked in from the input pin (SI) into either buffer 1 or buffer 2. To load data into the standard DataFlash buffer (528 bytes), a 1-byte opcode, 84H for buffer 1 or 87H for buffer 2, must be clocked into the device, followed by three address bytes comprised of 14 don't care bits and 10 buffer address bits (BFA9 - BFA0). The 10 buffer address bits specify the first byte in the buffer to be written. To load data into the binary buffers (512 bytes each), a 1-byte 84H opcode for buffer 1 or 87H opcode for buffer 2 must be clocked into the device, followed by three address bytes comprised of 15 don't care bits and 9 buffer address bits (BFA8 - BFA0). The nine buffer address bits specify the first byte in the buffer to be written. After the last address byte has been clocked into the device, data can then be clocked in on subsequent clock cycles. If the end of the data buffer is reached, the device will wrap around back to the beginning of the buffer. Data will continue to be loaded into the buffer until a low-to-high transition is detected on the $\overline{CS}$ pin.

5.2 Buffer to Main Memory Page Program with Built-in Erase

Data written into either buffer 1 or buffer 2 can be programmed into the main memory. A 1-byte opcode, 83H for buffer 1 or 86H for buffer 2, must be clocked into the device. For the standard DataFlash page size (528 bytes), the opcode must be followed by three address bytes consist of 1 don't care bit, 13 page address bits (PA12 - PA0) that specify the page in the main memory to be written, and 10 don't care bits. To perform a buffer to main memory page program with built-in erase for the binary page size (512 bytes), the 83H opcode for buffer 1 or 86H opcode for buffer 2 must be clocked into the device, followed by three address bytes consisting of 2 don't care bits, 13 page address bits (A21 - A9) that specify the page in the main memory to be written, and 9 don't care bits. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will first erase the selected page in main memory (the erased state is a logic one) and then program the data stored in the buffer into the specified page in main memory. The erase and the programming of the page are internally self-timed, and should take place in a maximum time of t_{EP}. During this time, the status register and the RDY/$\overline{BUSY}$ pin will indicate that the part is busy.

5.3 Buffer to Main Memory Page Program without Built-in Erase

A previously-erased page within main memory can be programmed with the contents of either buffer 1 or buffer 2. A one-byte opcode, 88H for buffer 1 or 89H for buffer 2, must be clocked into the device. For the standard DataFlash page size (528 bytes), the opcode must be followed by three address bytes that consist of 1 don't care bit, 13 page address bits (PA12 - PA0) that specify the page in the main memory to be written, and 10 don't care bits. To perform a buffer to main memory page program without built-in erase for the binary page size (512 bytes), the 88H opcode for buffer 1 or 89H opcode for buffer 2 must be clocked into the device, followed by three address bytes consisting of 2 don't care bits, 13 page address bits (A21 - A9) that specify the page in the main memory to be written, and 9 don't care bits. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will program the data stored in the buffer into the specified page in the main memory. It is necessary that the page in main memory being programmed has been previously erased using one of the erase commands (page erase or block erase). The programming of the page is internally self-timed, and should take place in a maximum time of t_P. During this time, the status register and the RDY/$\overline{BUSY}$ pin will indicate that the part is busy.

5.4 Page Erase

The page erase command can be used to individually erase any page in the main memory array, allowing the buffer to main memory page program to be utilized at a later time. To perform a page erase in the standard DataFlash page size (528 bytes), an opcode of 81H must be loaded into the device, followed by three address bytes comprised of 1 don't care bit, 13 page address bits (PA12 - PA0) that specify the page in the main memory to be erased, and 10 don't care bits. To perform a page erase in the binary page size (512 bytes), the 81H opcode must be loaded into the device, followed by three address bytes consisting of 2 don't care bits, 13 page address bits (A21 - A9) that specify the page in the main memory to be erased, and 9 don't care bits. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will erase the selected page (the erased state is a logical 1). The erase operation is internally self-timed, and should take place in a maximum time of t_{PE}. During this time, the status register and the RDY/$\overline{BUSY}$ pin will indicate that the part is busy.

5.5 Block Erase

A block of eight pages can be erased at one time. This command is useful when large amounts of data have to be written into the device. This will avoid using multiple page erase commands. To perform a block erase for the standard DataFlash page size (528-bytes), an opcode of 50H must be loaded into the device, followed by three address bytes comprised of 1 don't care bit, 10 page address bits (PA12-PA3), and 13 don't care bits. The 10 page address bits are used to specify which block of eight pages is to be erased. To perform a block erase for the binary page size (512 bytes), the 50H opcode must be loaded into the device, followed by three address bytes consisting of 2 don't care bits, 10 page address bits (A21 - A12), and 12 don't care bits. The 10 page address bits are used to specify which block of eight pages is to be erased. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will erase the selected block of eight pages. The erase operation is internally self-timed, and should take place in a maximum time of t_{BE}. During this time, the status register and the RDY/$\overline{BUSY}$ pin will indicate that the part is busy.

Table 5-1. Block Erase Addressing

PA12/ A21	PA11/ A20	PA10/ A19	PA9/ A18	PA8/ A17	PA7/ A16	PA6/ A15	PA5/ A14	PA4/ A13	PA3/ A12	PA2/ A11	PA1/ A10	PA0/ A9	Block
0	0	0	0	0	0	0	0	0	0	X	X	X	0
0	0	0	0	0	0	0	0	0	1	X	X	X	1
0	0	0	0	0	0	0	0	1	0	X	X	X	2
0	0	0	0	0	0	0	0	1	1	X	X	X	3
•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	0	0	X	X	X	1020
1	1	1	1	1	1	1	1	0	1	X	X	X	1021
1	1	1	1	1	1	1	1	1	0	X	X	X	1022
1	1	1	1	1	1	1	1	1	1	X	X	X	1023

5.6 Sector Erase

The sector erase command can be used to individually erase any sector in the main memory. There are 64 sectors, and only one sector can be erased at a time. To perform a sector 0a or sector 0b erase for the standard DataFlash page size (528 bytes), an opcode of 7CH must be loaded into the device, followed by three address bytes comprised of 1 don't care bit, 10 page address bits (PA12 - PA3), and 13 don't care bits. To perform a sector 1-63 erase, the 7CH opcode must be loaded into the device, followed by three address bytes comprised of 1 don't care bit, 6 page address bits (PA12 - PA7), and 17 don't care bits. To perform a sector 0a or sector 0b erase for the binary page size (512 bytes), an opcode of 7CH must be loaded into the device, followed by three address bytes comprised of 2 don't care bits, 10 page address bits (A21 - A12), and 12 don't care bits. To perform a sector 1-63 erase, the 7CH opcode must be loaded into the device, followed by three address bytes comprised of 2 don't care bits, 6 page address bits (A21 - A16), and 16 don't care bits. The page address bits are used to specify any valid address location within the sector to be erased. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will erase the selected sector. The erase operation is internally self-timed, and should take place in a maximum time of t_{SE}. During this time, the status register and the RDY/$\overline{BUSY}$ pin will indicate that the part is busy.

Table 5-2. Sector Erase Addressing

PA12/ A21	PA11/ A20	PA10/ A19	PA9/ A18	PA8/ A17	PA7/ A16	PA6/ A15	PA5/ A14	PA4/ A13	PA3/ A12	PA2/ A11	PA1/ A10	PA0/ A9	Sector
0	0	0	0	0	0	0	0	0	0	X	X	X	0a
0	0	0	0	0	0	0	0	0	1	X	X	X	0b
0	0	0	0	0	1	X	X	X	X	X	X	X	1
0	0	0	0	1	0	X	X	X	X	X	X	X	2
•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	0	0	X	X	X	X	X	X	X	60
1	1	1	1	0	1	X	X	X	X	X	X	X	61
1	1	1	1	1	0	X	X	X	X	X	X	X	62
1	1	1	1	1	1	X	X	X	X	X	X	X	63

5.7 Chip Erase[1]

The entire main memory can be erased at one time by using the chip erase command.

To execute the chip erase command, a four-byte command sequence, C7H, 94H, 80H, and 9AH, must be clocked into the device. Since the entire memory array is to be erased, no address bytes need to be clocked into the device, and any data clocked in after the opcode will be ignored. After the last bit of the opcode sequence has been clocked in, the $\overline{CS}$ pin can be deasserted to start the erase process. The erase operation is internally self-timed, and should take place in a time of t_{CE}. During this time, the status register will indicate that the device is busy.

The chip erase command will not affect sectors that are protected or locked down; the contents of those sectors will remain unchanged. Only those sectors that are not protected or locked down will be erased.

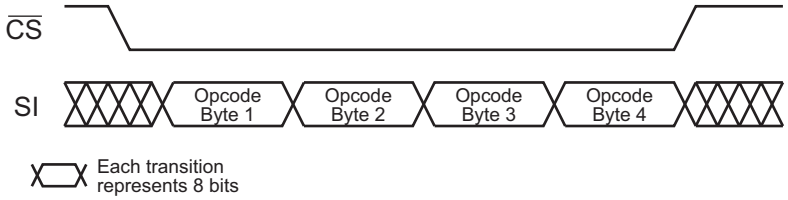
Note: 1. Refer to the errata regarding chip erase on page 50.

The $\overline{WP}$ pin can be asserted while the device is erasing, but protection will not be activated until the internal erase cycle completes.

Table 5-3. Chip Erase Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Chip erase	C7H	94H	80H	9AH

Figure 5-1. Chip Erase



Note: 1. Refer to the errata regarding chip erase on page 50.

5.8 Main Memory Page Program through Buffer

This operation is a combination of the buffer write and buffer to main memory page program with built-in erase operations. Data are first clocked into buffer 1 or buffer 2 from the input pin (SI), and then programmed into a specified page in the main memory. To perform a main memory page program through buffer for the standard DataFlash page size (528 bytes), a one-byte opcode, 82H for buffer 1 or 85H for buffer 2, must first be clocked into the device, followed by three address bytes. The address bytes are comprised of 1 don't care bit, 13 page address bits, (PA12 - PA0) that select the page in the main memory where data is to be written, and 10 buffer address bits (BFA9 - BFA0) that select the first byte in the buffer to be written. To perform a main memory page program through buffer for the binary page size (512 bytes), the 82H opcode for buffer 1 or 85H opcode for buffer 2 must be clocked into the device, followed by three address bytes consisting of 2 don't care bits, 13 page address bits (A21 - A9) that specify the page in the main memory to be written, and 9 buffer address bits (BFA8 - BFA0) that select the first byte in the buffer to be written. After all address bytes are clocked in, the part will take data from the input pins and store them in the specified data buffer. If the end of the buffer is reached, the device will wrap around back to the beginning of the buffer. When there is a low-to-high transition on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all ones, and then program the data stored in the buffer into that memory page. Both the erase and the programming of the page are internally self-timed, and should take place in a maximum time of t_{EP}. During this time, the status register and the RDY/$\overline{BUSY}$ pin will indicate that the part is busy.

6. Sector Protection

Two protection methods, hardware and software controlled, are provided for protection against inadvertent or erroneous program and erase cycles. The software controlled method relies on the use of software commands to enable and disable sector protection, while the hardware controlled method employs the use of the write protect ($\overline{WP}$) pin. The selection of which sectors are to be protected or unprotected against program and erase operations is specified in the nonvolatile sector protection register. The status of whether or not sector protection has been enabled or disabled by either the software or the hardware controlled methods can be determined by checking the status register.

6.1 Software Sector Protection

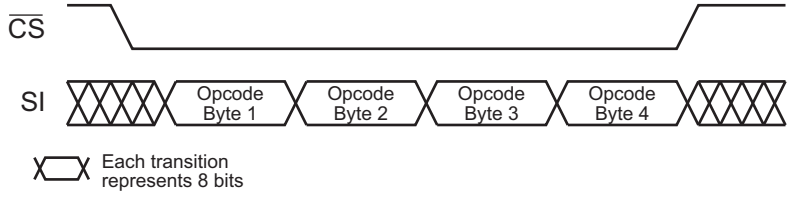
6.1.1 Enable Sector Protection Command

Sectors specified for protection in the sector protection register can be protected from program and erase operations by issuing the enable sector protection command. To enable sector protection using the software controlled method, the $\overline{CS}$ pin must first be asserted, as it would be with any other command. Once the $\overline{CS}$ pin has been asserted, the appropriate four-byte command sequence must be clocked in via the input pin (SI). After the last bit of the command sequence has been clocked in, the $\overline{CS}$ pin must be deasserted, after which the sector protection will be enabled.

Table 6-1. Enable Sector Protection Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Enable Sector Protection	3DH	2AH	7FH	A9H

Figure 6-1. Enable Sector Protection



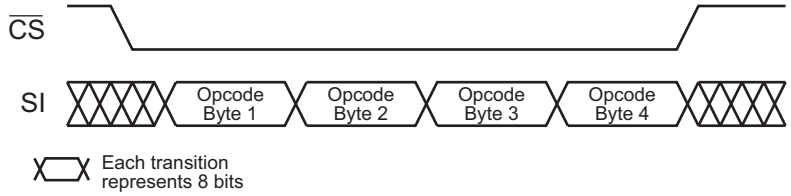
6.1.2 Disable Sector Protection Command

To disable sector protection using the software controlled method, the $\overline{CS}$ pin must first be asserted, as it would be with any other command. Once the $\overline{CS}$ pin has been asserted, the appropriate four-byte sequence for the disable sector protection command must be clocked in via the input pin (SI). After the last bit of the command sequence has been clocked in, the $\overline{CS}$ pin must be deasserted, after which the sector protection will be disabled. The $\overline{WP}$ pin must be in the deasserted state; otherwise, the disable sector protection command will be ignored.

Table 6-2. Disenable Sector Protection Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Disable sector protection	3DH	2AH	7FH	9AH

Figure 6-2. Disable Sector Protection



6.1.3 Various Aspects About Software Controlled Protection

Software controlled protection is useful in applications in which the $\overline{WP}$ pin is not or cannot be controlled by a host processor. In such instances, the $\overline{WP}$ pin may be left floating (the $\overline{WP}$ pin is internally pulled high), and sector protection can be controlled using the enable sector protection and disable sector protection commands.

If the device is power cycled, then the software controlled protection will be disabled. Once the device is powered up, the enable sector protection command should be reissued if sector protection is desired and if the $\overline{WP}$ pin is not used.

7. Hardware Controlled Protection

Sectors specified in the sector protection register for protection, and the sector protection register itself, can be protected from program and erase operations by asserting the $\overline{WP}$ pin and keeping the pin in its asserted state. The sector protection register and any sector specified for protection cannot be erased or reprogrammed as long as the $\overline{WP}$ pin is asserted. In order to modify the sector protection register, the $\overline{WP}$ pin must be deasserted. If the $\overline{WP}$ pin is permanently connected to GND, then the content of the sector protection register cannot be changed. If the $\overline{WP}$ pin is deasserted or permanently connected to V_{CC}, then the content of the sector protection register can be modified.

The $\overline{WP}$ pin will override the software controlled protection method, but only for protecting the sectors. For example, if the sectors were not previously protected by the enable sector protection command, then simply asserting the $\overline{WP}$ pin would enable sector protection within the maximum specified t_{WPE} time. However, when the $\overline{WP}$ pin is deasserted, sector protection would no longer be enabled (after the maximum specified t_{WPD} time) as long as the enable sector protection command was not issued while the $\overline{WP}$ pin was asserted. If the enable sector protection command was issued before or while the $\overline{WP}$ pin was asserted, then simply deasserting the $\overline{WP}$ pin would not disable sector protection. In this case, the disable sector protection command would need to be issued while the $\overline{WP}$ pin is deasserted to disable sector protection. The disable sector protection command is also ignored whenever the $\overline{WP}$ pin is asserted.

A noise filter is incorporated to help protect against spurious noise that may inadvertently assert or deassert the $\overline{WP}$ pin.

The table below details the sector protection status for various scenarios of the $\overline{WP}$ pin, the enable sector protection command, and the disable sector protection command.

Figure 7-1. $\overline{WP}$ Pin and Protection Status

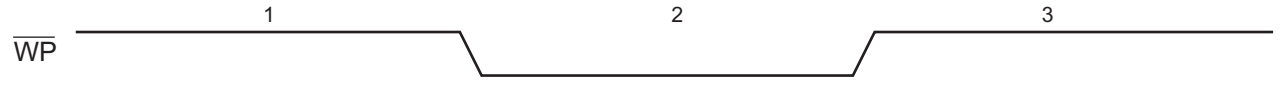


Table 7-1. $\overline{WP}$ Pin and Protection Status

Time Period	$\overline{WP}$ Pin	Enable Sector Protection Command	Disable Sector Protection Command	Sector Protection Status	Sector Protection Register
1	High	Command not issued previously – Issue command	X Issue command –	Disabled Disabled Enabled	Read/write Read/write Read/write
2	Low	X	X	Enabled	Read only
3	High	Command issued during period 1 or 2 – Issue command	Not issued yet issue command –	Enabled Disabled Enabled	Read/write Read/write Read/write

7.1 Sector Protection Register

The nonvolatile sector protection register specifies which sectors are to be protected or unprotected with either the software or hardware controlled protection method. The sector protection register contains 64 bytes of data, in which byte locations 0 through 63 contain values that specify whether sectors 0 through 63 will be protected or unprotected. The sector protection register is user modifiable, and must first be erased before it can be reprogrammed. Table 7-3 illustrates the format of the sector protection register.

Table 7-2. Sector Protection Register

Sector Number	0 (0a, 0b)	1 to 63
Protected	See Table 7-3	FFH
Unprotected		00H

Table 7-3. Sector 0 (0a, 0b)

	0a	0b			
	(Pages 0-7)	(Pages 8-127)			Data Value
	Bit 7, 6	Bit 5, 4	Bit 3, 2	Bit 1, 0	
Sectors 0a, 0b unprotected	00	00	xx	xx	0xH
Protect sector 0a (pages 0-7)	11	00	xx	xx	CxH
Protect sector 0b (pages 8-127)	00	11	xx	xx	3xH
Protect sectors 0a (pages 0-7), 0b (pages 8-127)(1)	11	11	xx	xx	FxH

Note: 1. The default value for bytes 0 through 63 when shipped from Atmel is 00H.
x = don't care.

7.1.1 Erase Sector Protection Register Command

In order to modify and change the value of the sector protection register, it must first be erased using the erase sector protection register command.

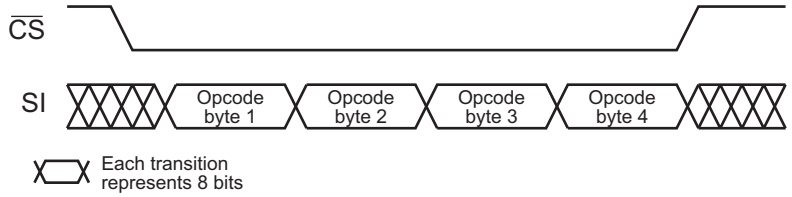
To erase the sector protection register, the $\overline{CS}$ pin must first be asserted, as it would be with any other command. Once the $\overline{CS}$ pin has been asserted, the appropriate four-byte opcode sequence must be clocked into the device via the SI pin. The four-byte opcode sequence must start with 3DH, and be followed by 2AH, 7FH, and CFH. After the last bit of the opcode sequence has been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed erase cycle. The erasing of the sector protection register should take place in a maximum time of t_{PE}, during which time the status register will indicate that the device is busy. If the device is powered down before the completion of the erase cycle, then the contents of the sector protection register cannot be guaranteed.

The sector protection register can be erased with sector protection enabled or disabled. Since the erased state (FFH) of each byte in the sector protection register is used to indicate that a sector is specified for protection, leaving sector protection enabled during the erasing of the register allows the protection scheme to be more effective in the prevention of accidental programming or erasing of the device. If for some reason an erroneous program or erase command is sent to the device immediately after erasing the sector protection register and before the register can be reprogrammed, then the erroneous program or erase command will not be processed because all sectors will be protected.

Table 7-4. Erase Sector Protection Register Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Erase sector protection register	3DH	2AH	7FH	CFH

Figure 7-2. Erase Sector Protection Register



7.1.2 Program Sector Protection Register Command

Once the sector protection register has been erased, it can be reprogrammed using the program sector protection register command.

To program the sector protection register, the $\overline{CS}$ pin must first be asserted, and then the appropriate four-byte opcode sequence must be clocked into the device via the SI pin. The four-byte opcode sequence must start with 3DH, and be followed by 2AH, 7FH, and FCH. After the last bit of the opcode sequence has been clocked into the device, the data for the contents of the sector protection register must be clocked in. As described in Section 7.1, the sector protection register contains 64 bytes of data, and so 64 bytes must be clocked into the device. The first byte of data corresponds to sector 0, the second byte corresponds to sector 1, and so on, with the last byte of data corresponding to sector 63.

After the last data byte has been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed program cycle. The programming of the sector protection register should take place in a maximum time of t_P, during which the status register will indicate that the device is busy. If the device is powered down during the program cycle, the contents of the sector protection register cannot be guaranteed.

If the proper number of data bytes is not clocked in before the $\overline{CS}$ pin is deasserted, then the protection status of the sectors corresponding to the bytes not clocked in can not be guaranteed. For example, if only the first two bytes are clocked in instead of the complete 62 bytes, then the protection status of the last 62 sectors cannot be guaranteed. Furthermore, if more than 64 bytes of data are clocked into the device, then the data will wrap back around to the beginning of the register. For instance, if 65 bytes of data are clocked in, then the 65^{th} byte will be stored at byte location 0 of the sector protection register.

If a value other than 00H or FFH is clocked into a byte location of the sector protection register, then the protection status of the sector corresponding to that byte location cannot be guaranteed. For example, if a value of 17H is clocked into byte location 2 of the sector protection register, then the protection status of sector 2 cannot be guaranteed.

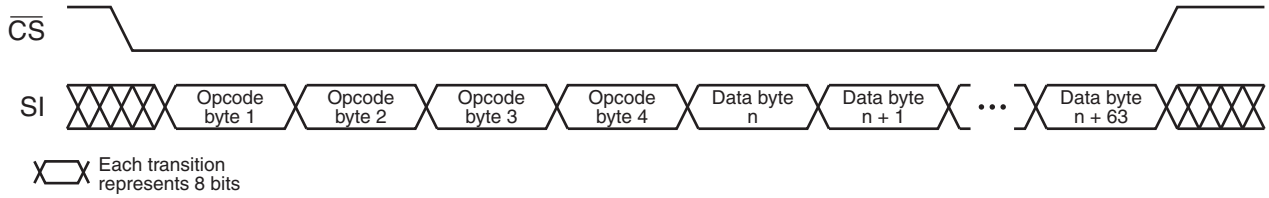
The sector protection register can be reprogrammed while sector protection is enabled or disabled. Being able to reprogram the sector protection register with sector protection enabled allows the user to temporarily disable the sector protection of an individual sector rather than disabling sector protection completely.

The program sector protection register command utilizes the internal SRAM buffer 1 for processing. Therefore, the contents of buffer 1 will be altered from its previous state when this command is issued.

Table 7-5. Program Sector Protection Register Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Program sector protection register	3DH	2AH	7FH	FCH

Figure 7-3. Program Sector Protection Register



7.1.3 Read Sector Protection Register Command

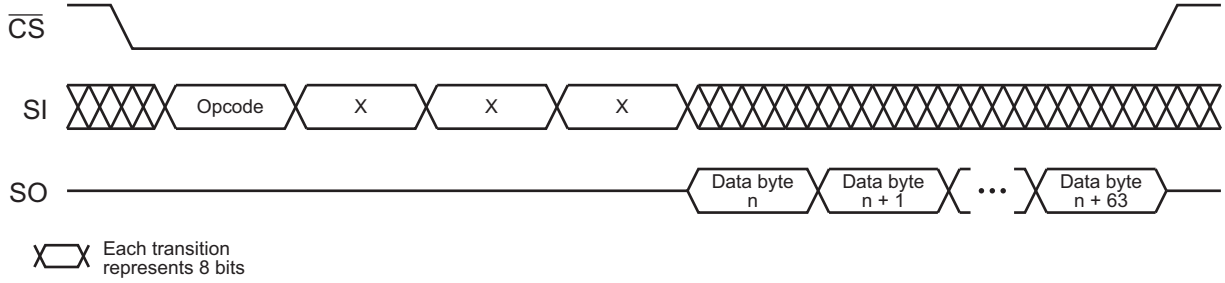
To read the sector protection register, the $\overline{CS}$ pin must first be asserted. Once the $\overline{CS}$ pin has been asserted, an opcode of 32H and three dummy bytes must be clocked in via the SI pin. After the last bit of the opcode and dummy bytes has been clocked in, any additional clock pulses on the SCK pins will result in data for the content of the sector protection register being output on the SO pin. The first byte corresponds to sector 0 (0a, 0b), the second byte corresponds to sector 1, and the last byte (byte 64) corresponds to sector 63. Once the last byte of the sector protection register has been clocked out, any additional clock pulses will result in undefined data being output on the SO pin. The $\overline{CS}$ pin must be deasserted to terminate the read sector protection register operation and put the output into a high-impedance state.

Table 7-6. Read Sector Protection Register Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Read sector protection register	32H	xxH	xxH	xxH

Note: xx = Dummy byte

Figure 7-4. Read Sector Protection Register



7.1.4 Various Aspects About the Sector Protection Register

The sector protection register is subject to a limit of 10,000 erase/program cycles. Users are encouraged to carefully evaluate the number of times the sector protection register will be modified during the course of the application's life cycle. If the application requires the sector protection register to be modified more than the specified limit of 10,000 cycles because the application needs to temporarily unprotect individual sectors (sector protection remains enabled while the sector protection register is reprogrammed), then the application will need to limit this practice. Instead, a combination of temporarily unprotecting individual sectors, along with disabling sector protection completely, will need to be implemented by the application to ensure that the limit of 10,000 cycles is not exceeded.

8. Security Features

8.1 Sector Lockdown

The device incorporates a sector lockdown mechanism that allows each individual sector to be permanently locked so that it becomes read only. This is useful for applications that require the ability to permanently protect a number of sectors against malicious attempts at altering program code or security information. **Once a sector is locked down, it can never be erased or programmed, and it can never be unlocked.**

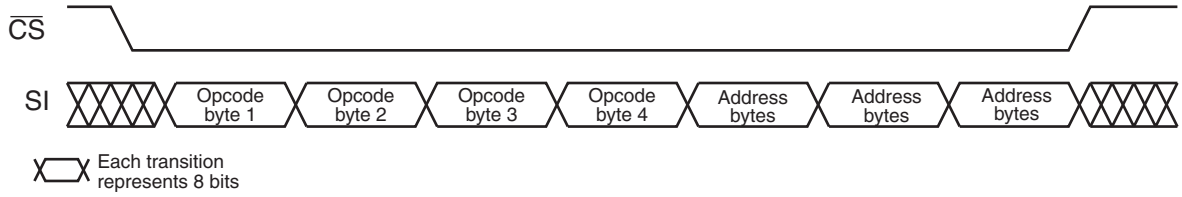
To issue the sector lockdown command, the $\overline{CS}$ pin must first be asserted, as it would be for any other command. Once the $\overline{CS}$ pin has been asserted, the appropriate four-byte opcode sequence must be clocked into the device in the correct order. The four-byte opcode sequence must start with 3DH, and be followed by 2AH, 7FH, and 30H. After the last byte of the command sequence has been clocked in, three address bytes specifying any address within the sector to be locked down must be clocked into the device. After the last address bit has been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed lockdown sequence.

The lockdown sequence should take place in a maximum time of t_P, during which the status register will indicate that the device is busy. If the device is powered down before the completion of the lockdown sequence, then the lockdown status of the sector cannot be guaranteed. In this case, it is recommended that the user read the sector lockdown register to determine the status of the appropriate sector lockdown bits or bytes and reissue the sector lockdown command, if necessary.

Table 8-1. Sector Lockdown

Command	Byte 1	Byte 2	Byte 3	Byte 4
Sector lockdown	3DH	2AH	7FH	30H

Figure 8-1. Sector Lockdown



8.1.1 Sector Lockdown Register

The nonvolatile sector lockdown register contains 64 bytes of data, as shown below:

Table 8-2. Sector Lockdown Register

Sector Number	0 (0a, 0b)	1 to 63
Locked	See Table 8-3	FFH
Unlocked		00H

Table 8-3. Sector 0 (0a, 0b)

	0a (Pages 0-7) Bit 7, 6	0b (Pages 8-127) Bit 5, 4	Bit 3, 2	Bit 1, 0	Data Value
Sectors 0a, 0b unlocked	00	00	00	00	00H
Sector 0a locked (pages 0-7)	11	00	00	00	C0H
Sector 0b locked (pages 8-127)	00	11	00	00	30H
Sectors 0a, 0b locked (pages 0-127)	11	11	00	00	F0H

8.1.2 Reading the Sector Lockdown Register

The sector lockdown register can be read to determine which sectors in the memory array are permanently locked down. To read the sector lockdown register, the $\overline{CS}$ pin must first be asserted. Once the $\overline{CS}$ pin has been asserted, an opcode of 35H and three dummy bytes must be clocked into the device via the SI pin. After the last bit of the opcode and dummy bytes has been clocked in, the data for the content of the sector lockdown register will be clocked out on the SO pin. The first byte corresponds to sector 0 (0a, 0b) the second byte corresponds to sector 1, and the last byte (byte 16) corresponds to sector 15. After the last byte of the sector lockdown register has been read, additional pulses on the SCK pin will simply result in undefined data being output on the SO pin.

Deasserting the $\overline{CS}$ pin will terminate the read sector lockdown register operation and put the SO pin into a high-impedance state.

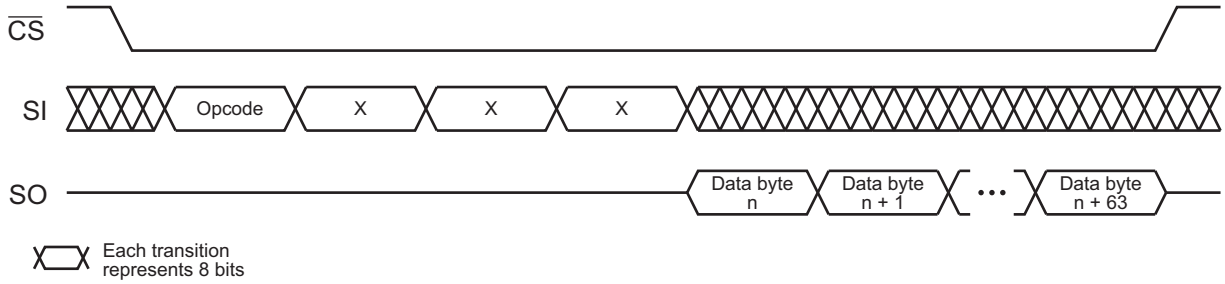
Table 8-4 details the values read from the sector lockdown register.

Table 8-4. Sector Lockdown Register

Command	Byte 1	Byte 2	Byte 3	Byte 4
Read sector lockdown register	35H	xxH	xxH	xxH

Note: xx = Dummy byte.

Figure 8-2. Read Sector Lockdown Register



8.2 Security Register

The device contains a specialized security register that can be used for purposes such as unique device serialization or locked key storage. The register is comprised of a total of 128 bytes that are divided into two portions. The first 64 bytes (byte locations 0 through 63) of the security register are allocated as a one-time user programmable space. Once these 64 bytes have been programmed, they cannot be reprogrammed. The remaining 64 bytes of the register (byte locations 64 through 127) are factory programmed by Atmel, and contain a unique value for each device. The factory programmed data are fixed and cannot be changed.

Table 8-5. Security Register

	Security Register Byte Number									
	0	1	· · ·	62	63	64	65	· · ·	126	127
Data type	One-time user programmable					Atmel factory programmed				

8.2.1 Programming the Security Register

The user programmable portion of the security register does not need to be erased before it is programmed.

To program the security register, the $\overline{CS}$ pin must first be asserted, and then the appropriate four-byte opcode sequence must be clocked into the device in the correct order. The four-byte opcode sequence must start with 9BH, and be followed by 00H, 00H, and 00H. After the last bit of the opcode sequence has been clocked into the device, the data for the content of the 64-byte user programmable portion of the security register must be clocked in.

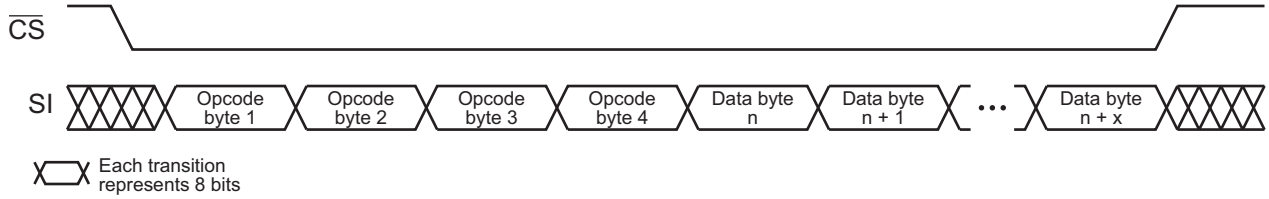
After the last data byte has been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed program cycle. The programming of the security register should take place in a maximum time of t_P, during which the status register will indicate that the device is busy. If the device is powered down during the program cycle, then the contents of the 64-byte user programmable portion of the security register cannot be guaranteed.

If the full 64 bytes of data are not clocked in before the $\overline{CS}$ pin is deasserted, then the values of the byte locations not clocked in cannot be guaranteed. For example, if only the first two bytes are clocked in instead of the complete 64 bytes, then the remaining 62 bytes of the user programmable portion of the security register cannot be guaranteed. Furthermore, if more than 64 bytes of data are clocked into the device, then the data will wrap back around to the beginning of the register. For instance, if 65 bytes of data are clocked in, then the 65th byte will be stored at byte location 0 of the security register.

The user programmable portion of the security register can be programmed only once. Therefore, it is not possible to program only the first two bytes of the register and then program the remaining 62 bytes at a later time.

The program security register command utilizes the internal SRAM buffer 1 for processing. Therefore, the contents of buffer 1 will be altered from its previous state when this command is issued.

Figure 8-3. Program Security Register

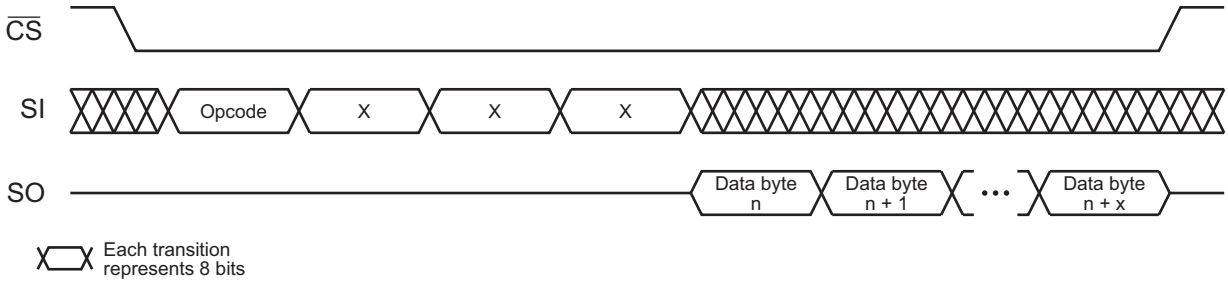


8.2.2 Reading the Security Register

The security register can be read by first asserting the $\overline{CS}$ pin and then clocking in an opcode of 77H, followed by three dummy bytes. After the last don't care bit has been clocked in, the content of the security register can be clocked out on the SO pin. After the last byte of the security register has been read, additional pulses on the SCK pin will simply result in undefined data being output on the SO pin.

Deasserting the $\overline{CS}$ pin will terminate the read security register operation and put the SO pin into a high-impedance state.

Figure 8-4. Read Security Register



9. Additional Commands

9.1 Main Memory Page to Buffer Transfer

A page of data can be transferred from the main memory to either buffer 1 or buffer 2. To start the operation for the standard DataFlash page size (528 bytes), a one-byte opcode, 53H for buffer 1 or 55H for buffer 2, must be clocked into the device, followed by three address bytes comprised of 1 don't care bit, 13 page address bits (PA12 - PA0) that specify the page in main memory that is to be transferred, and 10 don't care bits. To perform a main memory page to buffer transfer for the binary page size (512 bytes), the 53H opcode for buffer 1 or 55H opcode for buffer 2 must be clocked into the device, followed by three address bytes consisting of 2 don't care bits, 13 page address bits (A21 - A9) that specify the page in the main memory that is to be transferred, and 9 don't care bits. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode and the address bytes from the input pin (SI). The transfer of page of data from the main memory to the buffer will begin when the $\overline{CS}$ pin transitions from a low to a high state. During the transfer of a page of data (t_{XFR}), the status register can be read or the RDY/$\overline{BUSY}$ can be monitored to determine whether the transfer has been completed.

9.2 Main Memory Page to Buffer Compare

A page of data in the main memory can be compared to the data in buffer 1 or buffer 2. To initiate the operation for a standard DataFlash page size (528 bytes), a one-byte opcode, 60H for buffer 1 or 61H for buffer 2, must be clocked into the device, followed by three address bytes consisting of 1 don't care bit, 13 page address bits (PA12 - PA0) that specify the page in the main memory that is to be compared to the buffer, and 10 don't care bits. To start a main memory page to buffer compare for a binary page size (512 bytes), the 60H opcode for buffer 1 or 61H opcode for buffer 2 must be clocked into the device, followed by three address bytes consisting of 2 don't care bits, 13 page address bits (A21 - A9) that specify the page in the main memory that is to be compared to the buffer, and 9 don't care bits. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode and the address bytes from the input pin (SI). On the low-to-high transition of the $\overline{CS}$ pin, the data bytes in the selected main memory page will be compared with the data bytes in buffer 1 or buffer 2. During this time (t_{COMP}), the status register and the RDY/$\overline{BUSY}$ pin will indicate that the part is busy. On completion of the compare operation, bit 6 of the status register is updated with the result of the compare.

9.3 Auto Page Rewrite

This mode is needed only when multiple bytes within a page or multiple pages of data are modified in a random fashion within a sector. This mode is a combination of two operations:

1. Main memory page to buffer transfer, and
2. Buffer to main memory page program, with built-in erase.

A page of data is first transferred from the main memory to buffer 1 or buffer 2, and then the same data (from buffer 1 or buffer 2) are programmed back into their original page of main memory. To start the rewrite operation for the standard DataFlash page size (528 bytes), a one-byte opcode, 58H for buffer 1 or 59H for buffer 2, must be clocked into the device, followed by three address bytes comprised of 1 don't care bit, 13 page address bits (PA12-PA0) that specify the page in main memory to be rewritten, and 10 don't care bits. To initiate an auto page rewrite for a binary page size (512 bytes), the 58H opcode for buffer 1 or 59H opcode for buffer 2 must be clocked into the device, followed by three address bytes consisting of 2 don't care bits, 13 page address bits (A21 - A9) that specify the page in the main memory that is to be written, and 9 don't care bits. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will first transfer data from the page in main memory to a buffer and then program the data from the buffer back into same page of main memory. The operation is internally self-timed, and should take place in a maximum time of t_{EP}. During this time, the status register and the RDY/$\overline{BUSY}$ pin will indicate that the part is busy.

If a sector is programmed or reprogrammed sequentially page by page, then the programming algorithm shown in Figure 23-1, page 41 is recommended. Otherwise, if multiple bytes in a page or several pages are programmed randomly in a sector, then the programming algorithm shown in Figure 23-2, page 42 is recommended. Each page within a sector must be updated/rewritten at least once within every 20,000 cumulative page erase/program operations in that sector. Please contact Atmel for availability of devices that are specified to exceed the 20,000 cycle cumulative limit.

9.4 Status Register Read

The status register can be used to determine the device's ready/busy status, page size, a main memory page to buffer compare operation result, the sector protection status, or the device density. The status register can be read at any time, including during an internally self-timed program or erase operation. To read the status register, the $\overline{CS}$ pin must be asserted and the opcode of D7H must be loaded into the device. After the opcode is clocked in, the one-byte status register will be clocked out on the output pin (SO), starting with the next clock cycle. The data in the status register, starting with the msb (bit 7), will be clocked out on the SO pin during the next eight clock cycles. After the one byte of the status register has been clocked out, the sequence will repeat itself (as long as $\overline{CS}$ remains low and SCK is being toggled). The data in the status register is constantly updated, and so each repeating sequence will output new data.

Ready/busy status is indicated using bit 7 of the status register. If bit 7 is a one, then the device is not busy and is ready to accept the next command. If bit 7 is a zero, then the device is in a busy state. Since the data in the status register is constantly updated, the user must toggle the SCK pin to check the ready/busy status.

There are several operations that can cause the device to be in a busy state:

- Main memory page to buffer transfer
- Main memory page to buffer compare
- Buffer to main memory page program
- Main memory page program through buffer
- Page erase, block erase, sector erase, and chip erase
- Auto page rewrite

The result of the most recent main memory page to buffer compare operation is indicated using bit 6 of the status register. If bit 6 is a zero, then the data in the main memory page matches the data in the buffer. If bit 6 is a one, then at least one bit of the data in the main memory page does not match the data in the buffer.

Bit 1 of the status register is used to provide information to the user whether sector protection has been enabled or disabled, either by the software-controlled or hardware-controlled method. A logic one indicates that sector protection has been enabled, and logic zero indicates that sector protection has been disabled.

Bit 0 o the status register indicates whether the page size of the main memory array is configured for a "power of two" binary page size (512 bytes) or a standard DataFlash page size (528 bytes). If bit 0 is a one, then the page size is set to 512 bytes. If bit 0 is a zero, then the page size is set to 528 bytes.

The device density is indicated using bits 5, 4, 3, and 2 of the status register. For the AT45DB321D, the four bits are 1101. The decimal value of these four binary bits does not equate to the device density — the four bits represent a combinational code relating to differing densities of DataFlash devices. The device density is not the same as the density code indicated in the JEDEC device ID information. The device density is provided only for backward compatibility.

Table 9-1. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RDY/$\overline{BUSY}$	COMP	1	1	0	1	Protect	Page size

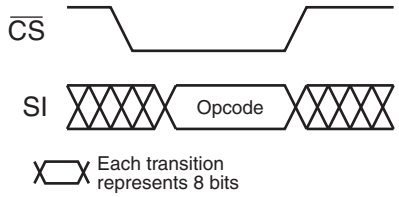
10. Deep Power-down

After an initial power-up, the device will default to standby mode. The deep power-down command allows the device to enter into the lowest power-consumption mode. To enter the deep power-down mode, the $\overline{CS}$ pin must first be asserted. Once the $\overline{CS}$ pin has been asserted, an opcode of B9H must be clocked in via the input pin (SI). After the last bit of the command has been clocked in, the $\overline{CS}$ pin must be deasserted to initiate deep power-down operation. After the $\overline{CS}$ pin is deasserted, the device will enter the deep power-down mode within a maximum time of t_{EDPD}. Once the device has entered the deep power-down mode, all instructions are ignored, except for the resume from deep power-down commands.

Table 10-1. Deep Power-down

Command	Opcode
Deep power-down	B9H

Figure 10-1. Deep Power-down



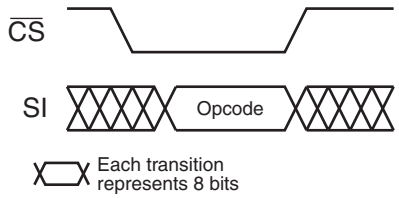
10.1 Resume from Deep Power-down

The resume from deep power-down command takes the device out of the deep power-down mode and returns it to the normal standby mode. To resume from deep power-down mode, the $\overline{CS}$ pin must first be asserted, and an opcode of ABH must be clocked in via the input pin (SI). After the last bit of the command has been clocked in, the $\overline{CS}$ pin must be deasserted to terminate the deep power-down mode. After the $\overline{CS}$ pin is deasserted, the device will return to the normal standby mode within a maximum time of t_{RDPD}. The $\overline{CS}$ pin must remain high during the t_{RDPD} time before the device can receive any commands. After resuming from deep power-down, the device will return to the normal standby mode.

Table 10-2. Resume from Deep Power-down

Command	Opcode
Resume from deep power-down	ABH

Figure 10-2. Resume from Deep Power-Down



11. “Power of Two” Binary Page Size Option

“Power of two” binary page size configuration register is a user programmable, nonvolatile register that allows the page size of the main memory to be configured for binary page size (512 bytes) or standard DataFlash page size (528 bytes). The power of two page size is a one-time programmable configuration register, and once the device is configured for power of two page size, it cannot be reconfigured again. The devices are initially shipped with the page size set to 528 bytes. The user has the option of ordering binary page size (512-byte) devices from the factory. For details, please refer to Section 24. “Ordering Information” on page 43.

For the binary power of two page size to become effective, the following steps must be followed:

1. Program the one-time programmable configuration resister using the opcode sequence: 3DH, 2AH, 80H, and A6H (see Section 11.1).
2. Power cycle the device (i.e., power down and power up again).
3. The page for the binary page size can now be programmed.

If the above steps to set the page size prior to page programming are not followed, incorrect data during a read operation may be encountered.

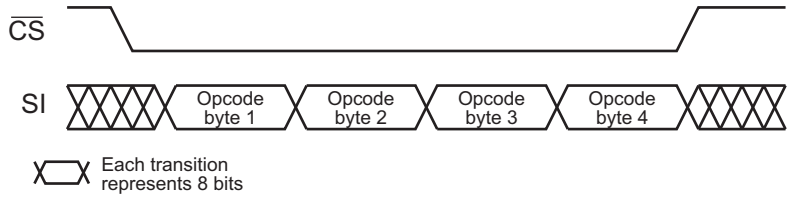
11.1 Programming the Configuration Register

To program the configuration register for power of two binary page size, the $\overline{CS}$ pin must first be asserted, as it would be with any other command. Once the $\overline{CS}$ pin has been asserted, the appropriate four-byte opcode sequence must be clocked into the device in the correct order. The four-byte opcode sequence must start with 3DH, followed by 2AH, 80H, and A6H. After the last bit of the opcode sequence has been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed program cycle. The programming of the configuration register should take place in a maximum time of t_P, during which time the status register will indicate that the device is busy. The device must be power cycled after the completion of the program cycle to set the power of two page size. If the device is powered-down before the completion of the program cycle, then setting the configuration register cannot be guaranteed. However, the user should check bit 0 of the status register to see whether the page size was configured for binary page size or not. If not, the command can be issued again.

Table 11-1. Programming the Configuration Register

Command	Byte 1	Byte 2	Byte 3	Byte 4
Power of two page size	3DH	2AH	80H	A6H

Figure 11-1. Erase Sector Protection Register



12. Manufacturer and Device ID Read

Identification information can be read from the device to enable systems to electronically query and identify the device while it is in the system. The identification method and the command opcode comply with the JEDEC standard for “Manufacturer and Device ID Read Methodology for SPI Compatible Serial Interface Memory Devices.” The type of information that can be read from the device includes the JEDEC-defined manufacturer ID, the vendor-specific device ID, and the vendor-specific extended device information.

To read the identification information, the $\overline{CS}$ pin must first be asserted, and then the opcode of 9FH must be clocked into the device. After the opcode has been clocked in, the device will begin outputting the identification data on the SO pin during the subsequent clock cycles. The first byte to be output will be the manufacturer ID, followed by two bytes of device ID information. The fourth byte output will be the extended device information string length, which will be 00H to indicate that no extended

device information follows. As indicated in the JEDEC standard, reading the extended device information string length and any subsequent data is optional.

Deasserting the $\overline{CS}$ pin will terminate the manufacturer and device ID read operation and put the SO pin into a high-impedance state. The $\overline{CS}$ pin can be deasserted at any time, and does not require that a full byte of data be read.

12.1 Manufacturer and Device ID Information

12.1.1 Byte 1 – Manufacturer ID

Hex Value	JEDEC Assigned Code							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1FH	0	0	0	1	1	1	1	1

Manufacturer ID	1FH = Atmel

12.1.2 Byte 2 – Device ID (Part 1)

Hex Value	Family Code			Density Code				
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
27H	0	0	1	0	0	1	1	1

Family code	001 = DataFlash
Density code	00111 = 32Mb

12.1.3 Byte 3 – Device ID (Part 2)

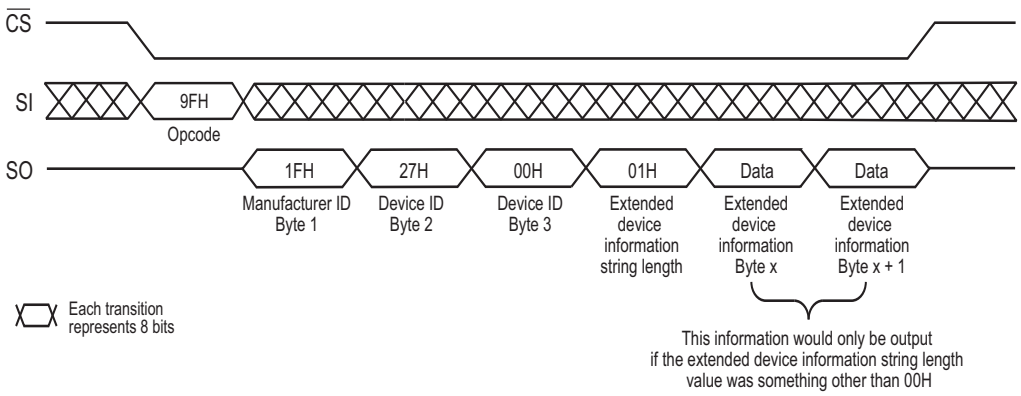
Hex Value	MLC Code			Product Version Code				
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	0	0	0	0	0	0	0	1

MLC code	000 = 1-bit/cell technology
Product version	00001 = Second version

12.1.4 Byte 4 – Extended Device Information String Length

Hex Value	Byte Count							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	0	0	0	0	0	0	0	0

Byte count	00H = 0 bytes of Information



Note: Based on JEDEC publication 106 (JEP106), manufacturer ID data can be comprised of any number of bytes. Some manufacturers may have manufacturer ID codes that are two, three, or even four bytes long, with the first byte(s) in the sequence being 7FH. A system should detect code 7FH as a “continuation code” and continue to read manufacturer ID bytes. The first non-7FH byte would signify the last byte of manufacturer ID data. For Atmel (and some other manufacturers), the manufacturer ID data is comprised of only one byte.

12.2 Operation Mode Summary

The commands described previously can be grouped into four different categories to make clearer which commands can be executed at what times.

Group A commands consist of:

1. Main memory page read
2. Continuous array read
3. Read sector protection register
4. Read sector lockdown register
5. Read security register

Group B commands consist of:

1. Page erase
2. Block erase
3. Sector erase
4. Chip erase
5. Main memory page to buffer 1 (or 2) transfer
6. Main memory page to buffer 1 (or 2) compare
7. Buffer 1 (or 2) to main memory page program, with built-in erase
8. Buffer 1 (or 2) to main memory page program, without built-in erase
9. Main memory page program through buffer 1 (or 2)
10. Auto page rewrite

Group C commands consist of:

1. Buffer 1 (or 2) read
2. Buffer 1 (or 2) write
3. Status register read
4. Manufacturer and device ID read

Group D commands consist of:

1. Erase sector protection register
2. Program sector protection register
3. Sector lockdown
4. Program security register

If a group A command is in progress (not fully completed), then another command from group A, B, C, or D should not be started. However, during the internally self-timed portion of group B commands, any command in group C can be executed. The group B commands using buffer 1 should use group C commands using buffer 2, and vice versa. Finally, during the internally self-timed portion of a group D command, only the status register read command should be executed.

13. Command Tables

Table 13-1. Read Commands

Command	Opcode
Main memory page read	D2H
Continuous array read (legacy command)	E8H
Continuous array read (low frequency)	03H
Continuous array read (high frequency)	0BH
Buffer 1 read (low frequency)	D1H
Buffer 2 read (low frequency)	D3H
Buffer 1 read	D4H
Buffer 2 read	D6H

Table 13-2. Program and Erase Commands

Command	Opcode
Buffer 1 write	84H
Buffer 2 write	87H
Buffer 1 to main memory page program, with built-in erase	83H
Buffer 2 to main memory page program, with built-in erase	86H
Buffer 1 to main memory page program, without built-in erase	88H
Buffer 2 to main memory page program, without built-in erase	89H
Page erase	81H
Block erase	50H
Sector erase	7CH
Chip erase	C7H, 94H, 80H, 9AH
Main memory page program through buffer 1	82H
Main memory page program through buffer 2	85H

Table 13-3. Protection and Security Commands

Command	Opcode
Enable sector protection	3DH + 2AH + 7FH + A9H
Disable sector protection	3DH + 2AH + 7FH + 9AH
Erase sector protection register	3DH + 2AH + 7FH + CFH
Program sector protection register	3DH + 2AH + 7FH + FCH
Read sector protection register	32H
Sector lockdown	3DH + 2AH + 7FH + 30H
Read sector lockdown register	35H
Program security register	9BH + 00H + 00H + 00H
Read security register	77H

Table 13-4. Additional Commands

Command	Opcode
Main memory page to buffer 1 transfer	53H
Main memory page to buffer 2 transfer	55H
Main memory page to buffer 1 compare	60H
Main memory page to buffer 2 compare	61H
Auto page rewrite through buffer 1	58H
Auto page rewrite through buffer 2	59H
Deep power-down	B9H
Resume from deep power-down	ABH
Status register read	D7H
Manufacturer and device ID read	9FH

Table 13-5. Legacy Commands[1]

Command	Opcode
Buffer 1 read	54H
Buffer 2 read	56H
Main memory page read	52H
Continuous array read	68H
Status register read	57H

Note: 1. These legacy commands are not recommended for new designs.

Table 13-6. Detailed Bit-level Addressing Sequence for Binary Page Size (512 Bytes)

Page Size = 512-bytes									Address Byte								Address Byte								Address Byte								Additional Don't Care Bytes
Opcode	Opcode								Reserved	Reserved	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
03h	0	0	0	0	0	0	1	1	x	x	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A
0Bh	0	0	0	0	1	0	1	1	x	x	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	1
50h	0	1	0	1	0	0	0	0	x	x	A	A	A	A	A	A	A	A	A	A	x	x	x	x	x	x	x	x	x	x	x	x	N/A
53h	0	1	0	1	0	0	1	1	x	x	A	A	A	A	A	A	A	A	A	A	A	A	A	x	x	x	x	x	x	x	x	x	N/A
55h	0	1	0	1	0	1	0	1	x	x	A	A	A	A	A	A	A	A	A	A	A	A	A	x	x	x	x	x	x	x	x	x	N/A
58h	0	1	0	1	1	0	0	0	x	x	A	A	A	A	A	A	A	A	A	A	A	A	A	x	x	x	x	x	x	x	x	x	N/A
59h	0	1	0	1	1	0	0	1	x	x	A	A	A	A	A	A	A	A	A	A	A	A	A	x	x	x	x	x	x	x	x	x	N/A
60h	0	1	1	0	0	0	0	0	x	x	A	A	A	A	A	A	A	A	A	A	A	A	A	x	x	x	x	x	x	x	x	x	N/A
61h	0	1	1	0	0	0	0	1	x	x	A	A	A	A	A	A	A	A	A	A	A	A	A	x	x	x	x	x	x	x	x	x	N/A
77h	0	1	1	1	0	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	N/A
7Ch	0	1	1	1	1	1	0	0	x	x	A	A	A	A	A	A	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	N/A
81h	1	0	0	0	0	0	0	1	x	x	A	A	A	A	A	A	A	A	A	A	A	A	A	x	x	x	x	x	x	x	x	x	N/A
82h	1	0	0	0	0	0	1	0	x	x	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A
83h	1	0	0	0	0	0	1	1	x	x	A	A	A	A	A	A	A	A	A	A	A	A	A	x	x	x	x	x	x	x	x	x	N/A
84h	1	0	0	0	0	1	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	A	A	A	A	A	A	A	A	A	N/A
85h	1	0	0	0	0	1	0	1	x	x	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A
86h	1	0	0	0	0	1	1	0	x	x	A	A	A	A	A	A	A	A	A	A	A	A	A	x	x	x	x	x	x	x	x	x	N/A
87h	1	0	0	0	0	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	A	A	A	A	A	A	A	A	A	N/A
88h	1	0	0	0	1	0	0	0	x	x	A	A	A	A	A	A	A	A	A	A	A	A	A	x	x	x	x	x	x	x	x	x	N/A
89h	1	0	0	0	1	0	0	1	x	x	A	A	A	A	A	A	A	A	A	A	A	A	A	x	x	x	x	x	x	x	x	x	N/A
9Fh	1	0	0	1	1	1	1	1					N/A							N/A								N/A					N/A
B9h	1	0	1	1	1	0	0	1					N/A							N/A								N/A					N/A
ABh	1	0	1	0	1	0	1	1					N/A							N/A								N/A					N/A
D1h	1	1	0	1	0	0	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	A	A	A	A	A	A	A	A	A	N/A
D2h	1	1	0	1	0	0	1	0	x	x	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	4
D3h	1	1	0	1	0	0	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	A	A	A	A	A	A	A	A	A	N/A
D4h	1	1	0	1	0	1	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	A	A	A	A	A	A	A	A	A	1
D6h	1	1	0	1	0	1	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	A	A	A	A	A	A	A	A	A	1
D7h	1	1	0	1	0	1	1	1					N/A							N/A								N/A					N/A
E8h	1	1	1	0	1	0	0	0	x	x	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	4

Note: x = Don't care.

Table 13-7. Detailed Bit-level Addressing Sequence for Standard DataFlash Page Size (528 Bytes)

Page Size = 528-bytes									Address Byte								Address Byte								Address Byte								Additional Don't Care Bytes
Opcode	Opcode								Reserved	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	BA9	BA8	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0	
03h	0	0	0	0	0	0	1	1	x	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	N/A
0Bh	0	0	0	0	1	0	1	1	x	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	1
50h	0	1	0	1	0	0	0	0	x	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	x	x	x	N/A
53h	0	1	0	1	0	0	1	1	x	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	N/A
55h	0	1	0	1	0	1	0	1	x	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	N/A
58h	0	1	0	1	1	0	0	0	x	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	N/A
59h	0	1	0	1	1	0	0	1	x	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	N/A
60h	0	1	1	0	0	0	0	0	x	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	N/A
61h	0	1	1	0	0	0	0	1	x	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	N/A
77h	0	1	1	1	0	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	N/A
7Ch	0	1	1	1	1	1	0	0	x	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	N/A
81h	1	0	0	0	0	0	0	1	x	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	N/A
82h	1	0	0	0	0	0	1	0	x	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	N/A
83h	1	0	0	0	0	0	1	1	x	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	N/A
84h	1	0	0	0	0	1	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	B	N/A
85h	1	0	0	0	0	1	0	1	x	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	N/A
86h	1	0	0	0	0	1	1	0	x	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	N/A
87h	1	0	0	0	0	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	B	N/A
88h	1	0	0	0	1	0	0	0	x	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	N/A
89h	1	0	0	0	1	0	0	1	x	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	N/A
9Fh	1	0	0	1	1	1	1	1				N/A								N/A								N/A					N/A
B9h	1	0	1	1	1	0	0	1				N/A								N/A								N/A					N/A
ABh	1	0	1	0	1	0	1	1				N/A								N/A								N/A					N/A
D1h	1	1	0	1	0	0	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	B	N/A
D2h	1	1	0	1	0	0	1	0	x	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	4
D3h	1	1	0	1	0	0	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	B	N/A
D4h	1	1	0	1	0	1	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	B	1
D6h	1	1	0	1	0	1	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	B	1
D7h	1	1	0	1	0	1	1	1				N/A								N/A								N/A					N/A
E8h	1	1	1	0	1	0	0	0	x	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	4

Note: P = Page address bit.
B = Byte/buffer address bit.
x = Don't care.

14. Power-on/Reset State

When power is first applied to the device, or when recovering from a reset condition, the device will default to Mode 3. In addition, the output pin (SO) will be in a high-impedance state, and a high-to-low transition on the $\overline{CS}$ pin will be required to start a valid instruction. The mode (Mode 3 or Mode 0) will be automatically selected on every falling edge of $\overline{CS}$ by sampling the inactive clock state.

14.1 Initial Power-up/Reset Timing Restrictions

At power-up, the device must not be selected until the supply voltage reaches V_{CC} (min.) and a further delay of t_{VCSL}. During power-up, the internal power-on reset circuitry keeps the device in reset mode until V_{CC} rises above the power-on reset threshold value (V_{POR}). At this time, all operations are disabled and the device does not respond to any commands. After power-up is applied and V_{CC} is at the minimum operating voltage, V_{CC} (min.), the t_{VCSL} delay is required before the device can be selected in order to perform a read operation.

Similarly, the t_{PUW} delay is required after V_{CC} rises above the power-on reset threshold value (V_{POR}) before the device can perform a write (program or erase) operation. After initial power-up, the device will default to standby mode.

Table 14-1. Initial Power-up/Reset Timing Restrictions

Symbol	Parameter	Min	Typ	Max	Unit
t_{VCSL}	V_{CC} (min.) to chip select low	70			µs
t_{PUW}	Power-up device delay before write allowed			20	ms
V_{POR}	Power-on reset voltage	1.5		2.5	V

15. System Considerations

The RapidS serial interface is controlled by the SCK clock, SI serial input, and $\overline{CS}$ chip select pins. These signals must rise and fall monotonically and be free from noise. Excessive noise or ringing on these pins can be misinterpreted as multiple edges and cause improper operation of the device. The PC board traces must be kept to a minimum distance or appropriately terminated to ensure proper operation. If necessary, decoupling capacitors can be added on these pins to provide filtering against noise glitches.

As system complexity continues to increase, voltage regulation is becoming more important. A key element of any voltage regulation scheme is its current sourcing capability. Like all flash memories, the peak current for a DataFlash device occurs during the programming and erase operation. The regulator needs to supply this peak current requirement. An under-specified regulator can cause current starvation. Besides increasing system noise, current starvation during programming or erase can lead to improper operation and possible data corruption.

16. Electrical Specifications

Temperature under bias . . . . . -55°C to +125°C

Storage temperature . . . . . -65°C to +150°C

All input voltages (except V_{CC} but including NC pins) with respect to ground . . . . . -0.6V to +6.25V

All output voltages with respect to ground . . . . . -0.6V to V_{CC} + 0.6V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. The "Absolute Maximum Ratings" are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Voltage Extremes referenced in the "Absolute Maximum Ratings" are intended to accommodate short duration undershoot/overshoot conditions and does not imply or guarantee functional device operation at these levels for any extended period of time.

Table 16-1. DC and AC Operating Range

	Atmel AT45DB321D (2.5V Version)	Atmel AT45DB321D
Operating temperature (case)	-40°C to 85°C	-40°C to 85°C
V_{CC} power supply	2.5V to 3.6V	2.7V to 3.6V

Table 16-2. DC Characteristics

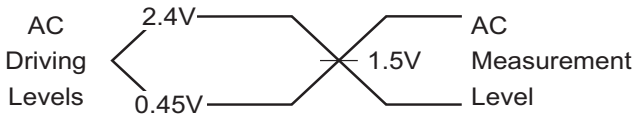
Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DP}	Deep power-down current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		15	25	µA
I_{SB}	Standby current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		25	50	µA
I_{CC1} (1)	Active current, read operation	f = 20MHz; I_{OUT} = 0mA; V_{CC} = 3.6V		7	10	mA
		f = 33MHz; I_{OUT} = 0mA; V_{CC} = 3.6V		8	12	mA
		f = 50MHz; I_{OUT} = 0mA; V_{CC} = 3.6V		10	14	mA
		f = 66MHz; I_{OUT} = 0mA; V_{CC} = 3.6V		11	15	mA
I_{CC2}	Active current, program/erase operation	V_{CC} = 3.6V		12	17	mA
I_{LI}	Input load current	V_{IN} = CMOS levels			1	µA
I_{LO}	Output leakage current	$V_{I/O}$ = CMOS levels			1	µA
V_{IL}	Input low voltage				V_{CC} × 0.3	V
V_{IH}	Input high voltage		V_{CC} × 0.7			V
V_{OL}	Output low voltage	I_{OL} = 1.6mA; V_{CC} = 2.7V			0.4	V
V_{OH}	Output high voltage	I_{OH} = -100µA	V_{CC} - 0.2V			V

Notes: 1. I_{CC1} during a buffer read is 20mA, maximum, @ 20MHz.
2. All inputs (SI, SCK, CS#, WP#, and RESET#) are guaranteed by design to be 5V tolerant.

Table 16-3. AC Characteristics – Atmel RapidS / Serial Interface

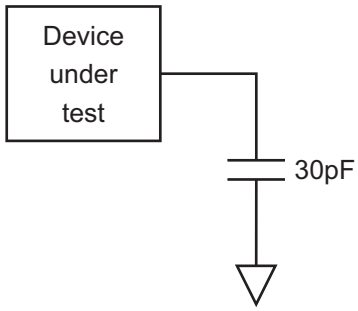
Symbol	Parameter	Atmel AT45DB321D (2.5V Version)			Atmel AT45DB321D			Unit
		Min	Typ	Max	Min	Typ	Max	
f_{SCK}	SCK frequency			50			66	MHz
f_{CAR1}	SCK frequency for continuous array read			50			66	MHz
f_{CAR2}	SCK frequency for continuous array read (Low frequency)			33			33	MHz
t_{WH}	SCK high time	6.8			6.8			ns
t_{WL}	SCK low time	6.8			6.8			ns
t_{SCKR}[1]	SCK rise time, peak-to-peak (slew rate)	0.1			0.1			V/ns
t_{SCKF}[1]	SCK fall time, peak-to-peak (slew rate)	0.1			0.1			V/ns
t_{CS}	Minimum $\overline{CS}$ high time	50			50			ns
t_{CSS}	$\overline{CS}$ setup time	5			5			ns
t_{CSH}	$\overline{CS}$ hold time	5			5			ns
t_{CSB}	$\overline{CS}$ high to RDY/$\overline{BUSY}$ low			100			100	ns
t_{SU}	Data in setup time	2			2			ns
t_{H}	Data in hold time	3			3			ns
t_{HO}	Output hold time	0			0			ns
t_{DIS}	Output disable time		27	35		27	35	ns
t_{V}	Output valid			8			6	ns
t_{WPE}	$\overline{WP}$ low to protection enabled			1			1	µs
t_{WPD}	$\overline{WP}$ high to protection disabled			1			1	µs
t_{EDPD}	$\overline{CS}$ high to deep power-down mode			3			3	µs
t_{RDPD}	$\overline{CS}$ high to standby mode			35			35	µs
t_{XFR}	Page to buffer transfer time			300			300	µs
t_{comp}	Page to buffer compare time			300			300	µs
t_{EP}	Page erase and programming time (512-/528-bytes)		17	40		17	40	ms
t_{P}	Page programming time (512/528 bytes)		3	6		3	6	ms
t_{PE}	Page erase time (512/528 bytes)		15	35		15	35	ms
t_{BE}	Block erase time (4,096/4,224 bytes)		45	100		45	100	ms
t_{SE}	Sector erase time (131,072/135,168 bytes)		1.6	5		1.6	5	s
t_{CE}	Chip erase time		TBD	TBD		TBD	TBD	s
t_{RST}	$\overline{RESET}$ pulse width	10			10			µs
t_{REC}	$\overline{RESET}$ recovery time			1			1	µs

17. Input Test Waveforms and Measurement Levels



t_R, t_F < 2ns (10% to 90%)

18. Output Test Load



19. AC Waveforms

Six different timing waveforms are shown on page 31. Waveform 1 shows the SCK signal being low when $\overline{CS}$ makes a high-to-low transition, and waveform 2 shows the SCK signal being high when $\overline{CS}$ makes a high-to-low transition. In both cases, output SO becomes valid while the SCK signal is still low (SCK low time is specified as t_{WL}). Timing waveforms 1 and 2 conform to RapidS serial interface, but for frequencies up to 66MHz. Waveforms 1 and 2 are compatible with SPI Mode 0 and SPI Mode 3, respectively.

Waveform 3 and waveform 4 illustrate general timing diagram for RapidS serial interface. These are similar to waveform 1 and waveform 2, except that output SO is not restricted to become valid during the t_{WL} period. These timing waveforms are valid over the full frequency range (maximum frequency = 66MHz) of the RapidS serial case.

Table 19-1. Waveform 1 – SPI Mode 0 Compatible (for frequencies up to 66MHz)

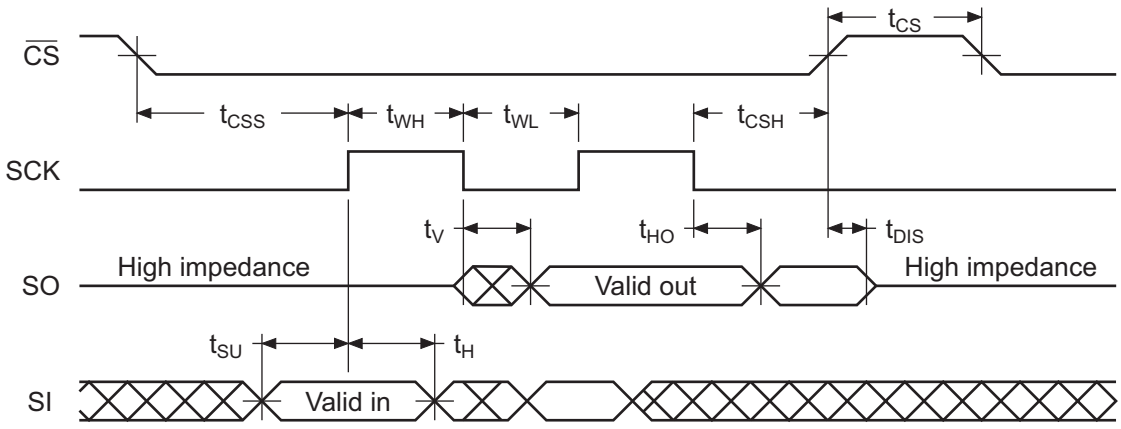


Table 19-2. Waveform 2 – SPI Mode 3 Compatible (for frequencies up to 66MHz)

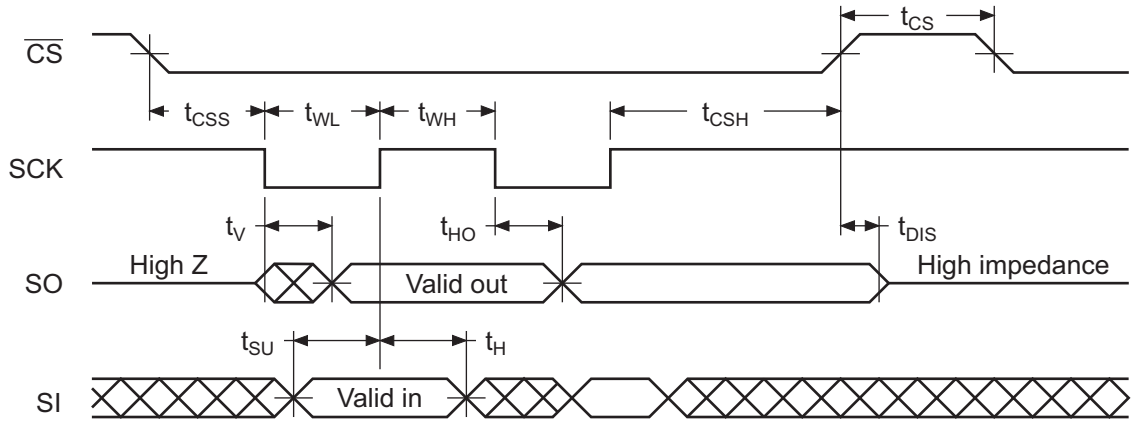


Table 19-3. Waveform 3 – Atmel RapidS Mode 0 (F_{MAX} = 66MHz)

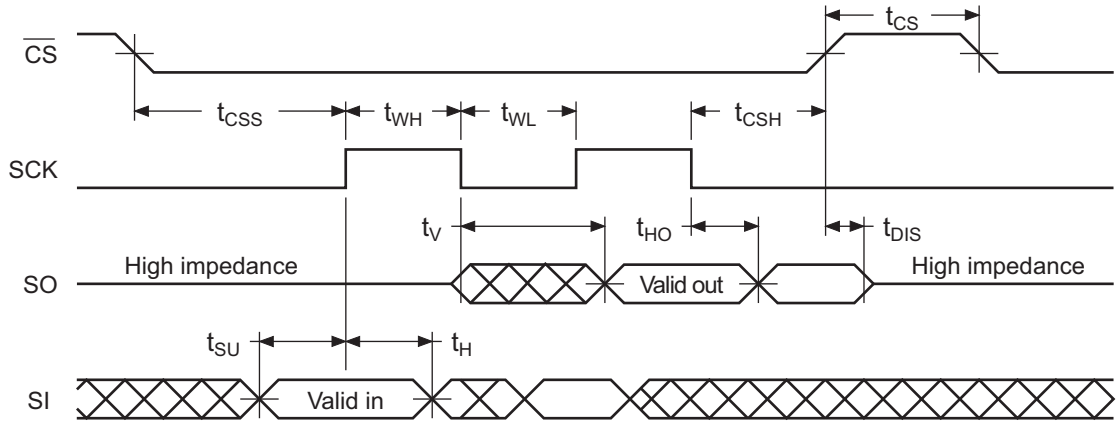
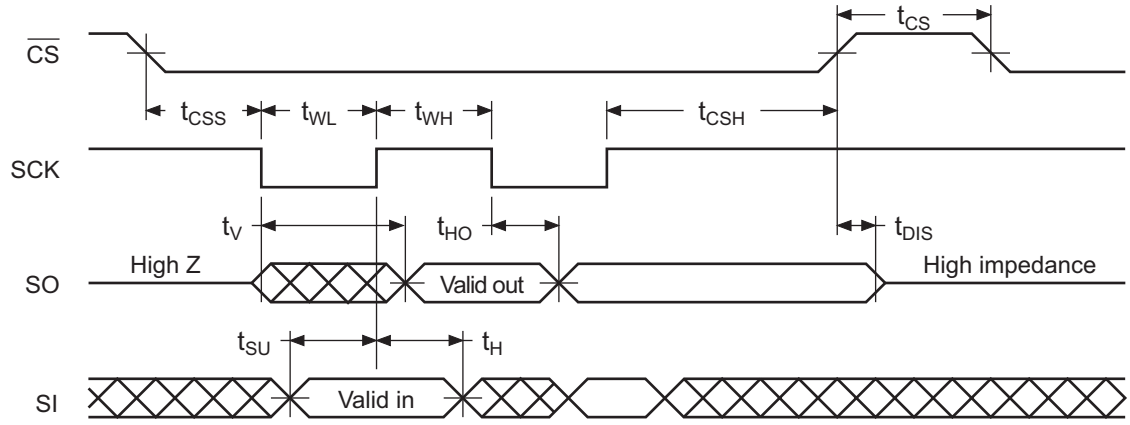


Table 19-4. Waveform 4 – Atmel RapidS Mode 3 (F_{MAX} = 66MHz)

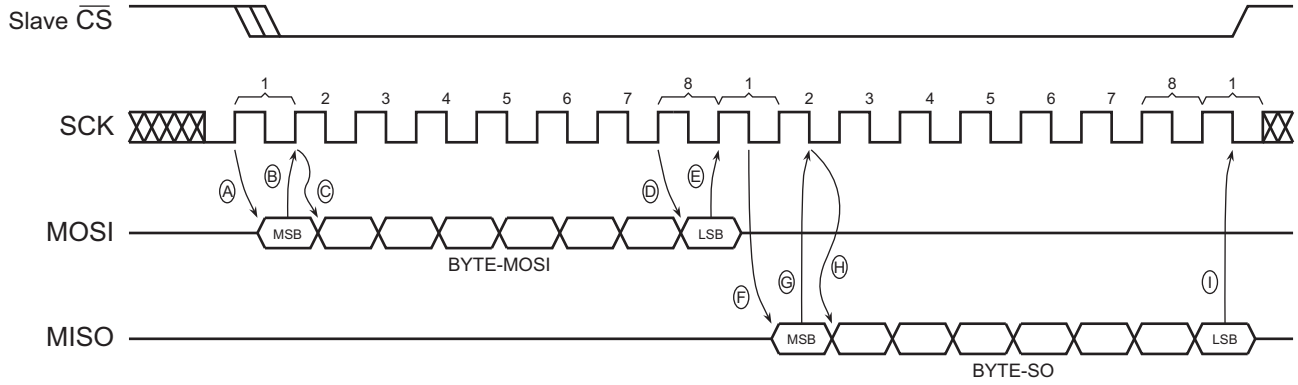


19.1 Utilizing the Atmel RapidS Function

To take advantage of the RapidS function's ability to operate at higher clock frequencies, a full clock cycle must be used to transmit data back and forth across the serial bus. The DataFlash device is designed to always clock its data out on the falling edge of the SCK signal and clock data in on the rising edge of SCK.

For full clock cycle operation to be achieved when the DataFlash device is clocking data out on the falling edge of SCK, the host controller should wait until the next falling edge of SCK to latch the data in. Similarly, the host controller should clock its data out on the rising edge of SCK in order to give the DataFlash device a full clock cycle to latch the incoming data in on the next rising edge of SCK.

Figure 19-1. Atmel RapidS Mode

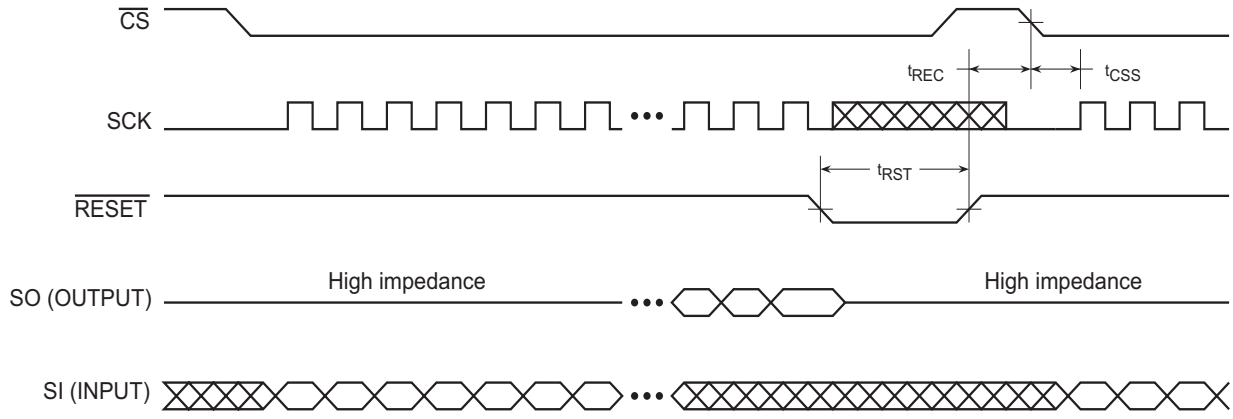


MOSI = Master Out, Slave In
MISO = Master In, Slave Out
The Master is the host controller and the Slave is the DataFlash

The Master always clocks data out on the rising edge of SCK and always clocks data in on the falling edge of SCK.
The Slave always clocks data out on the falling edge of SCK and always clocks data in on the rising edge of SCK.

A. Master clocks out first bit of BYTE-MOSI on the rising edge of SCK
B. Slave clocks in first bit of BYTE-MOSI on the next rising edge of SCK
C. Master clocks out second bit of BYTE-MOSI on the same rising edge of SCK
D. Last bit of BYTE-MOSI is clocked out from the Master
E. Last bit of BYTE-MOSI is clocked into the slave
F. Slave clocks out first bit of BYTE-SO
G. Master clocks in first bit of BYTE-SO
H. Slave clocks out second bit of BYTE-SO
I. Master clocks in last bit of BYTE-SO

Figure 19-2. Reset Timing



Note: The $\overline{CS}$ signal should be in the high state before the $\overline{RESET}$ signal is deasserted.

Figure 19-3. Command Sequence for Read/Write Operations for a 512-Byte Page Size (Except Status Register Read, Manufacturer, and Device ID Read)

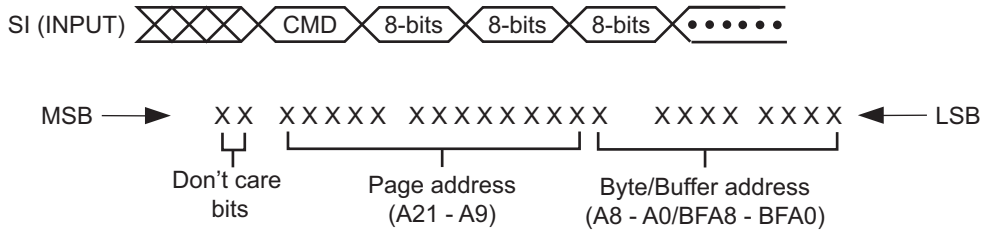
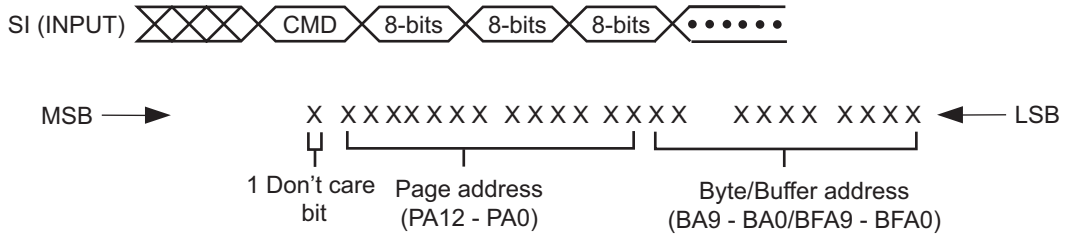


Figure 19-4. Command Sequence for Read/Write Operations for a 528-Byte Page Size (Except Status Register Read, Manufacturer, and Device ID Read)



20. Write Operations

The following block diagram and waveforms illustrate the various write sequences available.

Figure 20-1. Block Diagram

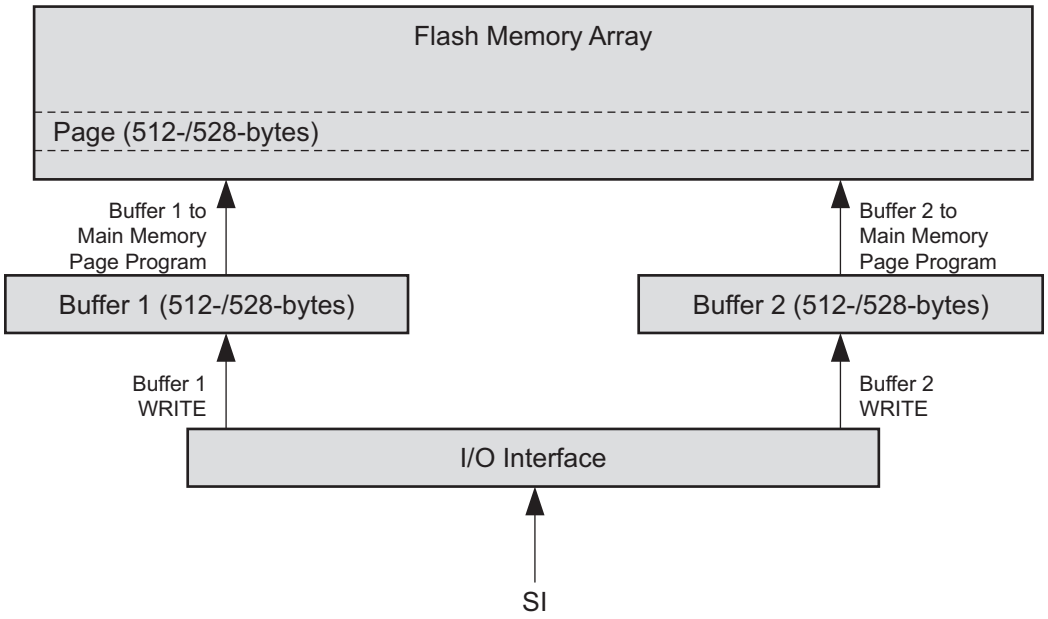


Figure 20-2. Buffer Write

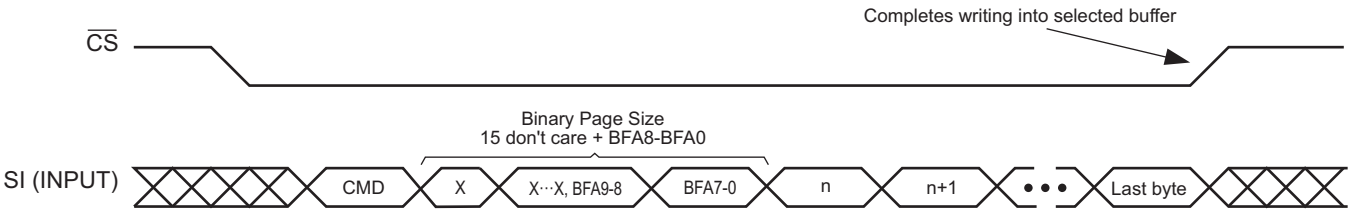
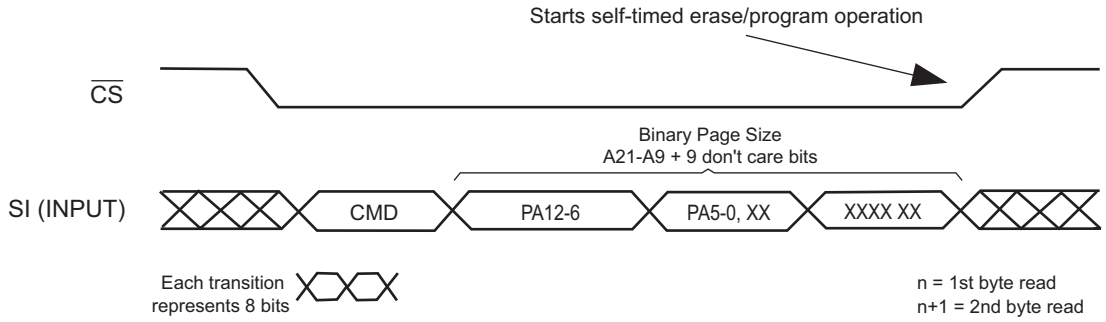


Figure 20-3. Buffer to Main Memory Page Program (Data from Buffer Programmed into Flash Page)



21. Read Operations

The following block diagram and waveforms illustrate the various read sequences available.

Figure 21-1. Block Diagram

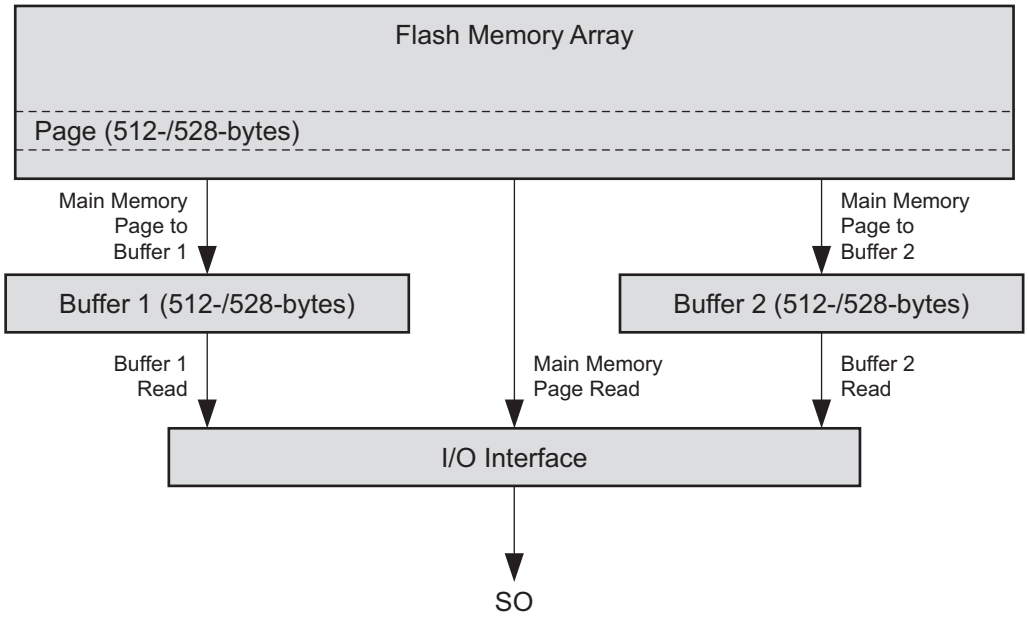


Figure 21-2. Main Memory Page Read

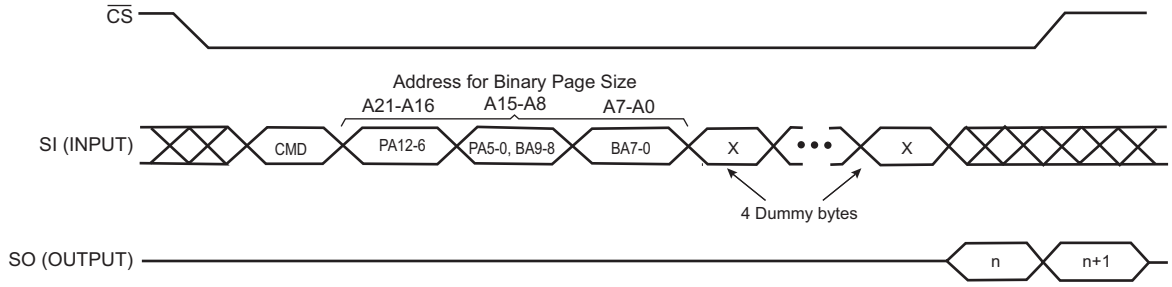


Figure 21-3. Main Memory Page to Buffer Transfer (Data from Flash Page Read into Buffer)

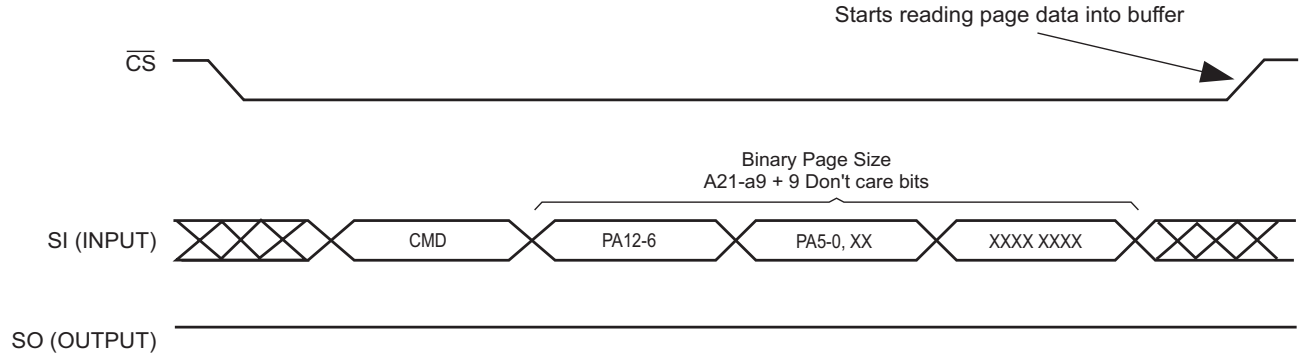
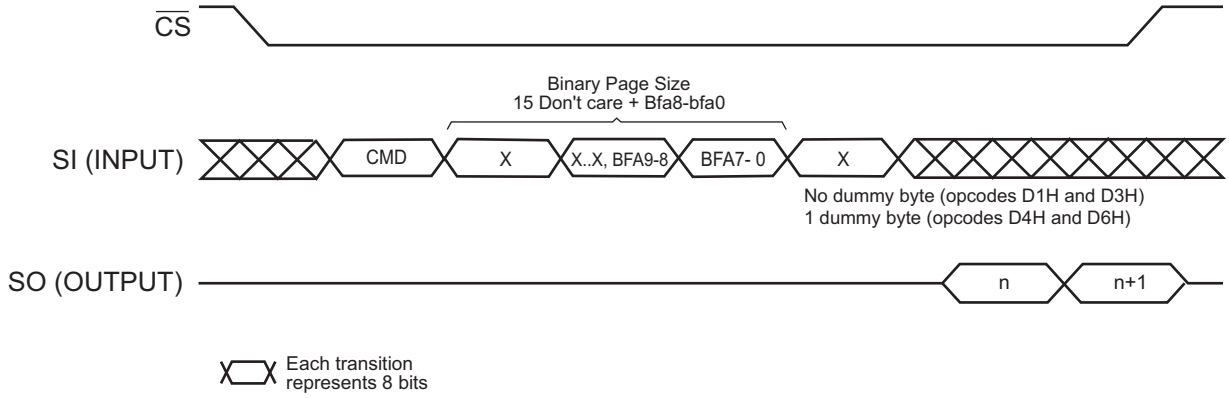


Figure 21-4. Buffer Read



22. Detailed Bit-level Read Waveform – Atmel RapidS Serial Interface Mode 0/Mode 3

Figure 22-1. Continuous Array Read (Legacy Opcode E8H)

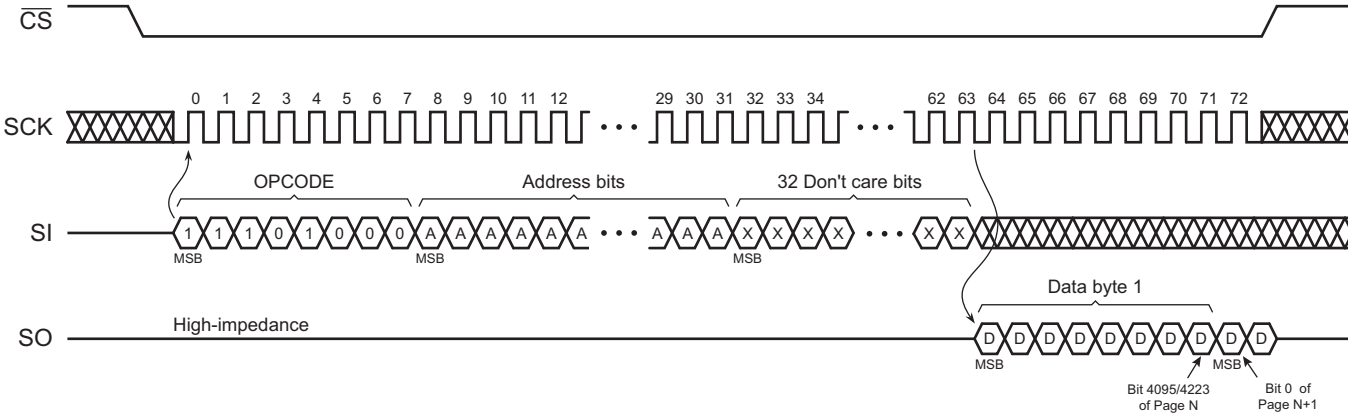


Figure 22-2. Continuous Array Read (Opcode 0BH)

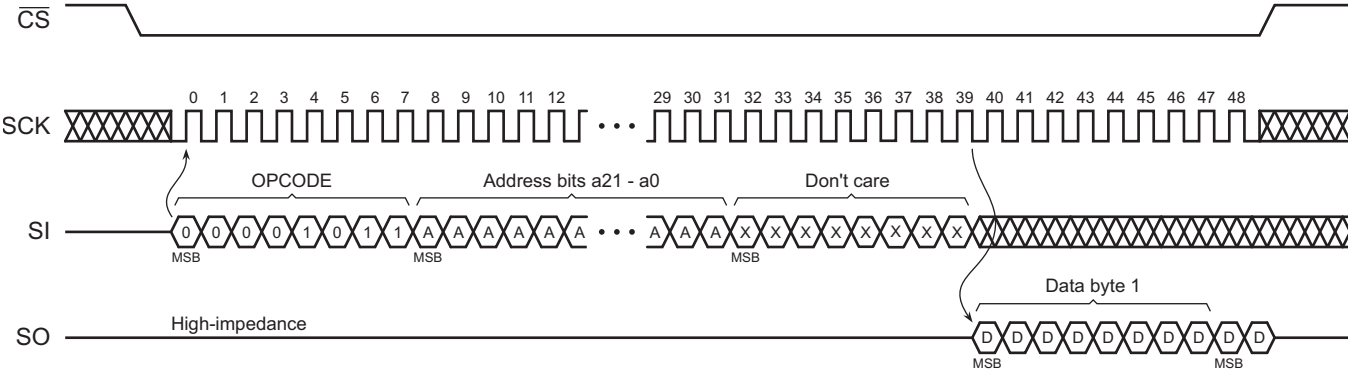


Figure 22-3. Continuous Array Read (Low Frequency: Opcode 03H)

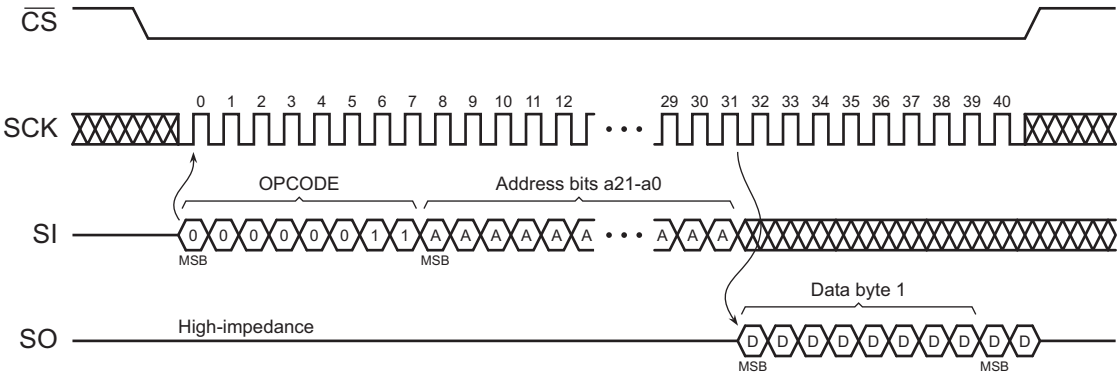


Figure 22-4. Main Memory Page Read (Opcode: D2H)

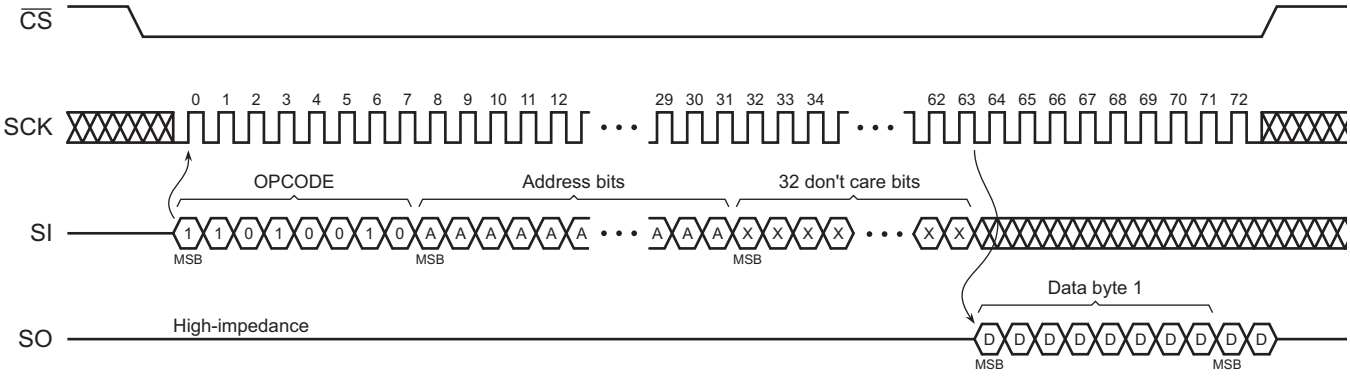


Figure 22-5. Buffer Read (Opcode D4H or D6H)

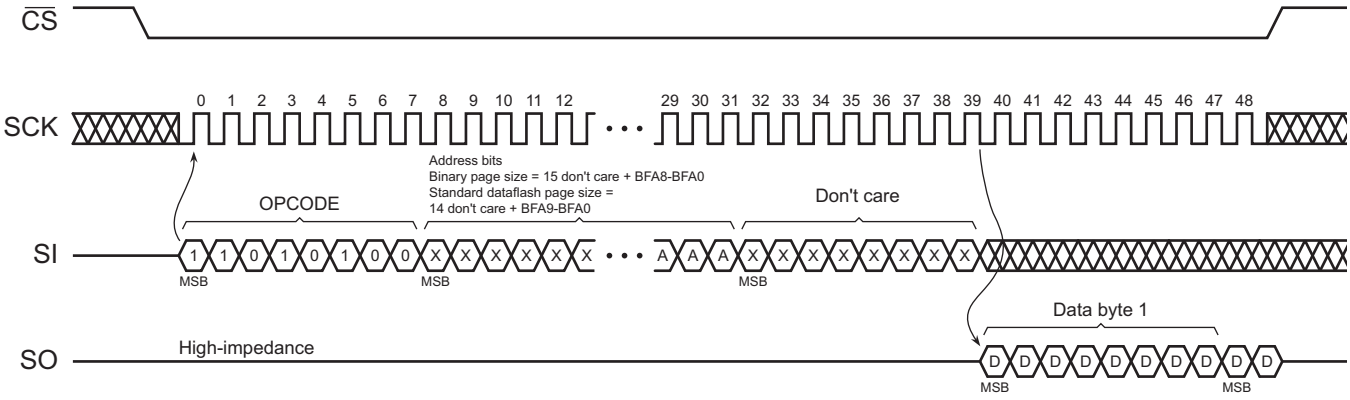


Figure 22-6. Buffer Read (Low Frequency: Opcode D1H or D3H)

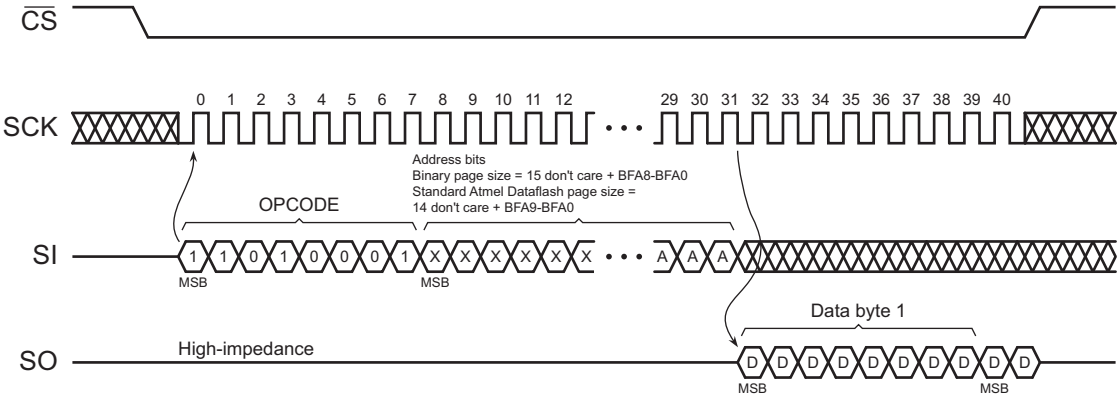


Figure 22-7. Read Sector Protection Register (Opcode 32H)

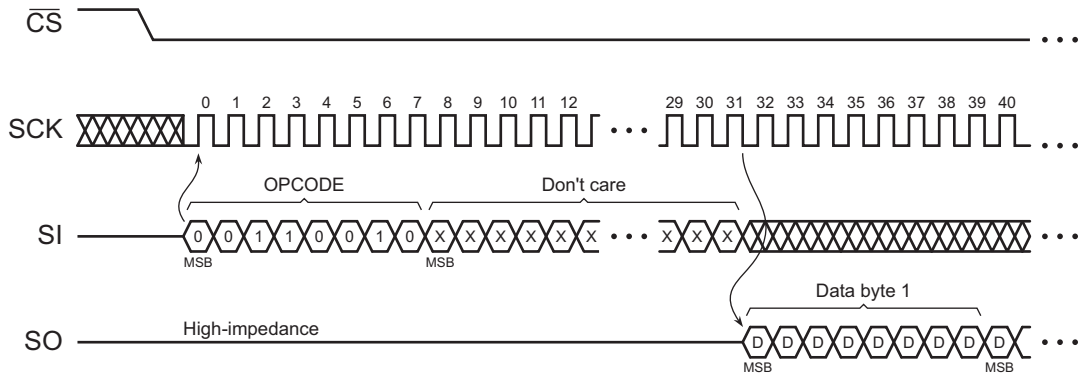


Figure 22-8. Read Sector Lockdown Register (Opcode 35H)

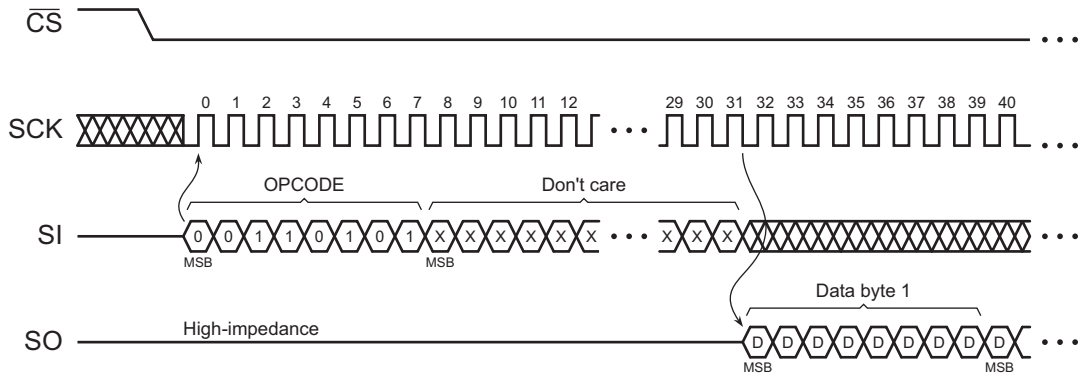


Figure 22-9. Read Security Register (Opcode 77H)

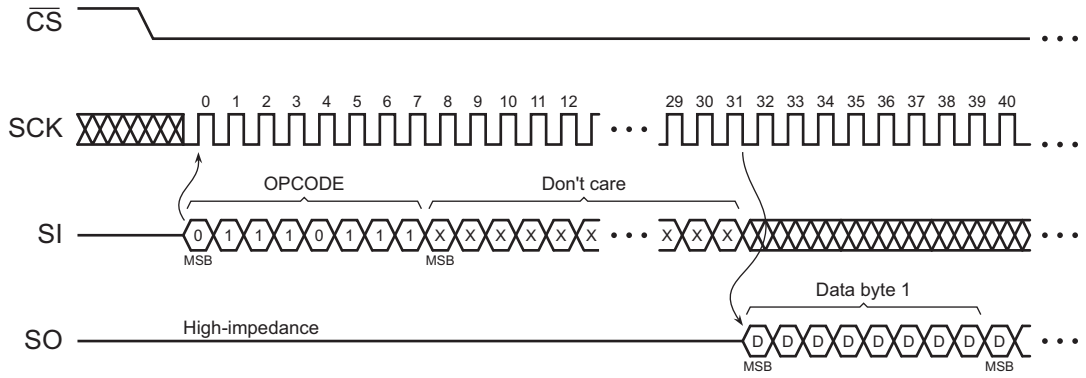


Figure 22-10.Status Register Read (Opcode D7H)

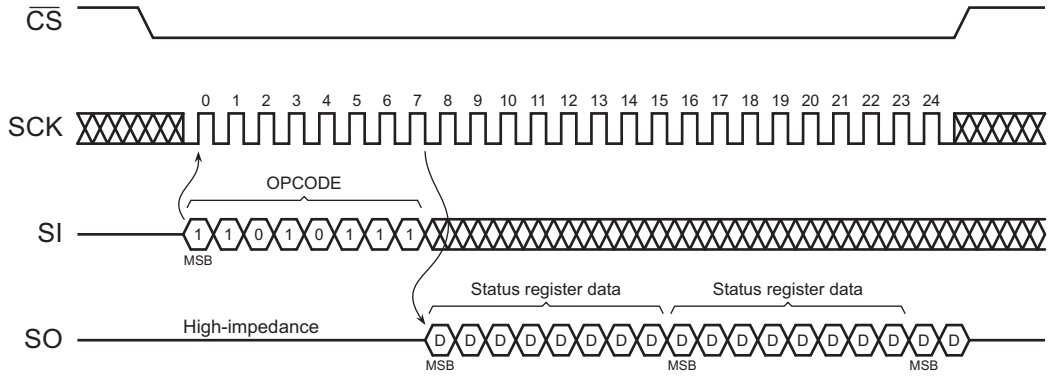
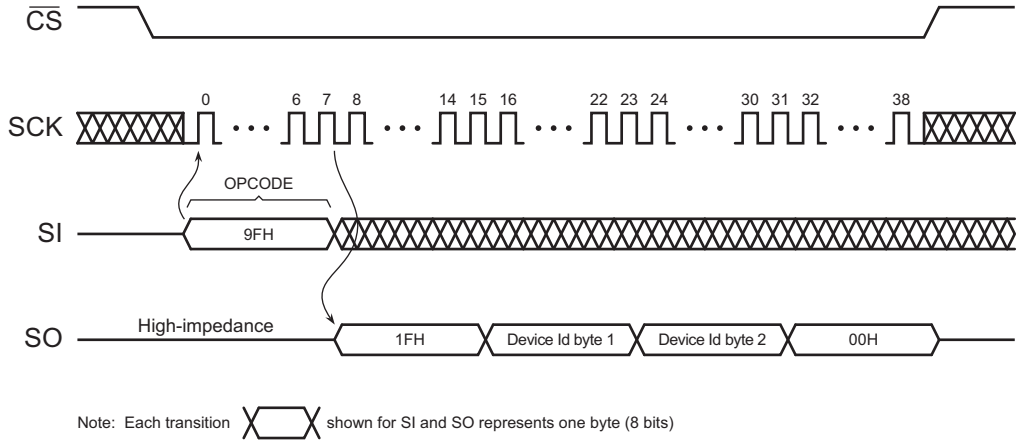


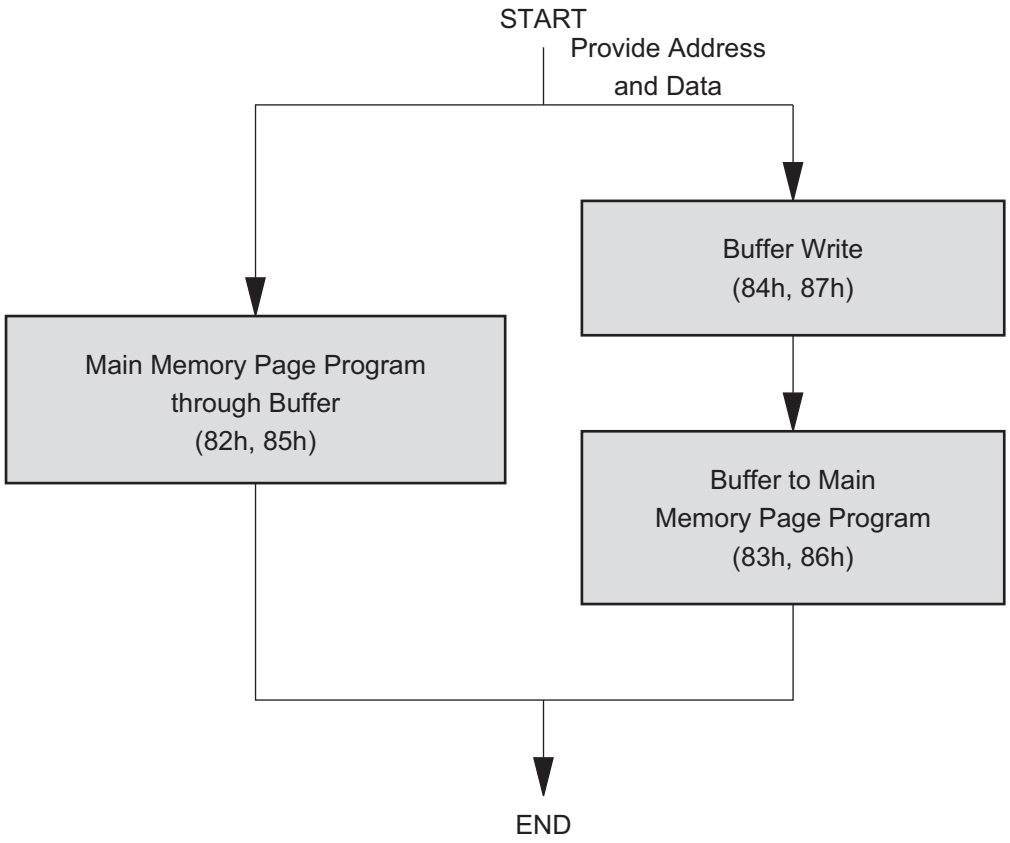
Figure 22-11.Manufacturer and Device Read (Opcode 9FH)



Note: Each transition shown for SI and SO represents one byte (8 bits)

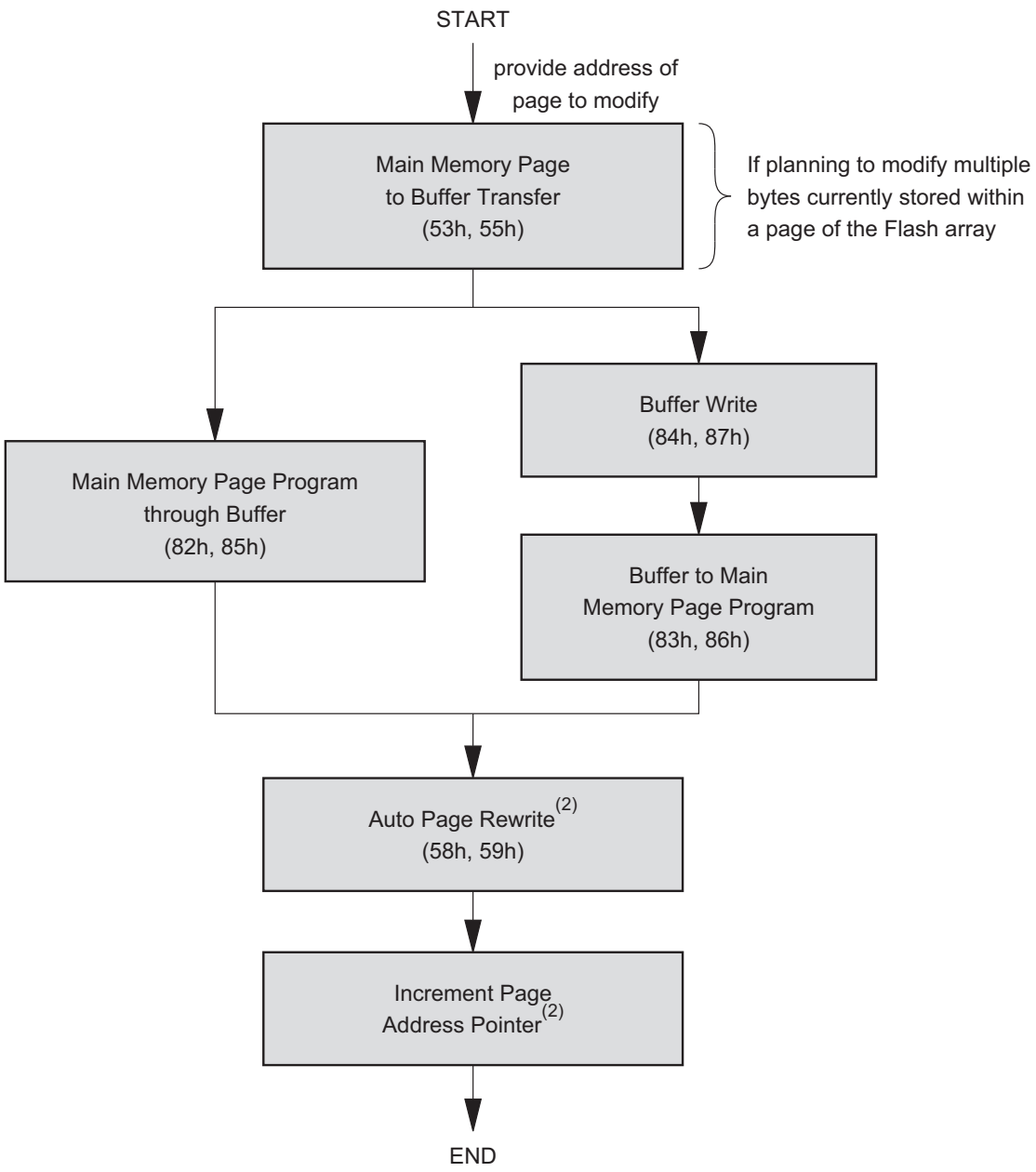
23. Auto Page Rewrite Flowchart

Figure 23-1. Algorithm for Programming or Reprogramming of the Entire Array Sequentially



Notes:
1. This type of algorithm is used for applications in which the entire array is programmed sequentially, filling the array page by page.
2. A page can be written using either a main memory page program operation, or a buffer write operation followed by a buffer to main memory page program operation.
3. The algorithm above shows the programming of a single page. The algorithm will be repeated sequentially for each page within the entire array.

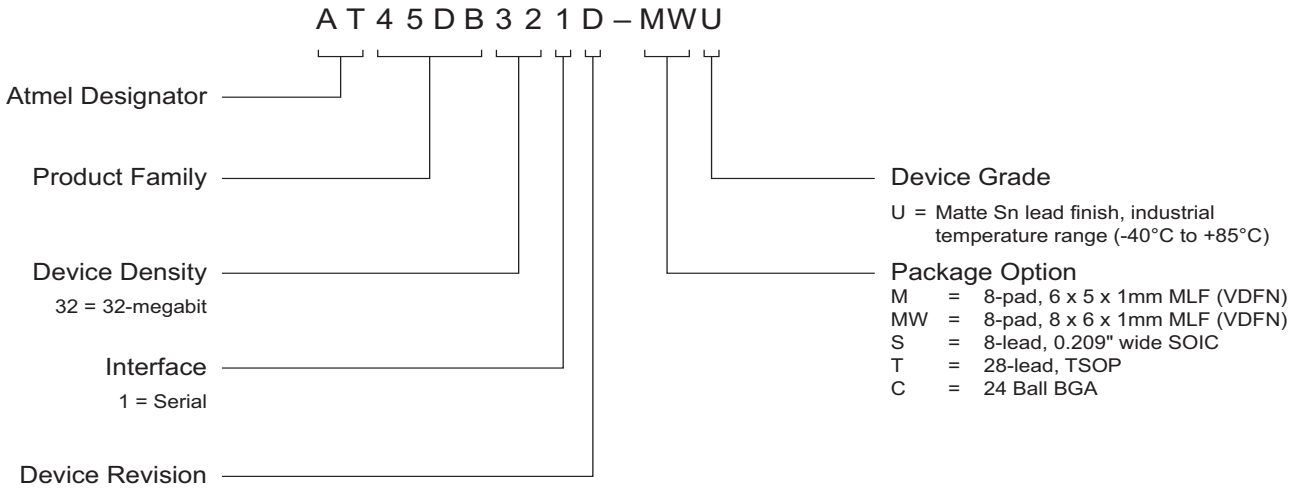
Figure 23-2. Algorithm for Randomly Modifying Data



Notes:
1. To preserve data integrity, each page of an Atmel DataFlash sector must be updated/rewritten at least once within every 20,000 cumulative page erase and program operations.
2. A page address pointer must be maintained to indicate which page is to be rewritten. The auto page rewrite command must use the address specified by the page address pointer.
3. Other algorithms can be used to rewrite portions of the flash array. Low-power applications may choose to wait until 20,000 cumulative page erase and program operations have accumulated before rewriting all pages of the sector. See application note AN-4 (“Using Atmel Serial DataFlash”) for more details.

24. Ordering Information

Ordering Code Detail



Green Package Options (Pb/Halide-free/RoHS Compliant)

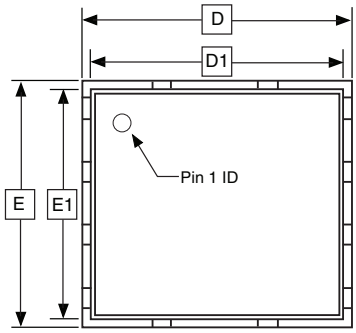
Ordering Code[1][2]	Package	Lead Finish	Operating Voltage	f_{SCK} (MHz)	Operation Range
AT45DB321D-MU AT45DB321D-MU-SL954[3] AT45DB321D-MU-SL955[4]	8M1-A	Matte Sn	2.7V to 3.6V	66	Industrial (-40°C to 85°C) 2.7V to 3.6V
AT45DB321D-MWU AT45DB321D-MWU-SL954[3] AT45DB321D-MWU-SL955[4]	8MW				
AT45DB321D-SU AT45DB321D-SU-SL954[3] AT45DB321D-SU-SL955[4]	8S2				
AT45DB321D-TU	28T				
AT45DB321D-CU	24C3	Matte Sn	2.7V to 3.6V	66	
AT45DB321D-MU-2.5	8M1-A	Matte Sn	2.5V to 3.6V	50	
AT45DB321D-SU-2.5	8S2				

Notes:
1. The shipping carrier option is not marked on the devices.
2. Standard parts are shipped with the page size set to 528 bytes. The user is able to configure these parts to a 512-byte page size, if desired.
3. Parts ordered with suffix SL954 are shipped in bulk, with the page size set to 512 bytes. Parts will have “954” or “SL954” marked on them.
4. Parts ordered with suffix SL955 are shipped in tape and reel, with the page size set to 512 bytes. Parts will have “955” or “SL955” marked on them.

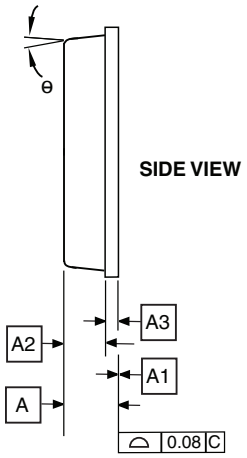
Package Type	
8M1-A	8-pad, 6 x 5 x 1.0mm, very thin micro lead-frame package MLF™ (VDFN)
8MW	8-pad, 8 x 6 x 1.0mm, very thin micro lead-frame package MLF (VDFN)
8S2	8-lead, 0.209in-wide, plastic gull wing small outline package (EIAJ SOIC)
28T	28-lead, 8mm x 13.4mm, plastic thin small outline package, type I (TSOP)
24C3	24-ball, 6mm x 8mm x 1.4mm ball grid array with a 1mm pitch 5 x 5 ball matrix

25. Packaging Information

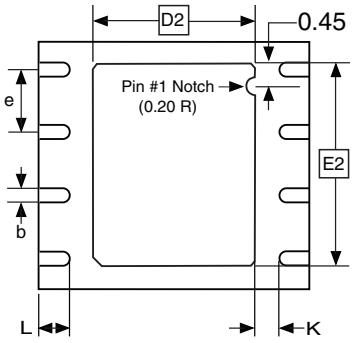
8M1-A – MLF (VDFN)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

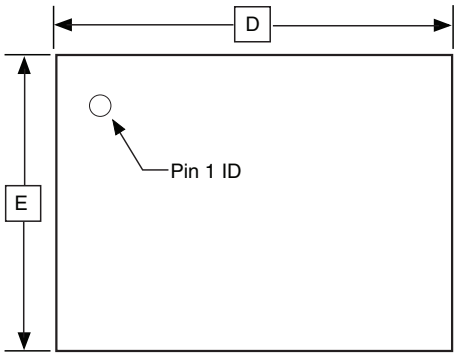
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	0.85	1.00	
A1	–	–	0.05	
A2		0.65 TYP		
A3		0.20 TYP		
b	0.35	0.40	0.48	
D	5.90	6.00	6.10	
D1	5.70	5.75	5.80	
D2	3.20	3.40	3.60	
E	4.90	5.00	5.10	
E1	4.70	4.75	4.80	
E2	3.80	4.00	4.20	
e		1.27		
L	0.50	0.60	0.75	
θ	–	–	12°	
K	0.25	–	–	

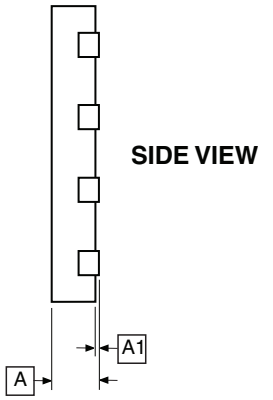
8/28/08

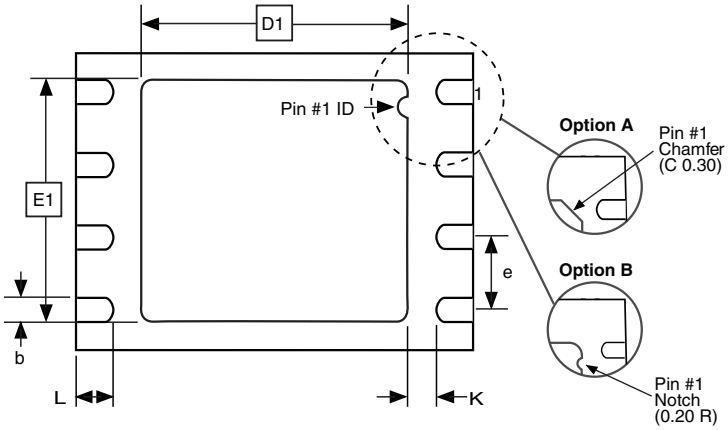
	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**8M1-A,** 8-pad, 6 x 5 x 1.00mm Body, Thermally Enhanced Plastic Very Thin Dual Flat No Lead Package (VDFN)	YBR	8M1-A	D

8MW – MLF (VDFN)



TOP VIEW





BOTTOM VIEW

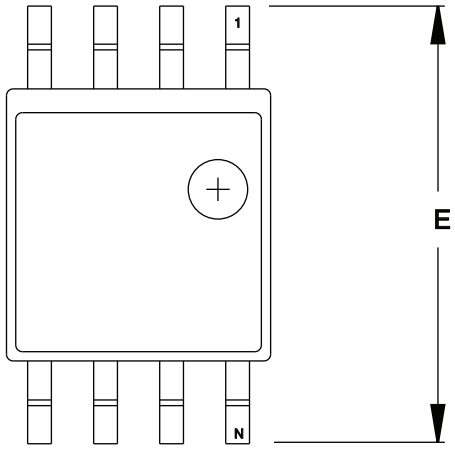
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.00	
A1	–	–	0.05	
b	0.35	0.40	0.48	
D	7.90	8.00	8.10	
D1	6.30	6.40	6.50	
E	5.90	6.00	6.10	
E1	4.70	4.80	4.90	
e	1.27			
L	0.45	0.50	0.55	
K	0.30 REF			

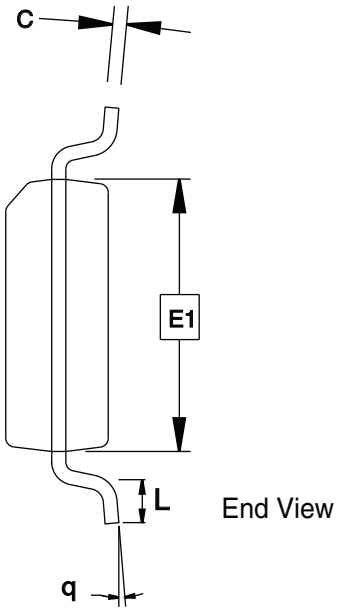
5/25/06

Package Drawing Contact: packagedrawings@atmel.com	**TITLE** **8MW,** 8-pad, 8 x 6 x 1.0mm Body, Very Thin Dual Flat Package No Lead (MLF)	**DRAWING NO.** 8MW	**REV.** B

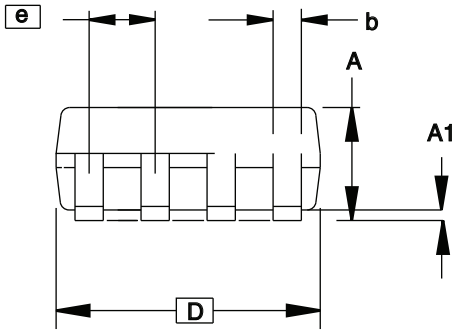
8S2 – EIAJ SOIC



Top View



End View



Side View

Notes:
1. This drawing is for general information only; refer to EIAJ Drawing EDR-7320 for additional information.
2. Mismatch of the upper and lower dies and resin burrs are not included.
3. Determines the true geometric position.
4. Values b,C apply to plated terminal. The standard thickness of the plating layer shall measure between 0.007 to .021mm.

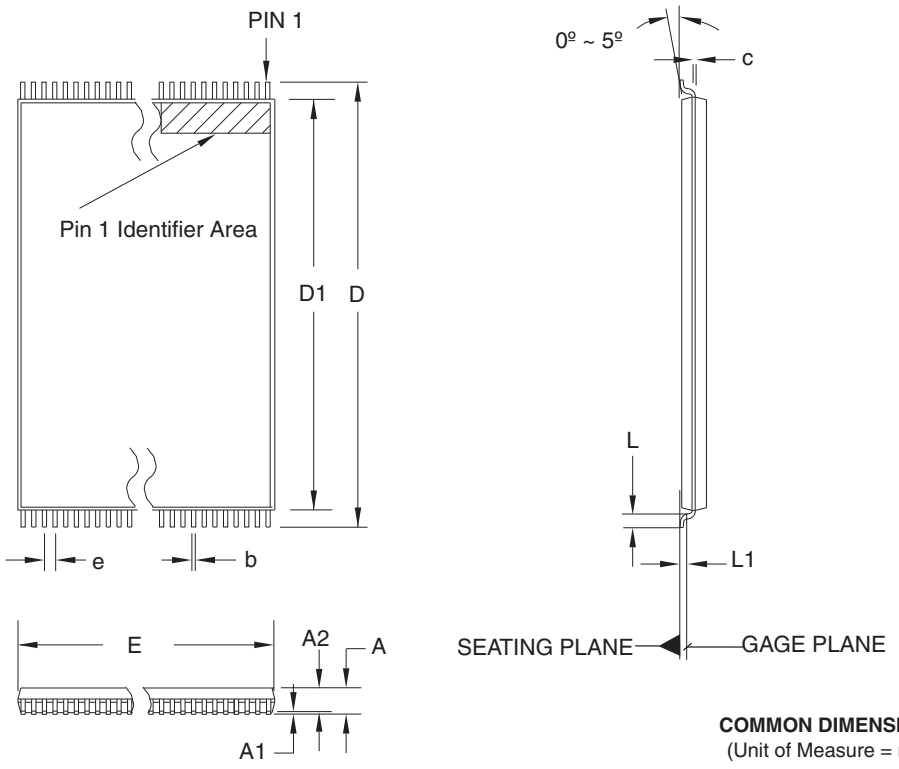
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.70		2.16	
A1	0.05		0.25	
b	0.35		0.48	4
C	0.15		0.35	4
D	5.13		5.35	
E1	5.18		5.40	2
E	7.70		8.26	
L	0.51		0.85	
q	0°		8°	
e	1.27 BSC			3

4/15/08

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**8S2**, 8-lead, 0.208” Body, Plastic Small Outline Package (EIAJ)	STN	8S2	F

28T – TSOP, Type 1



COMMON DIMENSIONS
(Unit of Measure = mm)

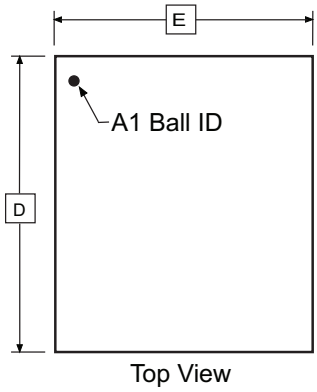
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.90	1.00	1.05	
D	13.20	13.40	13.60	
D1	11.70	11.80	11.90	Note 2
E	7.90	8.00	8.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.55 BASIC			

Notes:
1. This package conforms to JEDEC reference MO-183.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15mm per side and on D1 is 0.25mm per side.
3. Lead coplanarity is 0.10mm maximum.

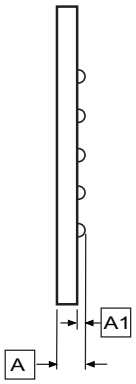
12/06/02

	TITLE	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**28T**, 28-lead (8 x 13.4mm) Plastic Thin Small Outline Package, Type I (TSOP)	28T	C

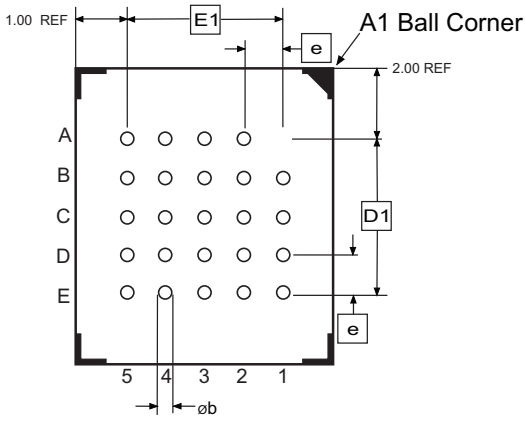
24C3 – CBGA



Top View



Side View



Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
E	5.90	6.00	6.10	
E1		4.0 TYP		
D	7.90	8.00	8.10	
D1		4.0 TYP		
A	–	–	1.20	
A1	0.25	–	–	
e		1.00 BSC		
b		0.40 TYP		

9/10/04

	TITLE	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	24C3, 24-ball (5 x 5 Array), 1.0 mm Pitch, 6 x 8 x 1.20 mm, Chip-scale Ball Grid Array Package (CBGA)	24C3	A

26. Revision History

Doc. Rev.	Date	Comments
3597Q	06/2011	In Table 16-3, - Increased $t_{XFR,}$ page to buffer transfer time and $t_{COMP,}$ page to buffer compare time max values from 200us to 300us - Changed t_{CE} typical time and max time are TBD, see errata - Changed t_{SE} typical time is 1.6s and the max time is 5s Replace 24C1 with 24C3 Updated template
3597P	05/2010	Changed t_{SE} (Typ) 1.6 to 0.7 and (Max) 5 to 1.3 Changed from 10,000 to 20,000 cumulative page erase/program operations and added the please contact Atmel statement in section 11.3
3597O	10/2009	Added the 2.5V V_{CC} option Removed AT45DB321D-MWU-2.5 and AT45DB321D-TU-2.5 from the ordering Information table
3597N	04/2009	Updated Absolute Maximum Ratings Added 24C1 24 Ball BGA package Option Deleted Atmel DataFlash Card Package Option
3597M	03/2009	Changed deep power-down current values - Increased typical value from 5µA to 15µA - Increased maximum value from 15µA to 25µA
3597L	02/2009	Changed t_{DIS} (Typ and Max) to 27ns and 35ns, respectively
3597K	09/2008	Corrected typographical errors in Sector Erase section. Corrected A17+A16 from x (Don't care) to A for opcode 7Ch in Table 15-6 Corrected PA8+PA7 from x (Don't care) to P for opcode 7Ch in Table 15-7
3597J	04/2008	Added part number ordering code details for suffixes SL954/955 Added ordering code details
3597I	08/2007	Added additional text to "power of two" binary page size option Changed t_{VSCL} from 50µs to 70µs Changed t_{RDPD} from 30µs to 35µs Changed t_{XFR} and t_{COMP} values from 400µs to 200µs Removed AT45DB321D-CNU from ordering information and corresponding 8CN3 package
3597H	02/2007	Added AT45DB321D-CNU to ordering information and corresponding 8CN3 package Removed "not recommended for new designs" comment from 8MW package drawing
3597G	09/2006	Removed "not recommended for new designs" note from ordering information for 8MW package
3597F	08/2006	Added errata regarding Chip Erase Added AT45DB321D-SU to ordering information and corresponding 8S2 package
3597E	07/2006	Corrected typographical errors
3597D	04/2006	Added 8 x 6mm MLF (VDFN) package Changed the sector size of 0a and 0b to 8 pages and 120 pages respectively Changed the Product Version Code to 00001
3597C	03/2006	Added preliminary Changed the sector size from 256-Kbytes to 64-Kbytes Added the "Legacy Commands" table

Doc. Rev.	Date	Comments
3597B	01/2006	Added 6 x 5mm MLF (VDFN) package Added text, in “Programming the Configuration Register”, to indicate that power cycling is required to switch to “power of two” page size after the opcode enable has been executed. Corrected typographical error regarding the opcode for chip erase in “Program and Erase Commands” table
3597A	11/2005	Initial release

27. Errata

27.1 Chip Erase

27.1.1 Issue

In a certain percentage of units, the chip erase feature may not function correctly and may adversely affect device operation. Therefore, it is recommended that the chip erase commands (opcodes C7H, 94H, 80H, and 9AH) not be used.

27.1.2 Workaround

Use block erase (opcode 50H) as an alternative. The block erase function is not affected by the chip erase issue.

27.1.3 Resolution

The chip erase feature may be fixed with a new revision of the device. Please contact Atmel for the estimated availability of devices with the fix.



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