Features

- ARM7TDMI® ARM® Thumb® Processor Core
  - High-performance 32-bit RISC
  - High-density 16-bit Thumb Instruction Set
  - Leader in MIPS/Watt
  - Embedded ICE (In Circuit Emulation)
- 4 Kbytes Internal RAM
- Clock Manager (CM) with Programmable PLL
  - PLL Multiplier from x2 to x20
  - 32.768 kHz Oscillator for Low-power Operation
  - Master Clock Divider/multiplier
- Fully Programmable External Bus Interface (EBI) through Advanced Memory Controller (AMC)
  - Maximum External Address Space of 16 Mbytes, Up to Six Chip Select Lines
- 8-level Priority, Vectored Interrupt Controller
  - Individually Maskable, Two External Interrupts including One Fast Interrupt Line
- 11-channel Peripheral Data Controller (PDC)
- 49 Programmable I/O Lines
- One 3-channel 16-bit General Purpose Timers (GPT)
  - Three Configurable Modes: Counter, PWM, Capture
  - Three Multi-purpose I/O Pins Per Channel
- Four 16-bit Simple Timers (ST)
- 4-channel 16-bit Pulse Width Modulation (PWM)
- Two 16-bit Capture Modules (CAPT)
- CAN Controller 2.0A and 2.0B Full CAN (16 Buffers)
- Three USARTs
  - Six Peripheral Data Controller (PDC) Channels
  - Support for Up to 9-bit Data Lengths
  - Support for LIN (Software) Protocol
- Master SPI Interface
  - Two Peripheral Data Controller (PDC) Channels
  - 8- to 16-bit Programmable Data Length
  - Four External Chip Select Lines
- One 8-channel 10-bit Analog-to-digital Converter (ADC)
  - One Peripheral Data Controller (PDC) Channel
- Programmable Watch Timer (WT)
- Programmable Watchdog (WD)
- Power Management Controller (PMC)
  - CPU and Peripherals Can Be Deactivated Individually
- Fully Static Operation Up to 40 MHz
  - 3.0V to 3.6V Core, Memory and Analog Voltage Range
  - 3.0 V to 5.5V Compliant I/Os
  - -40° to +85°C Operating Temperature Range
- Available in a 144-pin LQFP

AT91 ARM Thumb-based Microcontrollers

AT91SAM7A1

Summary

NOTE: This is a summary document. The complete document is available on the Atmel website at www.atmel.com.

6048C–ATARM–29-Jun-06

1. Description

The AT91SAM7A1 is a member of the Atmel Smart ARM Microcontrollers product family, based on the ARM7TDMI embedded processor. This processor has a high-performance 32-bit RISC architecture with a high-density 16-bit instruction set and very low power consumption.

In addition, a large number of internally banked registers result in very fast exception handling, making the device ideal for real-time control applications.

The AT91SAM7A1 has a direct connection to off-chip memory, including Flash, through the fully-programmable External Bus Interface.

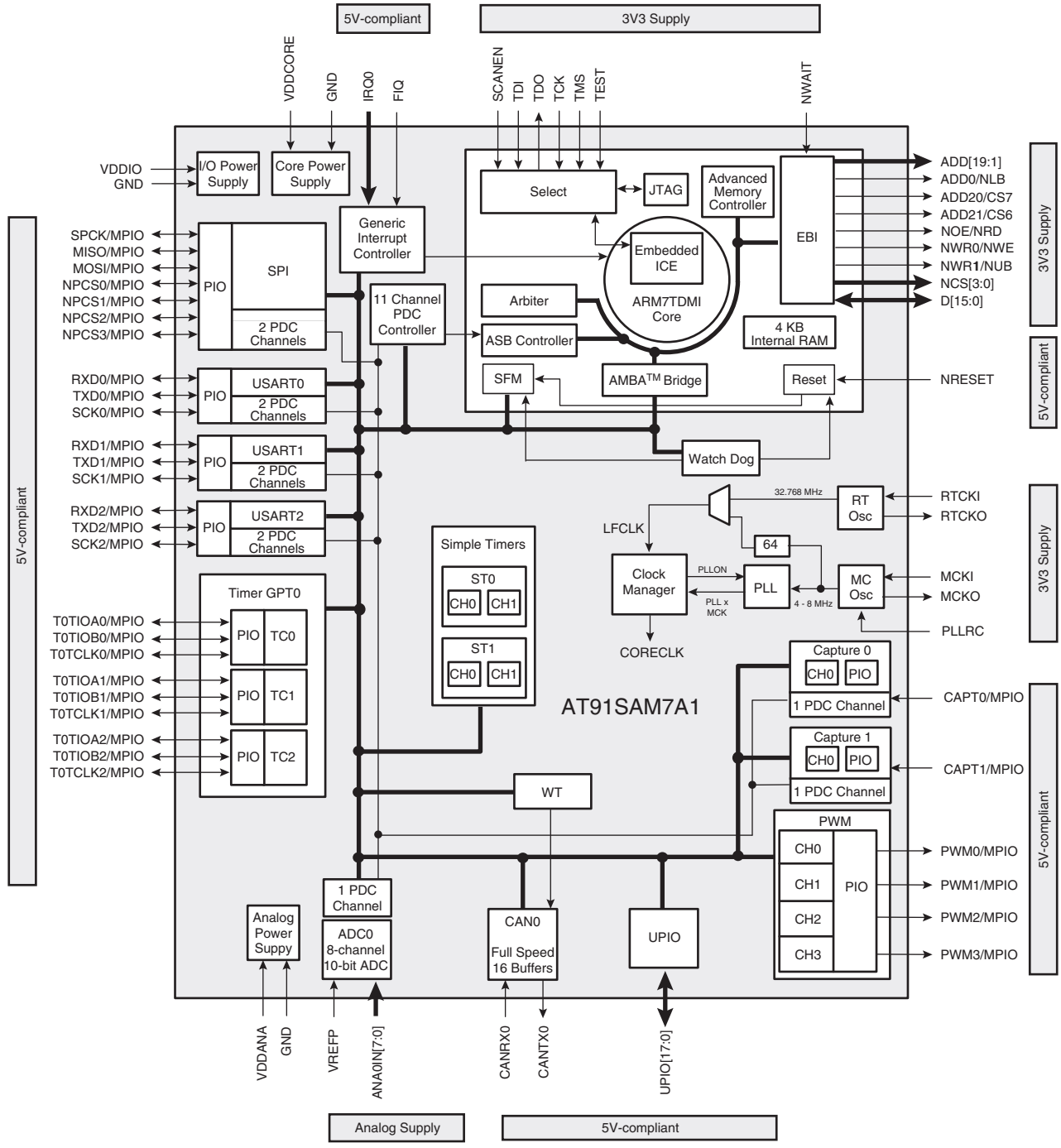
An 8-level priority vectored Interrupt Controller in conjunction with the Peripheral Data Controller significantly improves the real-time performance of the device.

The device is manufactured using high-density CMOS technology.

By combining the ARM7TDMI processor with an on-chip RAM and a wide range of peripheral functions on a monolithic chip, the AT91SAM7A1 is a powerful device that provides a flexible, cost-effective solution to many compute-intensive embedded control applications in the industrial world.

2. Block Diagram

Figure 2-1. AT91SAM7A1 Block Diagram



3. Pin Configuration

Table 3-1. Pin Configuration

Pin	Name	Pad	Pin	Name	Pad	Pin	Name	Pad	Pin	Name	Pad
1	D0	PC3B01D	37	ADD11	PC3T02	73	GND		109	ANA0IN1	AIMUX1
2	D8	PC3B01D	38	ADD12	PC3T02	74	PIOA2	MC5B04	110	ANA0IN2	AIMUX1
3	D1	PC3B01D	39	ADD13	PC3T02	75	PIOA3	MC5B04	111	ANA0IN3	AIMUX1
4	D9	PC3B01D	40	ADD14	PC3T02	76	VDDIO		112	ANA0IN4	AIMUX1
5	VDDCORE		41	ADD15	PC3T02	77	PIOA4	MC5B03	113	ANA0IN5	AIMUX1
6	GND[2]		42	GND		78	PIOA5	MC5B03	114	ANA0IN6	AIMUX1
7	VDDCORE[1]		43	VDDCORE[1]		79	PIOA6	MC5B03	115	ANA0IN7	AIMUX1
8	D2	PC3B01D	44	VDDIO		80	PIOA7	MC5B03	116	GND	
9	D10	PC3B01D	45	IRQ0	MC5D00	81	PIOA8	MC5B03	117	VDDCORE	
10	D3	PC3B01D	46	FIQ	MC5D00	82	PIOA9	MC5B03	118	MCKI	OSC16M
11	D11	PC3B01D	47	T0TIOA0/MPIO	MC5B01	83	GND		119	MCKO	OSC16M
12	D4	PC3B01D	48	T0TIOB0/MPIO	MC5B01	84	PIOA10	MC5B02	120	PLLRC	PLL080M1
13	D12	PC3B01D	49	T0TCLK0/MPIO	MC5B01	85	PIOA11	MC5B02	121	GND	
14	D5	PC3B01D	50	T0TIOA1/MPIO	MC5B01	86	PIOA12	MC5B01	122	VDDCORE	
15	D13	PC3B01D	51	T0TIOB1/MPIO	MC5B01	87	PIOA13	MC5B01	123	RTCKI	OSC33K
16	D6	PC3B01D	52	T0TCLK1/MPIO	MC5B01	88	PIOA14	MC5B01	124	RTCKO	OSC33K
17	D14	PC3B01D	53	T0TIOA2/MPIO	MC5B01	89	PIOA15	MC5B01	125	GND	
18	D7	PC3B01D	54	T0TIOB2/MPIO	MC5B01	90	PIOA16	MC5B01	126	VDDIO	
19	D15	PC3B01D	55	GND		91	PIOA17	MC5B01	127	GND[2]	
20	ADD17	PC3T02	56	T0TCLK2/MPIO	MC5B01	92	PWM0/MPIO	MC5B01	128	GND	
21	ADD16	PC3T02	57	TXD0/MPIO	MC5B01	93	VDDIO		129	SCANEN	PC3D01D
22	NWR0/NWE	PC3B02	58	RXD0/MPIO	MC5B01	94	PWM1/MPIO	MC5B01	130	TEST	PC3D01D
23	ADD19	PC3T02	59	SCK0/MPIO	MC5B01	95	PWM2/MPIO	MC5B01	131	TMS	PC3D21U
24	ADD18	PC3T02	60	TXD1/MPIO	MC5B01	96	PWM3/MPIO	MC5B01	132	TDO	PC3T03
25	ADD7	PC3T02	61	RXD1/MPIO	MC5B01	97	CAPT0/MPIO	MC5B01	133	TDI	PC3D21U
26	ADD6	PC3T02	62	SCK1/MPIO	MC5B01	98	CAPT1/MPIO	MC5B01	134	TCK	PC3D21U
27	GND[2]		63	VDDIO		99	NRESET	MC5D20	135	NWAIT	PC3D01U
28	VDDCORE[1]		64	SPCK/MPIO	MC5B01	100	CANRX0	MC5D00	136	ADD21/CS6	PC3T02
29	ADD2	PC3T02	65	MISO/MPIO	MC5B01	101	CANTX0	MC5O01	137	NCS3	PC3T02
30	ADD3	PC3T02	66	MOSI/MPIO	MC5B01	102	TXD2/MPIO	MC5B01	138	NCS2	PC3T02
31	ADD4	PC3T02	67	NPCS0/MPIO	MC5B01	103	RXD2/MPIO	MC5B01	139	NWR1/NUB	PC3B02
32	ADD5	PC3T02	68	NPCS1/MPIO	MC5B01	104	SCK2/MPIO	MC5B01	140	ADD0/NLB	PC3T02
33	ADD8	PC3T02	69	NPCS2/MPIO	MC5B01	105	GND		141	NCS1	PC3T02
34	ADD20/CS7	PC3T02	70	NPCS3/MPIO	MC5B01	106	VDDANA		142	NOE/NRD	PC3B02
35	ADD9	PC3T02	71	PIOA0	MC5B04	107	VREFP	ANAIN	143	NCS0	PC3T02
36	ADD10	PC3T02	72	PIOA1	MC5B04	108	ANA0IN0	AIMUX1	144	ADD1	PC3T02

Notes: 1. Pins 7, 28 and 43 are connected internally.
2. Pins 6, 27 and 127 are connected internally.

4. Pin Description

Table 4-1. Pin Description

Module	Name	Function	Type[1]	Level[1]	Comments
EBI[2]	ADD[19:1]	External address bus	O	(Z)	The EBI is tri-stated when NRESET is at a logical low level. Internal pull-downs on data bus bits. ADD20 and ADD21 are address lines at reset.
	ADD0/NLB	External address line/Lower byte enable	O	L (Z)	
	ADD20/CS7	External address line/Chip select	O	H (Z)	
	ADD21/CS6	External address line/Chip select	O	H (Z)	
	D[15:0][3]	External data bus	I/O	(Z)	
	NOE/NRD	Output enable	O	L (Z)	
	NWR0/NWE	Write enable	O	L (Z)	
	NCS[3:0]	Chip select lines	O	L (Z)	
	NWR1/NUB	Upper byte enable	O	L (Z)	
	NWAIT	Wait Input	I	L	Internal pull-up (must be connected to VCC or leave unconnected for normal operation)
GIC	IRQ0	External interrupt line	I		
	FIQ	Fast interrupt line	I		
Power-on Reset	NRESET	Hardware reset input	I	L	Schmitt input with internal filter
Master Clock	MCKI	Master clock input	I		Connected to external crystal (4 to 16 MHz)
	MCKO	Master clock output	O		
	PLLRC	PLL RC network input	I		
Real-time Clock	RTCKI	32.768 kHz clock input	I		Connected to external 32.768 kHz crystal
	RTCKO	32.768 kHz clock output	O		
UPIO	UPIO[17:0]	Unified I/O	I/O (I)	(Z)	General-purpose I/O
USART0	SCK0/MPIO	USART0 clock line	I/O (I)	(Z)	Multiplexed with general-purpose I/O
	RXD0/MPIO	USART0 receive line	I/O (I)	(Z)	Multiplexed with general-purpose I/O
	TXD0/MPIO	USART0 transmit line	I/O (I)	(Z)	Multiplexed with general-purpose I/O
USART1	SCK1/MPIO	USART1 clock line	I/O (I)	(Z)	Multiplexed with general-purpose I/O
	RXD1/MPIO	USART1 receive line	I/O (I)	(Z)	Multiplexed with general-purpose I/O
	TXD1/MPIO	USART1 transmit line	I/O (I)	(Z)	Multiplexed with general-purpose I/O
USART2	SCK2/MPIO	USART2 clock line	I/O (I)	(Z)	Multiplexed with general-purpose I/O
	RXD2/MPIO	USART2 receive line	I/O (I)	(Z)	Multiplexed with general-purpose I/O
	TXD2/MPIO	USART2 transmit line	I/O (I)	(Z)	Multiplexed with general-purpose I/O
Capture	CAPT[1:0]/MPIO	Capture input	I/O (I)	(Z)	Multiplexed with general-purpose I/O
PWM	PWM[3:0]/MPIO	Pulse Width Modulation output	I/O (I)	(Z)	Multiplexed with general-purpose I/O

Table 4-1. Pin Description

Module	Name	Function	Type[1]	Level[1]	Comments
Timer T0	T0TIOA[2:0]/MPIO	Capture/waveform I/O	I/O (I)	(Z)	Multiplexed with a general-purpose I/O
	T0TIOB[2:0]/MPIO	Trigger/waveform I/O	I/O (I)	(Z)	Multiplexed with a general-purpose I/O
	T0TCLK[2:0]/MPIO	External clock/trigger/input	I/O (I)	(Z)	Multiplexed with a general-purpose I/O
ADC	ANAIN[7:0]	Analog input	I		
	VREFP	Positive voltage reference	I		
SPI	SPCK/MPIO	SPI clock line	I/O (I)	(Z)	Multiplexed with a general-purpose I/O
	MISO/MPIO	SPI master in slave out	I/O (I)	(Z)	Multiplexed with a general-purpose I/O
	MOSI/MPIO	SPI master out slave in	I/O (I)	(Z)	Multiplexed with a general-purpose I/O
	NPCS[3:1]/MPIO	SPI chip select	I/O (I)	(Z)	Multiplexed with a general-purpose I/O
	NPCS0/MPIO	SPI chip select	I/O (I)	(Z)	Multiplexed with a general-purpose I/O
CAN0	CANRX0	CAN0 receive line	I	L	
	CANTX0	CAN0 transmit line	O	L (H)	
JTAG	SCANEN	Scan enable (Factory test)	I	H	Internal pull-down (must be connected to GND or leave unconnected for normal operation)
	TDI	Test Data In	I		Schmitt trigger, internal pull-up
	TDO	Test Data Out	O		
	TMS	Test Mode Select	I		Schmitt trigger, internal pull-up
	TCK	Test Clock	I		Schmitt trigger, internal pull-up
	TEST	Factory test	I	H	Internal pull-down (must be connected to GND or leave unconnected for normal operation)
Power Supplies	VDDCORE	Core Power Supply	–		3.3V
	VDDANA	Analog Power Supply	–		3.3V
	VDDIO	I/O Lines Power Supply	–		3.3V to 5V
	GND	Ground	–		

Notes: 1. Values in brackets are values at reset H (high level), L (low level), Z (tri-state), I (input), O (output).

2. The EBI bus (address bus A[21:0], data bus D[15:0] and control lines NOE/NRD, NWR0/NWE, NWR1/NUB and NCS[3:0]) is tri-stated when NRESET is at a logical 0. This allows external equipment to access the external memory devices (e.g., for Flash programming). It is up to the application to add an external pull-up on the chip select lines in order to avoid EBI conflicts at reset.

3. The EBI data bus D[15:0] has an internal pull-down.

5. Architectural Overview

The AT91SAM7A1 architecture consists of two main buses, the Advanced System Bus (ASB) and the Advanced Peripheral Bus (APB). The ASB is designed for maximum performance. It interfaces the processor with the on-chip 32-bit memories and the external memories and devices by means of the External Bus Interface (EBI). The APB is designed for accesses to on-chip peripherals and is optimized for low power consumption. The AMBA™ Bridge provides an interface between the ASB and the APB.

The AT91SAM7A1 peripherals are designed to be programmed with a minimum number of instructions. Each peripheral has a 16 Kbyte address space allocated in the upper 1 Mbytes of the 4 Gbyte address space. Except for the interrupt controller, the peripheral base address is the lowest address of its memory space. The peripheral register set is composed of control, mode, data, status and interrupt registers. To maximize the efficiency of bit manipulation, frequently-written registers are mapped into three memory locations. The first address is used to set the individual register bits, the second resets the bits and the third address reads the value stored in the register. A bit can be set or reset by writing a one to the corresponding position at the appropriate address. Writing a zero has no effect. Individual bits can thus be modified without having to use costly read-modify-write and complex bit manipulation instructions.

The ARM7TDMI processor operates in little-endian mode in the AT91SAM7A1 microcontroller. The processor's internal architecture and the ARM and Thumb instruction sets are described in the ARM7TDMI datasheet. The ARM Standard In-Circuit-Emulation debug interface is supported via the ICE port of the AT91SAM7A1 microcontroller (This is not a standard IEEE 1149.1 JTAG Boundary Scan interface).

6. Advanced Memory Controller (AMC)

The AT91SAM7A1 embeds 4 Kbytes of internal SRAM. The internal memory is directly connected to the 32-bit data bus and is single-cycle accessible. This provides maximum performance of 36 MIPS @ 40 MHz by using the ARM instruction set of the processor, minimizing system power consumption and improving on the performance of separate memory solutions.

7. External Bus Interface (EBI)

The EBI generates the signals that control the accesses to the external memories or peripheral devices. The EBI is fully programmable and can address up to 6 Mbytes. It has four chip selects and a 21-bit address bus, the upper bit of which is multiplexed with a chip select. Separate read and write control signals allow for direct memory and peripheral interfacing. The EBI supports different access protocols, allowing single clock cycle memory accesses. The main features are:

- External Memory Mapping
- Up to 4 chip select lines
- Byte write or byte select lines
- 8-bit or 16-bit data bus
- External wait
- Remap of boot memory
- Two different read protocols
- Programmable wait state generation

8. Generic Interrupt Controller (GIC)

The AT91SAM7A1 has an 8-level priority, individually maskable, vectored interrupt controller. This feature substantially reduces the software and real time overhead in handling internal and external interrupts. The interrupt controller is connected to the nFIQ (fast interrupt request) and the nIRQ (standard interrupt request) inputs of the ARM7TDMI processor. The processor's nFIQ line can only be asserted by the external fast interrupt request input, the FIQ. The nIRQ line can be asserted by the interrupts generated by the on-chip peripherals and the external interrupt request line, IRQ0. An 8-level priority encoder allows the customer to define the priority between the different nIRQ interrupt sources. Internal sources are programmed to be level sensitive or edge triggered. External sources can be programmed to be positive or negative edge triggered or high or low level sensitive.

9. Parallel I/O Controller (PIO)

The AT91SAM7A1 has 49 configurable I/O lines. Thirty-two pins (unified PIO) on the AT91SAM7A1 are dedicated as general purpose I/O pins (UPIO0 - UPIO31). Other I/O lines are multiplexed with an external signal of a peripheral to optimize the use of available package pins. The unified PIO pins are controlled by a dedicated module; the others pins are configured in each module.

10. Peripheral Data Controller (PDC)

An on-chip, 11-channel Peripheral Data Controller (PDC) transfers data between the on-chip peripherals and the on- and off-chip memories without processor intervention. One PDC channel is connected to the receiving channel and one to the transmitting channel of each USART and of the SPI. A single PDC channel is connected to each ADC and each Capture.

Most importantly, the PDC removes the processor interrupt handling overhead and significantly reduces the number of clock cycles required for a data transfer. It can transfer up to 64 Kbytes without reprogramming the starting address. As a result, the performance of the microcontroller is increased and the power consumption reduced.

11. Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The AT91SAM7A1 provides three identical, full-duplex Universal Synchronous/Asynchronous Receiver/Transmitters that are connected to the Peripheral Data Controller. The main features are:

- Programmable Baud Rate Generator
- Parity, framing and overrun error detection
- Line break generation and detection
- Automatic echo, local & remote loopback modes
- Multi-drop mode: address detection and generation
- Interrupt generation
- Two Dedicated Peripheral Data Controller channels
- 5-, 6-, 7-, 8- and 9-bit character length
- Idle flag for J1587 protocol.
- Smart card transmission error feature
- Support LIN 1.2 protocol with H/W layer

12. Serial Peripheral Interface (SPI)

The AT91SAM7A1 features an SPI that provides communication with external devices in master or slave mode. The SPI has four external chip selects that can be connected to up to 15 devices. The data length is programmable from 8-bit to 16-bit.

As for the USART, a two-channel PDC is used to move data directly between memory and the SPI without CPU intervention for maximum real-time processing throughput.

13. Controller Area Network (CAN)

The AT91SAM7A1 provides one CAN (2.0A and 2.0B). These are serial communications protocols that efficiently support distributed real-time control with a very high level of security (16 mailboxes). The main features are:

- Prioritization of messages
- Multi-master
- System wide data consistency
- Error detection and error signaling
- Automatic retransmission of corrupted messages
- Automatic reply after receive a remote frame
- Time stamp on each transfer
- Multicast reception with time synchronization
- Continuous reception mode

14. General-purpose Timer (GPT)

The AT91SAM7A1 features three general-purpose timers. Each timer can be independently programmed to perform a wide range of functions including frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse width modulation.

Each general-purpose timer has one external clock input, five internal clock inputs, and three multi-purpose input/output signals that can be configured by the user. Each timer drives an internal interrupt signal that can be programmed to generate processor interrupts via the GIC (Generic Interrupt Controller).

Three general-purpose timers are grouped in the same block. This block has two global registers that act upon all three GPTs. The Block Control Register allows the three timers to be started simultaneously with the same instruction. The Block Mode Register defines the external clock inputs for each timer, allowing them to be chained.

15. Simple Timer (ST)

Simple Timers provide basic functions for timing calculation. Each channel of this timer has a specific prescalar and a 16-bit counter. The prescalar defines the clock frequency of the channel counter. The 16-bit counter starts down-counting when a value different to zero is loaded. An interrupt is generated when the counter is null.

16. Capture Module (CAPT)

The capture module is a frame analyzer. It stores the period of time between two edges of a signal in a register. This period is described as a number of counter cycles. The capture allows data transfers with the PDC.

17. Pulse Width Modulator (PWM)

The AT91SAM7A1 includes four PWM channels. Each channel can generate pulses. The frequency and the duty cycle of each channel can be configured.

18. Watch Timer (WT)

The watch timer provides a seconds counter and an alarm function. The alarm register has a resolution of 30.5 µs. This allows a 32-bit register to have sufficient range to cater for a 24 or 36 hour period.

19. Watchdog (WD)

The AT91SAM7A1 has an internal watchdog that can be used to prevent system lock-up if the software becomes trapped in a deadlock.

20. Special Function Module (SFM)

The AT91SAM7A1 provides registers which implement the following special functions:

- Chip identification
- RESET status

21. Analog-to-digital Converter (ADC)

The 8-channel, 10-bit Analog-to-Digital Converter (ADC) is based on a Successive Approximation Register (SAR) approach. The ADC has eight analog input pins, ANA0IN0 to ANA0IN7, and provides an interrupt signal to the AIC. The ADC has two dedicated analog power supply pins, VDDANA and GND, and the input reference voltage pin, VREFP. Each channel can be enabled or disabled independently, and has its own data register. The ADC can be configured to automatically enter Sleep Mode after a conversion sequence, and can be triggered by the software. The ADC allows a data transfer with the PDC.

22. Power Management Controller (PMC)

The AT91SAM7A1 Power Management Controller allows optimization of power consumption. The PMC enables/disables the clock inputs of PDC and ARM core. Moreover, the main oscillator, the PLL and the analog peripherals can be put in standby mode, allowing minimum power consumption to be obtained. The PMC provides the following operating modes:

- Normal: Clock generator provides clock to chip
- Wait mode: ARM core clock is deactivated
- Slow mode: clock generator is deactivated, the system is clocked at 32.768 kHz

Each peripheral clock can be independently stopped or started directly in the peripheral to further reduce power consumption in Normal, Wait and Slow Modes.

23. ICE Debug Mode

ARM Standard Embedded In Circuit Emulation is supported via the ICE port. It is connected to a host computer via an external ICE Interface. In ICE Debug Mode, the ARM core responds with a non-JTAG chip ID which identifies the core to the ICE system. This is not JTAG IEEE 1149.1 compliant.

24. Packaging Information

Figure 24-1. 144-lead LQFP Package Orientation (Top View)

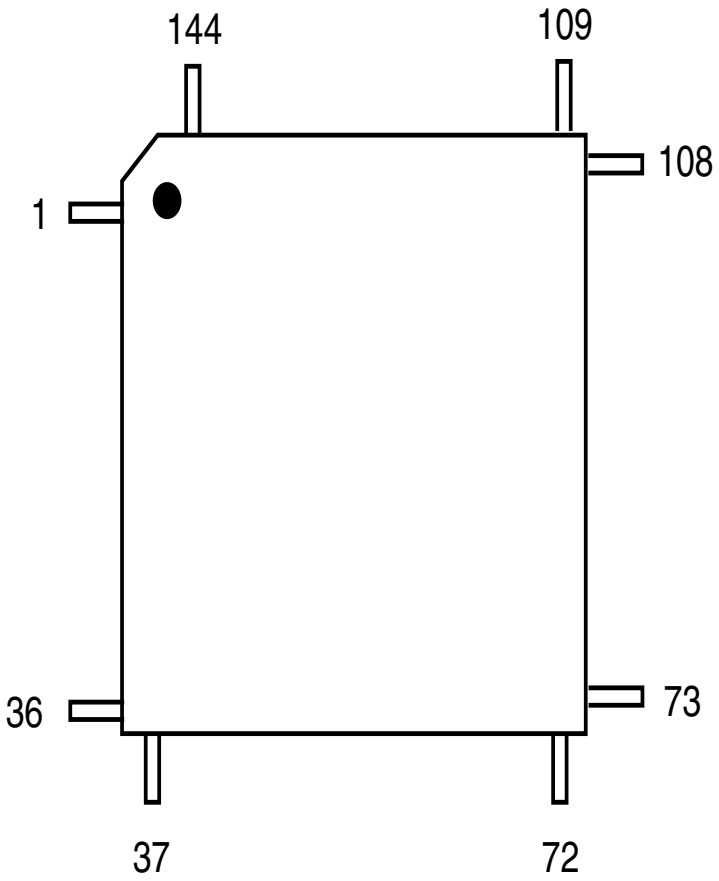


Figure 24-2. 144-pin LQFP Version A (Foundry Reference)

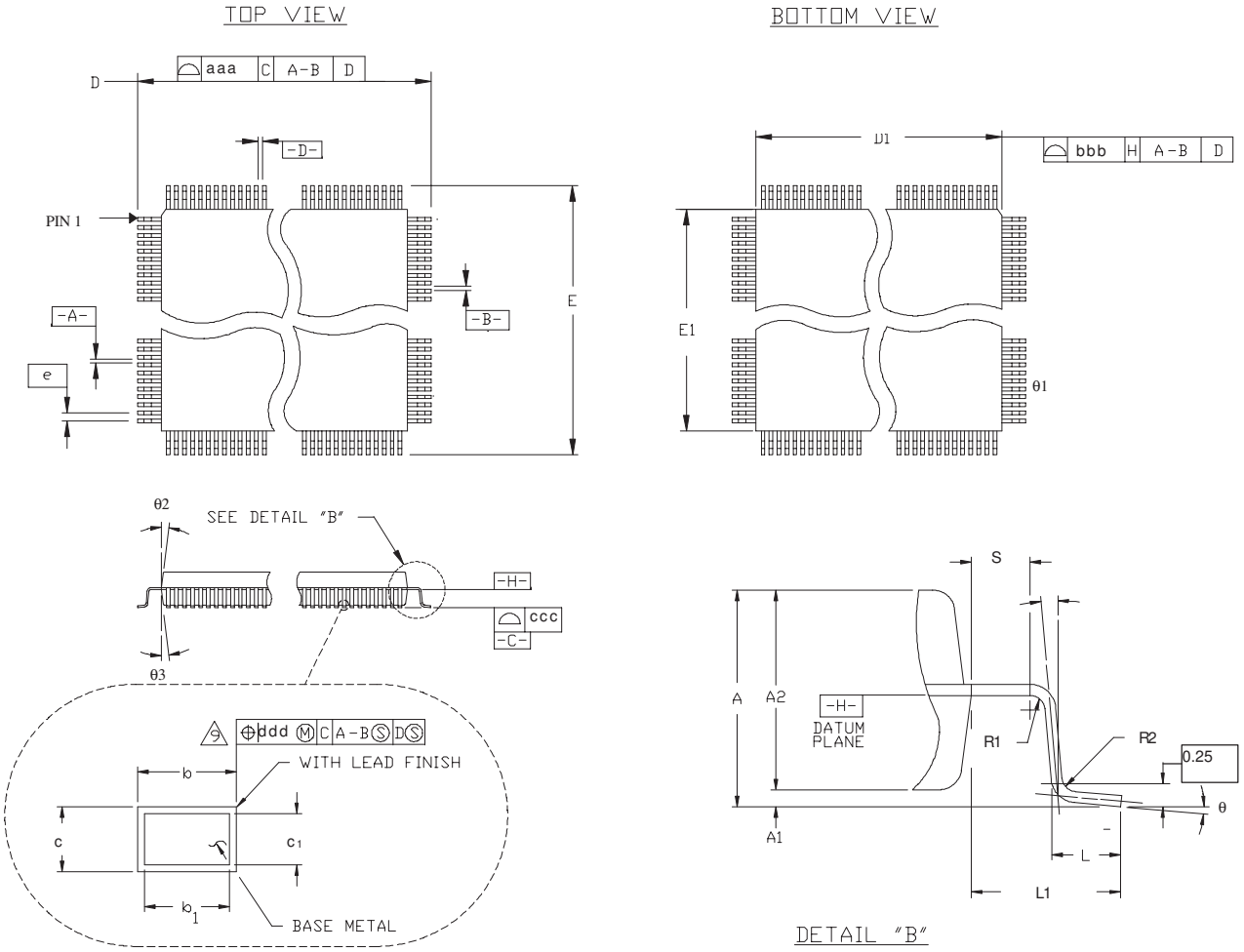


Table 24-1. Package Dimensions in mm

Symbol	Min	Nom	Max	Symbol	Min	Nom	Max
A			1.60	c	0.09		0.20
A1	0.05		0.15	L	0.45	0.60	0.75
A2	1.35	1.40	1.45	L1	1.00 REF		
D	22.00 BSC			S	0.20		
D1	20.00 BSC			b	0.17	0.20	0.27
E	22.00 BSC			e	0.50 BSC		
E1	20.00 BSC			D2	17.50		
R2	0.08		0.20	E2	17.50		
R1	0.08			Tolerances of form and position			
Q	0°	3.5°	7°	aaa	0.20		
Q1	0°			bbb	0.20		
Q2	11°	12°	13°	ccc	0.08		
Q3	11°	12°	13°	ddd	0.08		

25. Soldering Profile

Table 25-1 gives the recommended soldering profile from J-STD-20.

Table 25-1. Soldering Profile

	Convection or IR/Convection	VPR
Average Ramp-up Rate (183° C to Peak)	3° C/sec. max.	10° C/sec.
Preheat Temperature 125° C ±25° C	120 sec. max	
Temperature Maintained Above 183° C	60 sec. to 150 sec.	
Time within 5° C of Actual Peak Temperature	10 sec. to 20 sec.	60 sec.
Peak Temperature Range	220 +5/-0° C or 235 +5/-0° C	215 to 219° C or 235 +5/-0° C
Ramp-down Rate	6° C/sec.	10° C/sec.
Time 25° C to Peak Temperature	6 min. max	

Small packages may be subject to higher temperatures if they are reflowed in boards with larger components. In this case, small packages may have to withstand temperatures of up to 235° C, not 220° C (IR reflow).

Recommended package reflow conditions depend on package thickness and volume. See Table 25-2.

Table 25-2. Recommended Package Reflow Conditions(1, 2, 3)

Parameter	Temperature
Convection	220 +5/-0° C
VPR	215 to 219° C
IR/Convection	220 +5/-0° C

Notes:
1. The packages are qualified by Atmel by using IR reflow conditions, not convection or VPR.
2. By default, the package level 1 is qualified at 220° C (unless 235° C is stipulated).
3. The body temperature is the most important parameter but other profile parameters such as total exposure time to hot temperature or heating rate may also influence component reliability.

A maximum of three reflow passes is allowed per component.

26. Ordering Information

Table 26-1. AT91SAM7A1 Ordering Information

Ordering Code	Package	Package Type	Temperature Operating Range
AT91SAM7A1-AU	LQFP144	Green	Industrial (-40° C to +85° C)

Revision History

Doc. Rev.	Date	Comments	Change Request Ref.
6048AS	22-Jul-04	First issue.	
6048BS	03-Mar-05	Removed Preliminary status. Changed package from TQFP to LQFP, type Green.	
6048CS	29-JUN-06	Removed references to Automotive applications. "Features" on page 1, "Description" on page 2 replaced with features and description from full datasheet.	2740

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High-Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

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