

Figure 1. Physical Photos of ATDC1934

ORDERING GUIDE

Online Stores		Commission Fee	Unit Price (June 2024)	Buy Now
AS	shop.analogtechnologies **Our own online store**	Zero sale commission	$0.70/PCs (≥100PCs)	*
SZ	SMTZone **Our own online store**	Zero sale commission	$0.70/PCs (≥100PCs)	*
K	Digikey	≈32% sale commission	$2.81/PCs (≥100PCs)	*

Table 1. ATDC1934

Parameter	ATDC1934	LT1934
Input Voltage	4V~38V	3.2V~34V
Output Voltage	0.8V to 20V	
Output Current	700mA	300mA
Switching Frequency	750kHz	
Efficiency	≥92%@V_{IN}=12V V_{OUT}=5V	≥85%@V_{IN}=12V V_{OUT}=5V

FEATURES

- Wide Input Voltage Range: 4V to 38V
- Adjustable Output Voltage: 0.8V to 0.9V_{IN}
- Output Current: Up to 700mA
- Ultra Low Shutdown Current: 6μA
- 750kHz Switching Frequency
- High Efficiency Up to 95%@V_{IN} = 12V&I_{IN} = 400mA
- Internal Compensation and Soft-Start

APPLICATIONS

- Automotive Systems
- Automotive Battery Regulation
- Standby Power for Portable Products
- Distributed Supply Regulation
- Industrial Control Supplies
- FPGA, DSP, ASIC Power Supplies

DESCRIPTION

The ATDC1934 is a wide input range, high-efficiency, and high frequency DC-to-DC step-down switching regulator, capable of delivering up to 0.7A of output current. With a fixed switching frequency of 660kHz, this current mode PWM controlled converter allows the use of small external components, such as ceramic

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input and output caps, as well as small inductors. ATDC1934 also employs a proprietary control scheme that switches the device into a power save mode during light load, thereby extending the range of high efficiency operation. An OVP function protects the IC itself and its downstream system against input voltage surges. With this OVP function, the IC can stand off input voltage as high as 42V, making it an ideal solution for industrial applications such as smart meters as well as automotive applications.

In automotive systems, power comes from the battery, with its voltage typically between 9V and 24V. Including cold crank and double battery jump-starts, the minimum input voltage may be as low as 4V and the maximum up to 36V, with even higher transient voltages. With these high input voltages, linear regulators cannot be used for high supply currents without overheating the regulator. Instead, high efficiency switching regulators such as ATDC1934 must be used to minimize thermal dissipation.

ATDC1934 is available SOT23-6 Packages.

PIN CONFIGURATION

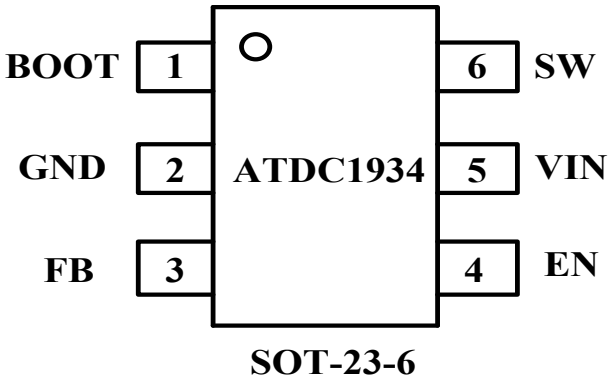


Figure 2. Pin Configuration

APPLICATION CIRCUIT

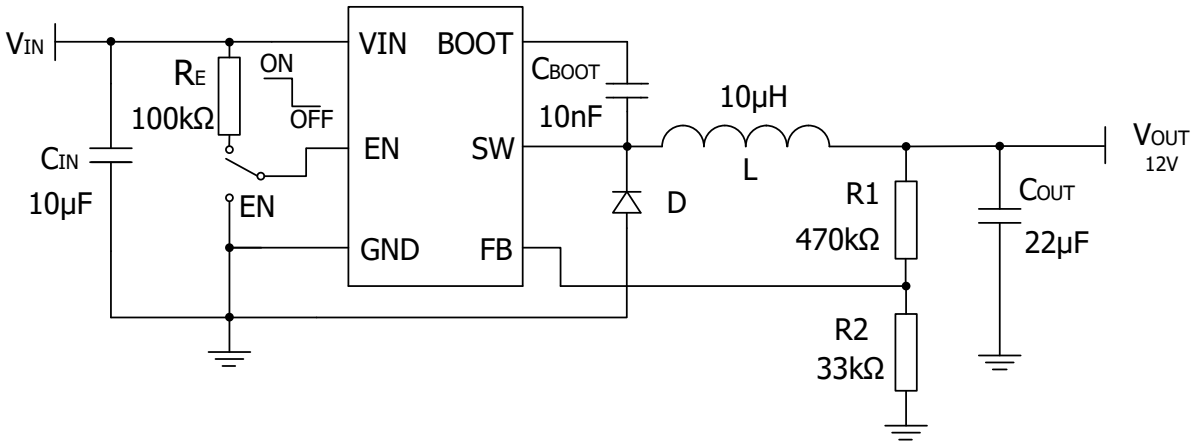


Figure 3. Typical Application Circuit

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PIN FUNCTIONS

Table 1. Pin Names, Types and Descriptions.

NO.	NAME	DESCRIPTION
1	BOOST	Bootstrap pin is used to provide a drive voltage, higher than the input voltage, to the topside power switch. Place a 10nF boost capacitor (C_{BOOT}) as close as possible to the IC between this pin and SW pin. Do not place a resistor in series with this pin.
2	GND	Ground. Connect all the input and output capacitors to GND.
3	FB	Feedback pin for programming the output voltage. The ATDC1934 regulates the FB pin to 0.8V. Connect the feedback resistor divider tap to this pin. If the FB voltage exceeds 110% of 0.8V, over-voltage protection (OVP) will stop all PWM switching.
4	EN	Enable pin should not be left open and it should not be driven above VIN + 0.3V. Device will operate when the EN pin is high and shut down when the EN pin is low. EN can be tied to VIN pin via a resistor if the shutdown feature is not required or to a logic input for controlling shutdown.
5	VIN	The VIN pin supplies current to the ATDC1934's internal regulator and to the internal power switch. This voltage is monitored by a UVLO lockout comparator. VIN is also connected to the drain of the converter top switch. Due to power switching, this pin has high di/dt transition edges and must be decoupled to the GND by input capacitors as close as possible to the GND pin to minimize the parasitic inductances.
6	SW	Switching node pin is the output of the internal power converter and should be connect to the output inductor. Bootstrap capacitor also connects to this pin. This node should be kept small on the PCB to minimize capacitive coupling, noise coupling and radiation.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Input Voltage V_{IN}	4V ~ 38V
BOOST Pin Above SW Pin	−0.3V to SW+6V
EN Pin	−0.3V to V_{IN}+0.3V
FB Voltage	−0.3V to 6V
SW Voltage	−0.3V to V_{IN}+0.3V
Operating Temperature Range	−40°C ~ 85°C
Maximum Junction Temperature	150°C
Storage Temperature Range	−55°C ~ 150°C
Lead Temperature (Soldering, 10 sec)	260°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input terminals are diode-clamped to the power supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less.

ESD CAUTION

ESD (electrostatic discharge) sensitive device.
Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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ELECTRICAL CHARACTERISTICS

Table 3. T_A = 25°C. V_{IN} = 12V, unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Unit/Note
Input Voltage		4	–	38	V
Input Standoff Voltage		42			V
Input UVLO	Rising, Hysteresis=140mV	–	3.80		V
Switching Frequency	Rising, Hysteresis=1.3V		38		V
Input Supply Current	V_{FB} =0.85V		0.6		mA
Input Shutdown Current			6		μA
FB Feedback Voltage		0.78	0.80	0.82	V
Switching Frequency			660		kHz
Maximum Duty Cycle		90			%
FoldBack Frequency	V_{FB} = 0V		60		kHz
High side Switch On Resistance	I_{SW} =200mA		400		mΩ
High side Switch Current Limit			1.2		A
SW Leakage Current	V_{IN}=12V, V_{SW}=0, EN= GND			10	μA
EN Input Current	V_{IN}=12V, V_{EN} =5V		1	5	μA
EN Input Low Voltage	Rising, Hysteresis=100mV	0.8	1.1	1.4	V
Thermal Shutdown	T_{SHDN}		150		°C
Thermal Shutdown Hysteresis	T_{HYS}		20		°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The ATDC1934 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The ATDC1934 specification is guaranteed over the –40°C to 125°C temperature range.

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TYPICAL PERFORMANCE CHARACTERISTICS

Typical values are at T_A=25°C, unless otherwise noted.

Start-up Waveform with EN

V_{IN}=12V V_{OUT}=5V I_{OUT}=0A

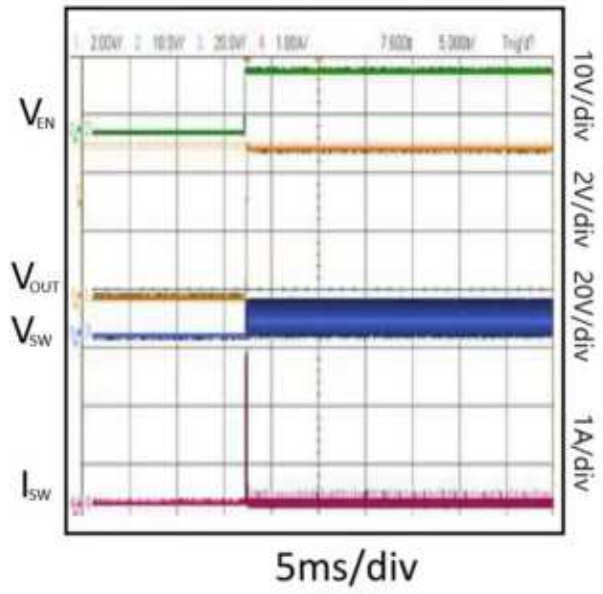


Figure 4. Start-up

Shut-down Waveform with EN

V_{IN}=12V V_{OUT}=5V I_{OUT}=0.5A

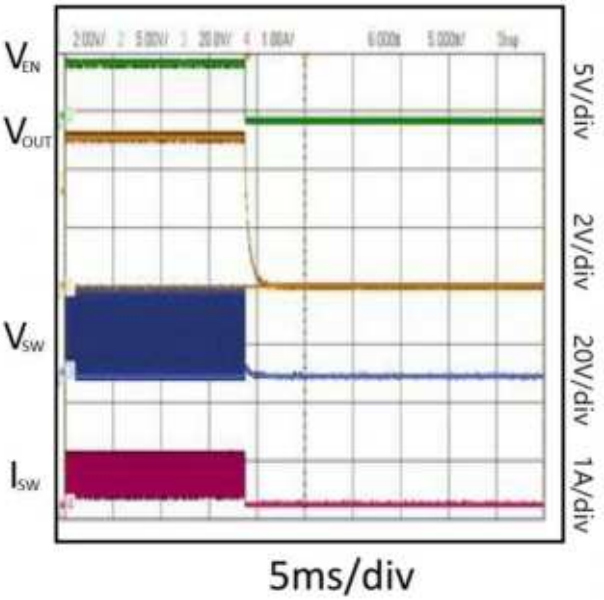


Figure 5. Shut-down

Switching Waveform

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0.1A

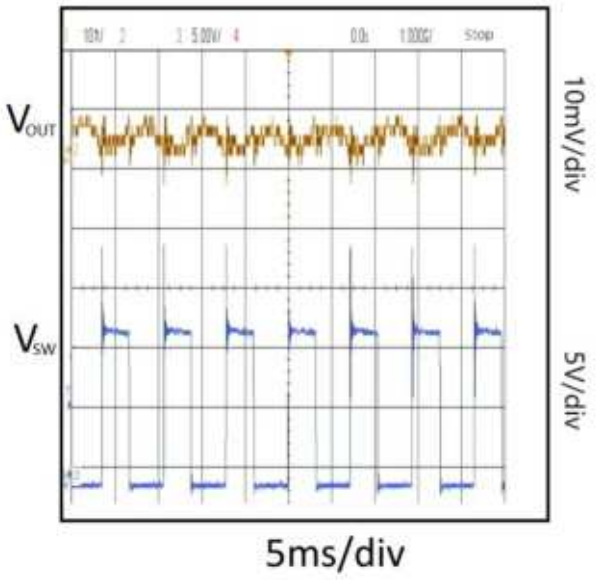


Figure 6. Switching Waveform

Switching Waveform

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0.3A

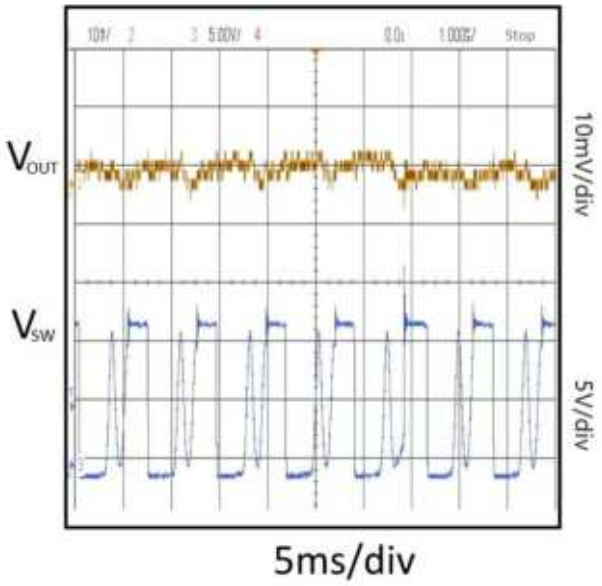


Figure 7. Switching Waveform

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Load Transient Response

V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=0 to 0.5A

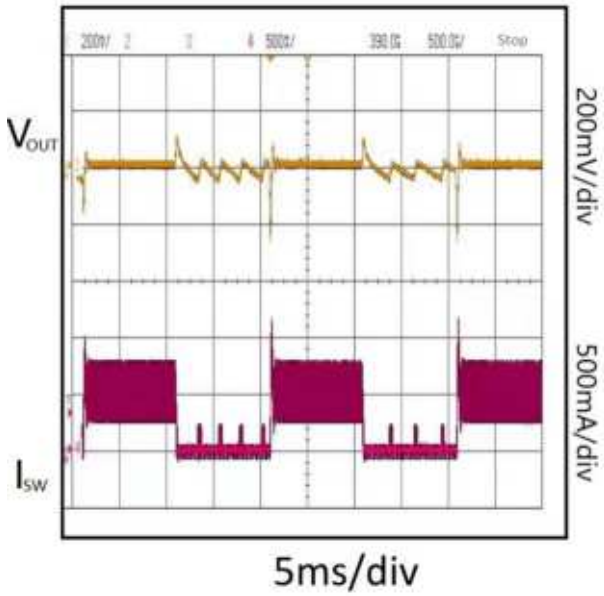


Figure 8. Load Transient Response

Load Transient Response

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0 to 0.5A

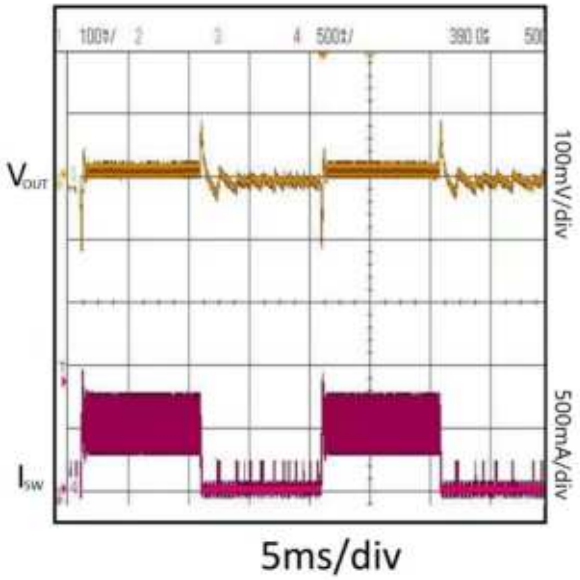


Figure 9. Load Transient Response

Short-Circuit Response

V_{IN}=24V, V_{OUT}=5V, I_{OUT}=0 to Short

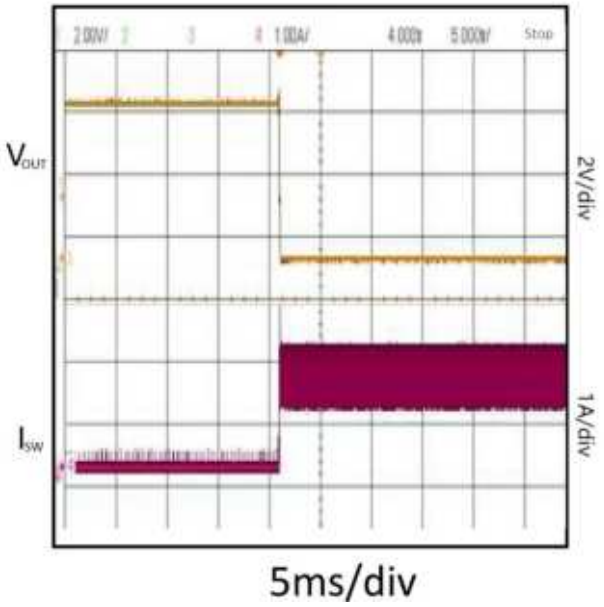


Figure 10. Short-Circuit

Short-Circuit Recovery

V_{IN}=24V, V_{OUT}=5V, I_{OUT}= Short to 0A

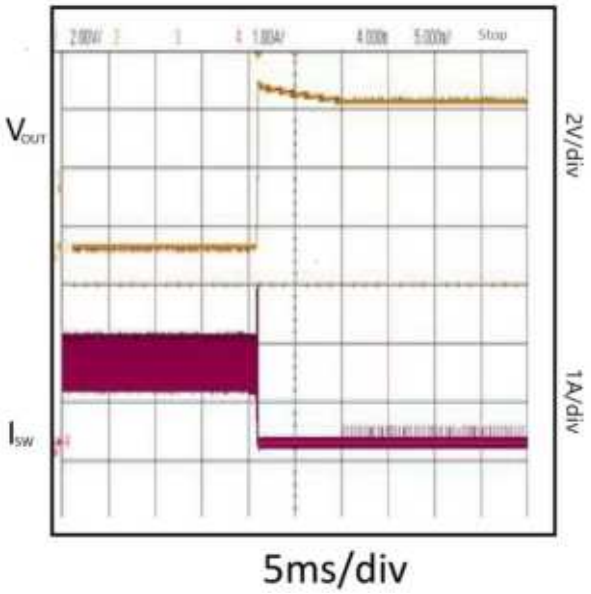


Figure 11. Short-Circuit

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TYPICAL PERFORMANCE CHARACTERISTICS

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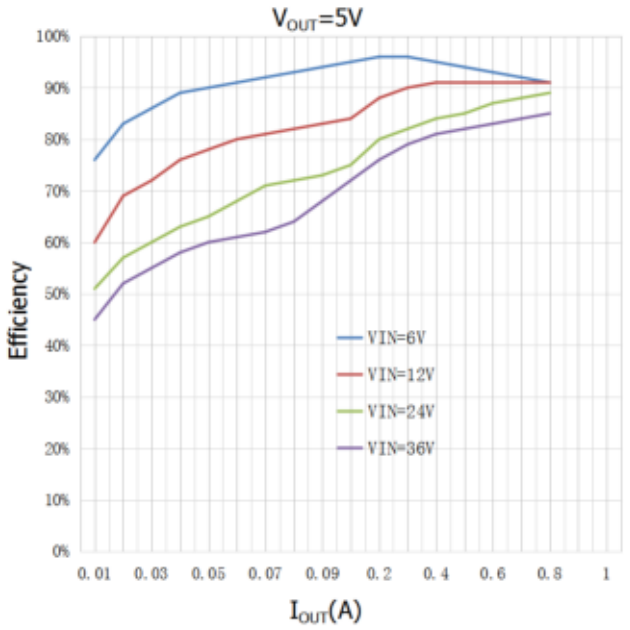


Figure 12. Efficiency vs. I_{OUT}

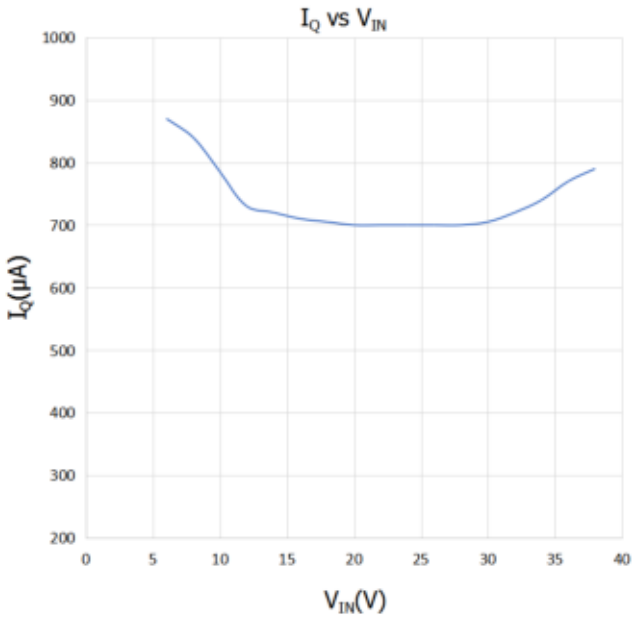


Figure 14. Efficiency vs. I_{OUT}

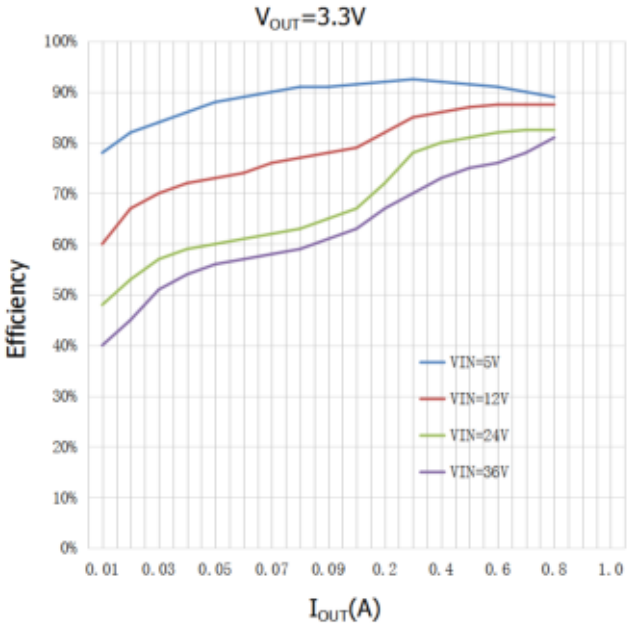


Figure 13. Efficiency vs. I_{OUT}

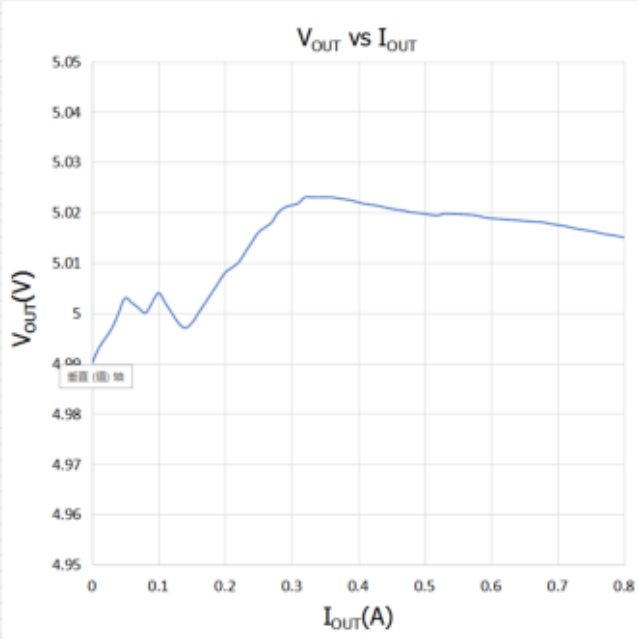


Figure 15. Output Voltage vs. I_{OUT}

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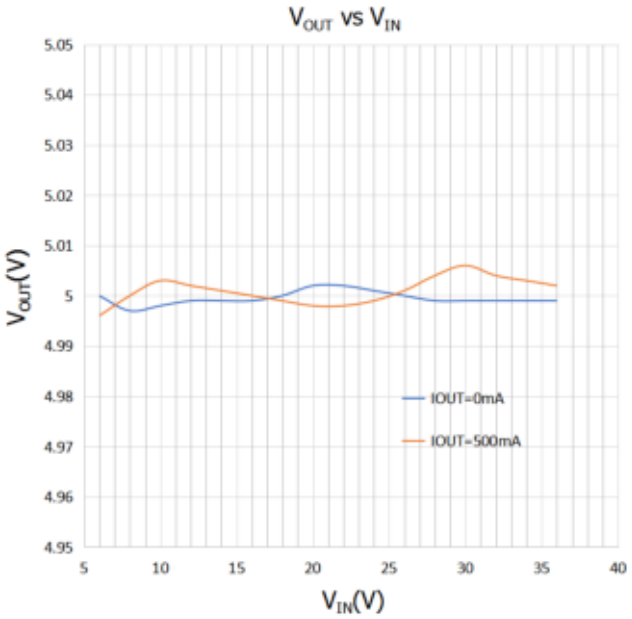


Figure 16. V_{OUT} vs. I_{OUT}

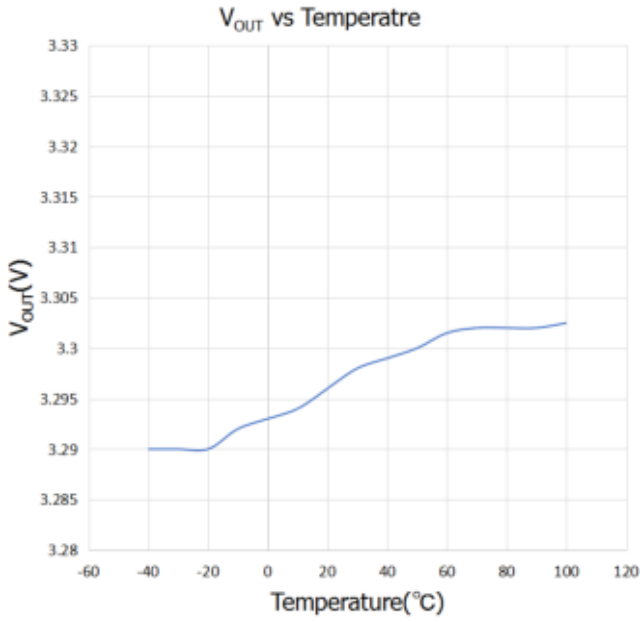


Figure 17. V_{OUT} vs. Temperature

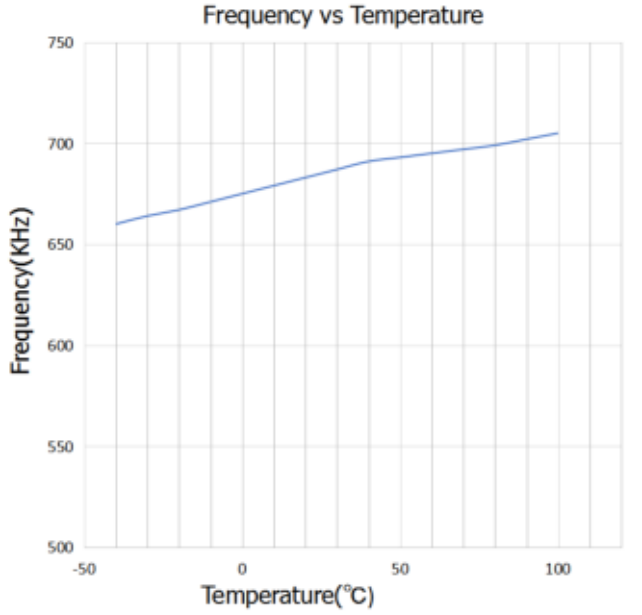


Figure 18. Frequency vs. Temperature

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FUNCTIONAL BLOCK DIAGRAM

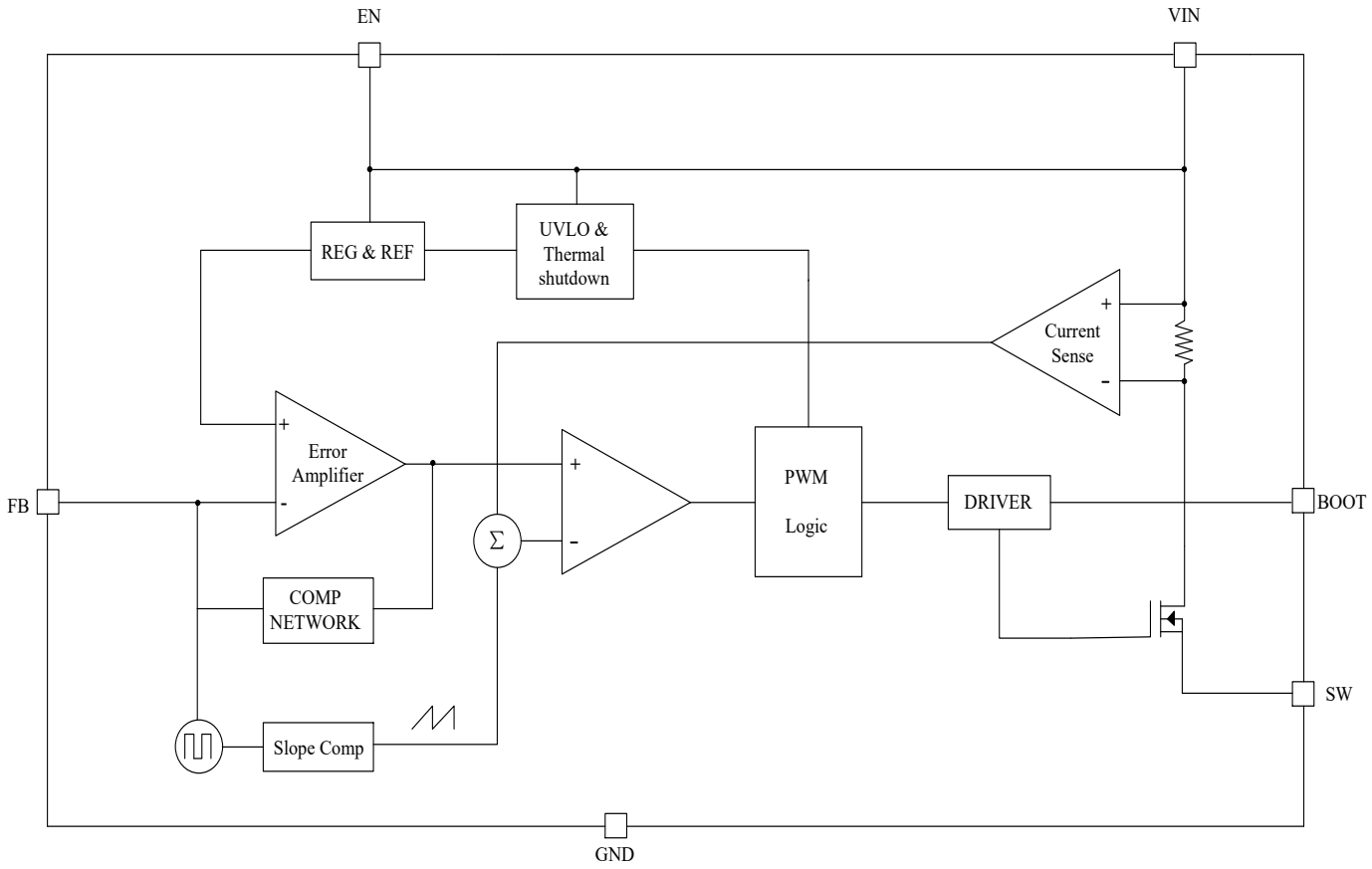


Figure 19. Block Diagram

APPLICATION INFOR MATION

The ATDC1934 is an internally compensated wide input range current mode controlled synchronous step-down converter. It is designed for high reliability and is particularly suitable for power conditioning from unregulated sources or battery-powered applications that need low sleep/shutdown currents. It also features a power-save mode in which operating frequency is adaptively reduced under light load conditions to reduce switching and gate losses and keep high efficiency. At no load and with switching stopped, the total operating current is approximately 14μA. If the device is disabled, the total consumption is typically 0.6μA.

Figure 19 shows the simplified block diagram of the ATDC1934. The power level integrated MOSFET switches have overcurrent protection and can provide up to 600mA of continuous current to the load. Current limiting of the switches also prevents inductor current runaway. The converter switches are optimized for high efficiency at low duty cycle.

During initial power-up of the device (soft-start), current limit and frequency fold-back are activated to prevent inductor current runaway while the output capacitor is charging to the desired V_{OUT}.

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Peak-Current Mode (PWM Control)

Figure 19 shows the functional block diagram and Figure 20 shows the switching node operating waveforms of the ATDC1934. Switching node voltage is generated by controlling the duty cycles of the complementary high-side and low-side switches. The duty cycle of the high-side switch is used as control parameter of the buck converter to regulate output voltage and is defined as: $D = t_{ON}/t_{SW}$, where t_{ON} is the high-side switch on-time and t_{SW} is the switching period. During high-side switch on-time, the SW pin voltage swings up to approximately V_{IN}, and the inductor current, I_L, linearly rises with a slope of $(V_{IN}-V_{OUT})/L$. When control logic turns off the high-side switch, the low-side switch will turn on after a short dead time. During off-time, inductor current discharges through the low-side switch with a slope of $(-V_{OUT}/L)$. In ideal case, where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage $D = V_{OUT}/V_{IN}$.

The ATDC1934 employs fixed-frequency peak-current mode control in continuous conduction mode (when inductor minimum current is above zero). In light load conditions (when the inductor current reaches zero) the ATDC1934 will enter discontinuous conduction mode and the control mode will change to shift frequency, peak-current mode to reduce the switching frequency and the associated switching and gate driving losses (power-save mode).

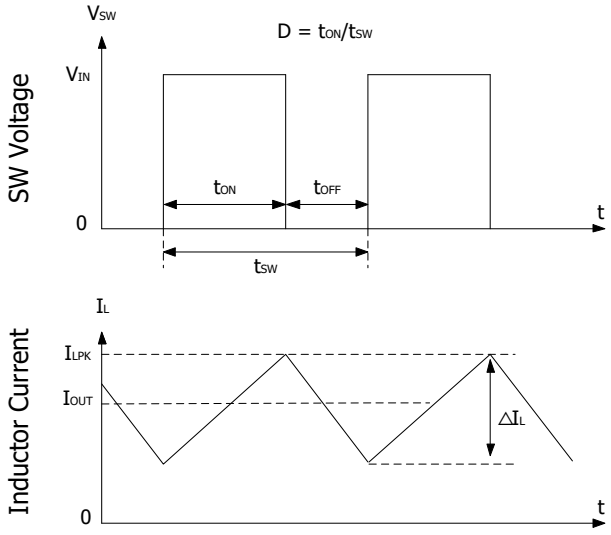


Figure 20. SW Node and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

DETAILED DESCRIPTION

In continuous conduction mode,ATDC1934 operates at fixed-frequency using peak-current mode control scheme. The controller has an outer voltage feedback loop to get accurate DC voltage regulation. The output of the outer loop is fed to an inner peak-current control loop as reference command that adjusts the peak-current of the inductor.

The voltage feedback loop is internally compensated, which allows for fewer external components, simpler design, and stable operation with almost any combination of output capacitors.

Power-Save Mode

Note that the on-time of synchronous rectifier switch should always be long enough to fully charge the bootstrap capacitor and prevent bootstrap under voltage lockout due to insufficient voltage for the high-side switch gaLoop Operationte driver.

Loop Operation

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The ATDC1934 is a wide input range, high-efficiency,DC-to-DC step-down switching regulator, capable of delivering up to 0.7A of output current, integrated with a 400mΩ MOSFET. It uses a PWM current-mode control scheme. An error amplifier integrates error between the FB signal and the internal reference voltage. The outputof the integrator is then compared to the sum of a current-sense signaland the slope compensation ramp. This operation generates a PWM signal that modulates the duty cycle of the power MOSFET to achieve regulation for output voltage.

APPLICATION INFORMATION

Setting Output Voltages

Output voltages are set by external resistors. The FB threshold is 0.8V.

$R_{TOP} = R_{BOTTOM} \times [(V_{OUT} / 0.8) - 1]$

Inductor Selection

The peak-to-peak ripple is limited to 30% of the maximum output current. This places the peak current far enough from the minimum overcurrent trip level to ensure reliable operation while providing enough current ripples for the current mode converter to operate stably. In this case, for 0.7A maximum output current, the maximum inductor ripple current is 300 mA. The inductor size is estimated as following equation:

$L_{IDEAL} = (V_{IN(MAX)}-V_{OUT})/I_{RIPPLE}*D_{MIN}*(1/F_{OSC})$

Therefore, for V_{OUT}=5V, the inductor values is calculated to be L = 13μH. Chose 10μH or 15μH.

For V_{OUT} =3.3V, the inductor values is calculated to be L = 9.2μH. Chose 10μH.

Output Capacitor Selection

For most applications a nominal 22μF or larger capacitor is suitable. The ATDC1934 internal compensation is designed for a fixed corner frequency that is equal to FC=8.7kHz For example, for V_{OUT}=5V, L=15μH, C_{OUT}=22μF. The output capacitor keeps output ripple small and ensures control-loop stability. The output capacitor must also have low impedance at the switching frequency. Ceramic, polymer, and tantalum capacitors are suitable, with ceramic exhibiting the lowest ESR and high-frequency impedance. Output ripple with a ceramic output capacitor is approximately as follows:

$V_{RIPPLE} = I_{L(PEAK)}[1/(2\pi \times f_{OSC} \times C_{OUT})]$ If the capacitor has significant ESR, the output ripple component due to capacitor ESR is as follows:

$V_{RIPPLE}(ESR) = I_{L(PEAK)} \times ESR$

Input Capacitor Selection

The input capacitor in a DC-to-DC converter reduces current peaks drawn from the battery or other input power source and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source. The output capacitor keeps output ripple small and ensures control-loop stability.

Components Selection

V_{OUT}	C_{OUT}	L
8V	22μH	15μH to 22μH
5V	22μH	10μH to 15μH
3.3V	22μH	6.5μH to 10μH

The minimum and maximum duty cycles without frequency fold-back are given by:

$$D_{MIN} = t_{ON_MIN} \times f_{SW} \quad (1)$$

and

$$D_{MAX} = 1 - t_{OFF_MIN} \times f_{SW} \quad (2)$$

Given a required output voltage, the maximum V_{IN} without frequency fold-back is given by:

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$$V_{IN\text{-}MAX} = \frac{V_{OUT}}{f_{SW} \times t_{ON\text{-}MIN}} \quad (3)$$

and the minimum V_{IN} without frequency fold-back can be calculated by:

$$V_{IN\text{-}MIN} = \frac{V_{OUT}}{1 - f_{SW} \times t_{OFF\text{-}MIN}} \quad (4)$$

Input Voltage

The ATDC1934 can operate efficiently for inputs as high as 38V. For CCM operation (continuous conduction mode) keep duty cycle between 12% and 88%

Output Voltage

The output voltage can be stepped down to as low as the 0.8V reference voltage (V_{REF}). As explained before, when the output voltage is set to 0.8V and there is no voltage divider, a minimum small load will be needed.An 80kΩ resistor to ground will prevent the output voltage floating up.

Soft-Start

The integrated soft-start circuit in ATDC1934 limits the input inrush current right after power-up or enabling the device. Soft-start is implemented by slowly ramping up the reference voltage that in turn slowly ramps up the output voltage to its target regulation value.

Enable

EN pin turns the ATDC1934 operation on or off. An applied voltage of less than 0.5V shuts down the device, and a voltage of more than 1.2V is required to start the regulator. The EN pin is an input and must not be left open. The simplest way to enable the device is to connect the EN pin to VIN pin via a resistor. This allows for self-startup of the AT1934 when VIN is within the operating range.

An external logic signal can be used to drive the EN input for power savings, power supply sequencing and/or protection. If the EN pin is driven by an external logic signal, a 10kΩ resistor in series with the input is recommended.

Note: Voltage on the EN pin should never exceed V_{IN} +0.3V. Do not drive the EN pin with a logic level if V_{IN} is not present. This can damage the EN pin and the device.

Thermal Shutdown

The ATDC1934 provides an internal thermal shutdown to protect the device when the junction temperature exceeds +150°C. Both switches stop switching in thermal shutdown. Once the die temperature falls below +130°C, the device reinitiates the power-up sequence by the internal soft-start.

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APPLICATION INFORMATION

Output Voltage Programming

Output voltage can be set with a resistor divider feedback network between output and FB pin as shown in Figure 3 . Usually, a design is started by selecting lower resistor R_1 and calculating R_2 with the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (5)$$

where V_{REF} =0.8V.

To keep operating quiescent current small and prevent voltage errors due to leakage currents, it is recommended to choose R1 in the range of 10kΩ to 100kΩ.

If the output has no load other than the FB divider, make sure the divider draws at least 10μA from V_{OUT} or an internal current source (5μA ~ 6μA) from BOOT to SW will slowly charge the output capacitor beyond the desired voltage.

Inductor Selection

The critical parameters for selecting the inductor are the inductance (L), saturation current (I_{sat}) and the maximum RMS current ($I_{rms,max}$). The inductance is selected based on the desired peak-to-peak ripple current ΔI_L that is given in Equation 6 for CCM. Since the ripple current increases with the input voltage, the maximum input voltage is usually considered to calculate the minimum inductance L_{MIN} that is given in Equation 7. K_{IND} is a design parameter that represents the ratio of inductor ripple current to its maximum operating DC current. Lower K_{IND} means higher inductance value that needs a larger size and higher KIND results in more ripple and loss in the core. Typically, a reasonable value for K_{IND} is around 20%~40%. Inductor peak-current should never exceed the saturation even in transients to avoid over-current protection. Also inductor RMS rating should always be larger than operating RMS current even at maximum ambient temperature.c

$$\triangle I_L = \frac{V_{OUT} \times (V_{IN\text{-}MAX} - V_{OUT})}{V_{IN\text{-}MAX} \times L \times f_{SW}} \quad (6)$$

$$L_{MIN} = \frac{V_{IN\text{-}MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\text{-}MAX} \times f_{SW}} \quad (7)$$

where $K_{IND} = \triangle I_L / I_{OUT}$ (max DC current).

Note that lower inductance is usually preferred in a switching power supply, because it usually corresponds to faster transient response and bandwidth, smaller DCR, and reduced size for a more compact design. On the other hand, if the inductance is too small, current ripple will increase which can trigger over-current protection. Larger inductor current ripple also implies larger output voltage ripple with the same output capacitors. For peak-current mode control, it is recommended to choose large current ripple, because controller comparator performs better with higher signal to noise ratio. So, for this design example, K_{IND} = 0.4 is chosen, and the minimum inductor value is calculated to be 15.3μH. The nearest standard value would be a 22μH ferrite inductor with a 1A RMS current rating and 1.5A saturation current that are well above the designed converter output current RMS and DC respectively.

Bootstrap Capacitor Selection

The ATDC1934 requires a small external bootstrap capacitor, C_{BOOT}, between the BOOT and SW pins to provide the gate drive supply voltage for the MOSFET. The bootstrap capacitor is refreshed when the MOSFET is off An X7R or X5R 10nF ceramic capacitor with a voltage rating of 16V or higher is recommended for stable operating performance over temperature and

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voltage variations.

APPLICATION INFORMATION

Input Capacitor Selection

The ATDC1934 requires high frequency input decoupling capacitor(s). The recommended high frequency decoupling capacitor value is 10μF X5R or X7R or higher. It is recommended to choose the voltage rating of the capacitor(s) at least twice the maximum input voltage to avoid derating of the ceramic capacitors with DC voltage. Some bulk capacitances may be needed, especially if the ATDC1934 is not located within 5cm distance from the input voltage source for input stability.

Bulk capacitors have high Equivalent Series Resistance(ESR) and can provide the damping needed to prevent input voltage spiking due to the wiring inductance of the input. The value for this capacitor is not critical but must be rated to handle the maximum input voltage including ripple.

For this design, one 10μF, X7R, 50V is used for the input decoupling capacitor. The ESR is approximately 10mΩ, and the current rating is 1A. To improve high frequency filtering a small parallel 0.1μF capacitor may be placed as close as possible to the device pins.

Output Capacitor Selection

The device is designed to be used with a wide variety of LC filters. It is generally desired to use as little outpour capacitance as possible to keep cost and size down and bandwidth high. The output capacitor(s), C_{OUT}, should be chosen carefully since it directly affects the steady state output voltage ripple, loop stability and the voltage over/undershoot during load current transients. The output voltage ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the ESR of the output capacitors:

$$\Delta V_{OUT_ESR} = \Delta I_L \times ESR = K_{IND} \times I_{OUT} \times ESR \quad (8)$$

The other part is caused by the inductor current ripple charging and discharging the output capacitors:

$$\triangle V_{OUT\text{-}C} = \frac{\triangle I_L}{8 \times f_{SW} \times C_{OUT}} \times \frac{I_{OUT} \times K_{IND}}{8 \times f_{SW} \times C_{OUT}} \quad (9)$$

The two components in the voltage ripple are not in phase, so the actual peak-to-peak ripple is smaller than the sum of the two peaks.

Output capacitance is usually limited by transient performance specifications if the system requires tight voltage regulation in presence of large current steps and/or fast slew rate. When a large load step happens, output capacitors provide the required charge before the inductor current can slew up to the appropriate level. The regulator's control loop usually needs 8 or more clock cycles to regulate the inductor current equal to the new load level. The output capacitance must be large enough to supply the current difference for 8 clock cycles to maintain the output voltage within the specified range. Equation 10 shows the minimum output capacitance needed for specified output over/undershoot.

$$C_{OUT} > \frac{1}{2} \times \frac{8 \times (I_{OH} - I_{OL})}{f_{SW} \times \triangle C_{OUT_SHOOT}} \quad (10)$$

where:

I_{OL} = Low level of the output current step during load transient.

I_{OH} = High level of the output current during load transient.

V_{OUT_SHOOT} = Target output voltage over/undershoot.

For this design example, the target output ripple is 30mV. Assuming $\Delta V_{OUT_ESR}=\Delta V_{OUT_C}=30mV$, and choosing K_{IND} = 0.4, Equation 8 requires ESR to be less

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than 125mΩ and Equation 9 requires C_{OUT}>0.83μF. The target over/undershoot range of this design is ΔV_{OUT_SHOOT} = 5% × V_{OUT} = 250mV. From Equation 10, C_{OUT}>8μF. So, in summary, the most stringent criteria for the output capacitor is transient constrain of C_{OUT}> 8μF. For the derating margin, one 22μF, 10V, X7R ceramic capacitor with 10mΩ ESR is used.

PCB LAYOUT

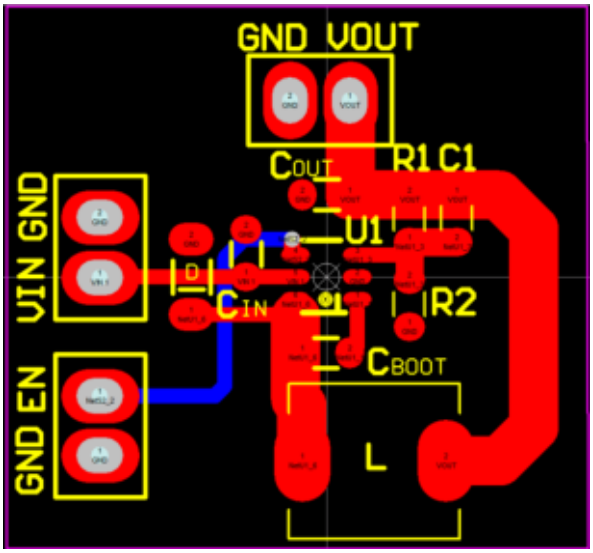


Figure 21. PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figure 21 shows the recommended component placement with trace, ground plane and via locations. Note that large, switched currents flow in the ATDC1934 VIN and SW pins, the catch diode (D) and the input capacitor (C_{IN}). The loop formed by these components should be as small as possible. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane below these components. The SW and BOOST nodes should be as small as possible. Finally, keep the FB nodes small so that the ground traces will shield them from the SW and BOOST nodes. The Exposed Pad on the bottom of the package must be soldered to ground so that the pad acts as a heat sink. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the ATDC1934 to additional ground planes within the circuit board and on the bottom side.

PACKAGE OUTLINE DUTLINE DIMENSIONS

SOT-23-6

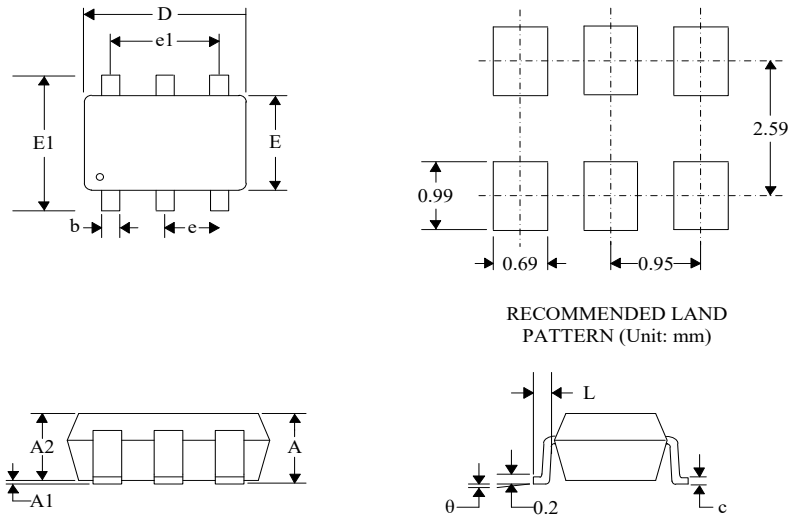
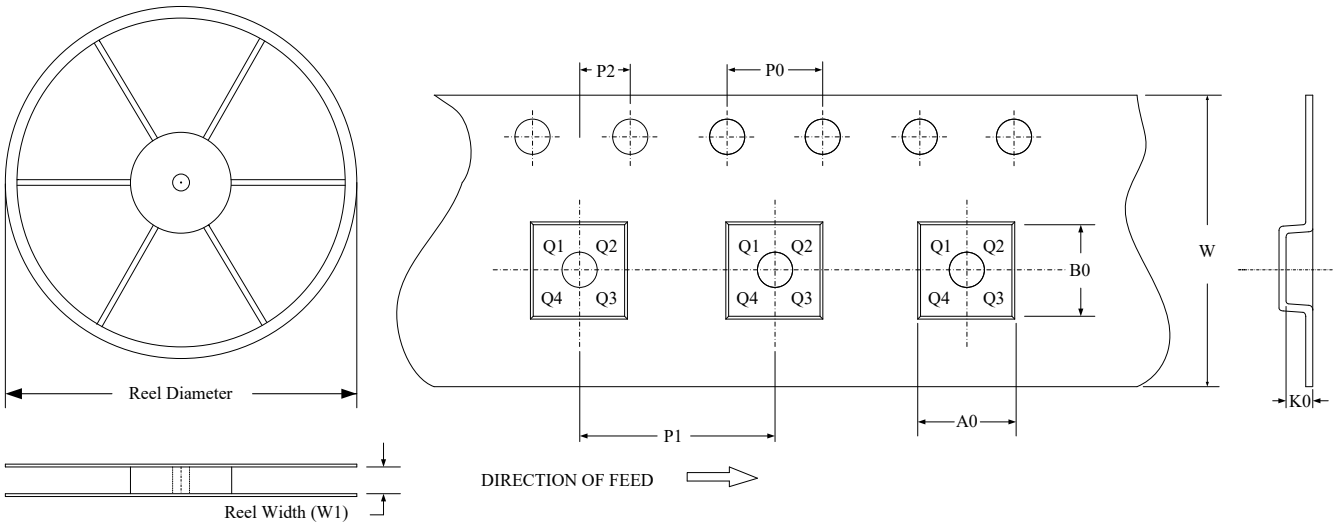


Figure 22. Dimensions

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Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.05	1.25	0.041	0.049
A1	0.00	0.10	0.000	0.004
A2	1.05	1.15	0.041	0.045
b	0.30	0.50	0.012	0.20
c	0.10	0.20	0.004	0.008
D	2.82	3.02	0.111	0.119
E	1.50	1.70	0.059	0.067
E1	2.65	2.95	0.104	0.116
e	0.950 BSC		0.037 BSC	
e1	1.900 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

TAPE AND REEL INFORMATION



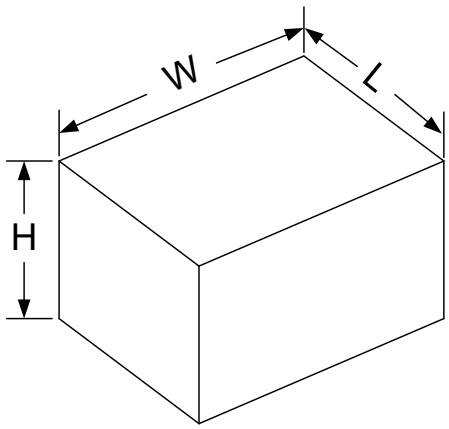
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KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-6	7″	9.5	3.17	3.23	1.37	4.0	4.0	2.0	0.8	Q3

CARTON BOX DIMENSIONS



Note: The picture is only for reference.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

ORDERING INFORMATION

Part Number	Buy Now
ATDC1934	

*: both and are our online store icons. Our products can be ordered from either one of them with the same pricing and delivery time.

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