DATA SHEET

AU5780A
SAE/J1850/VPW transceiver

Product data
Supersedes data of 1999 Jan 28

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SAE/J1850/VPW transceiver AU5780A

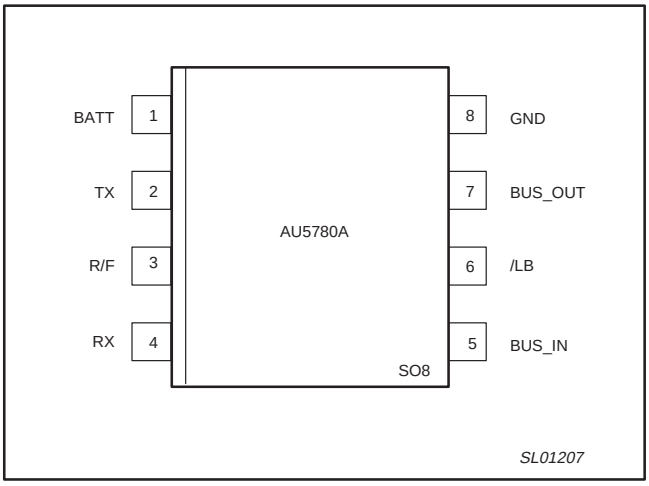
FEATURES

- Supports SAE/J1850 VPW standard for in-vehicle class B multiplexing
- Bus speed 10.4 kbps nominal
- Drive capability 32 bus nodes
- Low RFI due to output waveshaping with adjustable slew rate
- Direct battery operation with protection against +50V load dump, jump start and reverse battery
- Bus terminals proof against automotive transients up to –200V/+200V
- Thermal overload protection
- Very low bus idle power consumption
- Diagnostic loop-back mode
- 4X mode (41.6 kbps) reception capability
- ESD protected to 9 KV on bus and battery pins
- 8-pin SOIC

DESCRIPTION

The AU5780A is a line transceiver being primarily intended for in-vehicle multiplex applications. It provides interfacing between a link controller and the physical bus wire. The device supports the SAE/J1850 VPWM standard with a nominal bus speed of 10.4 kbps.

PIN CONFIGURATION



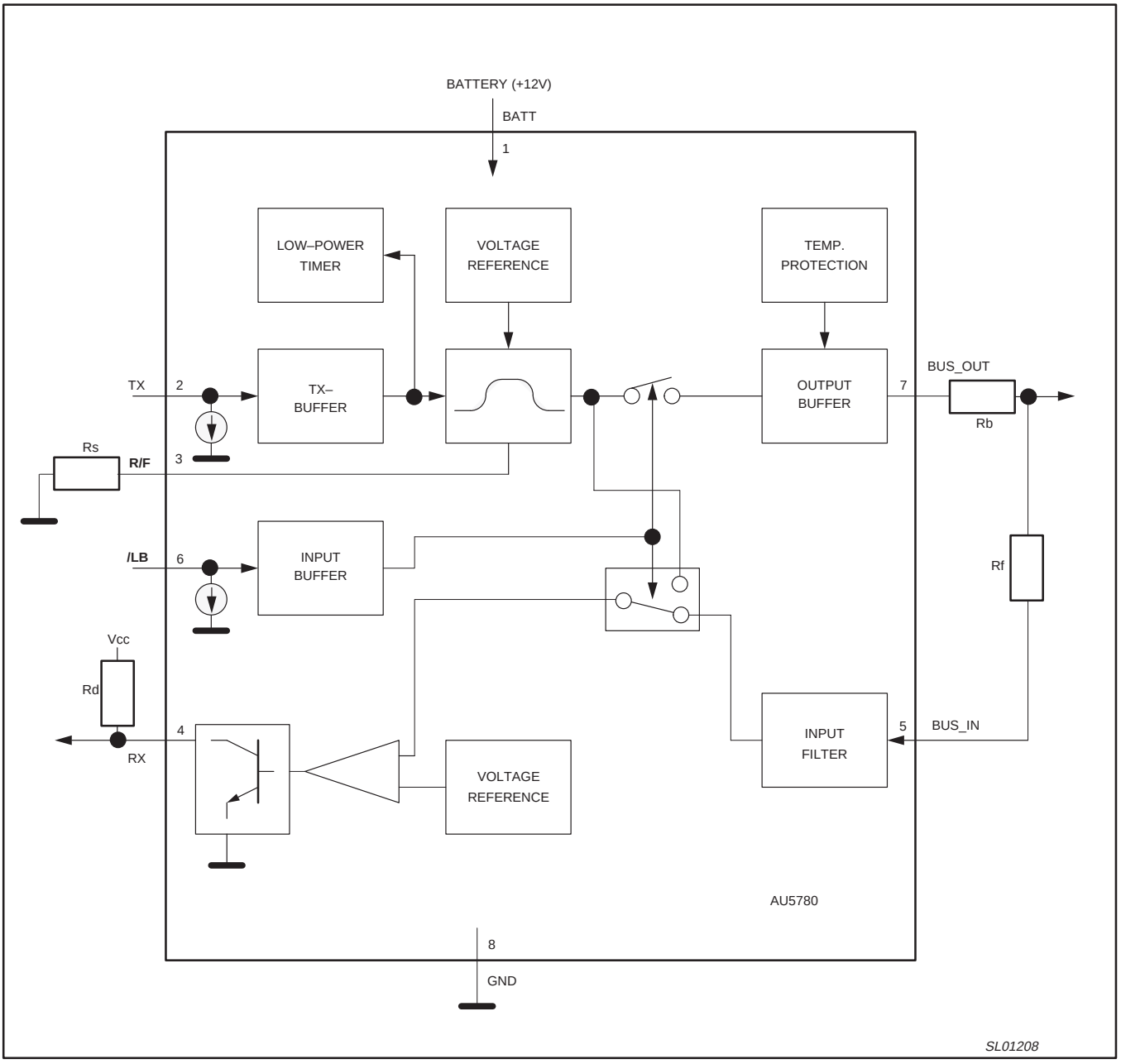
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{BATT.op}$	Operating supply voltage		6	12	24	V
T_A	Operating ambient temperature		–40		+125	°C
$V_{BATT.ld}$	Battery voltage	load dump; 1s			+50	V
$I_{BATT.lp}$	Bus idle supply current	V_{BATT}=12V			220	µA
V_B	Bus voltage	$0 < V_{BATT} < 24V$	–20		+20	V
V_{BOH}	Bus output voltage	$300\Omega < R_L < 1.6k\Omega$	7.3		8.0	V
$-I_{BO.LIM}$	Bus output source current	$0V < V_{BO} < +6.0V$	27		50	mA
V_{BI}	Bus input threshold		3.65		4.1	V
t_{bo}	Delay TX to BUS_OUT, normal battery	Measured at 3.875V	13		21	µs
t_r, t_f	BUS_OUT transition times, rise and fall, normal battery	Measured between 1.5 V and (V_{BATT} – 2.75 V), $9 < V_{BATT} < 16$ V, t_r tested at an additional bus load of R_{LOAD} = 400 Ω and C_{LOAD} = 22000 pF	11		18	µs

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
SO8: 8-pin plastic small outline package	–40 to +125°C	AU5780AD	SOT96-1

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN	DESCRIPTION
BATT	1	Battery supply input (12V nom.)
TX	2	Transmit data input; low: transmitter passive; high: transmitter active
R/F	3	Rise/fall slew rate set input
RX	4	Receive data output; low: active bus condition detected; float/high: passive bus condition detected
BUS_IN	5	Bus line receive input
/LB	6	Loop-back test mode control input; low: loop-back mode; high: normal communication mode
BUS_OUT	7	Bus line transmit output
GND	8	Ground

FUNCTIONAL DESCRIPTION

The AU5780A is an integrated line transceiver IC that interfaces an SAE/J1850 protocol controller IC to the vehicle's multiplexed bus line. It is primarily intended for automotive "Class B" multiplexing applications in passenger cars using VPW (Variable Pulse Width) modulated signals with a nominal bit rate of 10.4 kbps. The AU5780A also receives messages in the so-called 4X mode where data is transmitted with a typical bit rate of 41.6 kbps. The device provides transmit and receive capability as well as protection to a J1850 electronic module.

A J1850 link controller feeds the transmit data stream to the transceiver's TX input. The AU5780A transceiver waveshapes the TX data input signal with controlled rise & fall slew rates and rounded shape. The bus output signal is transmitted with both voltage and current control. The BUS_IN input is connected to the physical bus line via an external resistor. The external resistor and an internal capacitance provides filtering against RF bus noise. The incoming signal is output at the RX pin being connected to the J1850 link controller.

If the TX input is idle for a certain time, then the AU5780A enters a low-power mode. This mode is dedicated to help meet ignition-off current draw requirements. The BUS_IN input comparator is kept alive in the low-power mode. Normal power mode will be entered again upon detection of activity, i.e., rising edge at the TX input. The device is able to receive and transmit a valid J1850 message when initially in low-power mode.

The AU5780A features special robustness at its BATT and BUS_OUT pins hence the device is well suited for applications in the automotive environment. Specifically, the BATT input is protected against 50V load dump, jump start and reverse battery condition. The BUS_OUT output is protected against wiring fault conditions, e.g., short circuit to battery voltage as well as typical automotive transients (i.e., –200V / +200V). In addition, an overtemperature shutdown function with hysteresis is incorporated which protects the device under system fault conditions. The chip temperature is sensed at the bus drive transistor in the output buffer. In case of the chip temperature reaching the trip point, the AU5780A will latch-off the transceiver function. The device is reset on the first rising edge on the TX input after a small decrease of the chip temperature.

The AU5780A also provides a loop-back mode for diagnostic purpose. If the /LB pin is open circuit or pulled low, then TX signal is internally looped back to the RX output independent of the signals on the bus. In this mode the electronic module is disconnected from the bus, i.e., the TX signal is not output to the physical bus line. In this mode, it can be used, e.g., for self-test purpose.

The AU5780A is an enhanced successor of the AU5780. The AU5780A provides improved wave shaping when exiting the low power standby mode for reduced EMI. Several parameters that were formerly only characterized to the maximum normal operating supply of 16 volts, have now been characterized to 24 volt supplies. These parameters which are tested and guaranteed to 24 volts are identified with appropriate test conditions in the "conditions" columns of the Characteristics tables, otherwise the conditions at the top of the characteristic table applies to all parameters.

CONTROL INPUT SUMMARY

TX	/LB	MODE	BIT VALUE	BUS_OUT	RX (out)
0	0	Loop-back	TX passive (default state)	float	float (high)
1	0	Loop-back	TX active	float	low
0	1	Communication	Transmitter passive	float	bus state[1]
1	1	Communication	Transmitter active	high	low

NOTE:
1. RX outputs the bus state. If the bus level is below the receiver threshold (i.e., all transmitters passive), then RX will be floating (i.e., high, considering external pull-up resistance). Otherwise, if the bus level is above the receiver threshold (i.e., at least one transmitter is active), then RX will be low.

ABSOLUTE MAXIMUM RATINGS

According to the IEC 134 Absolute Maximum System; operation is not guaranteed under these conditions; all voltages are referenced to pin 8 (GND); positive currents flow into the IC; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{BATT}	supply voltage		–20	+24	V
$V_{BATT.ld}$	short-term supply voltage	load dump; t < 1s		+50	V
$V_{BATT.tr1}$	transient supply voltage	SAE J1113 pulse 1	–100		V
$V_{BATT.tr2}$	transient supply voltage	SAE J1113 pulses 2		+150	V
$V_{BATT.tr3}$	transient supply voltage	SAE J1113 pulses 3A, 3B	–200	+200	V
V_B	Bus voltage	R_f > 10 kΩ ; Rb >10Ω [1]	–20	+20	V
$V_{B.tr1}$	transient bus voltage	SAE J1113 pulse 1	–50		V
$V_{B.tr2}$	transient bus voltage	SAE J1113 pulses 2		+100	V
$V_{B.tr3}$	transient bus voltage	SAE J1113 pulses 3A, 3B	–200	+200	V
V_I	DC voltage on pins TX, R/F, RX, /LB		–0.3	7	V
ESD_{BATT}	ESD capability of BATT pin	Air gap discharge, R=2kΩ, C=150pF	–9	+9	kV
ESD_{bus}	ESD capability of BUS_OUT and BUS_IN pins	Air gap discharge, R=2kΩ, C=150pF, R_f > 10 kΩ	–9	+9	kV
ESD_{logic}	ESD capability of TX, RX, R/F, and /LB pins	Human Body, R=1.5kΩ, C=100pF	–2	+2	kV
P_{tot}	maximum power dissipation	at T_{amb} = +125 °C		164	mW
Θ_{JA}	thermal impedance			152	°C/W
T_{amb}	operating ambient temperature		–40	+125	°C
T_{stg}	storage temperature		–40	+150	°C
T_{vj}	junction temperature		–40	+150	°C
T_{LEAD}	Lead temperature	Soldering, 10 seconds maximum		265	°C
$I_{CL(BUS)}$	Bus output clamp current	No latch-up, $\|V_{BUS}\|$ = 25 V		100	mA
$I_{CL(BATT)}$	Battery clamp current	No latch-up or snap back, $\|V_{BATT}\|$ = 25 V		100	mA

NOTE:
1. For bus voltages –20V < V_{bus} < –17V and +17V < V_{bus} < +20V the current is limited by the external resistors R_b and R_f.

CHARACTERISTICS

$-40°C < T_{amb} < +125°C$; $6V < V_{BATT} < 16V$; $V_{/LB} > 3V$; $0 < V_{BUS} < +8.5V$;
$R_S = 56.2\ k\Omega$ $R_d = 10\ k\Omega$; $R_f = 15\ k\Omega$; $R_b = 10\Omega$; $300\ \Omega < R_L < 1.6\ k\Omega$;
all voltages are referenced to pin 8 (GND); positive currents flow into the IC; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{BATT.id}$	supply current; bus idle	TX low; Note 1			220	µA
$I_{BATT.p}$	supply current; passive state	TX low			1.5	mA
$I_{BATT.oc}$	supply current; no load	TX high			8	mA
$I_{BATT(SB)}$	supply current; bus output short to battery	BUS to V_{BATT}; no I_{BO} current, V_{TX} = high			10	mA
$I_{BATT.sc}$	supply current; bus short to GND	TX high, V_{BO} = 0V			60	mA
T_{sd}	Thermal shutdown		155		170	°C
T_{hys}	Thermal shutdown hysteresis		5		15	°C
$T_{DTYCY24}$	Thermal shutdown, transmit duty cycle, at 24 V	Bus load, R_{LOAD} = 300 Ω, C_{LOAD} = 16.55 nF, V_{BATT} = 24 V, T = 128 µs	33			%
$T_{DTYCY20}$	Thermal shutdown, transmit duty cycle, at 20 V	Bus load, R_{LOAD} = 300 Ω, C_{LOAD} = 16.55 nF, V_{BATT} = 20 V, T = 128 µs	45			%
Pins TX and /LB						
V_{ih}	High level input voltage	$6\ V < V_{BATT} < 24\ V$	3			V
V_{ILTX}	Low level input voltage, TX pin	$6\ V < V_{BATT} < 24\ V$			0.9	V
V_{ilB}	Low level input voltage, LB pin	$6V < V_{BATT} < 24\ V$			0.8	V
V_h	Input hysteresis		0.4			V
C_{TX}	TX input capacitance	Intrinsic to part			5	pf
I_{ih2}	TX high level input current	V_i = 5V	12		50	µA
I_{ih6}	/LB high level input current	V_i = 5V	4		10	µA
Pin RX						
V_{ol}	Low level output voltage	I_o = 1.6 mA			0.4	V
I_{ih}	High level output leakage	V_o = 5V, BUS_IN = low	–10		+10	µA
I_{rx}	RX output current	V_o = 5V	4		20	mA
Pin BUS_OUT						
V_{olb}	BUS_OUT in loop-back mode; TX high or low	/LB low or floating; $0 < V_{BATT} < 24V$; R_L=1.6kΩ			0.1	V
V_{ol}	BUS_OUT voltage; passive	TX low or floating; $0 < V_{BATT} < 24V$; R_L=1.6kΩ			0.075	V
V_{oh}	BUS_OUT voltage; active	TX high; Note 2 $9V < V_{BATT} < 24V$; $300\Omega < R_L < 1.6k\Omega$;	7.3		8	V
V_{ohLOWB}	BUS_OUT voltage; low battery	TX high; $6V < V_{BATT} < 9V$; $300\Omega < R_L < 1.6k\Omega$; Note 2	$V_{BATT} - 1.7$		8	V
$-I_{BO.LIM}$	BUS_OUT source current; bus positive	TX high; $9V < V_{BATT} < 24V$ $0V < V_{bus} < +6.0V$	27		50	mA
$-I_{BO.LIMn}$	BUS_OUT source current; bus negative	TX high; $9V < V_{BATT} < 24V$ $-17V < V_{bus} < 0V$	28		55	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-I_{BO.LK.HO}$	BUS_OUT leakage current; TX high; bus low or operational	$-17 < V_{BUS} < 8.5$ V; TX = high; $0 V < V_{BATT} < 24$ V	–10		$I_{BO.LIM}$	µA
$-I_{BO.LK.HH}$	BUS_OUT leakage current; TX high; bus positive	$8.5 V < V_{BUS} < 17$ V; TX = high; $0 V < V_{BATT} < 24$ V	–10		10	µA
$-I_{BO.LK}$	BUS_OUT leakage current; TX low; bus positive	TX low; $0V<V_{BATT}<24V$; $0.1V< V_{bus} <+17V$	–10		+10	µA
$-I_{BO.N}$	BUS_OUT leakage current; TX low; bus negative	TX low; $0.1V<V_{BATT}<24V$; $-17V< V_{bus} < 0V$	–10		+100	µA
$-I_{BO.LOG}$	BUS_OUT leakage current with loss of ground	$-17 V < V_{BUS} < 17$ V; $0 V <V_{BATT} < 1$ V	–10		100	µA
C_{BUSOUT}	Bus output capacitance				20	pF
Pin BUS_IN						
V_{ih}	Input high voltage		4.1			V
V_{il}	Input low voltage				3.65	V
V_h	Input hysteresis		100			mV
I_{BIN}	Input bias current	$-17V < V_{bus} < +17V$	–5		+5	µA
$I_{BIN(MAX)}$	BUS_IN input current maximum with and without loss of ground	$-17 < V_{BUS} < 17$ V; $0 V < V_{BATT} < 24$ V; VTX high or low	–100		100	µA
C_{BUSIN},	Bus input capacitance		10		20	pF
T_{DRXON}, t_{DRXOFF}	Bus line to RX propagation delay, normal and 4X modes	Measured at V_{BUSIN_HIGH} or V_{BUSIN_LOW} to $\overline{RX}$; $6 < V_{BATT} < 24$ V; of $R_{LOAD} = 10$ KΩ to 5 V	0.4		1.7	µs

DYNAMIC CHARACTERISTICS

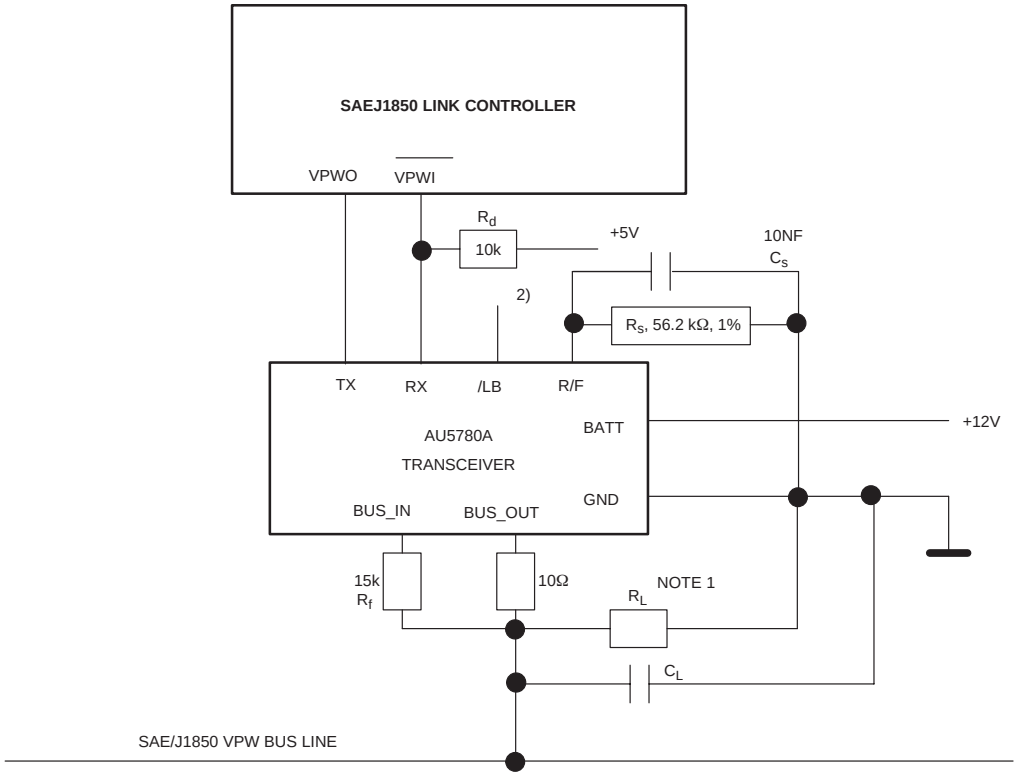
$-40°C < T_{amb} < +125°C$; $9V < V_{BATT} < 16V$; $V_{/LB} > 3V$; $0V < V_{BUS} < +8.5V$;
$R_S = 56.2\ k\Omega$; $R_d = 10\ k\Omega$; $R_f = 15\ k\Omega$; $R_b = 10\Omega$; BUS_OUT: $300\Omega < R_L < 1.6\ k\Omega$;
$1.7\ \mu s < (R_L * C_L) < 5.2\ \mu s$; $2.2\ nF < C_L < 16.55\ nF$; R_X: $C_L < 40pF$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins TX, RX, /LB						
t_{pl}	Delay TX to RX rising and falling edge in loop-back mode	/LB low $6\ V < V_{BATT} < 24\ V$	15		24	µs
t_{dlb}	Delay /LB to BUS_OUT	TX high, toggle /LB	1		10	µs
Pin BUS_OUT						
t_{bo}	Delay TX to BUS_OUT, normal battery	Measured at 3.875V, Note 3	13		21	µs
t_{bo_hibatt}	Delay TX to BUS_OUT, high battery	Measured at 3.875V, $16V < V_{BATT} < 24V$, Note 3	13		21	µs
t_{bo_lobatt}	Delay TX to BUS_OUT, low battery	Measured at 3.875V, $6V < V_{BATT} < 9V$, Note 3	13		22	µs
t_r, t_f	BUS_OUT transition times, rise and fall, normal battery	Measured between 1.5 V and (V_{BATT} – 2.75 V), $9 < V_{BATT} < 16\ V$, t_r tested at an additional bus load of $R_{LOAD} = 400\ \Omega$ and $C_{LOAD} = 22000\ pF$	11		18	µs
t_{r_hibatt}, t_{f_hibatt}	BUS_OUT transition times, rise and fall, high battery	Measured between 1.5 V and 6.25 V, $16 < V_{BATT} < 24\ V$, t_r tested at an additional bus load of $R_{LOAD} = 400\ \Omega$ and $C_{LOAD} = 22000\ pF$	11		18	µs
t_{r_lobatt}, t_{f_lobatt}	BUS_OUT transition times, rise and fall, low battery	Measured between 1.5 V and 6.25 V, $6 < V_{BATT} < 9\ V$, t_r tested at an additional bus load of $R_{LOAD} = 400\ \Omega$ and $C_{LOAD} = 22000\ pF$	(V_{BATT} – 4.25) / 0.43		(V_{BATT} – 4.25) / 0.264	µs
I_{sr}	Bus output current slew rate	$6V < V_{BATT} < 16V$; $R_S = 56.2\ k\Omega$ $R_L = 100\Omega$; measured at 30% and 70% of waveform, DC offset 0 to –2V	0.90		2.4	mA/µs
V_{dB_limit}	Bus emissions voltage output	$0\ V < DC_offset < 1\ V$, $9\ V < V_{BATT} < 24\ V$, $R_L = 500\ \Omega$, $C_L = 6\ nF$			–50	dBV
$V_{dB_limit-1}$	Bus emissions voltage output, negative bus offset	$-1\ V < DC_offset < 0\ V$, $9\ V < V_{BATT} < 24\ V$, $R_L = 500\ \Omega$, $C_L = 6\ nF$			–50	dBV
N_R	Bus noise rejection from battery	$30\ Hz < f < 250kHz$	20			dB
N_I	Bus noise isolation from battery	$250\ kHz < f < 200\ MHz$	17			dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pin BUS_IN						
C_{BIN}	Bus Input capacitance		10		20	pF
T_{DRXON}; t_{DRXOFF}	Bus line to RX propagation delay, normal and 4x modes	Measured at V_{BUSIN_HIGH} or V_{BUSIN_LOW} to RX; $6 < V_{BATT} < 24$ V; of R_{LOAD} = 10 kΩ to 5V	0.4		1.7	µs
T_{DRX_Δ}	Bus line to RX propagation delay mismatch, normal and 4x modes	$t_{DRXOFF} - t_{DRXON}$	–1.3		+1.3	µs
Pin BATT						
t_{low_power}	time-out to low power state	TX low	1		4	ms

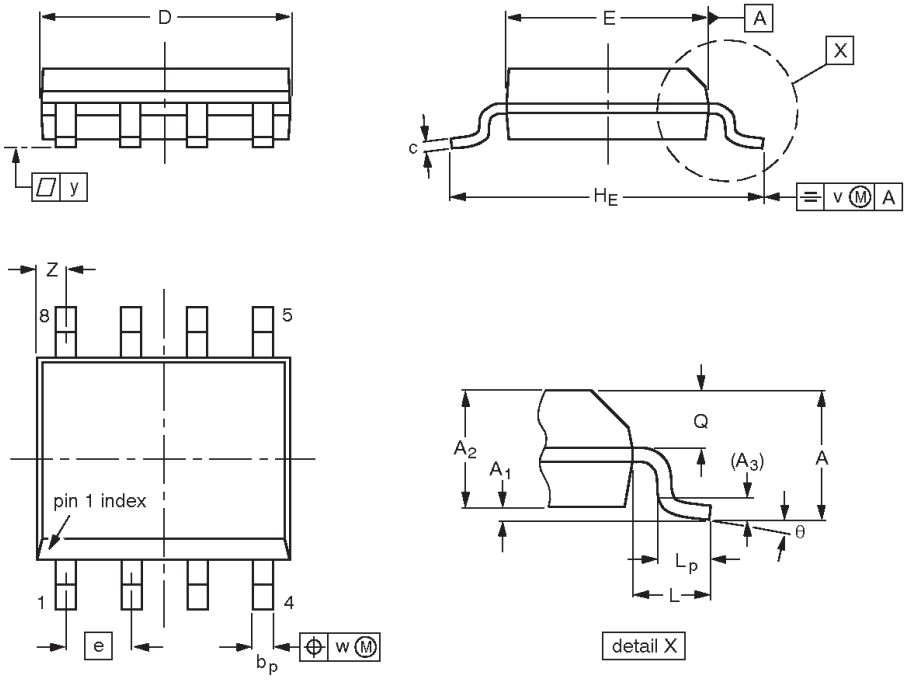
NOTES;
1. TX < 0.9V for more than 4 ms
2. For $6V < V_{BATT} < 9V$ the bus output voltage is limited by the supply voltage. For $16V < V_{BATT} < 24V$ (jump start) the load is limited by the package power dissipation ratings; the duration of this condition is recommended to be less than 90 seconds.
3. Tested with a bus load of R_{LOAD} = 400 Ω and C_{LOAD} = 22,000 pF.

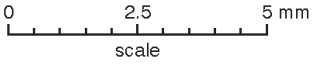
APPLICATION INFORMATION



NOTES:
1. Value depends, e.g., on type of bus node. Example: primary node R_L=1.5kΩ , secondary node R_L=10.7kΩ.
2. For connection of /LB there are different options, e.g., connect to V_{CC} or to low-active reset or to a port pin.
3. The value of C_L is suggested to be in the range 330 pF < C_L < 470 pF.

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				~~97-05-22~~ 99-12-27

Data sheet status

Data sheet status [1]	Product status [2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued datasheet before initiating or completing a design.
[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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