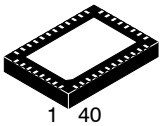
AX8052F151

SoC Ultra-Low Power RF-Microcontroller for the 400 - 470 MHz and 800 - 940 MHz Bands

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QFN40 7x5, 0.5P
CASE 485EG

ORDERING INFORMATION

Device	Type	Qty
AX8052F151−2−TB05	Tape & Reel	500
AX8052F151−2−TX30	Tape & Reel	3,000

OVERVIEW

The AX8052F151 is a single chip ultra−low−power RF−microcontroller SoC primarily for use in SRD bands. The on−chip transceiver consists of a fully integrated RF front−end with modulator, and demodulator. Base band data processing is implemented in an advanced and flexible communication controller that enables user friendly communication.

Features

SoC Ultra−low Power RF−microcontroller for Wireless Communication Applications

- QFN40 Package
- Supply Range 2.2 V − 3.6 V (1.8 V MCU)
- −40°C to 85°C
- Ultra−low Power Consumption:
  - CPU Active Mode 150 μA/MHz
  - Sleep Mode with 256 Byte RAM Retention and Wake−up Timer running 900 nA
  - Sleep Mode 4 kByte RAM Retention and Wake−up Timer running 1.9 μA
  - Sleep Mode 8 kByte RAM Retention and Wake−up Timer running 2.6 μA
  - Radio RX−mode in Low Power Mode 17 mA
  - Radio TX−mode 22 mA at 10 dBm Output Power
  - Wake−on−Radio Mode 100 kbps, 1 s Duty Cycle 6 μA

AX8052 Features

- Ultra−low Power MCU Core Compatible with Industry Standard 8052 Instruction Set
- Down to 500 nA Wake−up Current
- Single Cycle/Instruction for many Instructions
- 64 kByte In−system Programmable FLASH
- Code Protection Lock
- 8.25 kByte SRAM
- 3−wire (1 dedicated, 2 shared) In−circuit Debug Interface
- Three 16−bit Timers with ΣΔ Output Capability
- Two 16−bit Wakeup Timers
- Two Input Captures
- Two Output Compares with PWM Capability
- 10−bit 500 ksample/s Analog−to−Digital Converter
- Temperature Sensor
- Two Analog Comparators
- Two UARTs
- One General Purpose Master/Slave SPI
- Two Channel DMA Controller
- Multi−megabit/s AES Encryption/Decryption Engine, supports AES−128, AES−192 and AES−256 with True Random Number Generator (TRNG)
  NOTE: The AES Engine and the TRNG require Software Enabling and Support.
- Ultra−low Power 10 kHz/640 Hz Wakeup Oscillator, with Automatic Calibration against a Precise Clock
- Internal 20 MHz RC Oscillator, with Automatic Calibration against a Precise Clock for Flexible System Clocking
- Low Frequency Tuning Fork Crystal Oscillator for Accurate Low Power Time Keeping
- Brown−out and Power−on−Reset Detection

High−performance RF Transceiver compatible to AX5051

- 400 − 470 MHz and 800 − 940 MHz SRD Bands
- Wide Variety of Shaped Modulations Supported (ASK, PSK, MSK, FSK)
- Flexible Shaping for the Modulations
- Data Rates from 1 to 350 kbps (FSK, MSK) and 1 to 600 kbps ASK, 10 to 600 kbps PSK

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- Fully Integrated RF Frequency Synthesizer with Ultra−fast Settling Time for Low−power Consumption
- RF Carrier Frequency and FSK Deviation Programmable in 1Hz Steps
- Variable Channel Filtering from 40 kHz to 600 kHz
- 802.15.4 Compatible
- Few External Components
- Channel Hopping up to 2000 hops/s
- Sensitivity down to −116 dBm at 1.2 kbps
- Up to +16 dBm at 433 MHz Programmable Transmitter Power Amplifier for Long Range Operation
- Crystal Oscillator with Programmable Transconductance and Programmable Internal Tuning Capacitors for Low Cost Crystals
- Digital RSSI
- Automatic Frequency Control (AFC)
- Integrated RX/TX Switching
- Differential Antenna Pins
- Support of Synchronous and Asynchronous Communication Systems

Applications

400 − 470 MHz and 800 − 940 MHz Data Transmission and Reception in the Short Range Devices (SRD) Band

- Suited for Systems targeting Compliance to EN 300 220 V2.3.1 and FCC CFR Part 15
- Suited for Systems targeting Compliance with Wireless M−Bus Standard EN 13757−4:2005
- 802.15.4 Compatible
- Telemetric Applications, Sensor Readout
- Toys
- Wireless Audio
- Automatic Meter Reading
- Wireless Networks
- Access Control
- Remote Keyless Entry
- Garage Door Openers
- Home Automation
- Pointing Devices and Keyboards
- Active RFID

BLOCK DIAGRAM

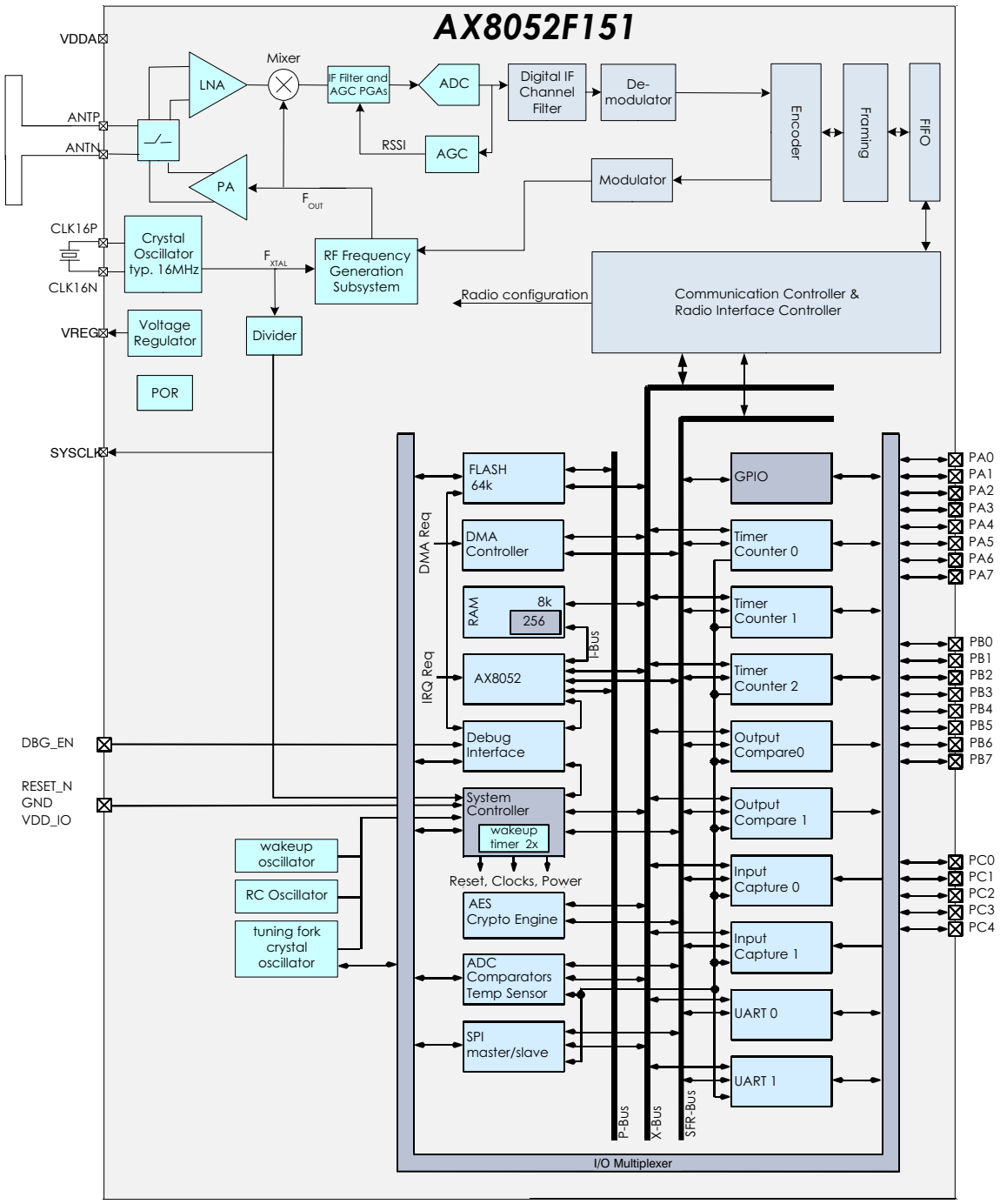


Figure 1. Functional Block Diagram of the AX8052F151

Table 1. PIN FUNCTION DESCRIPTIONS

Symbol	Pin(s)	Type	Description
GND	1	P	Ground
GND	2	P	Ground
VDDA	3	P	Power supply, must be supplied with regulated voltage VREG
GND	4	P	Ground
ANTP	5	A	Antenna input/output
ANTN	6	A	Antenna input/output
GND	7	P	Ground
VDDA	8	P	Power supply, must be supplied with regulated voltage VREG
TST1	9	I	Connected to GND
TST	10	I	Connected to GND
VDD_IO	11	P	Unregulated power supply (battery input)
SYSCLK	12	I/O/PU	System Clock Output
PC4	13	I/O/PU	General Purpose IO
PC3	14	I/O/PU	General Purpose IO
PC2	15	I/O/PU	General Purpose IO
PC1	16	I/O/PU	General Purpose IO
PC0	17	I/O/PU	General Purpose IO
PB0	18	I/O/PU	General Purpose IO
PB1	19	I/O/PU	General Purpose IO
PB2	20	I/O/PU	General Purpose IO
PB3	21	I/O/PU	General Purpose IO
PB4	22	I/O/PU	General Purpose IO
PB5	23	I/O/PU	General Purpose IO
PB6	24	I/O/PU	General Purpose IO, DBG_DATA
PB7	25	I/O/PU	General Purpose IO, DBG_CLK
DBG_EN	26	I/PD	In−Circuit Debugger Enable
RESET_N	27	I/PU	Optional reset pin If this pin is not used it must be connected to VDD_IO
GND	28	P	Ground
VDD_IO	29	P	Unregulated power supply (battery input)
PA0	30	I/O/A/PU	General Purpose IO
PA1	31	I/O/A/PU	General Purpose IO
PA2	32	I/O/A/PU	General Purpose IO
PA3	33	I/O/A/PU	General Purpose IO
PA4	34	I/O/A/PU	General Purpose IO
PA5	35	I/O/A/PU	General Purpose IO
PA6	36	I/O/A/PU	General Purpose IO
PA7	37	I/O/A/PU	General Purpose IO
VREG	38	P	Regulated output voltage VDDA pins must be connected to this supply voltage A 1 μF low ESR capacitor to GND must be connected to this pin
CLK16P	39	A	Crystal oscillator input/output (RF reference)

Table 1. PIN FUNCTION DESCRIPTIONS

Symbol	Pin(s)	Type	Description
CLK16N	40	A	Crystal oscillator input/output (RF reference)
GND	Center pad	P	Ground on center pad of QFN, must be connected

A = analog input
I = digital input signal
O = digital output signal
PU = pull−up
I/O = digital input/output signal
N = not to be connected
P = power or ground
PD = pull−down

All digital inputs are Schmitt trigger inputs, digital input and output levels are LVCMOS/LVTTL compatible. Port A Pins (PA0 − PA7) must not be driven above VDD_IO, all other digital inputs are 5 V tolerant. Pull−ups are programmable for all GPIO pins.

Alternate Pin Functions

GPIO Pins are shared with dedicated Input/Output signals of on−chip peripherals. The following table lists the available functions on each GPIO pin.

Table 2. ALTERNATE PIN FUNCTIONS

GPIO	Alternate Functions			
PA0	T0OUT	IC1	ADC0	
PA1	T0CLK	OC1	ADC1	
PA2	OC0	U1RX	ADC2	COMPI00
PA3	T1OUT		ADC3	LPXTALP
PA4	T1CLK	COMPO0	ADC4	LPXTALN
PA5	IC0	U1TX	ADC5	COMPI10
PA6	T2OUT	ADCTRIG	ADC6	COMPI01
PA7	T2CLK	COMPO1	ADC7	COMPI11
PB0	U1TX	IC1	EXTIRQ0	
PB1	U1RX	OC1		
PB2	IC0	T2OUT		
PB3	OC0	T2CLK	EXTIRQ1	DSWAKE
PB4	U0TX	T1CLK		
PB5	U0RX	T1OUT		
PB6	DBG_DATA			
PB7	DBG_CLK			
PC0	SSEL	T0OUT	EXTIRQ0	
PC1	SSCK	T0CLK	COMPO1	
PC2	SMOSI	U0TX		
PC3	SMISO	U0RX	COMPO0	
PC4	COMPO1	ADCTRIG	EXTIRQ1	

Pinout Drawing

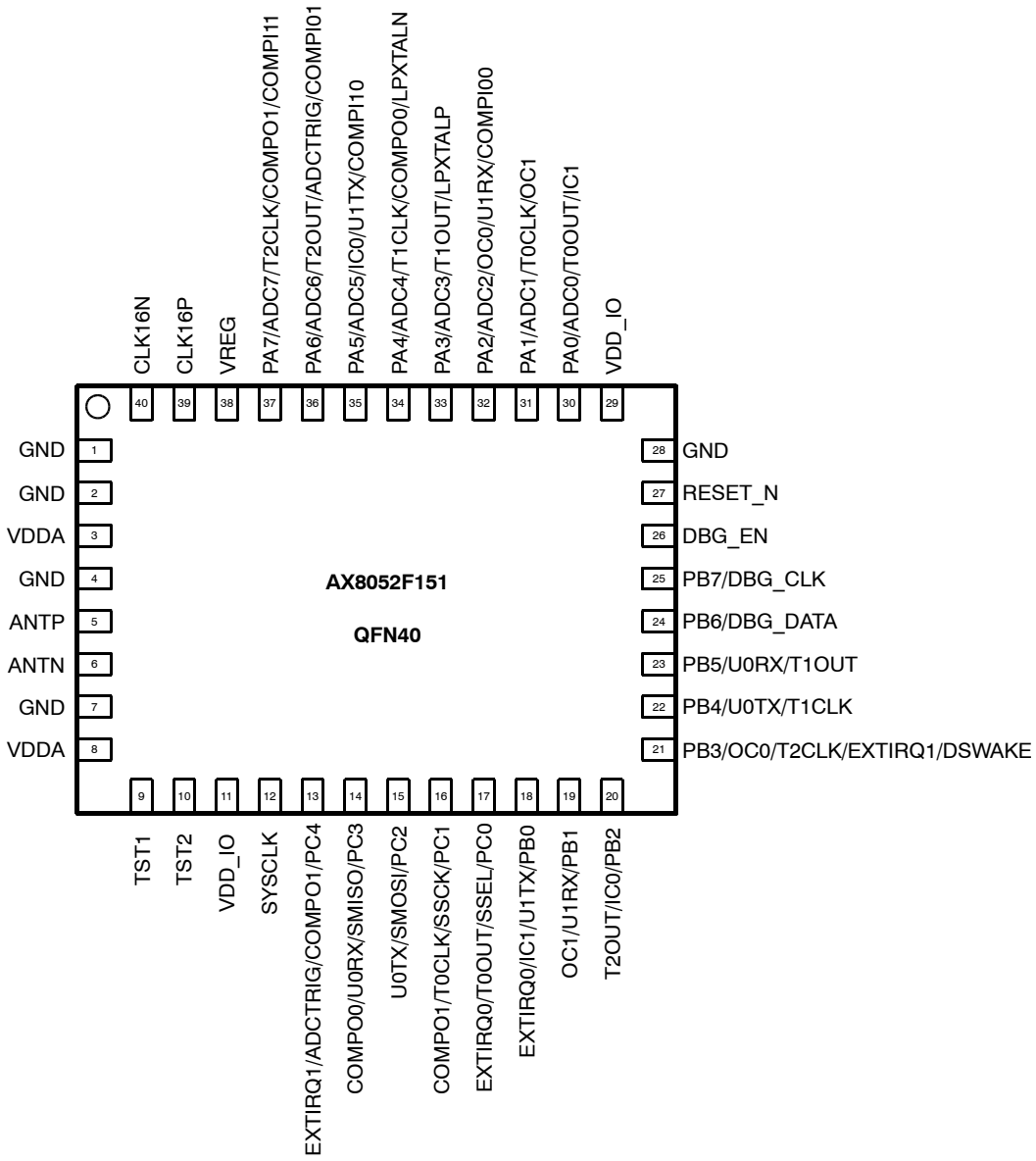


Figure 2. Pinout Drawing (Top View)

SPECIFICATIONS

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Condition	Min	Max	Units
VDD_IO	Supply voltage		−0.5	5.5	V
IDD	Supply current			100	mA
P_{tot}	Total power consumption			800	mW
P_i	Absolute maximum input power at receiver input			15	dBm
I_{I1}	DC current into any pin except ANTP, ANTN		−10	10	mA
I_{I2}	DC current into pins ANTP, ANTN		−100	100	mA
I_O	Output Current			40	mA
V_{ia}	Input voltage ANTP, ANTN pins		−0.5	5.5	V
	Input voltage digital pins		−0.5	5.5	V
V_{es}	Electrostatic handling	HBM	−2000	2000	V
T_{amb}	Operating temperature		−40	85	°C
T_{stg}	Storage temperature		−65	150	°C
T_j	Junction Temperature			150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Table 4. SUPPLIES

Symbol	Description	Condition	Min	Typ	Max	Units
T_{AMB}	Operational ambient temperature		−40	27	85	°C
VDD_IO	I/O and voltage regulator supply voltage	RX operation or TX operation up to 4 dBm output power	2.2	3.0	3.6	V
		TX operation up to 16 dBm output power	2.4	3.0	3.6	
		Transceiver switched off	1.8	3.0	3.6	
VDD_{IO_R1}	I/O voltage ramp for reset activation; Note 1	Ramp starts at VDD_IO ≤ 0.1 V	0.1			V/ms
VDD_{IO_R2}	I/O voltage ramp for reset activation; Note 1	Ramp starts at 0.1 V < VDD_IO < 0.7 V	3.3			V/ms
VREG	Internally regulated analog supply voltage	Power−down mode AX5051_PWRMODE = 0x00		1.7		V
		All other power modes	2.1	2.5	2.8	V
$I_{DEEPSLEEP}$	Deep Sleep current			500		nA
$I_{SLEEP256PIN}$	Sleep current, 256 Bytes RAM retained	Wakeup from dedicated pin		900		nA
$I_{SLEEP256}$	Sleep current, 256 Bytes RAM retained	Wakeup Timer running at 640 Hz		1.3		μA
$I_{SLEEP4K}$	Sleep current, 4.25 kBytes RAM retained	Wakeup Timer running at 640 Hz		1.9		μA
$I_{SLEEP8K}$	Sleep current, 8.25 kBytes RAM retained	Wakeup Timer running at 640 Hz		2.6		μA
I_{RX-HS}	Current consumption RX; High sensitivity mode: VCO_I = 001; REF_I = 011	Bit rate 10 kbit/s		19		mA
I_{RX-LP}	Current consumption RX; Low power mode: VCO_I = 001; REF_I = 101	Bit rate 10 kbit/s		17		mA

1. If VDD_IO ramps cannot be guaranteed, an external reset circuit is recommended, see the AX8052 Application Note: Power On Reset.
2. The PA voltage is regulated to 2.5 V. For VDD_IO levels in the range of 2.2 V to 2.5 V the output power drops by typically 1 dBm.

Table 4. SUPPLIES

Symbol	Description	Condition	Min	Typ	Max	Units
I_{TX}	Current consumption TX VCO_I = 001; REF_I = 011; LOCURST= 1 Note 2	868 MHz, 10 dBm		22		mA
		868 MHz, 0 dBm		13		
		868 MHz, 15 dBm		45		
		433 MHz, 10 dBm		22		
		433 MHz, 0 dBm		13		
		433 MHz, 15 dBm		45		
TX_{varvdd}	Variation of output power over voltage	VDD_IO > 2.5 V, Note 2		±0.5		dB
$TX_{vartemp}$	Variation of output power over temperature	VDD_IO > 2.5 V, Note 2		±0.5		dB
I_{MCU}	Microcontroller running power consumption	All peripherals disabled		150		µA/ MHz
I_{VSUP}	Voltage supervisor	Run and standby mode		85		µA
$I_{XTALOSC}$	Crystal oscillator current (RF reference oscillator)	16 MHz		160		µA
$I_{LFXTALOSC}$	Low frequency crystal oscillator current	32 kHz		700		nA
I_{RCOSC}	Internal oscillator current	20 MHz		210		µA
I_{LPOSC}	Internal Low Power Oscillator current	10 kHz		650		nA
		640 Hz		210		nA
I_{ADC}	ADC current	311 kSample/s, DMA 5 MHz		1.1		mA
I_{WOR}	Typical wake−on−radio duty cycle current	1 s, 100 kbps		6		µA

1. If VDD_IO ramps cannot be guaranteed, an external reset circuit is recommended, see the AX8052 Application Note: Power On Reset.
2. The PA voltage is regulated to 2.5 V. For VDD_IO levels in the range of 2.2 V to 2.5 V the output power drops by typically 1 dBm.

Note on current consumption in TX mode

To achieve best output power the matching network has to be optimized for the desired output power and frequency. As a rule of thumb a good matching network produces about 50% efficiency with the AX8052F151 power amplifier although over 90% are theoretically possible. A typical matching network has between 1 dB and 2 dB loss (P_{loss}).

The current consumption can be calculated as

$$I_{TX}[mA] = \frac{1}{PA_{efficiency}} \times 10^{\frac{P_{out}[dBm] + P_{loss}[dB]}{10}} \div 2.5V + I_{offset}$$

I_{offset} is about 12 mA for the VCO at 400 – 470 MHz and 11 mA for 800 – 940 MHz. The following table shows calculated current consumptions versus output power for P_{loss} = 1 dB, $PA_{efficiency}$ = 0.5 and I_{offset} = 11 mA at 868 MHz.

Table 5.

Pout [dBm]	I [mA]
0	13.0
1	13.2
2	13.6
3	14.0
4	14.5
5	15.1
6	16.0
7	17.0
8	18.3
9	20.0
10	22.0
11	24.6
12	27.96
13	32.1
14	37.3
15	43.8

The AX8052F151 power amplifier runs from the regulated VDD supply and not directly from the battery. This has the advantage that the current and output power do not vary much over supply voltage and temperature from 2.55 V to 3.6 V supply voltage. Between 2.55 V and 2.2 V a drop of about 1 dB in output power occurs.

Table 6. LOGIC

Symbol	Description	Condition	Min	Typ	Max	Units
Digital Inputs						
V_{T+}	Schmitt trigger low to high threshold point	VDD_IO = 3.3 V		1.55		V
V_{T-}	Schmitt trigger high to low threshold point			1.25		V
V_{IL}	Input voltage, low				0.8	V
V_{IH}	Input voltage, high		2.0			V
V_{IPA}	Input voltage range, Port A		−0.5		VDD_IO	V
V_{IPBC}	Input voltage range, Ports B, C		−0.5		5.5	V
I_L	Input leakage current		−10		10	μA
R_{PU}	Programmable Pull−Up Resistance			65		kΩ
Digital Outputs						
I_{OH}	P[ABC]x Output Current, high	V_{OH} = 2.4 V	8			mA
I_{OL}	P[ABC]x Output Current, low	V_{OL} = 0.4 V	8			mA
I_{OH}	SYSCLK Output Current, high	V_{OH} = 2.4 V	8			mA
I_{OL}	SYSCLK Output Current, low	V_{OL} = 0.4 V	8			mA
I_{OZ}	Tri−state output leakage current		−10		10	μA

AC Characteristics

Table 7. CRYSTAL OSCILLATOR (RF REFERENCE OSCILLATOR)

Symbol	Description	Condition	Min	Typ	Max	Units
f_{XTAL}	Crystal frequency	Notes 1, 3	15.5	16	25	MHz
gm_{osc}	Transconductance oscillator	AX5051_XTALOSCGM = 0000		1		mS
		AX5051_XTALOSCGM = 0001		2		
		AX5051_XTALOSCGM = 0010 default		3		
		AX5051_XTALOSCGM = 0011		4		
		AX5051_XTALOSCGM = 0100		5		
		AX5051_XTALOSCGM = 0101		6		
		AX5051_XTALOSCGM = 0110		6.5		
		AX5051_XTALOSCGM = 0111		7		
		AX5051_XTALOSCGM = 1000		7.5		
		AX5051_XTALOSCGM = 1001		8		
		AX5051_XTALOSCGM = 1010		8.5		
		AX5051_XTALOSCGM = 1011		9		
		AX5051_XTALOSCGM = 1100		9.5		
		AX5051_XTALOSCGM = 1101		10		
		AX5051_XTALOSCGM = 1110		10.5		
		AX5051_XTALOSCGM = 1111		11		
C_{osc}	Programmable tuning capacitors at pins CLK16N and CLK16P	AX5051_XTALCAP = 000000 default		2		pF
		AX5051_XTALCAP = 111111		33		
$C_{osc-lsb}$	Programmable tuning capacitors, increment per LSB of AX5051_XTALCAP			0.5		pF
f_{ext}	External clock input (TCXO)	Notes 2, 3	15.5	15	25	MHz
RIN_{osc}	Input DC impedance		10			kΩ

1. Tolerances and start−up times depend on the crystal used. Depending on the RF frequency and channel spacing the IC must be calibrated to the exact crystal frequency using the readings of the register AX5051_TRKFREQ.
2. If an external clock is used, it should be input via an AC coupling at pin CLK16P with the oscillator powered up and AX5051_XTALCAP = 000000
3. Lower frequencies than 15.5 MHz or higher frequencies than 25 MHz can be used. However, not all typical RF frequencies can then be generated.

Table 8. RF FREQUENCY GENERATION SUBSYSTEM (SYNTHESIZER)

Symbol	Description	Condition	Min	Typ	Max	Units
f_{REF}	Reference frequency	Note 1		16 24		MHz
f_{range_hi}	Frequency range	BANDSEL = 0	800		940	MHz
f_{range_low}		BANDSEL = 1	400		470	
f_{RESO}	Frequency resolution		1			Hz
BW_1	Synthesizer loop bandwidth VCO current: VCOI = 001	Loop filter configuration: FLT = 01 Charge pump current: PLLCPI = 010		100		kHz
BW_2		Loop filter configuration: FLT = 01 Charge pump current: PLLCPI = 001		50		
BW_3		Loop filter configuration: FLT = 11 Charge pump current: PLLCPI = 010		200		
BW_4		Loop filter configuration: FLT = 10 Charge pump current: PLLCPI = 010		500		
T_{set1}	Synthesizer settling time for 1 MHz step as typically required for RX/TX switching VCO current: VCO_I = 001	Loop filter configuration: FLT = 01 Charge pump current: PLLCPI = 010		15		μs
T_{set2}		Loop filter configuration: FLT = 01 Charge pump current: PLLCPI = 001		30		
T_{set3}		Loop filter configuration: FLT = 11 Charge pump current: PLLCPI = 010		7		
T_{set4}		Loop filter configuration: FLT = 10 Charge pump current: PLLCPI = 010		3		
T_{start1}	Synthesizer start−up time if crystal oscillator and reference are running VCO current: VCO_I = 001	Loop filter configuration: FLT = 01 Charge pump current: PLLCPI = 010		25		μs
T_{start2}		Loop filter configuration: FLT = 01 Charge pump current: PLLCPI = 001		50		
T_{start3}		Loop filter configuration: FLT = 11 Charge pump current: PLLCPI = 010		12		
T_{start4}		Loop filter configuration: FLT = 10 Charge pump current: PLLCPI = 010		5		
$PN868_1$	Synthesizer phase noise Loop filter configuration: FLT = 01 Charge pump current: PLLCPI = 010 VCO current: VCO_I = 001	868 MHz, 50 kHz from carrier		−85		dBc/Hz
		868 MHz, 100 kHz from carrier		−90		
		868 MHz, 300 kHz from carrier		−100		
		868 MHz, 2 MHz from carrier		−110		
$PN433_1$		433 MHz, 50 kHz from carrier		−90		
		433 MHz, 100 kHz from carrier		−95		
		433 MHz, 300 kHz from carrier		−105		
		433 MHz, 2 MHz from carrier		−115		
$PN868_2$	Synthesizer phase noise Loop filter configuration: FLT = 01 Charge pump current: PLLCPI = 001 VCO current: VCO_I = 001	868 MHz, 50 kHz from carrier		−80		dBc/Hz
		868 MHz, 100 kHz from carrier		−90		
		868 MHz, 300 kHz from carrier		−105		
		868 MHz, 2 MHz from carrier		−115		
$PN433_2$		433 MHz, 50 kHz from carrier		−90		
		433 MHz, 100 kHz from carrier		−95		
		433 MHz, 300 kHz from carrier		−110		
		433 MHz, 2 MHz from carrier		−122		

1. ASK, PSK and 1−200 kbps FSK with 16 MHz crystal, 200−350 kbps FSK with 24 MHz crystal.

Table 9. TRANSMITTER

Symbol	Description	Condition	Min	Typ	Max	Units
SBR	Signal bit rate	ASK	1		600	kbps
		PSK	10		600	
		FSK, (Note 2)	1		350	
		802.15.4 (DSSS) ASK and PSK	1		40	
		802.15.4 (DSSS) FSK	1		16	
PTX_{868}	Transmitter power @ 868 MHz	TXRNG = 1111 LOCURST = 1		15		dBm
PTX_{433}	Transmitter power @ 433 MHz	TXRNG = 1111 LOCURST = 1		16		dBm
$PTX_{868-harm2}$	Emission @ 2nd harmonic	(Note 1)		−50		dBc
$PTX_{868-harm3}$	Emission @ 3rd harmonic			−55		

1. Additional low−pass filtering was applied to the antenna interface, see applications section.
2. 1 − 200 kbps with a 16 MHz crystal, 200 − 350 kbps with 24 MHz crystal

Table 10. RECEIVER

	Input Sensitivity in dBm TYP. at SMA Connector for BER = 10^{-3} (433 or 868 MHz)					
Datarate [kbps]	ASK	FSK h = 1	FSK h = 4	FSK h = 8	FSK h = 16	PSK
1.2				−115	−116	
2				−115	−115	
10	−103			−109		−110
100	−97	−103	−98			−104
200	−94	−100				−100
600	−90					−98

Table 11.

Symbol	Description	Condition	Min	Typ	Max	Units
SBR	Signal bit rate	ASK	1		600	kbps
		PSK	10		600	
		FSK	1		350	
		802.15.4 (DSSS) ASK and PSK	1		40	
		802.15.4 (DSSS) FSK	1		16	
IL	Maximum input level				−20	dBm
CP_{1dB}	Input referred compression point	2 tones separated by 100 kHz		−35		dBm
IIP3	Input referred IP3			−25		
RSSIR	RSSI control range			85		dB
$RSSIS_1$	RSSI step size	Before digital channel filter; calculated from register AX5051_AGCCOUNTER		0.625		dB
$RSSIS_2$	RSSI step size	Behind digital channel filter; calculated from registers AX5051_AGCCOUNTER, AX5051_TRKAMPL		0.1		dB
SEL_{868}	Adjacent channel suppression	FSK 50 kbps, (Notes 1 & 2)		18		dB
	Alternate channel suppression			19		
	Adjacent channel suppression	FSK 100 kbps, (Notes 1 & 3)		16		dB
	Alternate channel suppression			30		
	Adjacent channel suppression	PSK 200 kbps, (Notes 1 & 4)		17		dB
	Alternate channel suppression			28		
BLK_{868}	Blocking at ± 1 MHz offset	FSK 100 kbps, (Note 5)		38		dB
	Blocking at − 2 MHz offset			40		
	Blocking at ± 10 MHz offset			60		
	Blocking at ± 100 MHz offset			82		
$IMRR_{868}$	Image rejection			30		

1. Interferer/Channel @ BER = 10^{-3}, channel level is +10 dB above the typical sensitivity, the interfering signal is a random data signal (except PSK200); both channel and interferer are modulated without shaping
2. FSK 50 kbps: 868 MHz, 200 kHz channel spacing, 25 kHz deviation, programming as recommended in Programming Manual
3. FSK 100 kbps: 868 MHz, 400 kHz channel spacing, 50 kHz deviation , programming as recommended in Programming Manual
4. PSK 200 kbps: 868 MHz, 400 kHz channel spacing, programming as recommended in AX5051 Programming Manual, interfering signal is a constant wave
5. Channel/Blocker @ BER = 10^{-3}, channel level is +10 dB above the typical sensitivity, the blocker signal is a constant wave; channel signal is modulated without shaping, the image frequency lies 2 MHz above the wanted signal

Table 12. LOW FREQUENCY CRYSTAL OSCILLATOR

Symbol	Description	Condition	Min	Typ	Max	Units
f_{LPXTAL}	Crystal frequency			32	150	kHz
gm_{lpxosc}	Transconductance oscillator	LPXOSCGM = 00110		3.5		μs
		LPXOSCGM = 01000		4.6		
		LPXOSCGM = 01100		6.9		
		LPXOSCGM = 10000		9.1		
RIN_{lpxosc}	Input DC impedance		10			MΩ

Table 13. INTERNAL LOW POWER OSCILLATOR

Symbol	Description	Condition	Min	Typ	Max	Units
f_{LPOSC}	Oscillation Frequency	LPOSCFAST = 0 Factory calibration applied. Over the full voltage and temperature range	630	640	650	Hz
		LPOSCFAST = 1 Factory calibration applied. Over the full voltage and temperature range	10.08	10.24	10.39	kHz

Table 14. INTERNAL RC OSCILLATOR

Symbol	Description	Condition	Min	Typ	Max	Units
f_{FRCOSC}	Oscillation Frequency	Factory calibration applied. Over the full temperature and voltage range	19.8	20	20.2	MHz

Table 15. MICROCONTROLLER

Symbol	Description	Condition	Min	Typ	Max	Units
$T_{SYSCLKL}$	SYSCLK Low		27			ns
$T_{SYSCLKH}$	SYSCLK High		21			ns
$T_{SYSCLKP}$	SYSCLK Period		47			ns
T_{FLWR}	FLASH Write Time	2 Bytes		20		μs
T_{FLPE}	FLASH Page Erase	1 kBytes		2		ms
T_{FLE}	FLASH Secure Erase	64 kBytes		10		ms
T_{FLEND}	FLASH Endurance: Erase Cycles		10 000	100 000		Cycles
$T_{FLRETroom}$	FLASH Data Retention	25°C See Figure 3 for the lower limit set by the memory qualification	100			Years
$T_{FLREThot}$		85°C See Figure 3 for the lower limit set by the memory qualification	10			

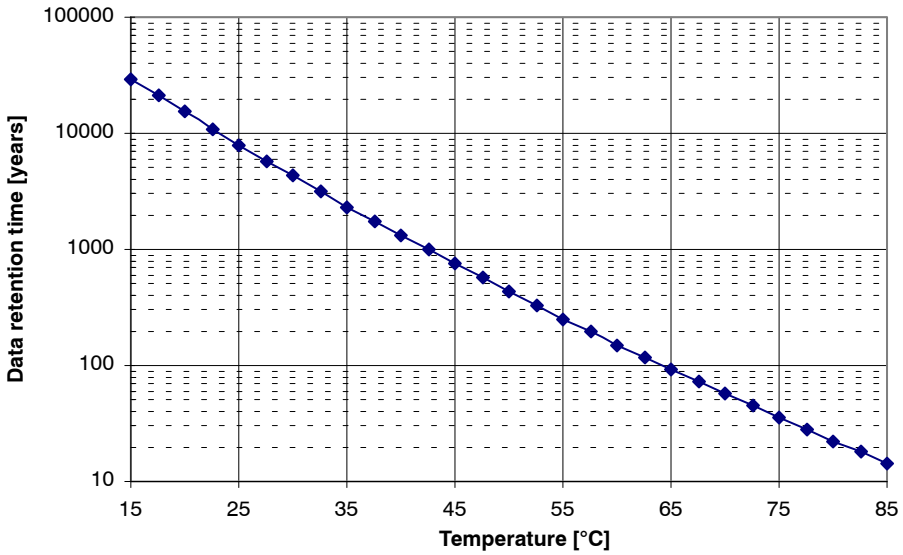


Figure 3. FLASH Memory Qualification Limit for Data Retention after 10k Erase Cycles

Table 16. ADC / COMPARATOR / TEMPERATURE SENSOR

Symbol	Description	Condition	Min	Typ	Max	Units
ADCSR	ADC sampling rate GPADC mode		30		500	kHz
ADCSR_T	ADC sampling rate temperature sensor mode		10	15.6	30	kHz
ADCRES	ADC resolution			10		Bits
V_{ADCREF}	ADC reference voltage & comparator internal reference voltage		0.95	1	1.05	V
Z_{ADC00}	Input capacitance				2.5	pF
DNL	Differential nonlinearity				± 1	LSB
INL	Integral nonlinearity			± 1		LSB
OFF	Offset			3		LSB
GAIN_ERR	Gain error			0.8		%
ADC in Differential Mode						
V_{ABS_DIFF}	Absolute voltages & common mode voltage in differential mode at each input		0		VDD_IO	V
V_{FS_DIFF01}	Full swing input for differential signals	Gain x1	−500		500	mV
V_{FS_DIFF10}		Gain x10	−50		50	mV
ADC in Single Ended Mode						
V_{MID_SE}	Mid code input voltage in single ended mode			0.5		V
V_{IN_SE00}	Input voltage in single ended mode		0		VDD_IO	V
V_{FS_SE01}	Full swing input for single ended signals	Gain x1	0		1	V
Comparators						
V_{COMP_ABS}	Comparator absolute input voltage		0		VDD_IO	V
V_{COMP_COM}	Comparator input common mode		0		VDD_IO − 0.8	V
$V_{COMPOFF}$	Comparator input offset voltage				20	mV
Temperature Sensor						
T_{RNG}	Temperature range		−40		85	°C
T_{RES}	Temperature resolution			0.1607		°C/LSB
T_{ERR_CAL}	Temperature error	Factory calibration applied	−2		2	°C

CIRCUIT DESCRIPTION

The AX8052F151 is a single chip ultra−low−power RF−microcontroller SoC primarily for use in SRD bands. The on−chip transceiver consists of a fully integrated RF front−end with modulator, and demodulator. Base band data processing is implemented in an advanced and flexible communication controller that enables user friendly communication.

The AX8052F151 contains a high speed microcontroller compatible to the industry standard 8052 instruction set. It contains 64 kBytes of FLASH and 8.25 kBytes of internal SRAM.

The AX8052F151 features 3 16−bit general purpose timers with ΣΔ capability, 2 output compare units for generating PWM signals, 2 input compare units to record timings of external signals, 2 16−bit wakeup timers, a watchdog timer, 2 UARTs, a Master/Slave SPI controller, a 10−bit 500 kSample/s A/D converter, 2 analog comparators, a temperature sensor, a 2 channel DMA controller, and a dedicated AES crypto controller. Debugging is aided by a dedicated hardware debug interface controller that connects using a 3−wire protocol (1 dedicated wire, 2 shared with GPIO) to the PC hosting the debug software.

While the radio carrier/LO synthesizer can only be clocked by the crystal oscillator (carrier stability requirements dictate a high stability reference clock in the MHz range), the microcontroller and its peripherals provide extremely flexible clocking options. The system clock that clocks the microcontroller, as well as peripheral clocks, can be selected from one of the following clock sources: the crystal oscillator, an internal high speed 20 MHz oscillator, an internal low speed 640 Hz/10 kHz oscillator, or the low frequency crystal oscillator. Prescalers offer additional flexibility with their programmable divide by a power of two capability. To improve the accuracy of the internal oscillators, both oscillators may be slaved to the crystal oscillator.

AX8052F151 can be operated from a 2.2 V to 3.6 V power supply over a temperature range of –40°C to 85°C, it consumes 11 – 45 mA for transmitting, depending on the output power, 19 – 20 mA for receiving in high sensitivity mode and 17 – 18 mA for receiving in low power mode.

The AX8052F151 features make it an ideal interface for integration into various battery powered SRD solutions such as ticketing or as transceiver for telemetric applications e.g. in sensors. As primary application, the transceiver is intended for UHF radio equipment in accordance with the European Telecommunication Standard Institute (ETSI) specification EN 300 220−1 and the US Federal Communications Commission (FCC) standard CFR47, part 15. The use of AX8052F151 in accordance to FCC Par 15.247, allows for improved range in the 915 MHz band. Additionally AX8052F151 is compatible with the low frequency standards of 802.15.4 (ZigBee) and suited for systems targeting compliance with Wireless M−Bus standard EN 13757−4:2005.

The AX8052F151 sends and receives data in frames. This standard operation mode is called Frame Mode. Pre and post ambles as well as checksums can be generated automatically.

AX8052F151 supports any data rate from 1 kbps to 350 kbps for FSK and MSK, from 1 kbps to 600 kbps for ASK and from 10 kbps to 600 kbps for PSK. To achieve optimum performance for specific data rates and modulation schemes several register settings to configure the AX8052F151 are necessary, they are outlined in the following, for details see the AX5051 Programming Manual.

Spreading and despreading is possible on all data rates and modulation schemes. The net transfer rate is reduced by a factor of 15 in this case. For ZigBee either 600 or 300 kbps modes have to be chosen.

The receiver supports multi−channel operation for all data rates and modulation schemes.

Microcontroller

The AX8052F151 microcontroller core executes the industry standard 8052 instruction set. Unlike the original 8052, many instructions are executed in a single cycle. The system clock and thus the instruction rate can be programmed freely from DC to 20 MHz.

Memory Architecture

The AX8052 Microcontroller features the highest bandwidth memory architecture of its class. Figure 4 shows the memory architecture. Three bus masters may initiate bus cycles:

- The AX8052 Microcontroller Core
- The Direct Memory Access (DMA) Engine
- The Advanced Encryption Standard (AES) Engine

Bus targets include:

- Two individual 4 kBytes RAM blocks located in X address space, which can be simultaneously accessed and individually shut down or retained during sleep mode
- A 256 Byte RAM located in internal address space, which is always retained during sleep mode
- A 64 kBytes FLASH memory located in code space.
- Special Function Registers (SFR) located in internal address space accessible using direct address mode instructions
- Additional Registers located in X address space (X Registers)

The upper half of the FLASH memory may also be accessed through the X address space. This simplifies and makes the software more efficient by reducing the need for generic pointers.

NOTE: Generic pointers include, in addition to the address, an address space tag.

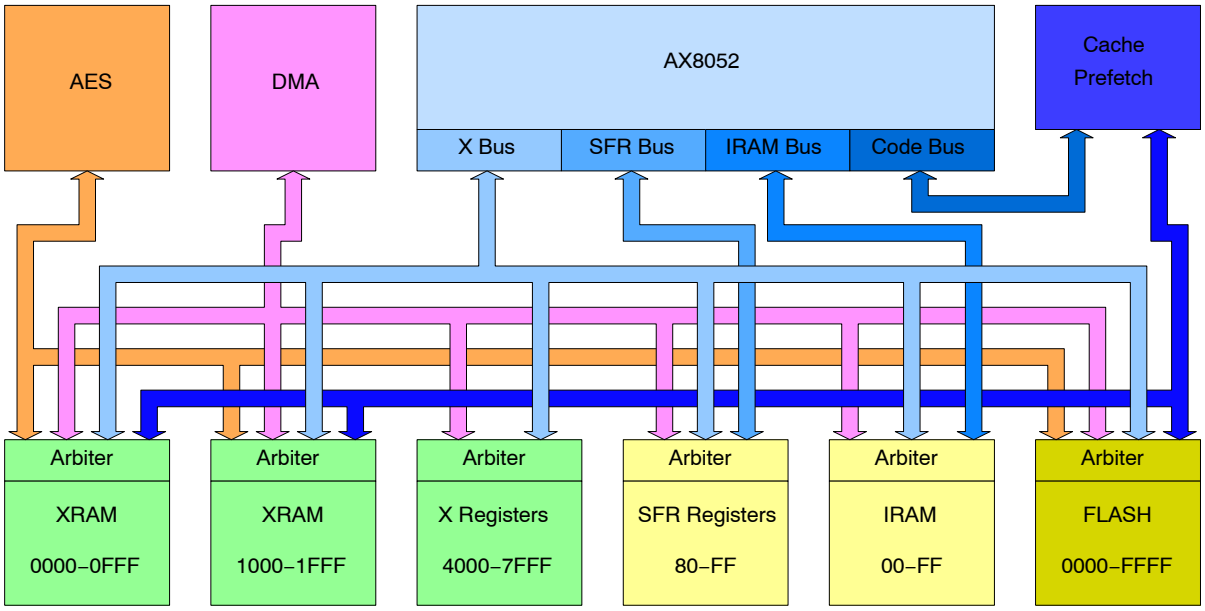


Figure 4. AX8052 Memory Architecture

SFR Registers are also accessible through X address space, enabling indirect access to SFR registers. This allows driver code for multiple identical peripherals (such as UARTs or Timers) to be shared.

The 4 word × 16 bit fully associative cache and a pre−fetch controller hide the latency of the FLASH.

The AX8052 Memory Architecture is fully parallel. All bus masters may simultaneously access different bus targets during each system clock cycle. Each bus target includes an arbiter that resolves access conflicts. Each arbiter ensures that no bus master can be starved.

Both 4 kBytes RAM blocks may be individually retained or switched off during sleep mode. The 256 Byte RAM is always retained during sleep mode.

The AES engine accesses memory 16 bits at a time. It is therefore slightly faster to align its buffers on even addresses.

Memory Map

The AX8052, like the other industry standard 8052 compatible microcontrollers, uses a Harvard architecture. Multiple address spaces are used to access code and data. Figure 5 shows the AX8052 memory map.

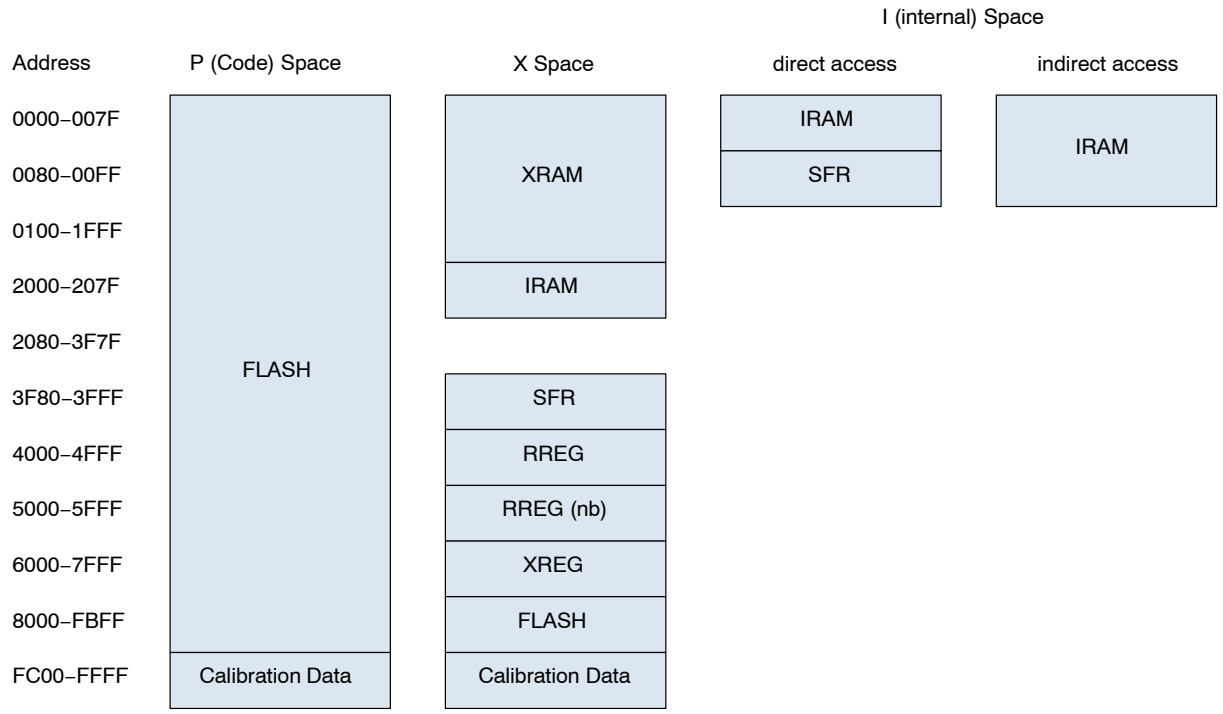


Figure 5. AX8052 Memory Map

The AX8052 uses P or Code Space to access its program. Code space may also be read using the MOVC instruction.

Smaller amounts of data can be placed in the Internal (see Note) or Data Space. A distinction is made in the upper half of the Data Space between direct accesses (MOV reg,addr; MOV addr,reg) and indirect accesses (MOV reg,@Ri; MOV @Ri,reg; PUSH; POP); Direct accesses are routed to the Special Function Registers, while indirect accesses are routed to the internal RAM.

NOTE: The origin of Internal versus External (X) Space is historical. External Space used to be outside of the chip on the original 8052 Microcontrollers.

Large amounts of data can be placed in the External or X Space. It can be accessed using the MOVX instructions. Special Function Registers, as well as additional Microcontroller Registers (XREG) and the Radio Registers (RREG) are also mapped into the X Space.

Detailed documentation of the Special Function Registers (SFR) and additional Microcontroller Registers can be found in the AX8052 Programming Manual.

The Radio Registers are documented in the AX5051 Programming Manual. Register Addresses given in the AX5051 Programming Manual are relative to the beginning of RREG, i.e. 0x4000 must be added to these addresses. It is recommended that the provided AX8052F151.h header file is used; Radio Registers are prefixed with AX5051_ in the AX8052F151.h header file to avoid clashes of same−name Radio Registers with AX8052 registers.

Normally, accessing Radio Registers through the RREG address range is adequate. Since Radio Register accesses have a higher latency than other AX8052 registers, the AX8052 provides a method for non−blocking access to the Radio Registers. Accessing the RREG (nb) address range initiates a Radio Register access, but does not wait for its completion. The details of mechanism is documented in the Radio Interface section of the AX8052 Programming Manual.

The FLASH memory is organized as 64 pages of 1 kBytes each. Each page can be individually erased. The write word size is 16 Bits. The last 1 kByte page is dedicated to factory calibration data and should not be overwritten.

Power Management

The microcontroller power mode can be selected independently from the transceiver. The microcontroller supports the following power modes:

Table 17. POWER MANAGEMENT

PCON register	Name	Description
00	RUNNING	The microcontroller and all peripherals are running. Current consumption depends on the system clock frequency and the enabled peripherals and their clock frequency.
01	STANDBY	The microcontroller is stopped. All register and memory contents are retained. All peripherals continue to function normally. Current consumption is determined by the enabled peripherals. STANDBY is exited when any of the enabled interrupts become active.
10	SLEEP	The microcontroller and its peripherals, except GPIO and the system controller, are shut down. Their register settings are lost. The internal RAM is retained. The external RAM is split into two 4 kByte blocks. Software can determine individually for both blocks whether contents of that block are to be retained or lost. SLEEP can be exited by any of the enabled GPIO or system controller interrupts. For most applications this will be a GPIO or wakeup timer interrupt.
11	DEEPSLEEP	The microcontroller, all peripherals and the transceiver are shut down. Only 4 bytes of scratch RAM are retained. DEEPSLEEP can only be exited by tying the PB3 pin low.

Clocking

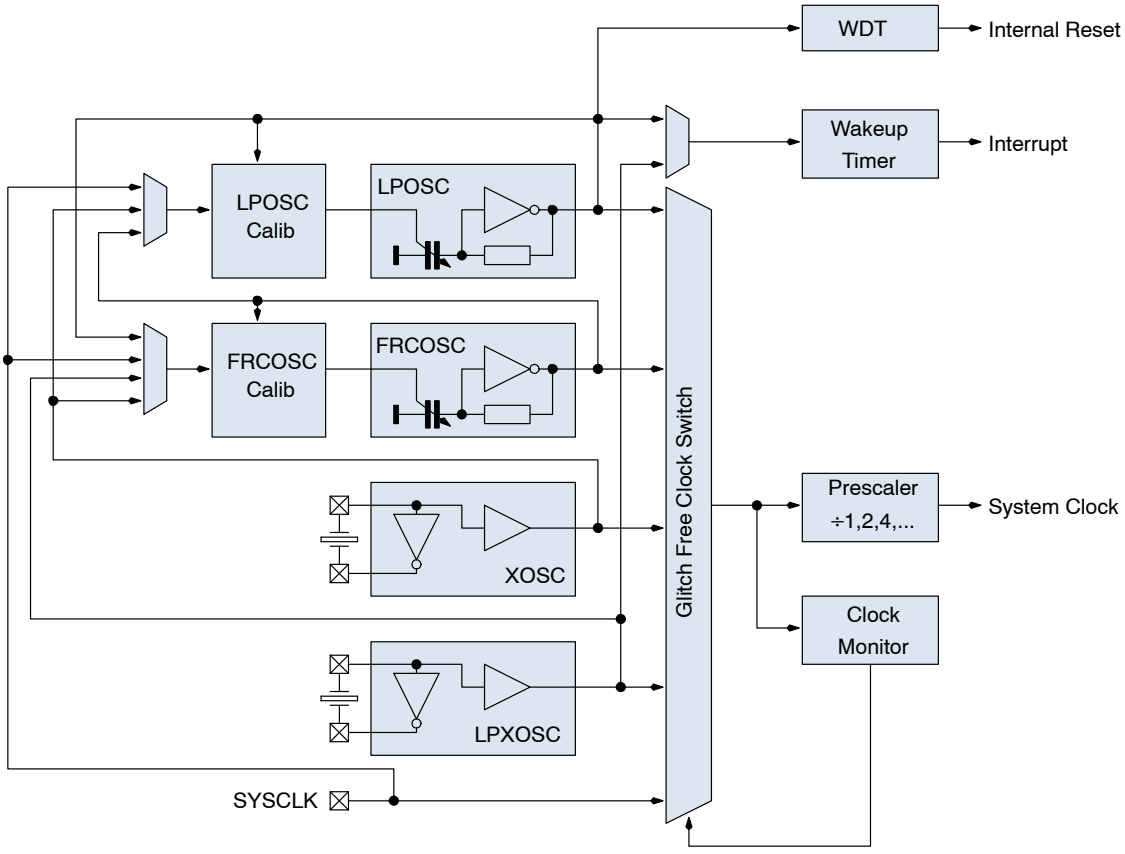


Figure 6. Clock System Diagram

The system clock can be derived from any of the following clock sources:

- The crystal oscillator (RF reference oscillator, typically 16 MHz, via SYSCLK)
- The low speed crystal oscillator (typical 32 kHz tuning fork)
- The internal high speed RC (20 MHz) oscillator
- The internal low power (640 Hz/10 kHz) oscillator

An additional pre−scaler allows the selected oscillator to be divided by a power of two. After reset, the microcontroller starts with the internal high speed RC oscillator selected and divided by two. I.e. at start−up, the microcontroller runs with 10 MHz ± 10%. Clocks may be switched any time by writing to the CLKCON register. In order to prevent clock glitches, the switching takes approximately $2\cdot(T_1+T_2)$, where T_1 and T_2 are the periods

of the old and the new clock. Switching may take longer if the new oscillator first has to start up. Internal oscillators start up instantaneously, but crystal oscillators may take a considerable amount of time to start the oscillation. CLKSTAT can be read to determine the clock switching status.

A programmable clock monitor resets the CLKCON register when no system clock transitions are found during a programmable time interval, thus reverts to the internal RC oscillator.

Both internal oscillators can be slaved to one of the crystal oscillators to increase the accuracy of the oscillation frequency. While the reference oscillator runs, the internal oscillator is slaved to the reference frequency by a digital frequency locked loop. When the reference oscillator is switched off, the internal oscillator continues to run unslaved with the last frequency setting.

Reset and Interrupts

After reset, the microcontroller starts executing at address 0x0000. Several events can lead to resetting the microcontroller core:

- POR or hardware RESET_N pin activated and released
- Leaving SLEEP or DEEPSLEEP mode
- Watchdog Reset
- Software Reset

The reset cause can be determined by reading the PCON register.

The microcontroller supports 22 interrupt sources. Each interrupt can be individually enabled and can be programmed to have one of two possible priorities. The interrupt vectors are located at 0x0003, 0x000B,…, 0x00AB.

Debugging

A hardware debug unit considerably eases debugging compared to other 8052 microcontrollers. It allows to reliably stop the microcontroller at breakpoints even if the stack is smashed. The debug unit communicates with the host PC running the debugger using a 3 wire interface. One wire is dedicated (DBG_EN), while two wires are shared with GPIO pins (PB6, PB7). When DBG_EN is driven high, PB6 and PB7 convert to debug interface pins and the GPIO functionality is no longer available. A pin emulation feature however allows bits PINB[7:6] to be set and PORTB[7:6] and DIRB[7:6] to be read by the debugger software. This allows for example switches or LEDs connected to the PB6, PB7 pins to be emulated in the debugger software whenever the debugger is active.

In order to protect the intellectual property of the firmware developer, the debug interface can be locked using a developer−selectable 64−bit key. The debug interface is then disabled and can only be enabled with the knowledge of this 64−bit key. Therefore, unauthorized persons cannot read the firmware through the debug interface, but debugging is still possible for authorized persons. Secure erase can be initiated without key knowledge; secure erase ensures that the main FLASH array is completely erased before erasing the key, reverting the chip into factory state.

The DebugLink peripheral looks like an UART to the microcontroller, and allows exchange of data between the microcontroller and the host PC without disrupting program execution.

Timer, Output Compare and Input Capture

The AX8052F151 features three general purpose 16−bit timers. Each timer can be clocked by the system clock, any of the available oscillators, or a dedicated input pin. The timers also feature a programmable clock inversion, a programmable prescaler that can divide by powers of two, and an optional clock synchronization logic that synchronizes the clock to the system clock. All three counters are identical and feature four different counting modes, as well as a ΣΔ mode that can be used to output an analog value on a dedicated digital pin only employing a simple RC lowpass filter.

Two output compare units work in conjunction with one of the timers to generate PWM signals.

Two input capture units work in conjunction with one of the timers to measure transitions on an input signal.

For software timekeeping, two additional 16−bit wakeup timers with 4 16−bit event registers are provided, generating an interrupt on match events.

UART

The AX8052F151 features two universal asynchronous receiver transmitters. They use one of the timers as baud rate generator. Word length can be programmed from 5 to 9 bits.

SPI Master/Slave Controller

The AX8052F151 features a master/slave SPI controller. Both 3 and 4 wire SPI variants are supported. In master mode, any of the on−chip oscillators or the system clock may be selected as clock source. An additional prescaler with divide by two capability provides additional clocking flexibility. Shift direction, as well as clock phase and inversion, are programmable.

ADC, Analog Comparators and Temperature Sensor

The AX8052F151 features a 10−bit, 500 kSample/s Analog to Digital converter. Figure 7 shows the block diagram of the ADC. The ADC supports both single ended and differential measurements. It uses an internal reference of 1 V. ×1, ×10 and ×0.1 gain modes are provided. The ADC may digitize signals on PA0…PA7, as well as VDD_IO and an internal temperature sensor. The user can define four channels which are then converted sequentially and stored in four separate result registers. Each channel configuration consists of the multiplexer and the gain setting.

The AX8052F151 contains an on−chip temperature sensor. Built−in calibration logic allows the temperature sensor to be calibrated in °C, °F or any other user defined temperature scale.

The AX8052F151 also features two analog comparators. Each comparator can either compare two voltages on dedicated PA pins, or one voltage against the internal 1 V reference. The comparator output can be routed to a dedicated digital output pin or can be read by software. The comparators are clocked with the system clock.

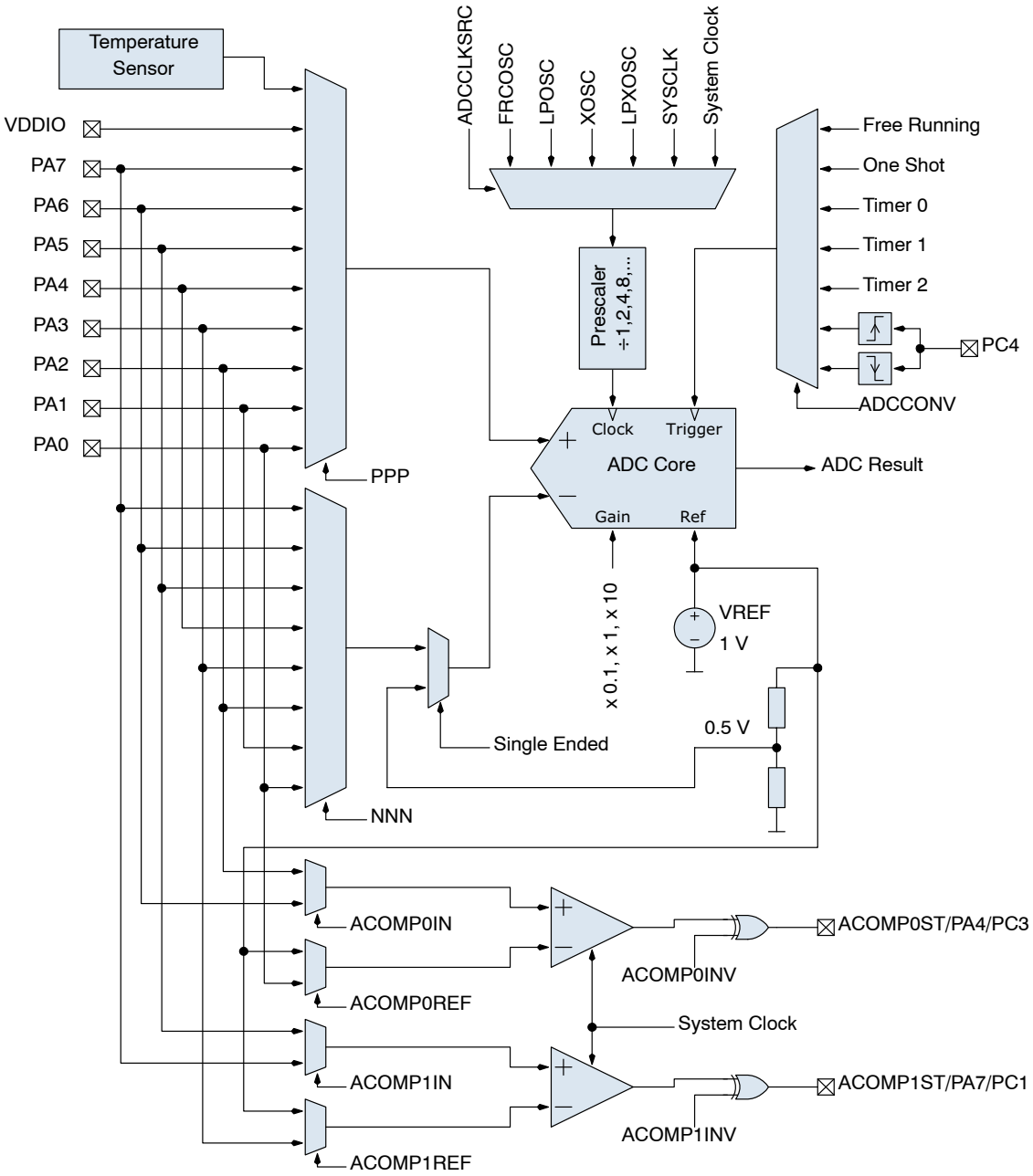


Figure 7. ADC Block Diagram

DMA Controller

The AX8052F151 features a dual channel DMA engine. Each DMA channel can either transfer data from XRAM to almost any peripheral on chip, or from almost any peripheral to XRAM. Both channels may also be cross−linked for memory−memory transfers. The DMA channels use buffer descriptors to find the buffers where data is to be retrieved or placed, thus enabling very flexible buffering strategies.

The DMA channels access XRAM in a cycle steal fashion. They access XRAM whenever XRAM is not used by the microcontroller. Their priority is lower than the microcontroller, thus interfering very little with the microcontroller. Additional logic prevents starvation of the DMA controller.

AES Engine

The AX8052F151 contains a dedicated engine for the government mandated Advanced Encryption Standard (AES). It features a dedicated DMA engine and reads input data as well as key stream data from the XRAM, and writes output data into a programmable buffer in the XRAM. The round number is programmable; the chip therefore supports AES−128, AES−192, and AES−256, as well as higher security proprietary variants. Keystream (key expansion) is performed in software, adding to the flexibility of the AES engine. ECB (electronic codebook), CFB (cipher feedback) and OFB (output feedback) modes are directly supported without software intervention.

Crystal Oscillator (RF Reference Oscillator)

The on−chip crystal oscillator allows the use of an inexpensive quartz crystal as the RF generation subsystem's timing reference. Although a wider range of crystal frequencies can be handled by the crystal oscillator circuit, it is recommended to use 16 MHz as reference frequency for ASK and PSK modulations independent of the data rate. For FSK it is recommended to use a 16 MHz crystal for data rates below 200 kbps and 24 MHz for data rates above 200 kbps.

The oscillator circuit is enabled by programming the AX5051_PWRMODE register. At power−up it is not enabled.

To adjust the circuit's characteristics to the quartz crystal being used, without using additional external components, both the transconductance and the tuning capacitance of the crystal oscillator can be programmed.

The transconductance is programmed via register bits XTALOSCGM[3:0] in register AX5051_XTALOSC.

The integrated programmable tuning capacitor bank makes it possible to connect the oscillator directly to pins CLK16N and CLK16P without the need for external capacitors. It is programmed using bits XTALCAP[5:0] in register AX5051_XTALCAP.

To synchronize the receiver frequency to a carrier signal, the oscillator frequency could be tuned using the capacitor bank however, the recommended method to implement frequency synchronization is to make use of the high resolution RF frequency generation sub−system together with the Automatic Frequency Control, both are described further down.

Alternatively a single ended reference (TCXO, CXO) may be used. The CMOS levels should be applied to CLK16P via an AC coupling with the crystal oscillator enabled.

SYSCLK Output

The SYSCLK pin outputs the RF reference clock signal divided by a programmable integer. Divisions from 1 to 2048 are possible. For divider ratios > 1 the duty cycle is 50%. Bits SYSCLK[3:0] in the AX5051_PINCFG1 register set the divider ratio. The SYSCLK output can be disabled.

Outputting a frequency that is identical to the IF frequency (default 1 MHz) on the SYSCLK pin is not recommended during receive operation, since it requires extensive decoupling on the PCB to avoid interference.

Power−on−Reset (POR) and RESET_N Input

AX8052F151 has an integrated power−on−reset block which is edge sensitive to VDD_IO. For many common application cases no external reset circuitry is required. However, if VDD_IO ramps cannot be guaranteed, an external reset circuit is recommended. For detailed recommendations and requirements see the AX8052 Application Note: Power On Reset.

After POR or reset all registers are set to their default values.

The RESET_N pin contains a weak pull−up. However, it is strongly recommended to connect the RESET_N pin to VDD_IO if not used, for additional robustness.

The AX8052F151 can be reset by software as well. The microcontroller is reset by writing 1 to the SWRESET bit of the PCON register. The transmitter can be reset by first writing 1 and then 0 to the RST bit in the AX5051_PWRMODE register.

Ports

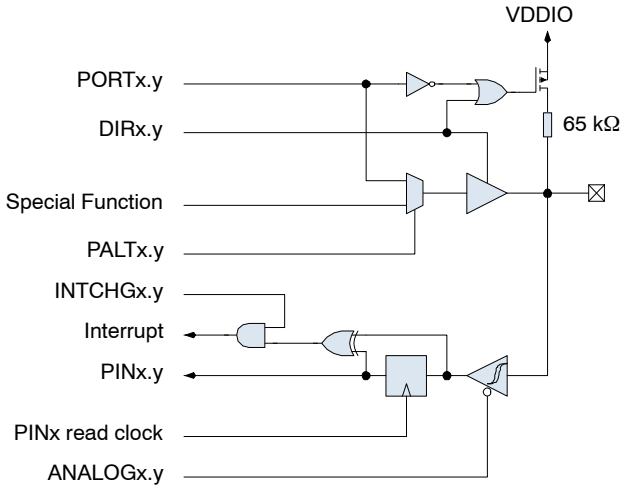


Figure 8. Port Pin Schematic

Figure 8 shows the GPIO logic. The DIR register bit determines whether the port pin acts as an output (1) or an input (0).

If configured as an output, the PALT register bit determines whether the port pin is connected to a peripheral output (1), or used as a GPIO pin (0). In the latter case, the PORT register bit determines the port pin drive value.

If configured as an input, the PORT register bit determines whether a pull−up resistor is enabled (1) or disabled (0). Inputs have Schmitt−trigger characteristic. Port A inputs may be disabled by setting the ANALOGA register bit; this prevents additional current consumption if the voltage level of the port pin is mid−way between logic low and logic high, when the pin is used as an analog input.

Port A, B and C pins may interrupt the microcontroller if their level changes. The INTCHG register bit enables the interrupt. The PIN register bit reflects the value of the port pin. Reading the PIN register also resets the interrupt if interrupt on change is enabled.

TRANSCEIVER

The transceiver block is controllable through its registers, which are mapped into the X data space of the microcontroller. The transceiver block features its own 4 word × 10 bit FIFO. The microcontroller can either be interrupted at a programmable FIFO fill level, or one of the DMA channels can be instructed to transfer between XRAM and the transceiver FIFO.

RF Frequency Generation Subsystem

The RF frequency generation subsystem consists of a fully integrated synthesizer, which multiplies the reference frequency from the crystal oscillator to get the desired RF frequency. The advanced architecture of the synthesizer enables frequency resolutions of 1 Hz, as well as fast settling times of 5 – 50 μs depending on the settings (see section AC Characteristics). Fast settling times mean fast start−up and fast RX/TX switching, enabling low−power system design.

For receive operation the RF frequency is fed to the mixer, for transmit operation to the power−amplifier.

The frequency must be programmed to the desired carrier frequency. The RF frequency shift by the IF frequency that is required for RX operation, is automatically set when the receiver is activated and does not need to be programmed by the user. The default IF frequency is 1 MHz. It can be programmed to other values. Changing the IF frequency and thus the center frequency of the digital channel filter can be used to adapt the blocking performance of the device to specific system requirements.

The synthesizer loop bandwidth can be programmed. This serves three purposes:

1. Start−up time optimization, start−up is faster for higher synthesizer loop bandwidths
2. TX spectrum optimization, phase−noise at 300 kHz to 1 MHz distance from the carrier improves with lower synthesizer loop bandwidths
3. Adaptation of the bandwidth to the data−rate. For transmission of FSK and MSK it is required that the synthesizer bandwidth must be in the order of the data−rate.

VCO

An on−chip VCO converts the control voltage generated by the charge pump and loop filter into an output frequency. This frequency is used for transmit as well as for receive operation. The frequency can be programmed in 1 Hz steps in the AX5051_FREQ registers. For operation in the 433 MHz band, the BANDSEL bit in the AX5051_PLLLOOP register must be programmed.

VCO Auto−Ranging

The AX8052F151 has an integrated auto−ranging function, which allows to set the correct VCO range for specific frequency generation subsystem settings automatically. Typically it has to be executed after power−up. The function is initiated by setting the RNG_START bit in the AX5051_PLLRANGING register. The bit is readable and a 0 indicates the end of the ranging process. The RNGERR bit indicates the correct execution of the auto−ranging.

Loop Filter and Charge Pump

The AX8052F151 internal loop filter configuration together with the charge pump current sets the synthesizer loop band width. The loop−filter has three configurations that can be programmed via the register bits FLT[1:0] in register AX5051_PLLLOOP, the charge pump current can be programmed using register bits PLLCPI[1:0] also in register AX5051_PLLLOOP. Synthesizer bandwidths are typically 50 – 500 kHz depending on the AX5051_PLLLOOP settings, for details see the section: AC Characteristics.

Registers

Table 18. REGISTERS

Register	Bits	Purpose
AX5051_PLLLOOP	FLT[1:0]	Synthesizer loop filter bandwidth, recommended usage is to increase the bandwidth for faster settling time, bandwidth increases of factor 2 and 5 are possible.
	PLLCPI[2:0]	Synthesizer charge pump current, recommended usage is to decrease the bandwidth (and improve the phase−noise) for low data−rate transmissions.
	BANDSEL	Switches between 868 MHz / 915 MHz and 433 MHz bands
AX5051_FREQ		Programming of the carrier frequency
AX5051_IFFREQHI, AX5051_IFFREQLO		Programming of the IF frequency
AX5051_PLLRANGING		Initiate VCO auto−ranging and check results

RF Input and Output Stage (ANTP/ANTN)

The AX8052F151 uses fully differential antenna pins. RX/TX switching is handled internally. An external RX/TX switch is not required.

LNA

The LNA amplifies the differential RF signal from the antenna and buffers it to drive the I/Q mixer. An external matching network is used to adapt the antenna impedance to the IC impedance. A DC feed to the regulated supply voltage VREG must be provided at the antenna pins. For recommendations see section: Application Information.

I/Q Mixer

The RF signal from the LNA is mixed down to an IF of typically 1 MHz. I− and Q−IF signals are buffered for the analog IF filter.

PA

In TX mode the PA drives the signal generated by the frequency generation subsystem out to the differential antenna terminals. The output power of the PA is programmed via bits TXRNG[3:0] in the register AX5051_TXPWR. Output power as well as harmonic content will depend on the external impedance seen by the PA, recommendations are given in the applications section.

Analog IF Filter

The mixer is followed by a complex band−pass IF filter, which suppresses the down−mixed image while the wanted signal is amplified. The center frequency of the filter is 1 MHz, with a pass−band width of 1 MHz. The RF frequency generation subsystem must be programmed in such a way that for all possible modulation schemes the IF frequency spectrum fits into the pass−band of the analog filter.

Digital IF Channel Filter and Demodulator

The digital IF channel filter and the demodulator extract the data bit−stream from the incoming IF signal. They must be programmed to match the modulation scheme as well as the data rate. Inaccurate programming will lead to loss of sensitivity.

The channel filter offers bandwidths of 40 kHz up to 600 kHz.

For detailed instructions how to program the digital channel filter and the demodulator see the AX5051 Programming Manual, an overview of the registers involved is given in the following table. The register setups typically must be done once at power−up of the device.

Table 19. REGISTERS

Register	Remarks
AX5051_CICDEC	This register programs the bandwidth of the digital channel filter.
AX5051_DATARATEHI, AX5051_DATARATELO	These registers specify the receiver bit rate, relative to the channel filter bandwidth.
AX5051_TMGGAINHI, AX5051_TMGGAINLO	These registers specify the aggressiveness of the receiver bit timing recovery. More aggressive settings allow the receiver to synchronize with shorter preambles, at the expense of more timing jitter and thus a higher bit error rate at a given signal−to−noise ratio.
AX5051_MODULATION	This register selects the modulation to be used by the transmitter and the receiver, i.e. whether ASK, PSK , FSK, MSK or OQPSK should be used.
AX5051_PHASEGAIN, AX5051_FREQGAIN, AX5051_FREQGAIN2, AX5051_AMPLGAIN	These registers control the bandwidth of the phase, frequency offset and amplitude tracking loops. Recommended settings are provided in the AX5051 Programming Manual.
AX5051_AGCATTACK, AX5051_AGCDECAY	These registers control the AGC (automatic gain control) loop slopes, and thus the speed of gain adjustments. The faster the bit rate, the faster the AGC loop should be. Recommended settings are provided in the AX5051 Programming Manual.
AX5051_TXRATE	These registers control the bit rate of the transmitter.
AX5051_FSKDEV	These registers control the frequency deviation of the transmitter in FSK mode. The receiver does not explicitly need to know the frequency deviation, only the channel filter bandwidth has to be set wide enough for the complete modulation to pass.

Encoder

The encoder is located between the Framing Unit, the Demodulator and the Modulator. It can optionally transform the bit−stream in the following ways:

- It can invert the bit stream.
- It can perform differential encoding. This means that a zero is transmitted as no change in the level, and a one is transmitted as a change in the level. Differential encoding is useful for PSK, because PSK transmissions can be received either as transmitted or inverted, due to the uncertainty of the initial phase. Differential encoding / decoding removes this uncertainty.
- It can perform Manchester encoding. Manchester encoding ensures that the modulation has no DC content and enough transitions (changes from 0 to 1 and from 1 to 0) for the demodulator bit timing recovery to function correctly, but does so at a doubling of the data rate.

- It can perform Spectral Shaping. Spectral shaping removes DC content of the bit stream, ensures transitions for the demodulator bit timing recovery, and makes sure that the transmitted spectrum does not have discrete lines even if the transmitted data is cyclic. It does so without adding additional bits, i.e. without changing the data rate. Spectral Shaping uses a self synchronizing feedback shift register.

The encoder is programmed using the register AX5051_ENCODING, details and recommendations on usage are given in the AX5051 Programming Manual.

Framing and FIFO

Most radio systems today group data into packets. The framing unit is responsible for converting these packets into a bit−stream suitable for the modulator, and to extract packets from the continuous bit−stream arriving from the demodulator.

The Framing unit supports four different modes:

- HDLC
- Raw
- Raw with Preamble Match
- 802.15.4 Compliant

The microcontroller communicates with the framing unit through a 4 level × 10 bit FIFO. The FIFO decouples microcontroller timing from the radio (modulator and demodulator) timing. The bottom 8 bits of the FIFO contain transmit or receive data. The top 2 bit are used to convey meta information in HDLC and 802.15.4 modes. They are unused in Raw and Raw with Preamble Match modes. The meta information consists of packet begin / end information and the result of CRC checks.

The framing unit contains one FIFO. Its direction is switched depending on whether transmit or receive mode is selected.

The FIFO can be operated in polled or interrupt driven modes. In polled mode, the microcontroller must periodically read the FIFO status register or the FIFO count register to determine whether the FIFO needs servicing.

In interrupt mode EMPTY, NOT EMPTY, FULL, NOT FULL and programmable level interrupts are provided. Interrupts are acknowledged by removing the cause for the interrupt, i.e. by emptying or filling the FIFO.

To lower the interrupt load on the microcontroller, one of the DMA channels may be instructed to transfer data between the transceiver FIFO and the XRAM memory. This way, much larger buffers can be realized in XRAM, and interrupts need only be serviced if the larger XRAM buffers fill or empty.

HDLC Mode

NOTE: HDLC mode follows High−Level Data Link Control (HDLC, ISO 13239) protocol.

HDLC Mode is the main framing mode of the AX8052F151. In this mode, the AX8052F151 performs automatic packet delimiting, and optional packet correctness check by inserting and checking a cyclic redundancy check (CRC) field.

The packet structure is given in the following table.

Table 20.

Flag	Address	Control	Information	FCS	Flag
8 bit	8 bit	8 or 16 bit	Variable length, 0 or more bits in multiples of 8	16 / 32 bit	8 bit

HDLC packets are delimited with flag sequences of content 0x7E.

In AX8052F151 the meaning of address and control is user defined. The Frame Check Sequence (FCS) can be programmed to be CRC−CCITT, CRC−16 or CRC−32.

The receiver checks the CRC, the result can be retrieved from the FIFO, the CRC is appended to the received data.

For details on implementing a HDLC communication see the AX5051 Programming Manual.

Raw Mode

In Raw mode, the AX8052F151 does not perform any packet delimiting or byte synchronization. It simply serializes transmit bytes and de−serializes the received bit−stream and groups it into bytes.

This mode is ideal for implementing legacy protocols in software.

Raw Mode with Preamble Match

Raw mode with preamble match is similar to raw mode. In this mode, however, the receiver does not receive anything until it detects a user programmable bit pattern (called the preamble) in the receive bit−stream. When it detects the preamble, it aligns the de−serialization to it.

The preamble can be between 4 and 32 bits long.

802.15.4 (ZigBee) DSSS

802.15.4 uses binary phase shift keying (PSK) with 300 kbit/s (868 MHz band) or 600 kbit/s (915 MHz band) on the radio. The usable bit rate is only a 15^{th} of the radio bit rate, however. A spreading function in the transmitter expands the user bit rate by a factor of 15, to make the transmission more robust. The despreader function of the receiver undoes that.

In 802.15.4 mode, the AX8052F151 framing unit performs the spreading and despreading function according to the 802.15.4 specification. In receive mode, the framing unit will also automatically search for the 802.15.4

preamble, meaning that no interrupts will have to be serviced by the microcontroller until a packet start is detected.

The 802.15.4 is a universal DSSS mode, which can be used with any modulation or data rate as long as it does not violate the maximum data rate of the modulation being used. Therefore the maximum DSSS data rate is 16 kbps for FSK and 40 kbps for ASK and PSK.

RX AGC and RSSI

AX8052F151 features two receiver signal strength indicators (RSSI):

1. RSSI before the digital IF channel filter.
   The gain of the receiver is adjusted in order to keep the analog IF filter output level inside the working range of the ADC and demodulator. The register AX5051_AGCCOUNTER contains the current value of the AGC and can be used as an RSSI. The step size of this RSSI is 0.625 dB. The value can be used as soon as the RF frequency generation sub−system has been programmed.
2. RSSI behind the digital IF channel filter.
   The demodulator also provides amplitude information in the AX5051_TRK_AMPLITUDE register. By combining both the AX5051_AGCCOUNTER and the AX5051_TRK_AMPLITUDE registers, a high resolution (better than 0.1 dB) RSSI value can be computed at the expense of a few arithmetic operations on the microcontroller. Formulas for this computation can be found in the AX5051 Programming Manual.

Modulator

Depending on the transmitter settings the modulator generates various inputs for the PA:

Table 21.

Modulation	Bit = 0	Bit = 1	Main Lobe Bandwidth	Max. Bitrate
ASK	PA off	PA on	BW = BITRATE	600 kBit/s
FSK/MSK	$\Delta f = -f_{deviation}$	$\Delta f = +f_{deviation}$	BW = (1 + h) ·BITRATE	350 kBit/s
PSK	$\Delta\Phi = 0°$	$\Delta\Phi = 180°$	BW = BITRATE	600 kBit/s

h = modulation index. It is the ratio of the deviation compared to the bit−rate; $f_{deviation} = 0.5 \cdot h \cdot BITRATE$, AX8052F151 can demodulate signals with $h < 32$.
ASK = amplitude shift keying
FSK = frequency shift keying
MSK = minimum shift keying; MSK is a special case of FSK, where h = 0.5, and therefore $f_{deviation} = 0.25 \cdot BITRATE$; the advantage of MSK over FSK is that it can be demodulated more robustly.
PSK = phase shift keying
OQPSK = offset quadrature shift keying. The AX8052F151 supports OQPSK. However, unless compatibility to an existing system is required, MSK should be preferred.

All modulation schemes are binary.

Automatic Frequency Control (AFC)

The AX8052F151 has a frequency tracking register AX5051_TRKFREQ to synchronize the receiver frequency to a carrier signal. For AFC adjustment, the frequency offset can be computed with the following formula:

$$\Delta f = \frac{TRKFREQ}{2^{16}} BITRATE \times FSKMUL$$

FSKMUL is the FSK oversampling factor, it depends on the FSK bit rate and deviation used. To determine it for a specific case, see the AX5051 Programming Manual. For modulations other than FSK, FSKMUL = 1.

PWRMODE Register

The AX8052F151 transceiver features its own independent power management, independent from the microcontroller. While the microcontroller power mode is controlled through the PCON register, the AX5051_PWRMODE register controls which parts of the transceiver are operating.

Table 22. PWRMODE REGISTER

AX5051_PWRMODE Register	Name	Description
0000	POWERDOWN	All digital and analog transceiver functions, except the register file, are disabled. VREG is reduced to conserve leakage power. The registers are still accessible.
0100	VREGON	All digital and analog transceiver functions, except the register file, are disabled. VREG, however is at its nominal value for operation, and all registers are accessible.
0101	STANDBY	The crystal oscillator is powered on; receiver and transmitter are off.

Table 22. PWRMODE REGISTER

AX5051_PWRMODE Register	Name	Description
1000	SYNTHRX	The synthesizer is running on the receive frequency. Transmitter and receiver are still off. This mode is used to let the synthesizer settle on the correct frequency for receive.
1001	FULLRX	Synthesizer and receiver are running.
1100	SYNTHTX	The synthesizer is running on the transmit frequency. Transmitter and receiver are still off. This mode is used to let the synthesizer settle on the correct frequency for transmit.
1101	FULLTX	Synthesizer and transmitter are running. Do not switch into this mode before the synthesizer has completely settled on the transmit frequency (in SYNTHTX mode), otherwise spurious spectral transmissions will occur.

Table 23. A TYPICAL AX5051_PWRMODE SEQUENCE FOR A TRANSMIT SESSION

Step	PWRMODE	Remarks
1	POWERDOWN	
2	STANDBY	The settling time is dominated by the crystal used, typical value 3 ms.
3	SYNTHTX	The synthesizer settling time is 5 – 50 μs depending on settings, see section AC Characteristics
4	FULLTX	Data transmission
5	SYNTHTX	**This step must be programmed after FULLTX mode, or the device will not enter POWERDOWN or STANDBY mode.**
6	POWERDOWN	

Table 24. A TYPICAL AX5051_PWRMODE SEQUENCE FOR A RECEIVE SESSION

Step	PWRMODE [3:0]	Remarks
1	POWERDOWN	
2	STANDBY	The settling time is dominated by the crystal used, typical value 3 ms.
3	SYNTHRX	The synthesizer settling time is 5 – 50 μs depending on settings, see section AC Characteristics
4	FULLRX	Data reception
5	POWERDOWN	

Voltage Regulator

The AX8052F151 transceiver uses its own dedicated on−chip voltage regulator to create a stable supply voltage for the transceiver circuitry at pin VREG from the primary supply VDD_IO. All VDDA pins of the device must be connected to VREG. The antenna pins ANTP and ANTN must be DC biased to VREG. The I/O level of the digital pins is VDD_IO.

The voltage regulator requires a 1 μF low ESR capacitor at pin VREG.

In power−down mode the voltage regulator typically outputs 1.7 V at VREG, if it is powered−up its output rises to typically 2.5 V. At device power−up the regulator is in power−down mode.

The voltage regulator must be powered−up before receive or transmit operations can be initiated. This is handled automatically when programming the device modes via the AX5051_PWRMODE register.

Register VREG contains status bits that can be read to check if the regulated voltage is above 1.3 V or 2.3 V, sticky versions of the bits are provided that can be used to detect low power events (brown−out detection).

APPLICATION INFORMATION

Typical Application Diagrams

Connecting to Debug Adapter

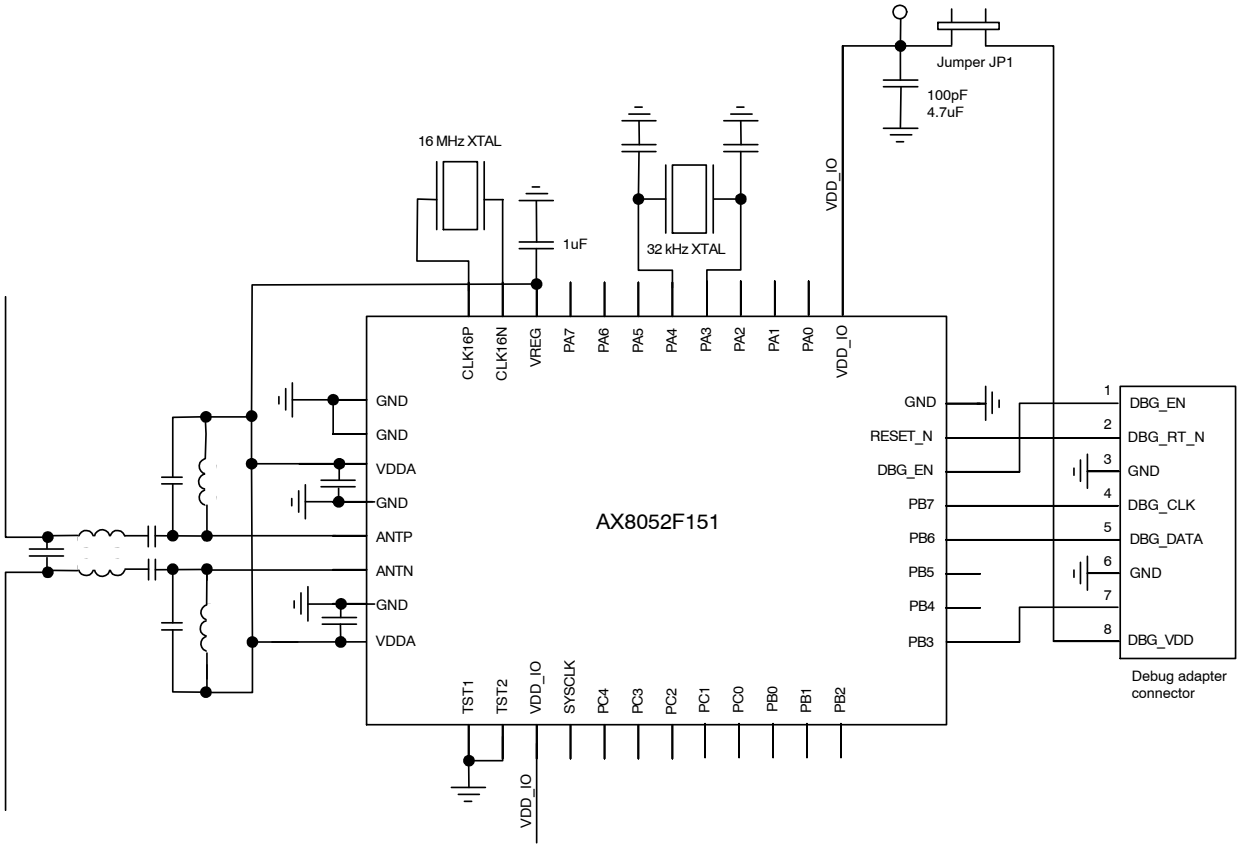


Figure 9. Typical Application Diagram with Connection to the Debug Adapter

Short Jumper JP1−1 if it is desired to supply the target board from the Debug Adapter (50 mA max). Connect the bottom exposed pad of the AX8052F151 to ground.

If the debugger is not running, PB6 and PB7 are not driven by the Debug Adapter. If the debugger is running, the PB6 and PB7 values that the software reads may be set using the Pin Emulation feature of the debugger.

PB3 is driven by the debugger only to bring the AX8052F151 out of Deep Sleep. It is high impedance otherwise.

The 32 kHz crystal is optional, the fast crystal at pins CLK16N and CLK16P is used as reference frequency for the RF RX/TX. Crystal load capacitances should be chosen according to the crystal's datasheet. At pins CLK16N and CLK16P they the internal programmable capacitors may be used, at pins PA3 and PA4 capacitors must be connected externally.

It is mandatory to add 1 μF (low ESR) between VREG and GND. Decoupling capacitors are not all drawn. It is recommended to add 100 nF decoupling capacitor for every VDDA and VDD_IO pin. In order to reduce noise on the antenna inputs it is recommended to add 27 pF on the VDD pins close to the antenna interface.

The AX8052F151 has an integrated voltage regulator for the analog supply voltages, which generates a stable supply voltage VREG from the voltage applied at VDD_IO. Use VREG to supply all the VDDA supply pins and also to DC power to the pins ANTP and ANTN.

Antenna Interface Circuitry

The ANTP and ANTN pins provide RF input to the LNA when AX8052F151 is in receiving mode, and RF output from the PA when AX8052F151 is in transmitting mode. A small antenna can be connected with an optional translation network. The network must provide DC power to the PA and LNA. A biasing to VREG is necessary.

Beside biasing and impedance matching, the proposed networks also provide low pass filtering to limit spurious emission.

Single−ended Antenna Interface

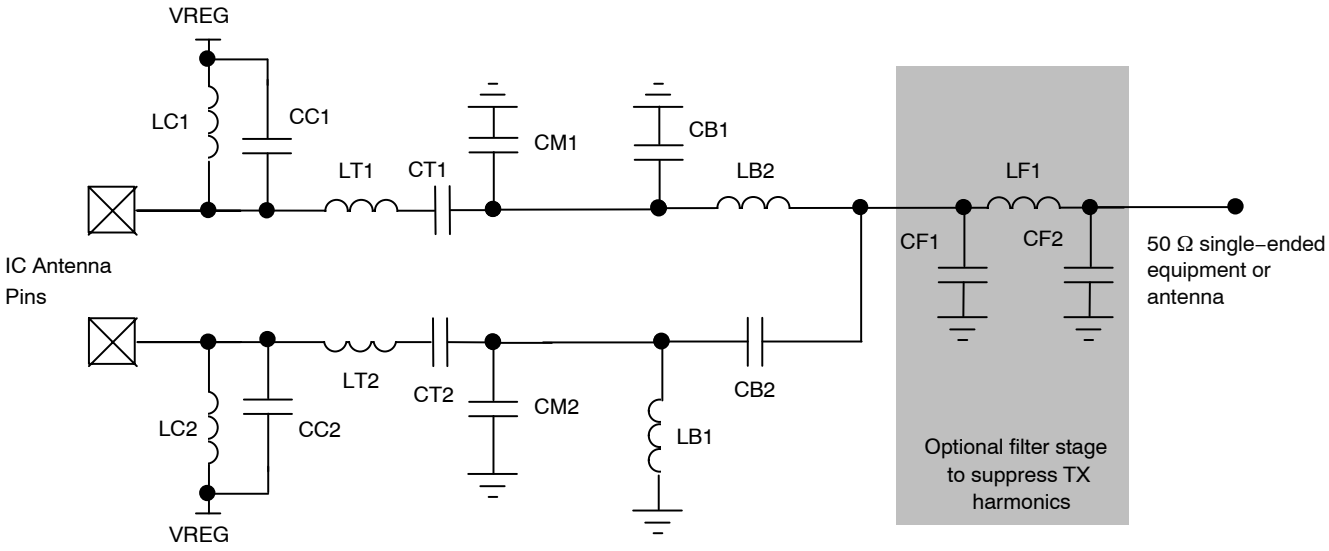


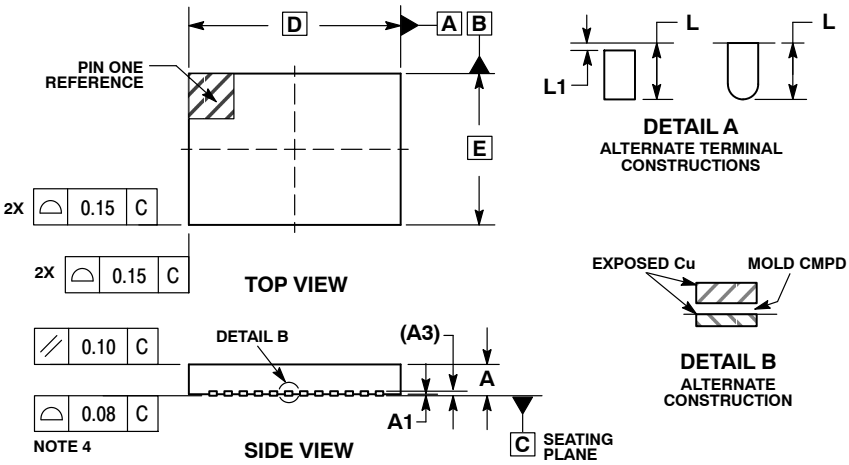
Figure 10. Structure of the Antenna Interface to 50 Ω Single−ended Equipment or Antenna

Table 25.

Frequency Band	LC1,2 [nH]	CC1,2 [pF]	LT1,2 [nH]	CT1,2 [pF]	CM1,2 [pF]	LB1,2 [nH]	CB1,2 [pF]	LF1 [nH]	CF1,2 [pF]
868 / 915 MHz	68	0.9	12	18	2.4	12	2.7	0 Ω	NC
433 MHz	120	2.2	39	7.5	6.0	27	5.2	0 Ω	NC

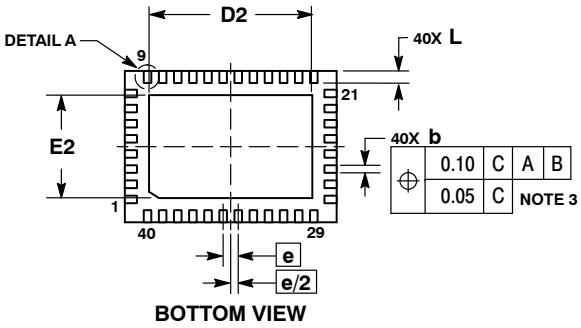
QFN40 PACKAGE INFORMATION

QFN40 7x5, 0.5P
CASE 485EG
ISSUE A

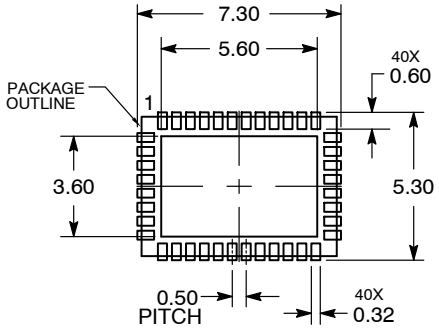


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	7.00 BSC	
D2	5.30	5.50
E	5.00 BSC	
E2	3.30	3.50
e	0.50 BSC	
L	0.30	0.50
L1	---	0.15



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

QFN40 Soldering Profile

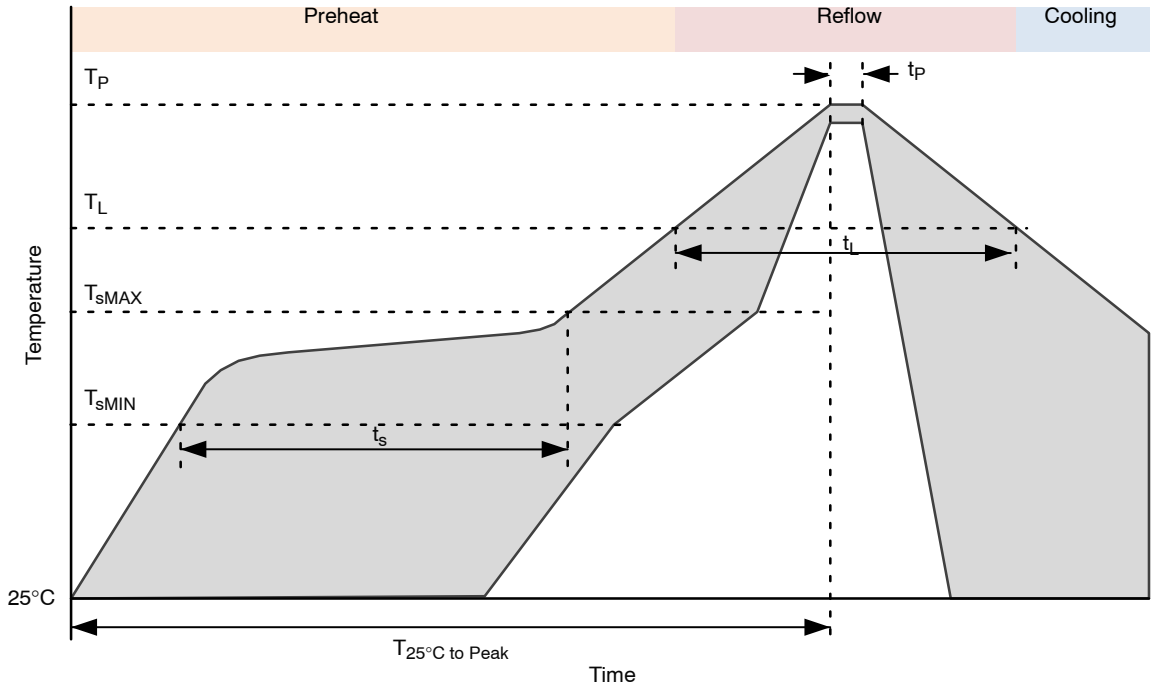


Figure 11. QFN40 Soldering Profile

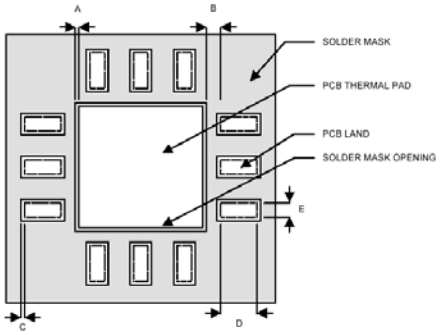
Table 26.

Profile Feature		Pb−Free Process
Average Ramp−Up Rate		3°C/s max.
Preheat Preheat		
Temperature Min	T_{sMIN}	150°C
Temperature Max	T_{sMAX}	200°C
Time (T_{sMIN} to T_{sMAX})	t_s	60 − 180 sec
Time 25°C to Peak Temperature	$T_{25°C\ to\ Peak}$	8 min max.
Reflow Phase		
Liquidus Temperature	T_L	217°C
Time over Liquidus Temperature	t_L	60 − 150 s
Peak Temperature	t_p	260°C
Time within 5°C of actual Peak Temperature	T_p	20 − 40 s
Cooling Phase		
Ramp−down rate		6°C/s max.

1. All temperatures refer to the top side of the package, measured on the the package body surface.

QFN40 Recommended Pad Layout

1. PCB land and solder masking recommendations are shown in Figure 12.



A = Clearance from PCB thermal pad to solder mask opening, 0.0635 mm minimum
B = Clearance from edge of PCB thermal pad to PCB land, 0.2 mm minimum
C = Clearance from PCB land edge to solder mask opening to be as tight as possible to ensure that some solder mask remains between PCB pads.
D = PCB land length = QFN solder pad length + 0.1 mm
E = PCB land width = QFN solder pad width + 0.1 mm

Figure 12. PCB Land and Solder Mask Recommendations

2. Thermal vias should be used on the PCB thermal pad (middle ground pad) to improve thermal conductivity from the device to a copper ground plane area on the reverse side of the printed circuit board. The number of vias depends on the package thermal requirements, as determined by thermal simulation or actual testing.
3. Increasing the number of vias through the printed circuit board will improve the thermal conductivity to the reverse side ground plane and external heat sink. In general, adding more metal through the PC board under the IC will improve operational heat transfer, but will require careful attention to uniform heating of the board during assembly.

Assembly Process

Stencil Design & Solder Paste Application

1. Stainless steel stencils are recommended for solder paste application.
2. A stencil thickness of 0.125 – 0.150 mm (5 – 6 mils) is recommended for screening.
3. For the PCB thermal pad, solder paste should be printed on the PCB by designing a stencil with an array of smaller openings that sum to 50% of the QFN exposed pad area. Solder paste should be applied through an array of squares (or circles) as shown in Figure 13.
4. The aperture opening for the signal pads should be between 50−80% of the QFN pad area as shown in Figure 14.
5. Optionally, for better solder paste release, the aperture walls should be trapezoidal and the corners rounded.
6. The fine pitch of the IC leads requires accurate alignment of the stencil and the printed circuit board. The stencil and printed circuit assembly should be aligned to within + 1 mil prior to application of the solder paste.
7. No−clean flux is recommended since flux from underneath the thermal pad will be difficult to clean if water−soluble flux is used.

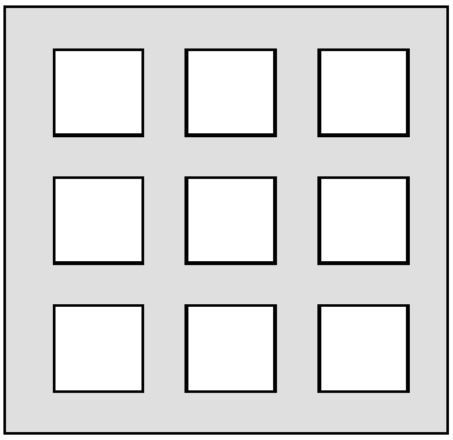


Figure 13. Solder Paste Application on Exposed Pad

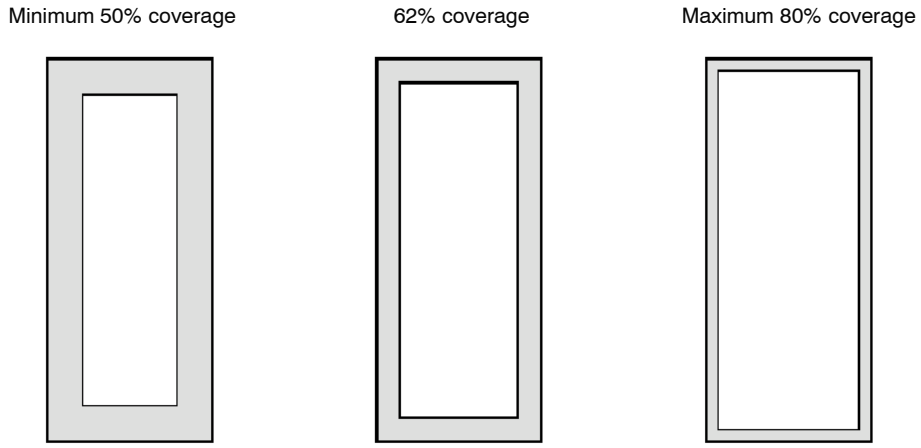


Figure 14. Solder Paste Application on Pins

Table 27. DEVICE VERSIONS

Device Marking	AX8052 Version	AX5051 Version
AX8052F151−1	1	1
AX8052F151−2	1C	1

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