Product Technical Specification

AirPrime HL7688



SIERRA WIRELESS®

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1. Introduction

This document is the Product Technical Specification for the AirPrime HL7688 Embedded Module. It defines the high level product features and illustrates the interfaces for these features. This document is intended to cover the hardware aspects of the product, including electrical and mechanical.

The AirPrime HL7688 belongs to the AirPrime HL Series from Essential Connectivity Module family. These are industrial grade Embedded Wireless Modules that provide data connectivity on wireless networks (as listed in Table 1 Supported Bands/Connectivity).

The HL7688 supports a large variety of interfaces such as USB 2.0, UART and GPIOs to provide customers with the highest level of flexibility in implementing high-end solutions.

Table 1. Supported Bands/Connectivity

RF Band	Transmit Band (Tx)	Receive Band (Rx)	Maximum Output Power
LTE B2	1850 to 1910 MHz	1930 to 1990 MHz	23 dBm (+/- 2dBm) Class 3bis
LTE B4	1710 to 1755 MHz	2110 to 2155 MHz	23 dBm (+/- 2dBm) Class 3bis
LTE B5	824 to 849 MHz	869 to 894 MHz	23 dBm (+/- 2dBm) Class 3bis
LTE B17	704 to 716 MHz	734 to 746 MHz	23 dBm (+/- 2dBm) Class 3bis
UMTS B2	1850 to 1910 MHz	1930 to 1990 MHz	23 dBm (+/- 2dBm) Class 3bis
UMTS B5	824 to 849 MHz	869 to 894 MHz	23 dBm (+/- 2dBm) Class 3bis

1.1. Common Flexible Form Factor (CF^3)

The AirPrime HL7688 belongs to the Common Flexible Form Factor (CF^3) family of modules. This family consists of a series of WWAN modules that share the same mechanical dimensions (same width and length with varying thicknesses) and footprint. The CF^3 form factor provides a unique solution to a series of problems faced commonly in the WWAN module space as it:

- Accommodates multiple radio technologies (from 2G to LTE advanced) and band groupings
- Supports bit-pipe (Essential Module Series) and value add (Smart Module Series) solutions
- Offers electrical and functional compatibility
- Provides Direct Mount as well as Socketability depending on customer needs

1.2. Physical Dimensions

AirPrime HL7688 modules are compact, robust, fully shielded modules with the following dimensions:

- Length: 23 mm
- Width: 22 mm
- Thickness: 2.5 mm
- Weight: 3.5 g

Note: Dimensions specified above are typical values.

1.3. General Features

The table below summarizes the AirPrime HL7688 features.

Table 2. General Features

Feature	Description
Physical	• Small form factor (146-pad solderable LGA pad) – 23mm x 22mm x 2.5mm (nominal) • Complete body shielding • RF connection pads (RF main interface) • Baseband signals connection
Electrical	Single or double supply voltage (VBATT and VBATT_PA) – 3.2V – 4.5V
RF	• Quad-band LTE: ▪ LTE B2: 1900 PCS ▪ LTE B4: 1700 AWS ▪ LTE B5: 850 CLR ▪ LTE B17: 700 • Dual-band UMTS: ▪ UMTS B2: 1900 PCS ▪ UMTS B5: 850 CLR
SIM interface	• Dual SIM Single Standby (DSSS) • 1.8V/3V support • SIM extraction / hot plug detection • SIM/USIM support • Conforms with ETSI UICC Specifications • Supports SIM application tool kit with proactive SIM commands
Application interface	• NDIS NIC interface support (Windows XP, Windows 7, Windows 8, Windows CE, Linux) • Multiple non-multiplexed USB channel support • Dial-up networking • USB selective suspend to maximize power savings • CMUX multiplexing over UART* • AT command interface – 3GPP 27.007 standard, plus proprietary extended AT commands

Feature	Description
Protocol Stack	• Single mode LTE operation: ▪ LTE FDD, bandwidth 1.4-20 MHz ▪ System Release: 3GPP Rel. 9 ▪ Category 1 (up to 10 Mbit/s in downlink, 5 Mbit/s in uplink) ▪ Rx Diversity ▪ Max modulation 64 QAM DL, 16 QAM UL ▪ Intra-frequency and inter-frequency mobility ▪ SMS over SGs and IMS ▪ SON ANR ▪ Public Warning System PWS • HSDPA (High Speed Downlink Packet Access) ▪ Evolved High Speed Downlink Packet Access (HSDPA+) ▪ Compliant with 3GPP Release 9 ▪ Up to Category 24 (DC, 42.2Mbps) ▪ Continuous Packet Connectivity (CPC) ▪ Enhance fractional DPCH ▪ IPv6 support • HSUPA (High Speed Uplink Packet Access) ▪ Compliant with 3GPP Release 9 ▪ Category 7 (11.5Mbps) ▪ Robust Header Compression (RoHC) • RXDIV Performance Enhancements ▪ Type 3i (HSDPA) • HSPA Enhancements ▪ MAC-ehs Rel. 7 ▪ HSDPA Enhanced CELL_FACH/PCH states ▪ HSUPA Enhanced CELL_FACH states (eFACH) Rel 8 ▪ MAC-i/is Rel.8 ▪ Serving cell change enhancements Rel. 8
SMS	• SMS over SGs and IMS • SMS MO and MT • SMS saving to SIM card or ME storage • SMS reading from SIM card or ME storage • SMS sorting • SMS concatenation • SMS Status Report • SMS replacement support • SMS storing rules (support of **AT+CNMI**, **AT+CNMA**)

Feature	Description
Connectivity	• Multiple (up to 20) cellular packet data profiles • Sleep mode for minimum idle power draw • Mobile-originated PDP context activation / deactivation • Support QoS profile ▪ Release 97 – Precedence Class, Reliability Class, Delay Class, Peak Throughput, Mean Throughput ▪ Release 99 QoS negotiation – Background, Interactive, and Streaming • Static and Dynamic IP address. The network may assign a fixed IP address or dynamically assign one using DHCP (Dynamic Host Configuration Protocol). • Supports PAP and CHAP authentication protocols • PDP context type (IPv4, IPv6, IPv4v6). IP Packet Data Protocol context • RFC1144 TCP/IP header compression
Environmental	Operating temperature ranges (industrial grade): • Class A: -30°C to +70°C • Class B: -40°C to +85°C
RTC	Real Time Clock (RTC) with calendar

1.4. Architecture

The figure below presents an overview of the AirPrime HL7688's internal architecture and external interfaces.

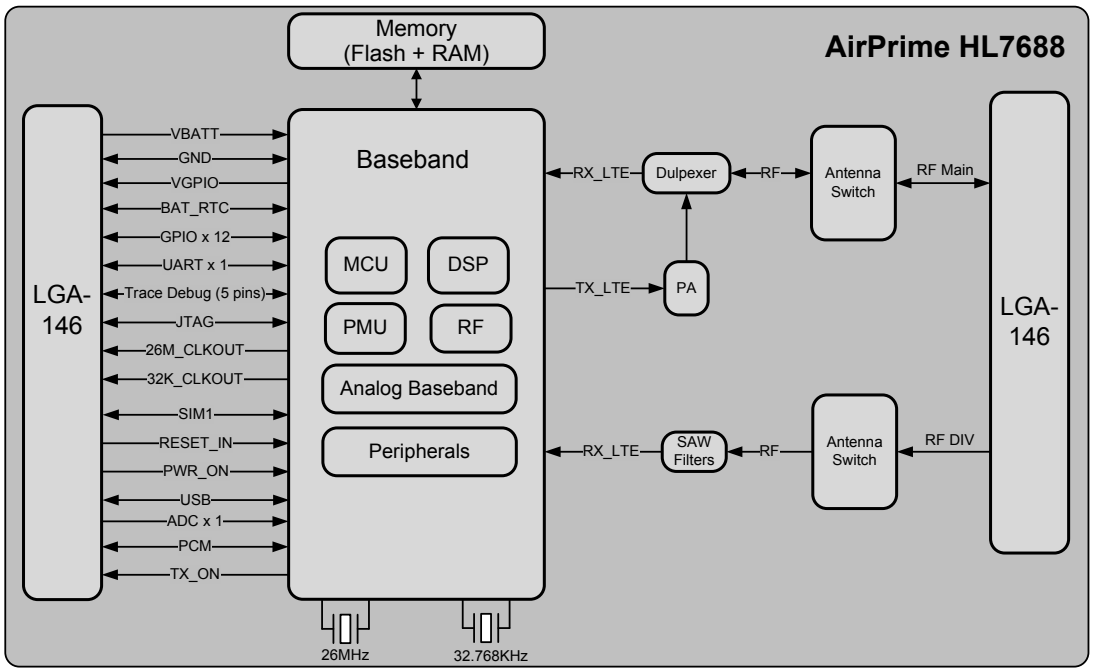


Figure 1. Architecture Overview

1.5. Interfaces

The AirPrime HL7688 module provides the following interfaces and peripheral connectivity:

- 1x – 8-wire UART
- 1x – Active Low RESET
- 1x – USB 2.0
- 1x – Backup Battery Interface
- 2x – System Clock Out
- 1x – Active Low POWER-ON
- 1x – 1.8V/3V SIM
- 1x – JTAG Interface
- 12x – GPIOs (2 of which have multiplexes)
- 1x – Main Antenna
- 1x – RX Diversity Antenna
- 1x – VGPIO
- 1x – TX_ON
- 1x – ADC
- 1x – PCM
- 1x – Debug Interface

1.6. Connection Interface

The AirPrime HL7688 module is an LGA form factor device. All electrical and mechanical connections are made through the 146 Land Grid Array (LGA) pads on the bottom side of the PCB.

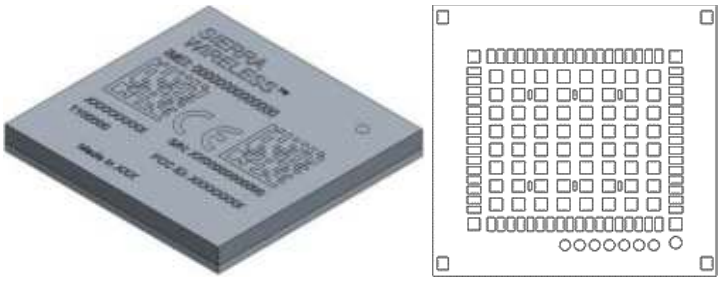


Figure 2. Mechanical Overview

The 146 pads have the following distribution:

- 66 inner signal pads, 1x0.5mm, pitch 0.8mm
- 1 reserved test point (do not connect), 1.0mm diameter
- 7 test point (JTAG), 0.8mm diameter, 1.20mm pitch
- 64 inner ground pads, 1.0x1.0mm, pitch 1.825mm/1.475mm
- 4 inner corner ground pads, 1x1mm
- 4 outer corner ground pads, 1x0.9mm

1.7. ESD

Refer to the following table for ESD Specifications.

Note: Information specified in the following table is preliminary and subject to change.

Table 3. ESD Specifications

Category	Connection	Specification
Operational	RF ports	IEC-61000-4-2 – Level (Electrostatic Discharge Immunity Test)
Non-operational	Host connector interface	Unless otherwise specified: • JESD22-A114 +/- 1kV Human Body Model • JESD22-A115 +/- 200V Machine Model • JESD22-C101C +/- 250V Charged Device Model
Signals	SIM connector	Adding ESD protection is highly recommended at the point where the USIM contacts are exposed, and for any other signals that would be subjected to ESD by the user.
	Other host signals	

1.8. Environmental and Certifications

1.8.1. Environmental Specifications

The environmental specification for both operating and storage conditions are defined in the table below.

Table 4. Environmental Specifications

Conditions	Range
Operating Class A	-30°C to +70°C
Operating Class B	-40°C to +85°C
Storage	-40°C to +85°C

Class A is defined as the operating temperature ranges that the device:

- Shall exhibit normal function during and after environmental exposure.
- Shall meet the minimum requirements of 3GPP or appropriate wireless standards.

Class B is defined as the operating temperature ranges that the device:

- Shall remain fully functional during and after environmental exposure
- Shall exhibit the ability to establish an SMS or DATA call (emergency call) at all times even when one or more environmental constraint exceeds the specified tolerance.
- Unless otherwise stated, full performance should return to normal after the excessive constraint(s) have been removed.

1.8.2. Regulatory

The AirPrime HL7688 is compliant with FCC regulations.

FCC compliance will be reflected on the AirPrime HL7688 label.

Table 5. Regulation Compliance

Document	Current Version	Description
GCF-CC	v3.56.1 or later	GCF Conformance Certification Criteria
NAPRD.03	V5.22 or later	North American Program Reference Document
FCC Part 22, 24, 27	NA	Federal Communications Commission

1.8.3. RoHS Directive Compliant

The AirPrime HL7688 module is compliant with RoHS Directive 2011/65/EU which sets limits for the use of certain restricted hazardous substances. This directive states that “from 1st July 2006, new electrical and electronic equipment put on the market does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE)”.

1.8.4. Disposing of the Product

This electronic product is subject to the EU Directive 2012/19/EU for Waste Electrical and Electronic Equipment (WEEE). As such, this product must not be disposed of at a municipal waste collection point. Please refer to local regulations for directions on how to dispose of this product in an environmental friendly manner.



1.9. References

[1] AirPrime HL Series Customer Process Guidelines
Reference Number: 4114330

[2] AirPrime HL7688 AT Commands Interface Guide
Reference Number: TBD

2. Pad Definition

AirPrime HL7688 pads are divided into 3 functional categories.

- **Core functions and associated pads** cover all the mandatory features for M2M connectivity and will be available by default across all CF[3] family of modules. These Core functions are always available and always at the same physical pad locations. A customer platform using only these functions and associated pads is guaranteed to be forward and/or backward compatible with the next generation of CF[3] modules.
- **Extension functions and associated pads** bring additional capabilities to the customer. Whenever an Extension function is available on a module, it is always at the same pad location.
- **Custom functions and associated pads** are specific to a given module, and make an opportunistic use of specific chipset functions and I/Os. Custom features should be used with caution as there is no guarantee that the custom functions available on a given module will be available on other CF[3] modules.

Other pads marked as “not connected” or “reserved” should not be used.

Table 6. Pad Definition

Pad #	Signal Name	Function	I/O	Active Low / High	Power Supply Domain	Recommendation for Unused Pads	Type
1	GPIO1	General purpose input/output	I/O		1.8V	Left Open	Extension
2	UART1_RI / TRACE_DATA3	UART1 Ring indicator / Trace data 3	O		1.8V	Connect to test point	Core / Custom
3	UART1_RTS	UART1 Request to send	I	L	1.8V	Connect to test point	Core
4	UART1_CTS	UART1 Clear to send	O	L	1.8V	Connect to test point	Core
5	UART1_TX	UART1 Transmit data	I		1.8V	Connect to test point	Core
6	UART1_RX	UART1 Receive data	O		1.8V	Connect to test point	Core
7	UART1_DTR	UART1 Data terminal ready	I	L	1.8V	Connect to test point	Core
8	UART1_DCD / TRACE_DATA1	UART1 Data carrier detect / Trace data 1	O	L	1.8V	Connect to test point	Core / Custom

Pad #	Signal Name	Function	I/O	Active Low / High	Power Supply Domain	Recommendation for Unused Pads	Type
9	UART1_DSR / TRACE_DATA0	UART1 Data set ready / Trace data 0	O	L	1.8V	Connect to test point	Core / Custom
10	GPIO2 / TRACE_DATA2	General purpose input/output / Trace data 2	I/O		1.8V	Connect to test point	Core / Custom
11	RESET_IN_N	Input reset signal	I	L	1.8V	Left Open	Core
12	USB_D-	USB Data Negative (Low / Full Speed)	I/O		3.3V	Connect to test point	Extension
		USB Data Negative (High Speed)			0.38V		
13	USB_D+	USB Data Positive (Low / Full Speed)	I/O		3.3V	Connect to test point	Extension
		USB Data Positive (High Speed)			0.38V		
14	NC	Not Connected (Reserved for future use)				Left Open	Not connected
15	NC	Not Connected (Reserved for future use)				Left Open	Not connected
16	USB_VBUS	USB VBUS	I		5V	Connect to test point	Extension
17	NC	Not Connected (Reserved for future use)				Left Open	Not connected
18	NC	Not Connected (Reserved for future use)				Left Open	Not connected
19	NC	Not Connected (Reserved for future use)				Left Open	Not connected
20	NC	Not Connected (Reserved for future use)				Left Open	Not connected
21	BAT_RTC	Power supply for RTC backup	I/O		1.8V	Left Open	Extension
22	26M_CLKOUT	26MHz System Clock Output	O		1.8V	Left Open	Extension
23	32K_CLKOUT	32.768kHz System Clock Output	O		1.8V	Left Open	Extension
24	ADC1	Analog to digital converter	I		1.2V	Left Open	Extension
25	NC	Not Connected (Reserved for future use)				Left Open	Not connected
26	UIM1_VCC	1.8V/3V SIM1 Power supply	O		1.8V/3V	Mandatory connection	Core
27	UIM1_CLK	1.8V/3V SIM1 Clock	O		1.8V/3V	Mandatory connection	Core
28	UIM1_DATA	1.8V/3V SIM1 Data	I/O		1.8V/3V	Mandatory connection	Core

Pad #	Signal Name	Function	I/O	Active Low / High	Power Supply Domain	Recommendation for Unused Pads	Type
29	UIM1_RESET	1.8V/3V SIM1 Reset	O	L	1.8V/3V	Mandatory connection	Core
30	GND	Ground	0V		0V	Mandatory connection	Extension
31	RF_DIV	RF Input - Diversity				Mandatory connection	Extension
32	GND	Ground	0V		0V	Mandatory connection	Extension
33	PCM_OUT	PCM data out	O		1.8V	Left Open	Extension
34	PCM_IN	PCM data in	I		1.8V	Left Open	Extension
35	PCM_SYNC	PCM sync out	I/O		1.8V	Left Open	Extension
36	PCM_CLK	PCM clock	I/O		1.8V	Left Open	Extension
37	GND	Ground	0V		0V	Mandatory connection	Core
38	NC	Not Connected (Reserved for future use)				Left Open	Not connected
39	GND	Ground	0V		0V	Mandatory connection	Core
40	GPIO7	General purpose input/output	I/O		1.8V	Left Open	Core
41	GPIO8 / TRACE_CLK	General purpose input/output / Trace clock	I/O		1.8V	Connect to test point	Core/Custom
42	NC	Not Connected (Reserved for future use)				Left Open	Not connected
43	NC	Not Connected (Reserved for future use)				Left Open	Not connected
44	GPIO13	General purpose input/output	O		1.8V	Left Open	Extension
45	VGPIO	GPIO voltage output	O		1.8V	Left Open	Core
46	GPIO6	General purpose input/output	I/O		1.8V	Left Open	Core
47	NC	Not Connected (Reserved for future use)				Left Open	Not connected
48	GND	Ground	0V		0V	Mandatory connection	Core

Pad #	Signal Name	Function	I/O	Active Low / High	Power Supply Domain	Recommendation for Unused Pads	Type
49	RF_MAIN	RF Input/output				Mandatory connection	Core
50	GND	Ground	0V		0V	Mandatory connection	Core
51	GPIO14	General purpose input/output	I		1.8V	Left Open	Extension
52	GPIO10	General purpose input/output	I/O		1.8V	Left Open	Extension
53	GPIO11	General purpose input/output	I/O		1.8V	Left Open	Extension
54	GPIO15	General purpose input/output	I/O		1.8V	Left Open	Extension
55	NC	Not Connected (Reserved for future use)				Left Open	Not connected
56	NC	Not Connected (Reserved for future use)				Left Open	Not connected
57	NC	Not Connected (Reserved for future use)				Left Open	Not connected
58	NC	Not Connected (Reserved for future use)				Left Open	Not connected
59	PWR_ON	Active Low Power On control signal	I	L	1.8V	Mandatory connection	Core
60	TX_ON	TX indicator	O		2.3V	Left Open	Extension
61	VBATT_PA	Power supply (refer to section 3.1 Power Supply for more information)	I		3.2V (min) 3.7V (typ) 4.5V (max)	Mandatory connection	Core
62	VBATT_PA	Power supply (refer to section 3.1 Power Supply for more information)	I		3.2V (min) 3.7V (typ) 4.5V (max)	Mandatory connection	Core
63	VBATT	Power supply	I		3.2V (min) 3.7V (typ) 4.5V (max)	Mandatory connection	Core
64	UIM1_DET	UIM1 Detection	I/O	H	1.8V	Left Open	Core
65	GPIO4	General purpose input/output	I/O	H	1.8V	Left Open	Extension
66	GPIO5	General purpose input/output	I/O		1.8V	Left Open	Extension
67-70	GND	Ground	GND		0V		Core

Pad #	Signal Name	Function	I/O	Active Low / High	Power Supply Domain	Recommendation for Unused Pads	Type
71 - 166	*Note: These pads are not available on the AirPrime HL7688 module.*						
167 - 234	GND	Ground	GND		0V		Core
236	JTAG_RESET	JTAG RESET	I	L	1.8V	Left Open	Extension
237	JTAG_TCK	JTAG Test Clock	I		1.8V	Left Open	Extension
238	JTAG_TDO	JTAG Test Data Output	O		1.8V	Left Open	Extension
239	JTAG_TMS	JTAG Test Mode Select	I		1.8V	Left Open	Extension
240	JTAG_TRST	JTAG Test Reset	I	L	1.8V	Left Open	Extension
241	JTAG_TDI	JTAG Test Data Input	I		1.8V	Left Open	Extension
242	JTAG_RTCK	JTAG Returned Test Clock	O		1.8V	Left Open	Extension

2.1. Pad Configuration (Top View, Through Module)

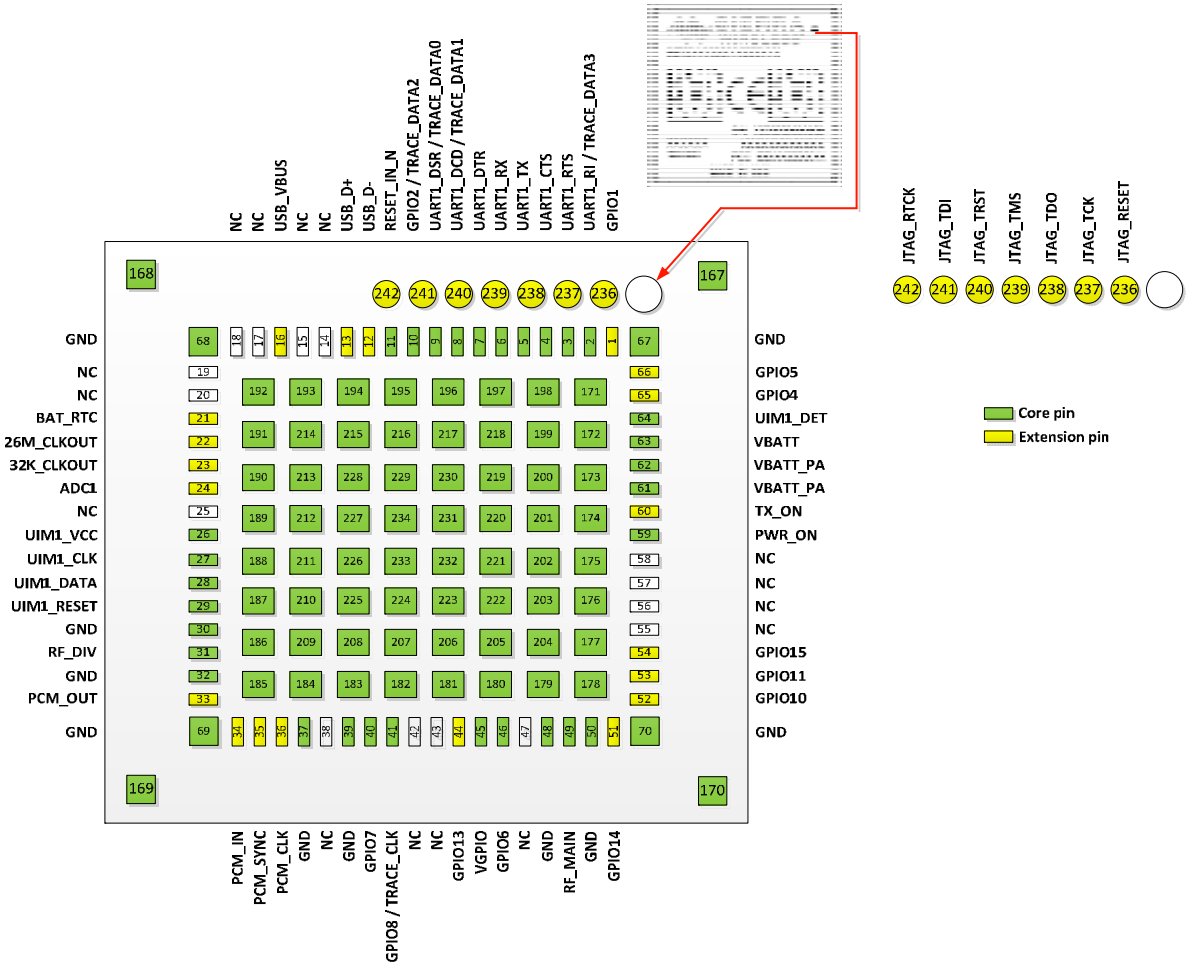


Figure 3. Pad Configuration

3. Detailed Interface Specifications

Note: If not specified, all electrical values are given for VBATT=3.7V and an operating temperature of 25°C.

For standard applications, VBATT and VBATT_PA must be tied externally to the same power supply. For some specific applications, AirPrime HL7688 modules support separate VBATT and VBATT_PA connection if requirements below are fulfilled.

3.1. Power Supply

The AirPrime HL7688 modules is supplied through the VBATT signal with the following characteristics.

Table 7. Power Supply

Supply	Minimum	Typical	Maximum
VBATT voltage (V)	3.2*	3.7	4.5
VBATT_PA voltage (V) Full Specification	3.2*	3.7	4.5
VBATT_PA voltage (V) Extended Range	2.8	3.7	4.5

* This value has to be guaranteed during the burst.

Note: Load capacitance for VBATT is around 32µF ± 20% embedded inside the module.
Load capacitance for VBATT_PA is around 10µF ± 20% embedded inside the module.

3.2. Current Consumption

The following table lists the current consumption of the AirPrime HL7688 at different conditions.

Note: The following data is with USB disconnected to achieve the lowest current consumption. An additional 0.6mA will be consumed if USB is connected.

Typical values are defined for VBATT/VBATT_PA at 3.7V and 25°C, for 50Ω impedance at all RF ports. Maximum values are provided for VSWR3:1 with worst conditions among supported ranges of voltages and temperature.

Table 8. Current Consumption

Parameter		Minimum	Typical	Maximum	Unit
Off mode		95	110	202	µA
Sleep mode – LTE DRX = 1.28s USB = disconnected	Band 2	1.2	1.4	6.2	mA
	Band 4	1.2	1.4	6.2	mA
	Band 5	1.2	1.4	6.2	mA
	Band 17	1.2	1.4	6.2	mA

Parameter		Minimum	Typical	Maximum	Unit
LTE in communication mode (TX Max)	Band 2	630	650	895	mA
	Band 4	510	610	945	mA
	Band 5	440	520	745	mA
	Band 17	540	560	780	mA
UMTS (TX Max)	Band 2	570	660	770	mA
	Band 5	400	460	500	mA

Table 9. Current Consumption per Power Supply

Parameter (at nominal voltage, 3.7 V)			Typical	Unit
VBATT_BB	LTE in communication mode (TX Max) USB = disconnected	Band 2	214	mA
		Band 4	207	mA
		Band 5	211	mA
		Band 17	218	mA
	UMTS (TX Max) USB = disconnected	Band 2	124	mA
		Band 5	118	mA
VBATT_PA	LTE in communication mode (TX Max) USB = disconnected	Band 2	436	mA
		Band 4	403	mA
		Band 5	309	mA
		Band 17	342	mA
	UMTS (TX Max) USB = disconnected	Band 2	536	mA
		Band 5	342	mA

3.3. VGPIO

The VGPIO output can be used to:

- Pull-up signals such as I/Os
- Supply the digital transistors driving LEDs

The VGPIO output is available when the AirPrime HL7688 module is switched ON.

Table 10. VGPIO Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Remarks
Voltage level (V)	1.7	1.8	1.9	Both active mode and sleep mode
Current capability Active Mode (mA)	-	-	50	Power management support up to 50mA output in Active mode
Current capability Sleep Mode (mA)	-	-	3	Power management support up to 3mA output in Sleep mode
Rise Time(ms)	-	-	1.5	Start-Up time from 0V

3.4. BAT_RTC

The AirPrime HL7688 module provides an input/output to connect a Real Time Clock power supply.

This pad is used as a back-up power supply for the internal Real Time Clock. The RTC is supported when VBATT is available but a back-up power supply is needed to save date and hour when VBATT is switched off.

If VBATT is available, the back-up battery can be charged by the internal 1.8V power supply regulator.

Table 11. BAT_RTC Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
Input voltage	-	1.8	-	V
Input current consumption	-	2.5 (TBC)	-	µA
Output voltage	-5%	1.8	+5%	V
Max charging current (@VBATT=3.7V)	-	25	-	mA

Note: When used with the HL Series snap-in socket, or when compatibility with HL6528x is needed, Sierra Wireless recommends adding a 10µF capacitor to the BAT_RTC pad.

3.5. SIM Interface

The AirPrime HL7688 has one physical SIM interface, UIM1, which has optional support for dual SIM application with an external SIM switch.

The UIM1 interface allows control of a 1.8V/3V SIM and is fully compliant with GSM 11.11 recommendations concerning SIM functions.

The five signals used by this interface are as follows:

- UIM1_VCC: power supply
- UIM1_CLK: clock
- UIM1_DATA: I/O port
- UIM1_RESET: reset
- UIM1_DET: SIM detection

Table 12. UIM1 Pad Description

Pad #	Signal Name	Description
26	UIM1_VCC	1.8V/3V SIM1 Power supply
27	UIM1_CLK	1.8V/3V SIM1 Clock
28	UIM1_DATA	1.8V/3V SIM1 Data
29	UIM1_RESET	1.8V/3V SIM1 Reset
64	UIM1_DET	UIM1 Detection

Table 13. Electrical Characteristics of UIM1

Parameter	Minimum	Typical	Maximum	Remarks
UIM1 Interface Voltage (V) (VCC,CLK,IO,RST)	-	2.9	-	The appropriate output voltage is auto detected and selected by software.
	-	1.80	-	
UIM1 Detect	-	1.80	-	High active
UIM1_VCC Current (mA)	-	-	10	Max output current in sleep mode = 3 mA
UIM1_VCC Line Regulation (mV/V)	-	-	50	At Iout_Max
UIM1_VCC Power-up Setting Time (µs) from power down	-	10	-	

3.5.1. UIM1_DET

UIM1_DET is used to detect and notify the application about the insertion and removal of a SIM device in the SIM socket connected to the SIM interface. When a SIM is inserted, the state of UIM1_DET transitions from logic 0 to logic 1. Inversely, when a SIM is removed, the state of UIM1_DET transitions from logic 1 to logic 0.

3.6. USB

The AirPrime HL7688 has one USB interface.

Table 14. USB Pad Description

Pad Number	Signal Name	I/O	Function
12	USB_D-	I/O	USB Data Negative
13	USB_D+	I/O	USB Data Positive
16	USB_VBUS	I	USB VBUS

Note: When the 5V USB supply is not available, connect USB_VBUS to VBATT to supply the USB interface.

3.7. Electrical Information for Digital I/O

The AirPrime HL7688 supports two groups of digital interfaces with varying current drain limits. The following list enumerates these interface groupings and the following table enumerates the electrical characteristics of each digital interface.

- Group 1 (6mA current drain limit)
  - GPIO2, GPIO4, GPIO6, GPIO8, GPIO10, GPIO11, GPIO13, GPIO14, GPIO15
- Group 2 (1mA current drain limit)
  - GPIO1, GPIO5, GPIO7
  - UART1
  - JTAG
  - PCM

Table 15. Digital I/O Electrical Characteristics

Parameter		Symbol	Minimum	Typical	Maximum	Remarks
Input Current-High(μA)		I_{IH}	-	-	240	
Input Current-Low(μA)		I_{IL}	-	-	240	
Group 1	DC Output Current-High (mA)	I_{OH}	-	-	6	
	DC Output Current-Low (mA)	I_{OL}	-6	-	-	
Group 2	DC Output Current-High (mA)	I_{OH}	-	-	1	
	DC Output Current-Low (mA)	I_{OL}	-1	-	-	
Input Voltage-High(V)		V_{IH}	1.19	-	2.10	
Input Voltage-Low(V)		V_{IL}	-0.20	-	0.38	
Output Voltage-High(V)		V_{OH}	1.35	-	-	I_{OH} = -6mA
		V_{OH}	1.50	-	-	I_{OH} = -0.1mA
Output Voltage-Low(V)		V_{OL}	-	-	0.35	I_{OH} = 6mA
		V_{OL}	-	-	0.2	I_{OH} = 0.1mA

3.8. General Purpose Input/Output (GPIO)

The AirPrime HL7688 module provides 12 GPIOs, 2 of which have multiplexes.

Table 16. GPIO Pad Description

Pad Number	Signal Name	Multiplex	I/O	Power Supply Domain
1	GPIO1		I/O	1.8V
10	GPIO2	TRACE_DATA2	I/O	1.8V
40	GPIO7		I/O	1.8V
41	GPIO8	TRACE_CLK	I/O	1.8V
44	GPIO13		I/O	1.8V
46	GPIO6		I/O	1.8V
51	GPIO14		I/O	1.8V
52	GPIO10		I/O	1.8V
53	GPIO11		I/O	1.8V
54	GPIO15		I/O	1.8V
65	GPIO4		I/O	1.8V
66	GPIO5		I/O	1.8V

3.9. Main Serial Link (UART1)

The main serial link (UART1) is used for communication between the AirPrime HL7688 module and a PC or host processor. It consists of a flexible 8-wire serial interface that complies with RS-232 interface.

The supported baud rates of the UART1 are 300, 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 500000, 750000, 921600, 1843200, 3000000 and 3250000 bit/s.

The signals used by UART1 are as follows:

- TX data (UART1_TX)
- RX data (UART1_RX)
- Request To Send (UART1_RTS)
- Clear To Send (UART1_CTS)
- Data Terminal Ready (UART1_DTR)
- Data Set Ready (UART1_DSR)
- Data Carrier Detect (UART1_DCD)
- Ring Indicator (UART1_RI)

Note: Signal names are according to PC view.

UART1 pad description is summarized in the table below.

Table 17. UART1 Pad Description

Pad #	Signal Name*	I/O*	Description
2	UART1_RI	O	Signal incoming calls (data only), SMS, etc.
3	UART1_RTS	I	Request to send
4	UART1_CTS	O	AirPrime HL7688 is ready to receive AT commands
5	UART1_TX	I	Transmit data
6	UART1_RX	O	Receive data
7	UART1_DTR	I (active low)	Prevents the AirPrime HL7688 from entering sleep mode, switches between data mode and command mode, and wakes the module up.
8	UART1_DCD	O	Signal data connection in progress
9	UART1_DSR	O	Signal UART interface is ON

* According to PC view.

3.10. POWER-ON Signal (PWR_ON_N)

A low level signal has to be provided to switch the AirPrime HL7688 module ON.

It is internally connected to the permanent 1.8V supply regulator inside the HL7688 via a pull-up resistor. Once VBAT is supplied to the HL7688 module, this 1.8V supply regulator will be enabled and so the PWR_ON_N signal is by default at high level.

The PWR_ON_N signal's characteristics are listed in the table below.

Table 18. PWR_ON_N Electrical Characteristics

Parameter	Minimum	Typical	Maximum
Input Voltage-Low (V)		-	0.51
Input Voltage-High (V)	1.33	-	2.2
Power-up period (ms) from PWR_ON_N falling edge	2000	-	-
PWR_ON_N assertion time (ms)	25		

Note: As PWR_ON_N is internally pulled up with 47kΩ, an open collector or open drain transistor must be used for ignition.

VGPIO is an output from the module that can be used to check if the module is active.

- When VGPIO = 0V, the module is OFF
- When VGPIO = 1.8V, the module is ON (it can be in idle, communication or sleep mode)

*Note: PWR_ON_N signal cannot be used to power the module off. To power the module off, use AT command **AT+CPWROFF**.*

3.11. Reset Signal (RESET_IN_N)

To reset the module, a low level pulse must be sent on the RESET_IN_N pad for 20ms. This action will immediately restart the AirPrime HL7688 module with the PWR_ON_N signal at low level. (If the PWR_ON_N signal is at high level, the module will be powered off.) As RESET_IN_N is internally pulled up, an open collector or open drain transistor has to be used to control this signal.

The RESET_IN_N signal will reset the registers of the CPU and reset the RAM memory as well, for the next power on.

Note: As RESET_IN_N is referenced to the VRTC (200kΩ pull-up resistor to VRTC 1.8V) an open collector or open drain transistor has to be used to control this signal.

Table 19. RESET_IN_N Electrical Characteristics

Parameter	Minimum	Typical	Maximum
Input Voltage-Low (V)		-	0.51
Input Voltage-High (V)	1.33	-	2.2
Reset assertion time (ms)	20	-	-
Power-up period (ms) from RESET_IN_N falling edge*	2000	-	-

* With the PWR_ON_N Signal at low level

3.12. Analog to Digital Converter (ADC1)

One Analog to Digital Converter input, ADC1, is provided by the AirPrime HL7688 module. This converter is a 10-bit resolution ADC ranging from 0 to 1.2V.

The following table describes the pad description of the ADC interface.

Table 20. ADC Interface Pad Description

Pad Number	Signal Name	I/O	Description
24	ADC1	I	Analog to digital converter

Typical ADC1 use is for monitoring external voltage; wherein an application is used to safely power OFF an external supply in case of overvoltage.

Table 21. ADC Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Remarks
ADC1 Resolution (bits)	-	10	-	
Input Voltage Range (V)	0	-	1.2	General purpose input
Update rate per channel (kHz)	-	-	125	
Integral Nonlinearity (bits)	-	-	±2	LSB
Offset Error (bits)	-	-	±1	LSB
Gain	849	853	858	
Input Resistance (MΩ)	1	-	-	
Input Capacitance (pF)	-	1	-	

3.13. Clock Interface

The AirPrime HL7688 module supports two digital clock interfaces.

The following table describes the pad description of the clock out interfaces.

Table 22. Clock Interface Pad Description

Pad Number	Signal Name	I/O	I/O Type	Description
22	26M_CLKOUT	O	1.8V	26MHz Digital Clock output
23	32K_CLKOUT	O	1.8V	32.768kHz Digital Clock output

Enabling or disabling the clock out feature can be done using AT commands. For more information about AT commands, refer to document [2] AirPrime HL7688 AT Commands Interface Guide.

3.14. PCM

The Digital Audio (PCM) Interface allows connectivity with standard audio peripherals. It can be used, for example, to connect an external audio codec.

The programmability of this interface allows addressing a large range of audio peripherals.

The signals used by the Digital Audio Interface are as follows:

- PCM_SYNC: The frame synchronization signal delivers an 8 kHz frequency pulse that synchronizes the frame data in and the frame data out.
- PCM_CLK: The frame bit clock signal controls data transfer with the audio peripheral.
- PCM_OUT: The frame “data out” relies on the selected configuration mode.
- PCM_IN: The frame “data in” relies on the selected configuration mode.

The PCM interface is a high speed full duplex interface that can be used to send and receive digital audio data to external audio ICs. The Digital Audio Interface also features the following:

- PCM master or slave
- 16 bits data word length, linear mode
- MSB first
- Configurable PCM bit clock rate on 256kHz, 384kHz or 512kHz
- Long frame sync

The following table describes the pad description of the PCM interface.

Table 23. PCM Interface Pad Description

Pad Number	Signal Name	I/O	Description
33	PCM_OUT	O	PCM data out
34	PCM_IN	I	PCM data in
35	PCM_SYNC	I/O	PCM sync out
36	PCM_CLK	I/O	PCM clock

Refer to the following table for the electrical characteristics of the digital audio interface.

Table 24. PCM Electrical Characteristics

Signal	Description	Minimum	Typical	Maximum	Unit
Tsync_low + Tsync_high	PCM-SYNC period		125		µs
Tsync_low	PCM-SYNC low time		62.5		µs
Tsync_high	PCM-SYNC high time		62.5		µs
TCLK-cycle	PCM-CLK period (T)	1.95	2.6	3.9	µs
TIN-setup	PCM-IN setup time	59.6			ns
TIN-hold	PCM-IN hold time	12			ns
TOUT-delay	PCM-OUT delay time			21.6	ns

Signal	Description	Minimum	Typical	Maximum	Unit
TSYNC-delay	PCM-SYNC output delay	-24		31.2	ns

The following figure shows the PCM timing waveform.

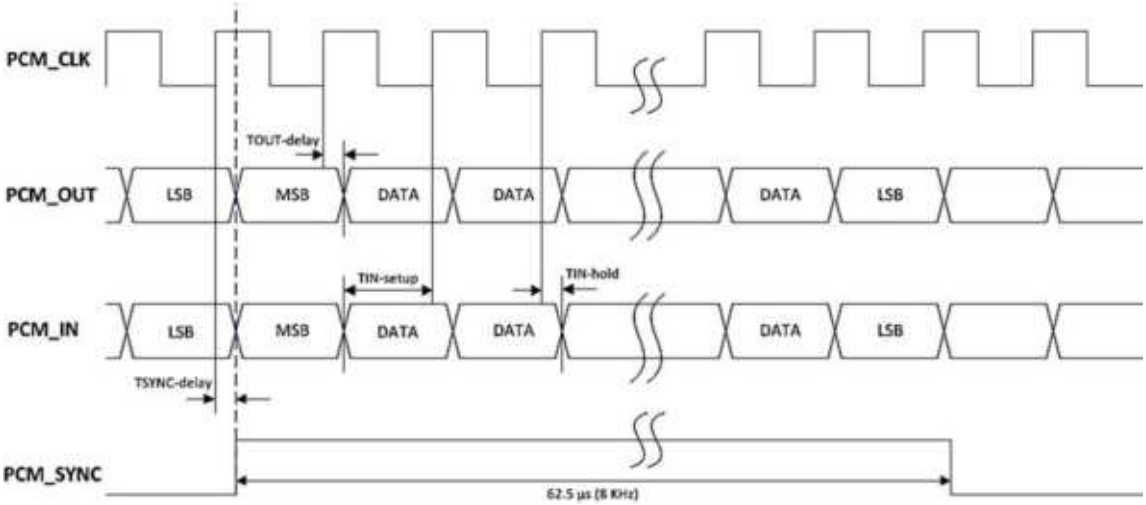


Figure 4. PCM Timing Waveform

3.15. Debug Interfaces

The AirPrime HL7688 module provides 2 interfaces for a powerful debug system.

3.15.1. Trace Debug

The AirPrime HL7688 module provides a Trace Debug interface, providing real-time instruction and data trace of the modem core.

Table 25. Trace Debug Pad Description

Pad Number	Signal Name	Function	Multiplex
2	TRACE_DATA3	Trace data 3	
8	TRACE_DATA1	Trace data 1	
9	TRACE_DATA0	Trace data 0	
10	TRACE_DATA2	Trace data 2	GPIO2
41	TRACE_CLK	Trace clock	GPIO8

Note: It is strongly recommended to provide access to this interface through Test Points.

3.15.2. JTAG

The JTAG interface provides debug access to the core of the AirPrime HL7688. These JTAG signals are accessible through solder-able test points.

Table 26. JTAG Pad Description

Pad Number	Signal Name	Function
236	JTAG_RESET	JTAG RESET
237	JTAG_TCK	JTAG Test Clock
238	JTAG_TDO	JTAG Test Data Output
239	JTAG_TMS	JTAG Test Mode Select
240	JTAG_TRST	JTAG Test Reset
241	JTAG_TDI	JTAG Test Data Input
242	JTAG_RTCK	JTAG Returned Test Clock

Note: It is recommended to provide access through Test Points to this interface the JTAG pads (for Failure Analysis debugging). All signals listed in table above shall be outputs on the customer board to allow JTAG debugging.

3.16. RF Interface

The RF interface of the HL7688 module allows the transmission of RF signals. This interface has a 50Ω nominal impedance.

3.16.1. RF Connection

A 50Ω stripline can be used to connect to standard RF connectors such as SMA, UFL, etc. for antenna connection.

Table 27. RF Main Connection

Pad Number	RF Signal	Impedance	VSWR Rx (max)	VSWR Tx (max)
49	RF_MAIN	50Ω	1.5:1	1.5:1

Table 28. RF Diversity Connection

Pad Number	RF Signal	Impedance	VSWR Rx (max)	VSWR Tx (max)
31	RF_DIV	50Ω	1.5:1	---

3.16.2. RF Performances

Note: Values in the tables below are preliminary and subject to change.

Table 29. Conducted RX Sensitivity – UMTS Bands

Frequency Band		Conducted Rx Sensitivity (dBm)	
		Primary (Typical)	Secondary (Typical)
Band 2	0.1% BER 12.2 kbps	-109.5	-110.0
Band 5		-110.0	-110.5

4G RF performances are compliant with 3GPP recommendation TS 36.101.

Table 30. Conducted RX Sensitivity – LTE Bands

Frequency Band		Conducted Rx Sensitivity (dBm)		
		Primary (Typical)	Secondary (Typical)	SIMO (Typical)
LTE B2	Full RB; BW: 20 MHz*	-93	-94	-97
LTE B4	Full RB; BW: 20 MHz*	-95	-95	-98
LTE B5	Full RB; BW: 10 MHz*	-98	-99	-101
LTE B17	Full RB; BW: 10 MHz*	-98	-99	-101

* Sensitivity values scale with bandwidth: x_MHz_Sensitivity = 10 MHz_Sensitivity – 10*log (10 MHz/x_MHz)

3.16.3. TX_ON Indicator (TX_ON)

The AirPrime HL7688 module provides a signal, TX_ON, for TX indication. The TX_ON is a 2.3V signal and its status signal depends on the module transmitter state.

Refer to the following table for the status of the TX_ON signal depending on the embedded module's state.

Table 31. TX_ON Indicator Pad Description

Pad Number	Signal Name	Function	I/O Type	Power Supply Domain
60	TX_ON	TX indicator	O	2.3V

Table 32. TX_ON Characteristics

Parameter	Minimum	Typical	Maximum
$T_{advance}$	30µs		
T_{delay}		10µs	

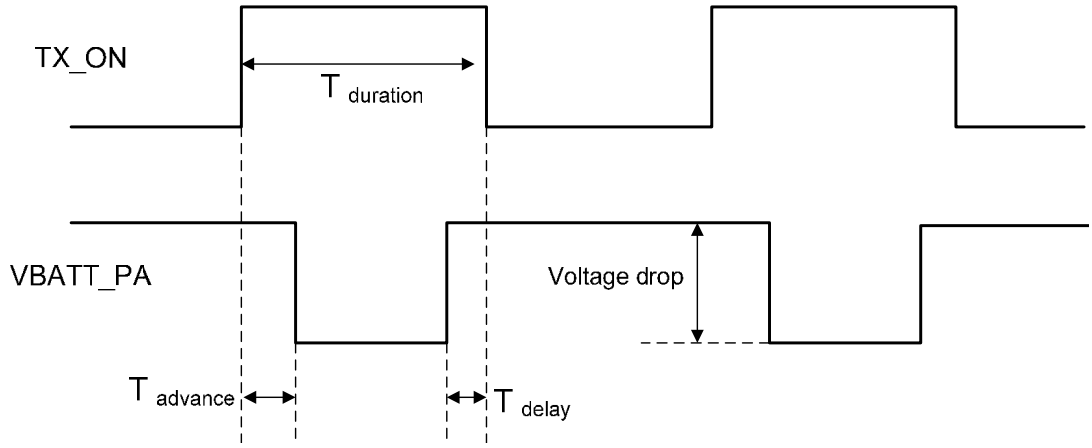


Figure 5. TX_ON State During Transmission

4. Mechanical Drawings

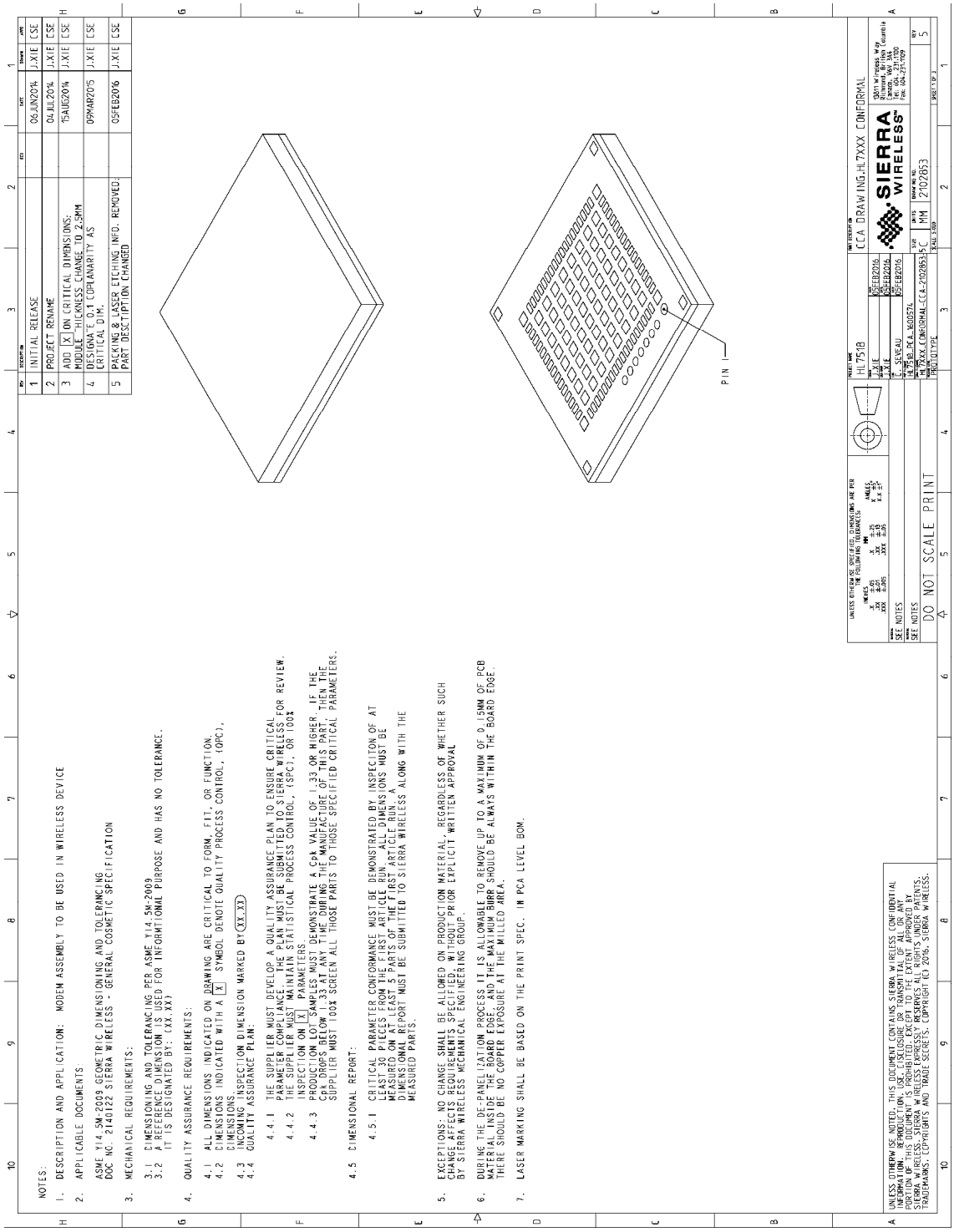


Figure 6. Mechanical Drawing

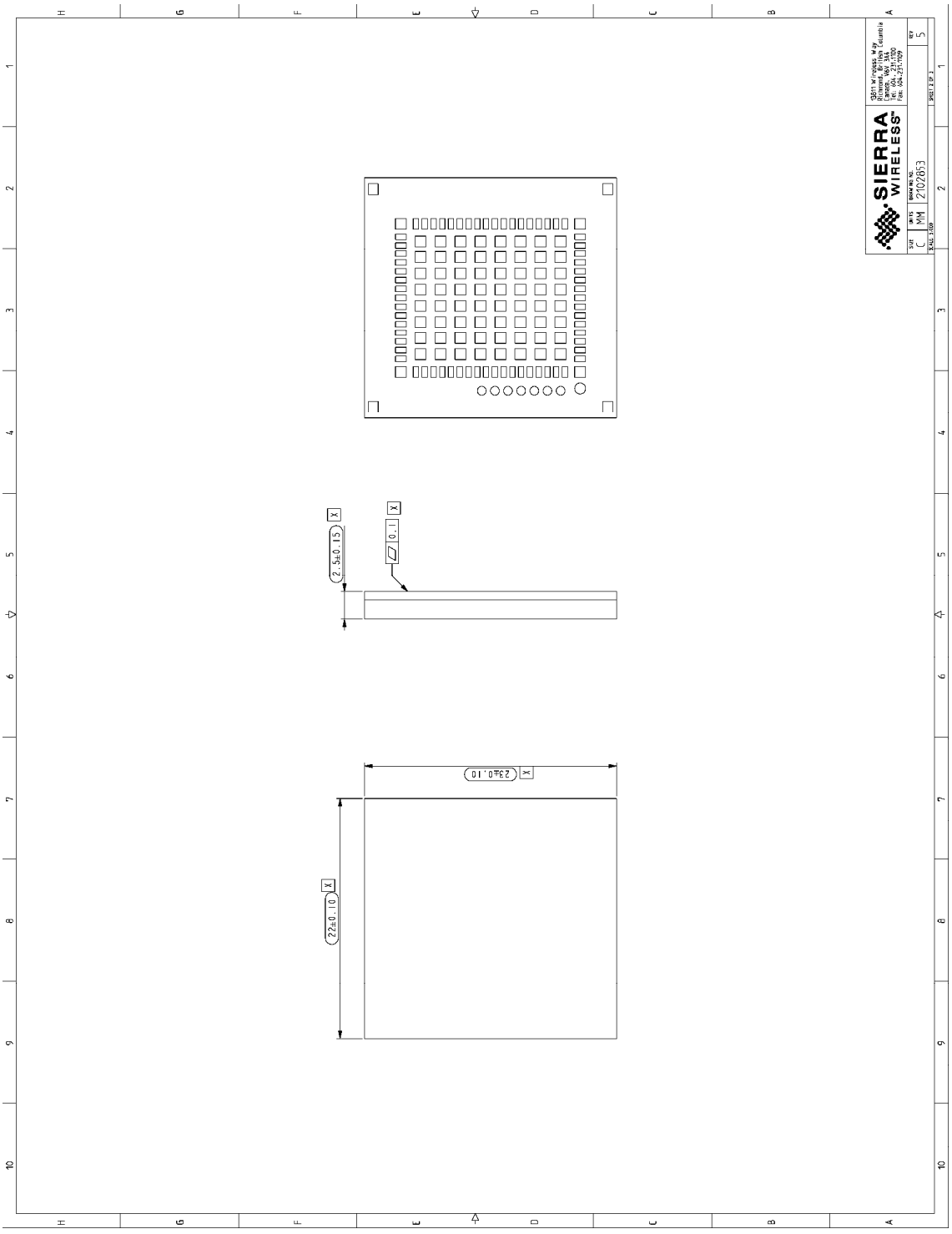


Figure 7. Dimensions Drawing

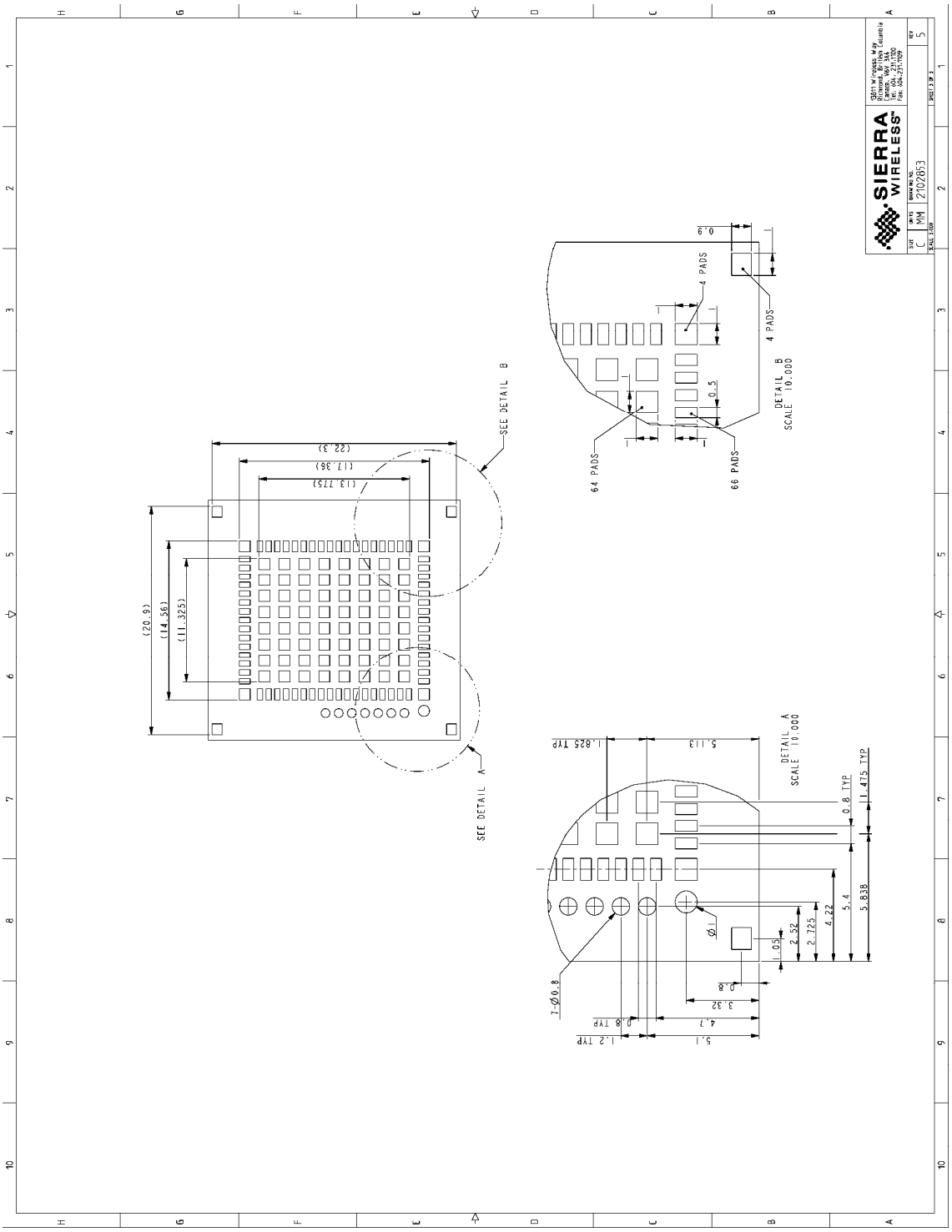


Figure 8. Footprint

5. Design Guidelines

5.1. Power-Up Sequence

Apply a LOW level logic to the PWR_ON_N pad (pad 59); within approximately 25ms, VGPIO will appear to be at 1.8V. Either UART1 or the USB interface could be used to send AT commands. The AT command interface is available in about 7 seconds after PWR_ON_N for either UART1 or USB.

When using UART1, the AT command interface is available after the transition of UART1_CTS from high to low level.

When using a USB connection, the HL7688 will start communicating with the host after USB enumeration. The time when AT commands can be sent will depend on the initialization time on the USB host.

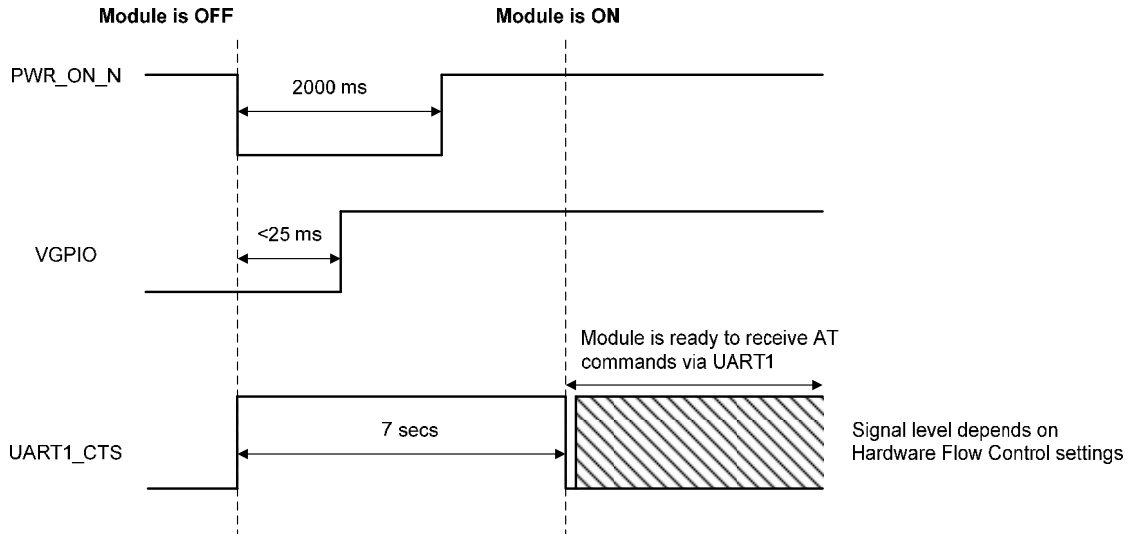


Figure 9. PWR_ON_N Sequence with VGPIO Information

Note: As PWR_ON_N is internally pulled up with 47kΩ, an open collector or open drain transistor must be used for ignition.

The PWR_ON_N pad has the minimum assertion time requirement of 25ms, with LOW active. Once the valid power on trigger is detected, the PWR_ON_N pad status can be left open.

The maximum inrush current is 1.3 A and lasts less than 1.5 ms.

5.2. Module Switch-Off

AT command **AT+CPWROFF** enables the user to properly switch the AirPrime HL7688 module off.

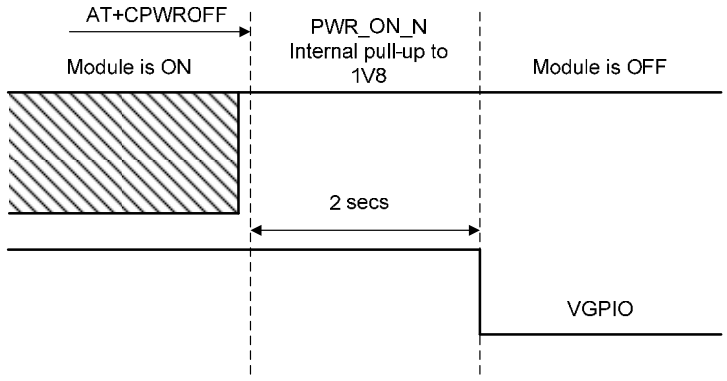


Figure 10. Power OFF Sequence for PWR_ON_N, VGPIO

Note: PWR_ON_N is internally pulled up by 47kΩ to 1.8V.

5.3. Emergency Power OFF

If required, the module can be switched off by controlling the RESET_IN_N pad (pad 11). This must only be used in emergency situations if the system freezes (not responding to AT commands).

To perform an emergency power off, a low level pulse must be sent on the RESET_IN_N pad for 20ms while the PWR_ON_N signal is inactive (high level). This action will immediately shut the HL7688 module down and the registers of the CPU and RAM memory will be reset for the next power on.

5.4. Sleep Mode Management

5.4.1. Using UART1

AT command **AT+KSLEEP** enables sleep mode configuration.

AT+KSLEEP=0:

- The module is active when DTR signal is active (low electrical level).
- When DTR is deactivated (high electrical level), the module enters sleep mode after a while.
- On DTR activation (low electrical level), the module wakes up.

AT+KSLEEP=1:

- The module determines when it enters sleep mode (when no more tasks are running).
- “0x00” character on the serial link wakes the module up.

AT+KSLEEP=2:

- The module never enters sleep mode.

5.4.2. Using USB

Use **AT+KSLEEP=1** to allows the module to automatically enter sleep mode while the USB interface is in use.

5.5. Power Supply Design

The AirPrime HL7688 module should not be supplied with voltage over 4.5V even temporarily or however briefly.

If the system's main board power supply unit is unstable or if the system's main board is supplied with over 4.5V, even in the case of transient voltage presence on the circuit, the module's power amplifier may be severely damaged.

To avoid such issues, add a voltage limiter to the module's power supply lines so that VBATT and VBATT_PA signal pads will never receive a voltage surge over 4.5V. The voltage limiter can be as simple as a Zener diode with decoupling capacitors as shown in the diagram below.

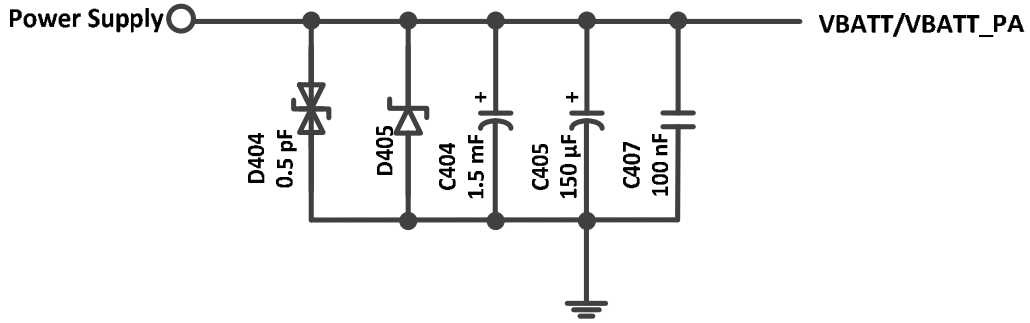


Figure 11. Voltage Limiter Example

5.6. ESD Guidelines for SIM Card

Decoupling capacitors must be added according to the drawings below as close as possible to the SIM card connectors on UIM1_CLK, UIM1_RST, UIM1_VCC, UIM1_DATA and UIM1_DET signals to avoid EMC issues and to comply with the requirements of ETSI and 3GPP standards covering the SIM electrical interface.

A typical schematic including SIM detection is provided below.

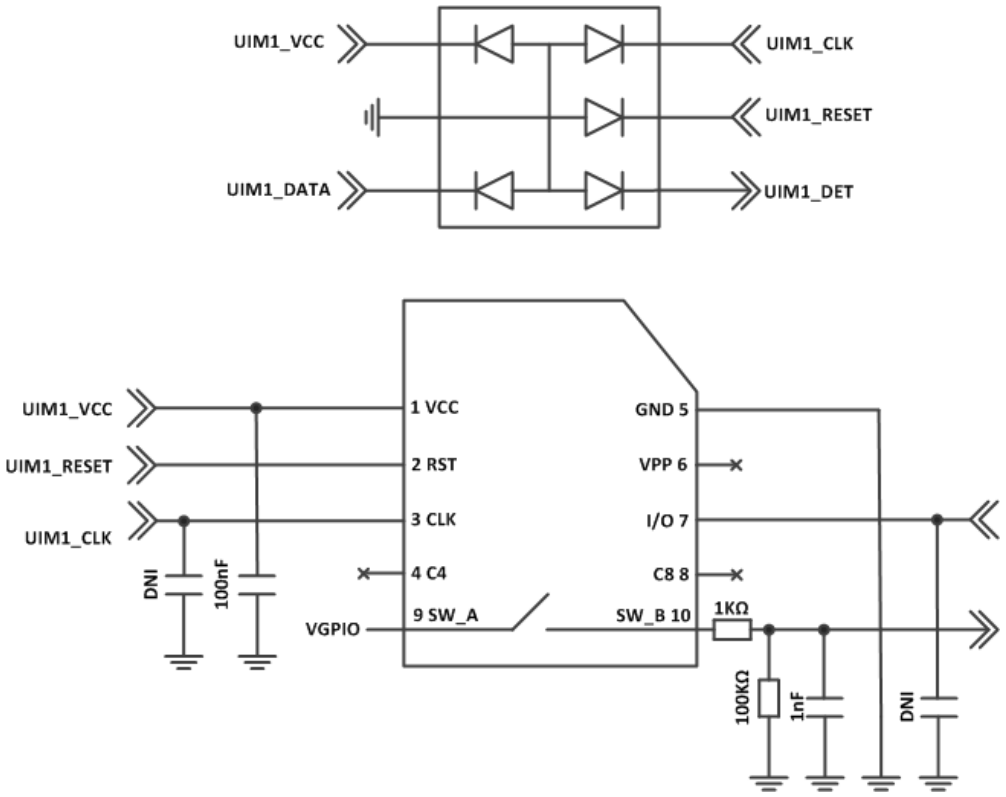


Figure 12. EMC and ESD Components Close to the SIM

5.7. ESD Guidelines for USB

When the USB interface is externally accessible, it is required to have ESD protection on the USB_VBUS, USB_D+ and USB_D- signals.

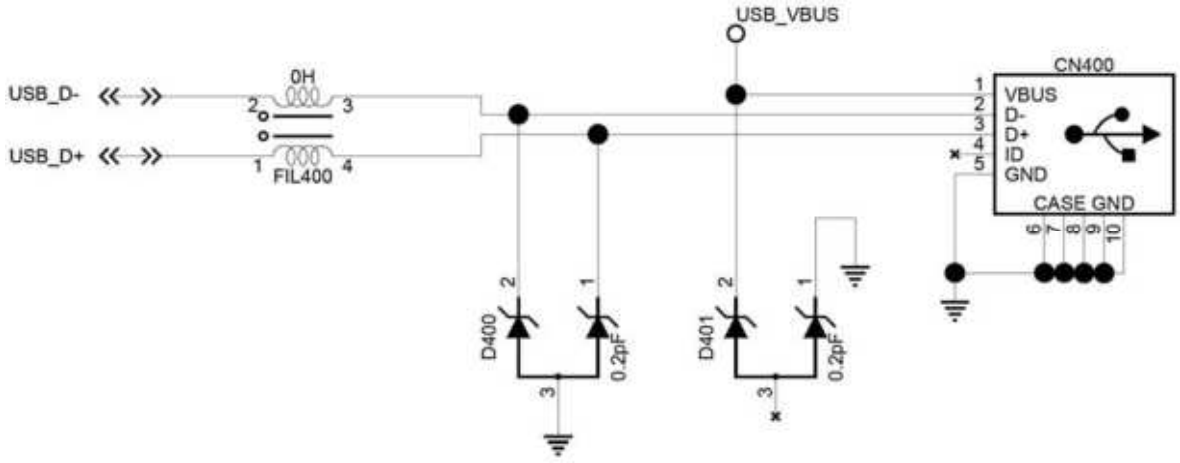


Figure 13. ESD Protection for USB

Note: It is not recommended to have an ESD diode with feedback path from USB_VBUS to either USB_D+ or USB_D-.

Sierra Wireless recommends using a 90Ω DLP0NSN900HL2L EMC filter and an RCLAMP0503N or ESD5V3U2U-03LRH ESD diode.

6. Reliability Specification

AirPrime HL7688 modules are tested against the Sierra Wireless Industrial Reliability Specification defined below.

6.1. Reliability Compliance

The AirPrime HL7688 module connected on a development kit board application is compliant with the following requirements.

Table 33. Standards Conformity

Abbreviation	Definition
IEC	International Electro technical Commission
ISO	International Organization for Standardization

6.2. Reliability Prediction Model

6.2.1. Life Stress Test

The following tests the AirPrime HL7688 module's product performance.

Table 34. Life Stress Test

Designation	Condition
Performance Test PT3T & PTRT 	Standard: N/A
	Special conditions: • Temperature: ▪ Class A: -30°C to +70°C ▪ Class B: -40°C to +85°C ▪ Rate of temperature change: ± 3°C/min • Recovery time: 3 hours
	Operating conditions: Powered
	Duration: 14 days

6.2.2. Environmental Resistance Stress Tests

The following tests the AirPrime HL7688 module's resistance to extreme temperature.

Table 35. Environmental Resistance Stress Tests

Designation	Condition
Cold Test Active **COTA** 	Standard: IEC 680068-2-1, Test Ad
	Special conditions: • Temperature: -40°C • Temperature variation: 1°C/min
	Operating conditions: Powered ON with a power cycle of 1 minute ON and 2 minutes OFF
	Duration: 3 days
Resistance to Heat Test **RH** 	Standard: IEC 680068-2-2, Test Bb
	Special conditions: • Temperature: +85°C • Temperature variation: 1°C/min
	Operating conditions: Powered ON with a power cycle of 15 minutes ON and 15 minutes OFF
	Duration: 50 days

6.2.3. Corrosive Resistance Stress Tests

The following tests the AirPrime HL7688 module's resistance to corrosive atmosphere.

Table 36. Corrosive Resistance Stress Tests

Designation	Condition
Humidity Test **HUT** 	Standard: IEC 60068-2-3, Test Ca
	Special conditions: • Temperature: +65°C • RH: 95% • Temperature variation: 3 +/- 0.6°C/min
	Operating conditions: Powered on, DUT is powered up for 15 minutes and OFF for 15 minutes
	Duration: 10 days

Designation	Condition
Component Solder Wettability CSW 	Standard: JESD22 – B102, Method 1/Condition C, Solderability Test Method
	Special conditions: • Test method: Dip and Look Test with Steam preconditioning 8 h+/-15min. dip for 5 +0/-0.5 seconds
	Operating conditions: Un-powered
	Duration: 1 day
Moist Heat Cyclic Test MHCT 	Standard: IEC 60068-2-30, Test Db
	Special conditions: • Upper temperature: +40 ± 2°C • Lower temperature: +25 ± 5°C • RH: ▪ Upper temperature: 93% ▪ Lower temperature: 95% • Number of cycles: 21 (1 cycle/24 hours) • Temperature Variation: 3 +/- 0.6°C/min
	Operating conditions: Powered ON for 15 minutes during each 3 hours ramp up and 3 hours ramp down (in middle) for every cycle
	Duration: 21 days

6.2.4. Thermal Resistance Cycle Stress Tests

The following tests the AirPrime HL7688 module's resistance to extreme temperature cycling.

Table 37. Thermal Resistance Cycle Stress Tests

Designation	Condition
Thermal Shock Test TSKT 	Standard: IEC 60068-2-14, Test Na
	Special conditions: • Temperature: -30°C to +80°C • Temperature Variation: less than 30s • Number of cycles: 600 • Dwell Time: 10 minutes
	Operating conditions: Un-powered
	Duration: 9 days

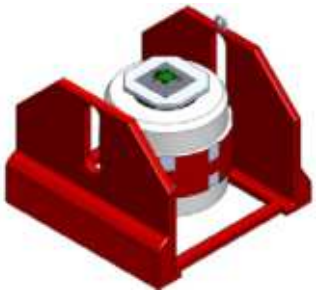
Designation	Condition
Temperature Change TCH 	Standard: IEC 60068-2-14, Test Nb
	Special conditions: • Temperature: -40°C to +90°C • Temperature Variation: 3 +/- 0.6°C/min • Number of cycles: 400 • Dwell Time: 10 minutes
	Operating conditions: Un-powered
	Duration: 29 days

6.2.5. Mechanical Resistance Stress Tests

The following tests the AirPrime HL7688 module's resistance to vibrations and mechanical shocks.

Table 38. Mechanical Resistance Stress Tests

Designation	Condition
Sinusoidal Vibration Test SVT 	Standard: IEC 60068-2-6, Test Fc
	Special conditions: • Frequency range: 16 Hz to 1000 Hz • Displacement: 0.35mm (peak-peak) • Acceleration: ▪ 5G from 16 to 62 Hz ▪ 3G from 62 to 200 Hz ▪ 1G from 200 to 1000 Hz • Sweep rate: 1 octave / cycle • Number of Sweep: 20 sweeps/axis • Sweep direction: +/- X,+/- Y, +/- Z
	Operating conditions: Un-powered
	Duration: 2 days
Random Vibration Test RVT 	Standard: IEC 60068-2-64, Test Fh
	Special conditions: • Frequency range: 10 Hz – 2000 Hz • Power Spectral Density in $[(m/s^2)^2/Hz]$ ▪ 0.1 g2/Hz at 10Hz ▪ 0.01 g2/Hz at 250Hz ▪ 0.005 g2/Hz at 1000Hz ▪ 0.005 g2/Hz at 2000Hz • Peak factor: 3 • Duration per Axis: 1 hr / axis
	Operating conditions: Un-powered
	Duration: 1 day
Mechanical Shock Test	Standard: IEC 60068-2-27, Test Ea

Designation	Condition
MST 	Special conditions: • Shock Test 1: ▪ Wave form: Half sine ▪ Peak acceleration: 30g ▪ Duration: 11ms ▪ Number of shocks: 8 ▪ Direction: ±X, ±Y, ±Z • Shock Test 2: ▪ Wave form: Half sine ▪ Peak acceleration: 100g ▪ Duration: 6ms ▪ Number of shocks: 3 ▪ Direction: ±X, ±Y, ±Z
	Operating conditions: Un-powered
	Duration: 72 hours

6.2.6. Handling Resistance Stress Tests

The following tests the AirPrime HL7688 module's resistance to handling malfunctions and damage.

Table 39. Handling Resistance Stress Tests

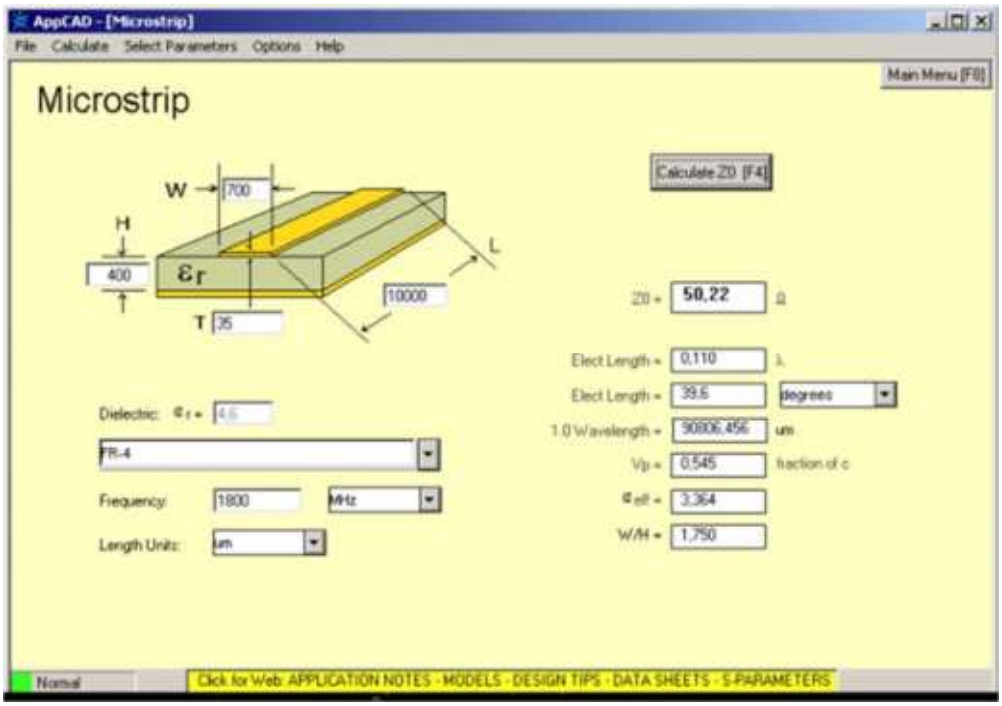
Designation	Condition
ESDC Test 	Standard: JESD22-A114, JESD22-A115, JESD22-C101
	Special conditions: • HBM (Human Body Model): 1KV (Class 1C) • MM (Machine Model): 200V • CDM (Charged Device Model): 250V (Class II)
	Operating conditions: Powered
	Duration: 3 days
ESD Test 	Standard: IEC 61000-4-2
	Special conditions: • Contact Voltage: ±2kV, ±4kV, ±6kV • Air Voltage: ±2kV, ±4kV, ±8kV
	Operating conditions: Powered
	Duration: 3 days
Free Fall Test **FFT 1**	Standard : IEC 60068-2-32, Test Ed
	Special conditions: • Number of drops: 2 drops per unit • Height: 1m

Designation	Condition
	Operating conditions: Un-powered
	Duration: 6 hours

7. FCC Regulations

The AirPrime HL7688 module has been granted modular approval for mobile applications. Integrators may use the HL7688 module in their final products without additional FCC certification if they meet the following conditions. Otherwise, additional FCC approvals must be obtained.

1. At least 20 cm separation distance between the antenna and the user's body must be maintained at all times.
2. To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, the maximum antenna gain including cable loss in a mobile-only exposure condition must not exceed:
   - 9.01 dBi in Band 2
   - 6.00 dBi in Band 4
   - 10.41 dBi in Band 5
   - 9.74 dBi in Band 17
3. The HL7688 module must not transmit simultaneously with other collocated radio transmitters within a host device.
4. The RF signal must be routed on the application board using tracks with a 50Ω characteristic impedance. Basically, the characteristic impedance depends on the dielectric, the track width and the ground plane spacing. In order to respect this constraint, Sierra Wireless recommends using MicroStrip or StripLine structure and computing the Tracks width with a simulation tool (like AppCad shown in the figure below and that is available free of charge at http://www.agilent.com).



If a multi-layered PCB is used, the RF path on the board must not cross any signal (digital, analog or supply).

If necessary, use StripLine structure and route the digital line(s) "outside" the RF structure. An example of proper routing is shown in the figure below.



Stripline and Coplanar design requires having a correct ground plane at both sides. Consequently, it is necessary to add some vias along the RF path. It is recommended to use Stripline design if the RF path is fairly long (more than 3cm), since MicroStrip design is not shielded. Consequently, the RF signal (when transmitting) may interfere with neighbouring electronics (AF amplifier, etc.). In the same way, the neighbouring electronics (micro-controllers, etc.) may degrade the reception performances. The antenna connector is intended to be directly connected to a 50Ω antenna and no matching is needed.

5. A label must be affixed to the outside of the end product into which the HL7688 module is incorporated, with a statement similar to the following:

   This device contains FCC ID: **N7NHL7688**

6. A user manual with the end product must clearly indicate the operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.

The end product with an embedded HL7688 module may also need to pass the FCC Part 15 unintentional emission testing requirements and be properly authorized per FCC Part 15.

Note:	*If this module is intended for use in a portable device, you are responsible for separate approval to satisfy the SAR requirements of FCC Part 2.1093.*

8. Ordering Information

Table 40. Ordering Information

Model Name	Description	Part Number
HL7688	HL7688 embedded module	Contact Sierra Wireless for the latest SKU
DEV-KIT	HL Series Development Kit	6000620

9. Terms and Abbreviations

Abbreviation	Definition
ADC	Analog to Digital Converter
AGC	Automatic Gain Control
AT	Attention (prefix for modem commands)
CDMA	Code Division Multiple Access
CF3	Common Flexible Form Factor
CLK	Clock
CODEC	Coder Decoder
CPU	Central Processing Unit
DAC	Digital to Analog Converter
DTR	Data Terminal Ready
EGNOS	European Geostationary Navigation Overlay Service
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EN	Enable
ESD	Electrostatic Discharges
ETSI	European Telecommunications Standards Institute
FDMA	Frequency-division multiple access
GAGAN	GPS aided geo augmented navigation
GLONASS	Global Navigation Satellite System
GND	Ground
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
GPRS	General Packet Radio Service
GSM	Global System for Mobile communications
Hi Z	High impedance (Z)
IC	Integrated Circuit
IMEI	International Mobile Equipment Identification
I/O	Input / Output
LED	Light Emitting Diode
LNA	Low Noise Amplifier
MAX	Maximum
MIN	Minimum
MSAS	Multi-functional Satellite Augmentation System
N/A	Not Applicable
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PCL	Power Control Level
PLL	Phase Lock Loop
PWM	Pulse Width Modulation
QZSS	Quasi-Zenith Satellite System

Abbreviation	Definition
RF	Radio Frequency
RFI	Radio Frequency Interference
RMS	Root Mean Square
RST	Reset
RTC	Real Time Clock
RX	Receive
SCL	Serial Clock
SDA	Serial Data
SIM	Subscriber Identification Module
SMD	Surface Mounted Device/Design
SPI	Serial Peripheral Interface
SW	Software
PSRAM	Pseudo Static RAM
TBC	To Be Confirmed
TBD	To Be Defined
TP	Test Point
TX	Transmit
TYP	Typical
UART	Universal Asynchronous Receiver-Transmitter
UICC	Universal Integrated Circuit Card
USB	Universal Serial Bus
UIM	User Identity Module
VBATT	Main Supply Voltage from Battery or DC adapter
VSWR	Voltage Standing Wave Ratio
WAAS	Wide Area Augmentation System