Adaptive Multi-Rail Power Platform – AmP

AmP4D/AmP8D/AmP12D

Product Description

The AmP™ device is an FPGA based platform for creating a custom Power Management Integrated Circuit (PMIC). The AmP device is customized by adding available Power Components designs based on system requirements. AmP device customization is as easy as using WebAmp™ application software to produce a customized PMIC in a very short period of time. AmP devices can be used to power FPGAs, Processors, Microcontrollers, and ASICs by integrating multiple power rails into single chip designs. The AmP device input voltage range is 4.75V to 20V. The AmP device is targeted for wall-powered applications or 2S-4S Li-Ion battery packs. AmP devices have up to 4 additional integrated LDOs of which two are fixed output voltages (3.3V and 1.2V) and two are user programmable.

Features

- Enables On-Demand power management
- Integrate application targeted Power Components
- Power Blocks for a variety of topologies
  - Scalable Integrated N-channel MOSFETs (SIM)
  - Current sense for protection, telemetry, regulation
  - Build Switching topologies - Buck, Boost, Buck-Boost
  - Build Linear topologies - LDO, Load Switch
  - Build Mixed topologies - Battery Charger
  - Build BLDC (Motor Control) topologies – H-Bridge
- Sensor Blocks, sensing voltages and currents
  - Regulation, protection and telemetry
  - Adaptive Digitizer (ADi)
  - Threshold Comparators (ThC)
  - Summation Amplifier (SuM)
  - Noise-Immune Reference (Nref) Array
- Analog fabric connectivity for sensor signals
- Digital µLogic fabric connectivity: Analog/Digital Blocks
  - Analog and Digital GPIOs, LUTs for logic & Interface
  - Integrated Compensator RAM (CRAM)
  - On-demand POL control loops and interfaces
  - Precision Modulation Timer Array
- Industry first: Analog Proficiency – Digital Flexibility

AmP Family

- Nine member 12 V platform family (AmP8D available now)
  - Four, Eight, Twelve Power & Sensor Blocks
  - Up to four, eight and twelve switcher or linear rails
  - 6A, 3A, 1A per DMOS MOSFETs; RDSon 30mΩ
  - Analog or Digital I/Os: 24
  - Packages: QFN 5x5 and 8x8 sq. mm
- Standard BCD process: 110nm, V_{DS}max 20V

AmP DMOS Platforms

Power Blocks	GPIOs	Device		
Four	12	AmP4D1	AmP4D3	AmP4D6
Eight	24	AmP8D1	AmP8D3	AmP8D6
Twelve	36	AmP12D1	AmP12D3	AmP12D6

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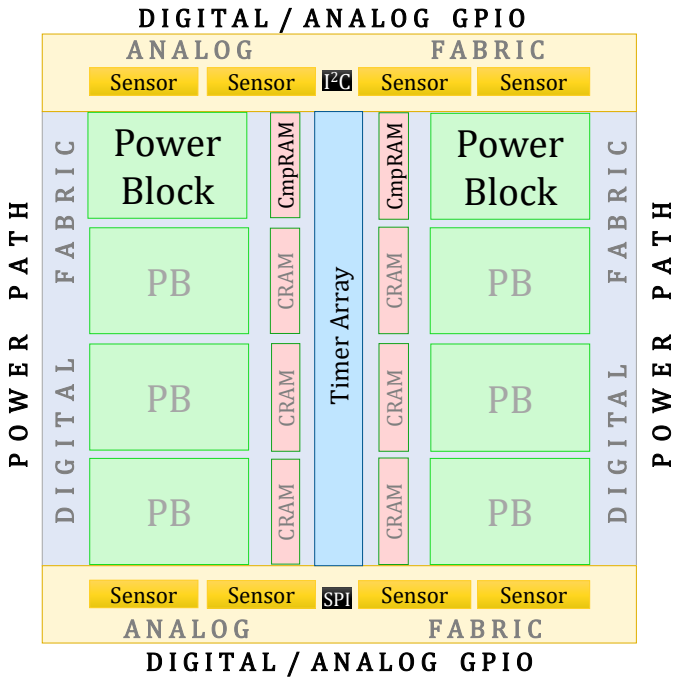

Applications

Power Component Integrator

- Build Buck, Boost, Buck-Boost POL topologies
- PWM – CV/CC, voltage mode or current mode
- Hysteretic – CON/COF
- Load Switch, LDO - Source/Drain, DDR LDO
- External Switching Controllers/Gate Drivers
- Peak efficiency > 92%, Soft start/stop

Digital power management IC

- Monitor and throttle/margin power rails
- Power ON/OFF/Sequence power rails
- Buck, Boost, Buck-Boost, LDO, Battery Chargers

Battery Charger

- Build trickle, CC, CV Charger
- Power Path integration
- I²C, SMBus, DVS for Telemetry and control
- Protection: On-demand OCP, OVP, OTP, UVLO

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AmP8D Platform Features

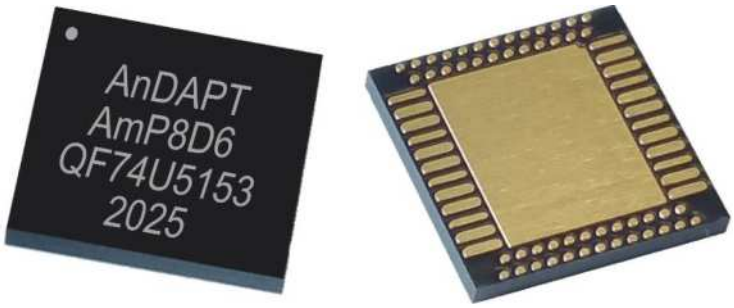
Device			8Dx1	8Dx3	8Dx6
Drain Current			1A	3A	6A
Power Blocks			8	8	8
Sensor Blocks			8	8	8
Nrefs			8	12	24
Timers			16	16	16
LDOs for GPIOs			2	2	4
µLogic Fabric LUTs			512	512	512
Package*			GPIOs		
QF65	5x5mm	8D MOSFETs	23	23	23
QF74	8x8mm	8D MOSFETs	24	24	24

*T_A: -40C to 85C, T_J: -40C to 125C;

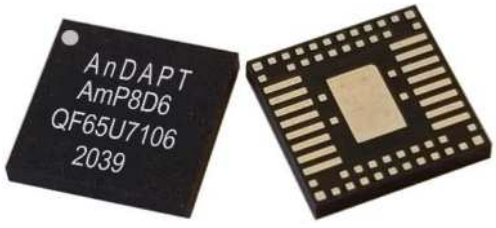
Order Information

Platform	MOSFETs	Technology	Current – A	Package	Part Number	Availability
AmP	8	D	1	QF74	AmP8D1QF74	Now
AmP	8	D	3	QF74	AmP8D3QF74	Now
AmP	8	D	6	QF74	AmP8D6QF74	Now
AmP	8	D	1	QF65	AmP8D1QF65	Now
AmP	8	D	3	QF65	AmP8D3QF65	Now
AmP	8	D	6	QF65	AmP8D6QF65	Now

Package Marking Example – QF74



Package Marking Example – QF65



Package Configuration

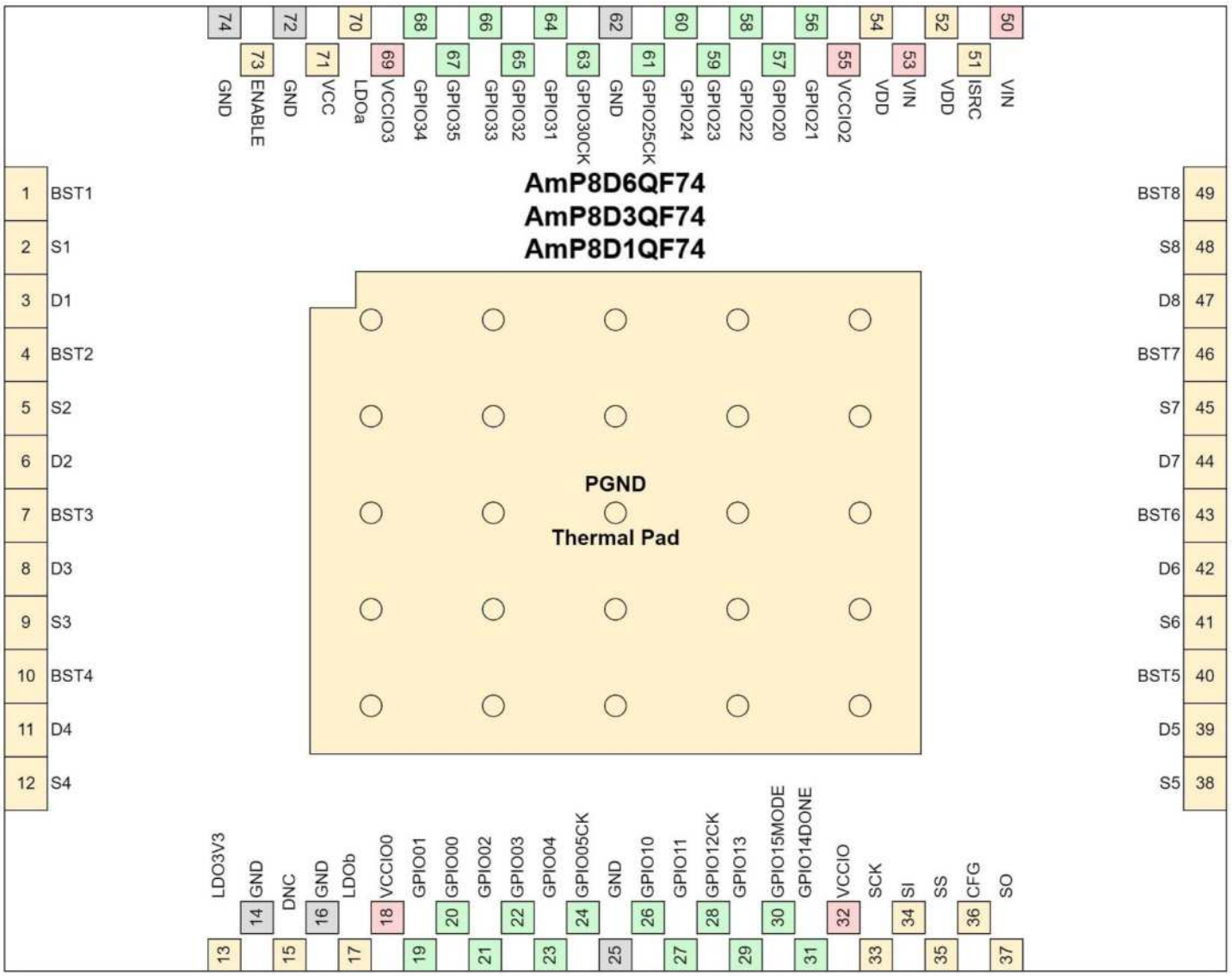
Top View (Pin and Thermal Pads are on bottom side)

AmP8D

QF74

8x8 mm

6A, 3A, 1A



Package Configuration

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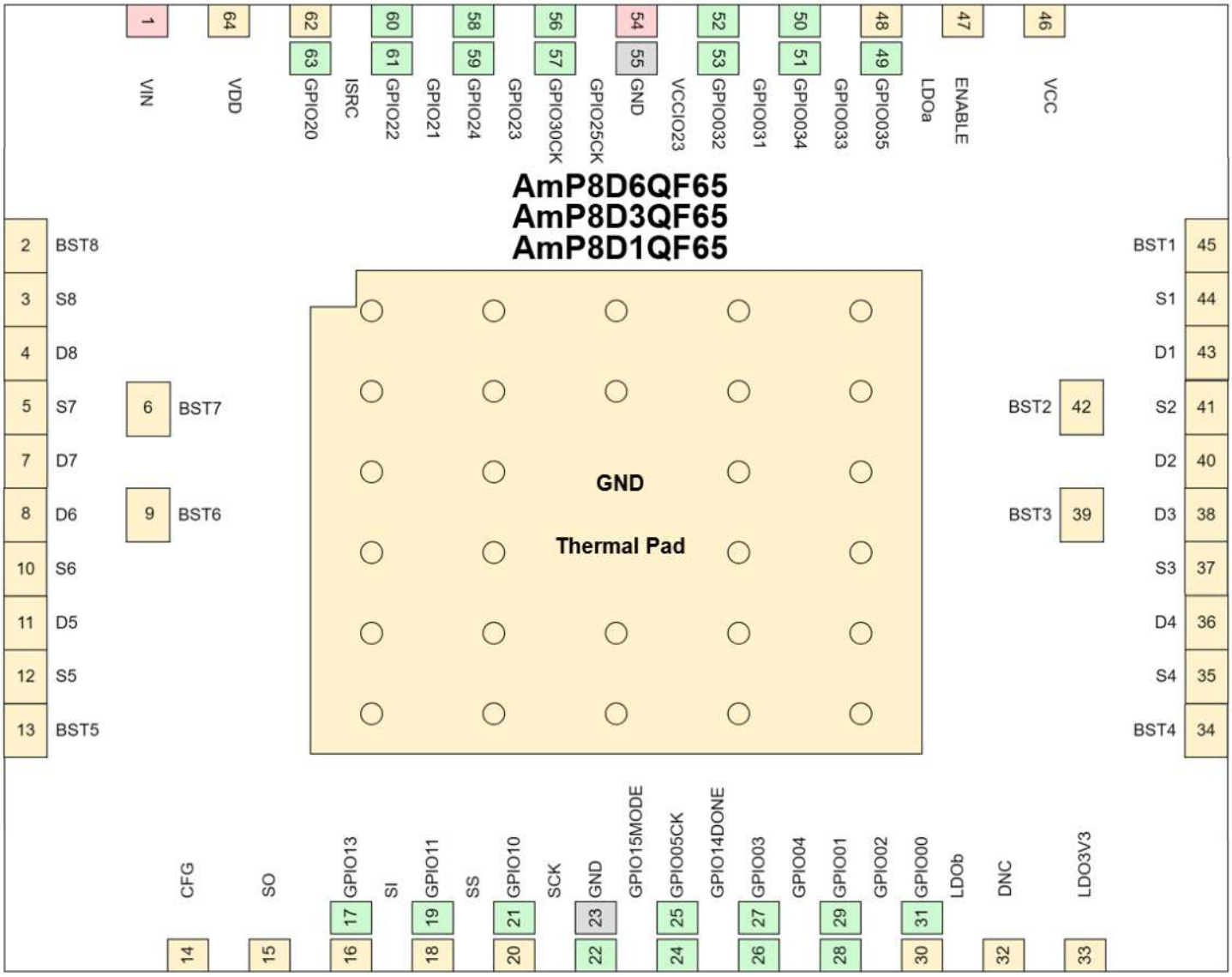
AmP8D

QF65

5X5 mm

6A, 3A, 1A



Pin Configurations

Name	QF74	QF65	Function
BST1	1	45	Boost
S1	2	44	Source
D1	3	43	Drain
BST2	4	42	Boost
S2	5	41	Source
D2	6	40	Drain
BST3	7	39	Boost
D3	8	38	Drain
S3	9	37	Source
BST4	10	34	Boost
D4	11	36	Drain
S4	12	35	Source
LDO3V3	13	33	LDO 3.3 V
GND	14		GND
DNC	15	32	DNC
GND	16		GND
LDOb	17	30	LDO Prog.
VCCIO0	18	*	IO bank supply
GPIO00	20	31	GPIO
GPIO01	19	29	GPIO
GPIO02	21	28	GPIO
GPIO03	22	27	GPIO
GPIO04	23	26	GPIO
GPIO05CK	24	25	GPIOCK
GND	25	23	GND
GPIO10	26	21	GPIO
GPIO11	27	19	GPIO
GPIO12CK	28		GPIOCK
GPIO13	29	17	GPIO
GPIO14DONE	31	24	GPIODONE
GPIO15MODE	30	22	GPIOMODE
VCCIO1	32	*	IO bank supply
SCK	33	20	SPI clock
SS	35	18	SPI select
SI	34	16	SPI serial in
SO	37	15	SPI serial out
CFG	36	14	Configuration

* Connected internally to 3.3V

Name	QF74	QF65	Function
S5	38	12	Source
D5	39	11	Drain
BST5	40	13	Boost
S6	41	10	Source
D6	42	8	Drain
BST6	43	9	Boost
D7	44	7	Drain
S7	45	5	Source
BST7	46	6	Boost
D8	47	4	Drain
S8	48	3	Source
BST8	49	2	Boost
ISRC	51	62	Prog. Cur. Src.
VIN	50	1	Supply
VIN	53		Supply
VDD	52	64	LDO 4.5V
VDD	54		LDO 4.5V
VCCIO2	55		IO bank supply
VCCIO23		54	IO bank supply
GPIO20	57	63	GPIO
GPIO21	56	60	GPIO
GPIO22	58	61	GPIO
GPIO23	59	58	GPIO
GPIO24	60	59	GPIO
GPIO25CK	61	56	GPIOCK
GND	62	55	GND
GPIO30CK	63	57	GPIOCK
GPIO31	64	52	GPIO
GPIO32	65	53	GPIO
GPIO33	66	50	GPIO
GPIO34	68	51	GPIO
GPIO35	67	49	GPIO
VCCIO3	69		IO bank supply
LDOa	70	48	LDO, prog.
GND	72		GND
VCC	71	46	LDO, 1.2 V
ENABLE	73	47	Enable AmP
GND	74	65	GND

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Pin Function and Description

Function	Description
Boost	Bootstrap pin for MOSFET gate drive
Drain	MOSFET drain
Source	MOSFET source
GND	Digital ground Analog ground, thermal pad
LDO 3.3V	LDO output 3.3V
DNC	Do not connect, floating
LDO Prog.	LDO output voltage programmable
IO bank supply	Supply input to GPIO bank
GPIO	General purpose input-output
GPIOCK	GPIO shared with input low skew global clock driver to digital fabric
GPIODONE	GPIO shared with DONE output
GPIOMODE	GPIO shared with MODE input, must sample high for Host mode at the beginning of configuration or sample low for Client mode at the beginning of configuration
SPI clock	SLK output clock when AmP is Host, input clock when AmP is Client
SPI select	SS output Client select when AmP is Host, input when AmP is Client
SPI serial in	SI input receives SPI data
SPI serial out	SO output transmits SPI commands
Configuration	CFG input active high configuration restart. AmP is held in reset while signal is high. Reconfiguration is triggered on negative edge.
Prog. Cur. Src.	Programmable current source
Supply	Vin bias supply for, VDD, VCC, LDO3V3, LDOa, LDOb
LDO 4.5V	VDD LDO 4.5V output
LDO 1.2V	VCC, LDO 1.2V output
Enable AmP	AmP Platform powered on when floating, powered down when pulled low. Use ENABLE Circuit below where AmP_EN signal may be used to power down.

ENABLE Circuit

