SMART ARM-based Microcontroller

SAM L21E / SAM L21G / SAM L21J Summary

DATASHEET SUMMARY

Introduction

Atmel® | SMART SAM L21 is a series of Ultra low-power microcontrollers using the 32-bit ARM® Cortex®-M0+ processor at max. 48MHz (2.46 CoreMark®/MHz) and up to 256KB Flash and 40KB of SRAM in a 32, 48, and 64 pin package. The sophisticated power management technologies, such as power domain gating, SleepWalking, Ultra low-power peripherals and more, allow for very low current consumptions. The highly configurable peripherals include a touch controller supporting capacitive interfaces with proximity sensing.

Features

- Processor
  - ARM Cortex-M0+ CPU running at up to 48MHz
    - Single-cycle hardware multiplier
    - Micro Trace Buffer
- Memories
  - 32/64/128/256KB in-system self-programmable Flash
  - 1/2/4/8KB Flash Read-While-Write section
  - 4/8/16/32KB SRAM Main Memory
  - 2/4/8/8KB SRAM Low power Memory
- System
  - Power-on reset (POR) and brown-out detection (BOD)
  - Internal and external clock options
  - External Interrupt Controller (EIC)
  - 16 external interrupts
  - One non-maskable interrupt
  - Two-pin Serial Wire Debug (SWD) programming, test and debugging interface
- Low Power
  - Idle, Standby, Backup, and Off sleep modes
  - SleepWalking peripherals

This is a summary document. A complete document is available on our Web site at www.atmel.com

  - Static and Dynamic Power Gating Architecture
  - Battery backup support
  - Two Performance Levels
  - Embedded Buck/LDO regulator supporting on-the-fly selection
- Peripherals
  - 16-channel Direct Memory Access Controller (DMAC)
  - 12-channel Event System
  - Up to five 16-bit Timer/Counters (TC) including one low-power TC, each configurable as:
    - 16-bit TC with two compare/capture channels
    - 8-bit TC with two compare/capture channels
    - 32-bit TC with two compare/capture channels, by using two TCs
  - Two 24-bit and one 16-bit Timer/Counters for Control (TCC), with extended functions:
    - Up to four compare channels with optional complementary output
    - Generation of synchronized pulse width modulation (PWM) pattern across port pins
    - Deterministic fault protection, fast decay and configurable dead-time between complementary output
    - Dithering that increase resolution with up to 5 bit and reduce quantization error
  - 32-bit Real Time Counter (RTC) with clock/calendar function
  - Watchdog Timer (WDT)
  - CRC-32 generator
  - One full-speed (12Mbps) Universal Serial Bus (USB) 2.0 interface
    - Embedded host and device function
    - Eight endpoints
  - Up to six Serial Communication Interfaces (SERCOM) including one low-power SERCOM, each configurable to operate as either:
    - USART with full-duplex and single-wire half-duplex configuration
    - I^2C up to 3.4MHz
    - SPI
    - LIN slave
  - One AES encryption engine
  - One True Random Generator (TRNG)
  - One Configurable Custom Logic (CCL)
  - One 12-bit, 1MSPS Analog-to-Digital Converter (ADC) with up to 20 channels
    - Differential and single-ended input
    - Automatic offset and gain error compensation
    - Oversampling and decimation in hardware to support 13-, 14-, 15-, or 16-bit resolution
  - Two 12-bit, 1MSPS Dual Output Digital-to-Analog Converter (DAC)
  - Two Analog Comparators (AC) with window compare function
  - Three Operational Amplifiers (OPAMP)
  - Peripheral Touch Controller (PTC)
    - 169-Channel capacitive touch and proximity sensing
    - Wake-up on touch in standby mode
- Oscillators
  - 32.768kHz crystal oscillator (XOSC32K)

  - 0.4-32MHz crystal oscillator (XOSC)
  - 32.768kHz internal oscillator (OSC32K)
  - 32.768kHz ultra-low-power internal oscillator (OSCULP32K)
  - 16/12/8/4MHz high-accuracy internal oscillator (OSC16M)
  - 48MHz Digital Frequency Locked Loop (DFLL48M)
  - 96MHz Fractional Digital Phased Locked Loop (FDPLL96M)
- I/O
  - Up to 51 programmable I/O pins
- Easy migration from SAM D family
- Packages
  - 64-pin TQFP, QFN, WLCSP
  - 48-pin TQFP, QFN
  - 32-pin TQFP, QFN
- Operating Voltage
  - 1.62V – 3.63V

Table of Contents

Introduction....1

1. Description....5

Features....1

2. Configuration Summary....7

3. Ordering Information....10

3.1. SAM L21J....10
3.2. SAM L21G....11
3.3. SAM L21E....11
3.4. Device Identification....11

4. Block Diagram....13

5. Pinout....15

5.1. SAM L21J....15
5.2. SAM L21J WLCSP64....16
5.3. SAM L21G....17
5.4. SAM L21E....18

6. Product Mapping....19

7. Processor and Architecture....20

7.1. Cortex M0+ Processor....20
7.2. Nested Vector Interrupt Controller....21
7.3. Micro Trace Buffer....23
7.4. High-Speed Bus System....24

8. Packaging Information....29

8.1. Thermal Considerations....29
8.2. Package Drawings....30
8.3. Soldering Profile....39

1. Description

Atmel® | SMART SAM L21 is a series of Ultra low-power microcontrollers using the 32-bit ARM® Cortex®-M0+ processor, and ranging from 32- to 64-pins with up to 256KB Flash and 40KB of SRAM. The SAM L21 devices operate at a maximum frequency of 48MHz and reach 2.46 CoreMark®/MHz. They are designed for simple and intuitive migration with identical peripheral modules, hex compatible code, identical linear address map and pin compatible migration paths between all devices in the product series. All devices include intelligent and flexible peripherals, Atmel Event System for inter-peripheral signaling, and support for capacitive touch button, slider and wheel user interfaces.

The Atmel SAM L21 devices provide the following features: In-system programmable Flash, 16-channel direct memory access (DMA) controller, 12-channel Event System, programmable interrupt controller, up to 51 programmable I/O pins, 32-bit real-time clock and calendar, up to five 16-bit Timer/Counters (TC) and three Timer/Counters for Control (TCC) where each TC/TCC can be configured to perform frequency and waveform generation, accurate program execution timing or input capture with time and frequency measurement of digital signals. The TCs can operate in 8- or 16-bit mode, selected TCs can be cascaded to form a 32-bit TC, and three timer/counters have extended functions optimized for motor, lighting and other control applications. Two TCC can operate in 24-bit mode, the third TCC can operate in 16-bit mode. The series provide one full-speed USB 2.0 embedded host and device interface; up to six Serial Communication Modules (SERCOM) that each can be configured to act as an USART, UART, SPI, I^2C up to 3.4MHz, SMBus, PMBus, and LIN slave; up to twenty channel 1MSPS 12-bit ADC with programmable gain and optional oversampling and decimation supporting up to 16-bit resolution, two 12-bit 1MSPS DACs, two analog comparators with window mode, three independent cascadable OPAMPs supporting internal connection with others analog features, Peripheral Touch Controller supporting up to 192 buttons, sliders, wheels and proximity sensing; programmable Watchdog Timer, brown-out detector and power-on reset and two-pin Serial Wire Debug (SWD) program and debug interface.

All devices have accurate and low-power external and internal oscillators. All oscillators can be used as a source for the system clock. Different clock domains can be independently configured to run at different frequencies, enabling power saving by running each peripheral at its optimal clock frequency, and thus maintaining a high CPU frequency while reducing power consumption.

The SAM L21 devices have four software-selectable sleep modes, idle, standby, backup and off. In idle mode the CPU is stopped while all other functions can be kept running. In standby all clocks and functions are stopped except those selected to continue running. In this mode all RAMs and logic contents are retained. The device supports SleepWalking. This feature allows the peripheral to wake up from sleep based on predefined conditions, and thus allows some internal operation like DMA transfer and/or the CPU to wake up only when needed, e.g. when a threshold is crossed or a result is ready. The Event System supports synchronous and asynchronous events, allowing peripherals to receive, react to and send events even in standby mode.

The SAM L21 devices have two software-selectable performance levels (PL0 and PL2) allowing the user to scale the lowest core voltage level that will support the operating frequency. To further minimize consumption, specifically leakage dissipation, the SAM L21 devices utilizes power domain gating technique with retention to turn off some logic area while keeping its logic state. This technique is fully handled by hardware.

The Flash program memory can be reprogrammed in-system through the SWD interface. The same interface can be used for nonintrusive on-chip debugging of application code. A boot loader running in the device can use any communication interface to download and upgrade the application program in the Flash memory.

The Atmel SAM L21 devices are supported with a full suite of programs and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers and evaluation kits.

2. Configuration Summary

	SAM L21J	SAM L21G	SAM L21E
Pins	64	48	32
General Purpose I/O-pins (GPIOs)	51	37	25
Flash	256/128/64KB	256/128/64KB	256/128/64/32KB
Flash RWW section	8/4/2KB	8/4/2KB	8/4/2/1KB
System SRAM	32/16/8KB	32/16/8KB	32/16/8/4KB
Low Power SRAM	8/8/4KB	8/8/4KB	8/8/4/2KB
Timer Counter (TC) instances(1)	5	3	3
Waveform output channels per TC instance	2	2	2
Timer Counter for Control (TCC) instances	3	3	3
Waveform output channels per TCC	8/4/2	8/4/2	6/4/2
DMA channels	16	16	16
USB interface	1	1	1
AES engine	1	1	1
Configurable Custom Logic (CCL) (LUTs)	4	4	4
True Random Generator (TRNG)	1	1	1
Serial Communication Interface (SERCOM) instances	6	6	6
Analog-to-Digital Converter (ADC) channels	20	14	10
Analog Comparators (AC)	2	2	2
Digital-to-Analog Converter (DAC) channels	2	2	2
Operational Amplifier (OPAMP)	3	3	3

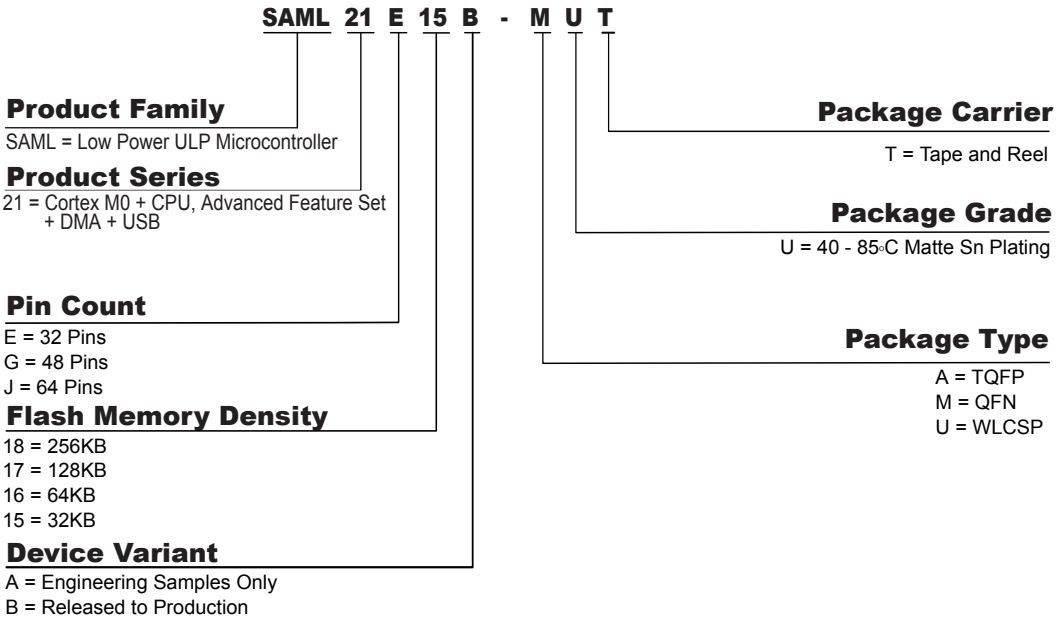
	SAM L21J	SAM L21G	SAM L21E
Real-Time Counter (RTC)	Yes	Yes	Yes
RTC alarms	1	1	1
RTC compare values	One 32-bit value or two 16-bit values	One 32-bit value or two 16-bit values	One 32-bit value or two 16-bit values
External Interrupt lines	16	16	16
Peripheral Touch Controller (PTC) channels (X- x Y-Lines) for mutual capacitance (2)	169 (13x13)	81 (9x9)	42 (7x6)
Peripheral Touch Controller (PTC) channels for self capacitance (Y-Lines only) (3)	16	10	7
Maximum CPU frequency	48MHz		
Packages	QFN TQFP WLCSP(4)	QFN TQFP	QFN TQFP
Oscillators	32.768kHz crystal oscillator (XOSC32K) 0.4-32MHz crystal oscillator (XOSC) 32.768kHz internal oscillator (OSC32K) 32KHz ultra-low-power internal oscillator (OSCULP32K) 16/12/8/4MHz high-accuracy internal oscillator (OSC16M) 48MHz Digital Frequency Locked Loop (DFLL48M) 96MHz Fractional Digital Phased Locked Loop (FDPLL96M)		
Event System channels	12	12	12
SW Debug Interface	Yes	Yes	Yes
Watchdog Timer (WDT)	Yes	Yes	Yes

Note:

1. For SAM L21E and SAM L21G, only TC0, TC1 and TC4 are available.
2. The number of X- and Y-lines depends on the configuration of the device, as some I/O lines can be configured as either X-lines or Y-lines. Refer to *Multiplexed Signals* for details. The number in the Configuration Summary is the maximum number of channels that can be obtained.

3. The number of Y-lines depends on the configuration of the device, as some I/O lines can be configured as either X-lines or Y-lines. The number given here is the maximum number of Y-lines that can be obtained.
4. WLCSP parts are programmed with a specific SPI bootloader. Refer to Application Note AT09002 for details.

3. Ordering Information



Note: The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

3.1. SAM L21J

Table 3-1. SAM L21J Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML21J16B-AUT	64K	8K	TQFP64	Tape & Reel
ATSAML21J16B-MUT			QFN64	
ATSAML21J17B-AUT	128K	16K	TQFP64	Tape & Reel
ATSAML21J17B-MUT			QFN64	
ATSAML21J17B-UUT			WLCSP64	
ATSAML21J18B-AUT	256K	32K	TQFP64	Tape & Reel
ATSAML21J18B-MUT			QFN64	
ATSAML21J18B-UUT			WLCSP64	

3.2. SAM L21G

Table 3-2. SAM L21G Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML21G16B-AUT	64K	8K	TQFP48	Tape & Reel
ATSAML21G16B-MUT			QFN48	
ATSAML21G17B-AUT	128K	16K	TQFP48	Tape & Reel
ATSAML21G17B-MUT			QFN48	
ATSAML21G18B-AUT	256K	32K	TQFP48	Tape & Reel
ATSAML21G18B-MUT			QFN48	

3.3. SAM L21E

Table 3-3. SAM L21E

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML21E15B-AUT	32K	4K	TQFP32	Tape & Reel
ATSAML21E15B-MUT			QFN32	
ATSAML21E16B-AUT	64K	8K	TQFP32	Tape & Reel
ATSAML21E16B-MUT			QFN32	
ATSAML21E17B-AUT	128K	16K	TQFP32	Tape & Reel
ATSAML21E17B-MUT			QFN32	
ATSAML21E18B-AUT	256K	32K	TQFP32	Tape & Reel
ATSAML21E18B-MUT			QFN32	

3.4. Device Identification

The DSU - Device Service Unit peripheral provides the Device Selection bits in the Device Identification register (DID.DEVSEL) in order to identify the device by software. The SAM L21 variants have a reset value of DID=0x1081drxx, with the LSB identifying the die number ('d'), the die revision ('r') and the device selection ('xx').

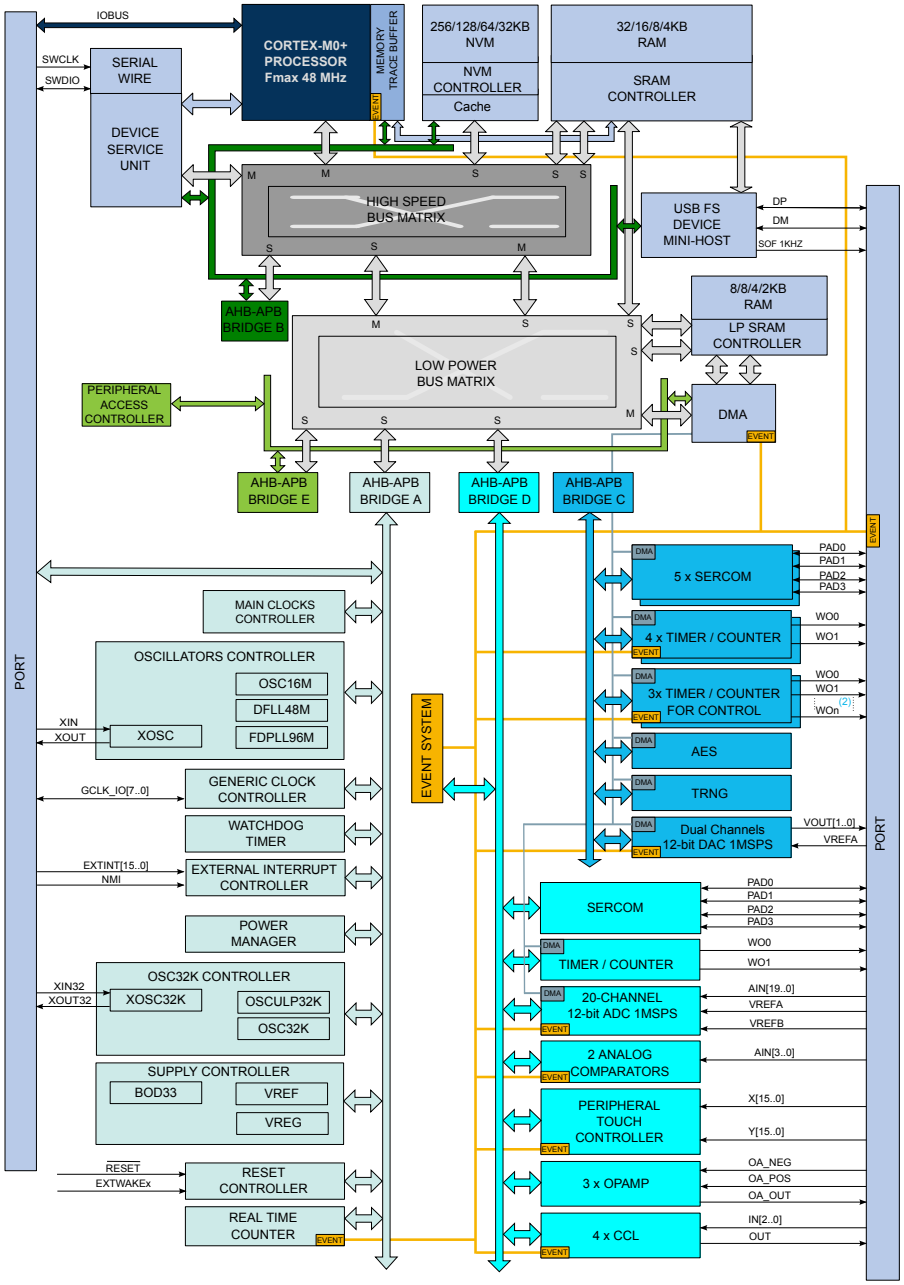
Table 3-4. SAM L21 Device Identification Values

DEVSEL (DID[7:0])	Device
0x00	SAML21J18A
0x01	SAML21J17A
0x02	SAML21J16A
0x03-0x04	Reserved
0x05	SAML21G18A

DEVSEL (DID[7:0])	Device
0x06	SAML21G17A
0x07	SAML21G16A
0x08-0x09	Reserved
0x0A	SAML21E18A
0x0B	SAML21E17A
0x0C	SAML21E16A
0x0D	SAML21E15A
0x0E	Reserved
0x0F	SAML21J18B
0x10	SAML21J17B
0x11	SAML21J16B
0x12-0x13	Reserved
0x14	SAML21G18B
0x15	SAML21G17B
0x16	SAML21G16B
0x17-0x18	Reserved
0x19	SAML21E18B
0x1A	SAML21E17B
0x1B	SAML21E16B
0x1C	SAML21E15B
0x1D-0xFF	Reserved

Note: The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

4. Block Diagram



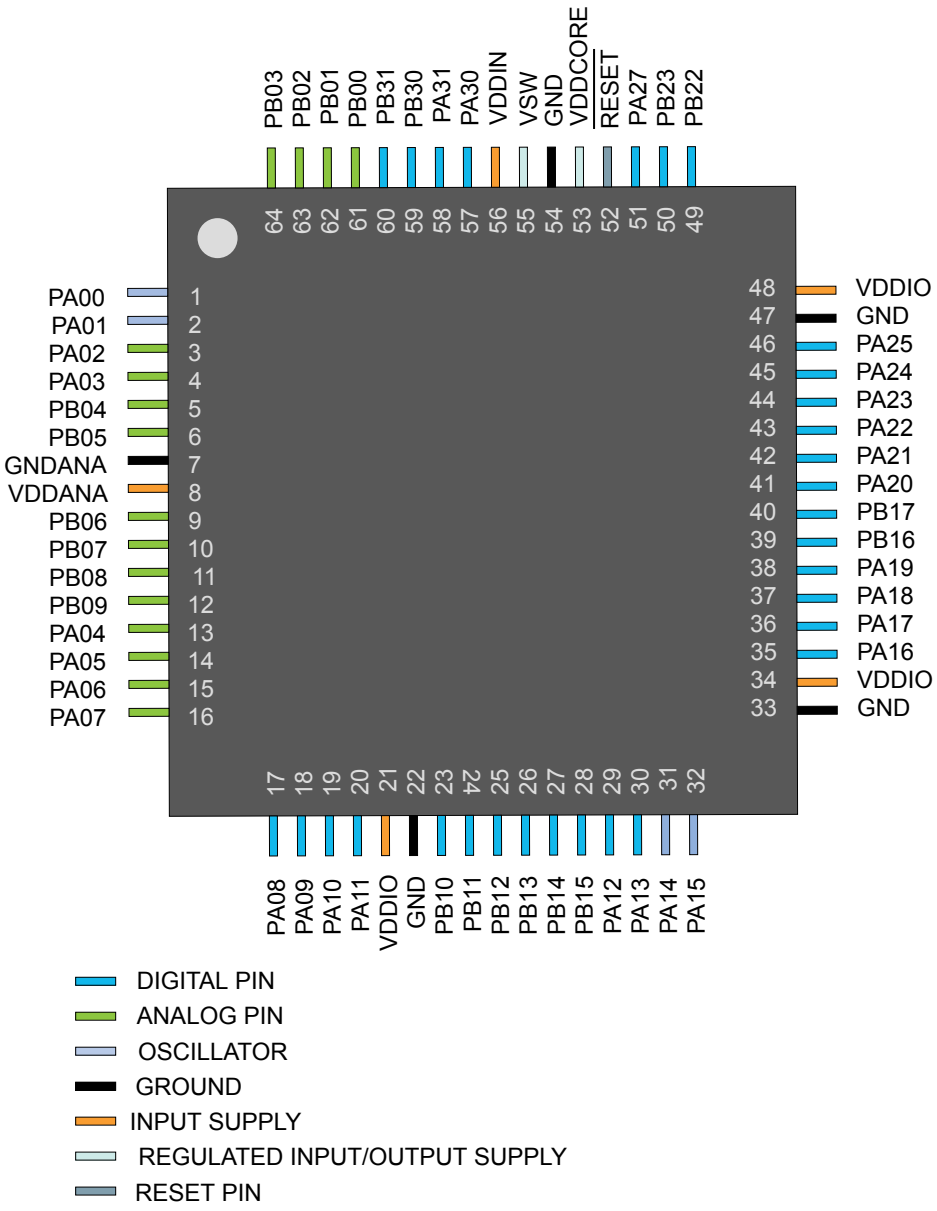
Note:

1. Some products have different number of SERCOM instances, Timer/Counter instances, PTC signals and ADC signals.

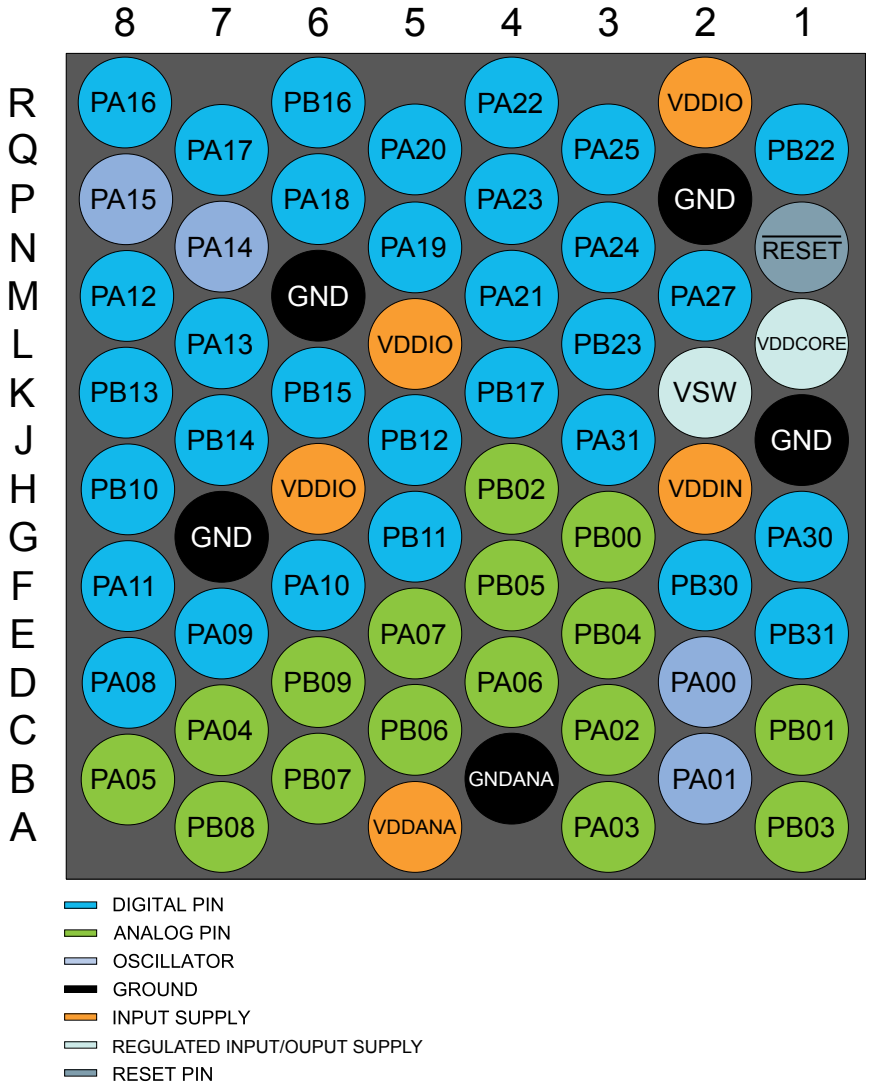
2. The three TCC instances have different configurations, including the number of Waveform Output (WO) lines.

5. Pinout

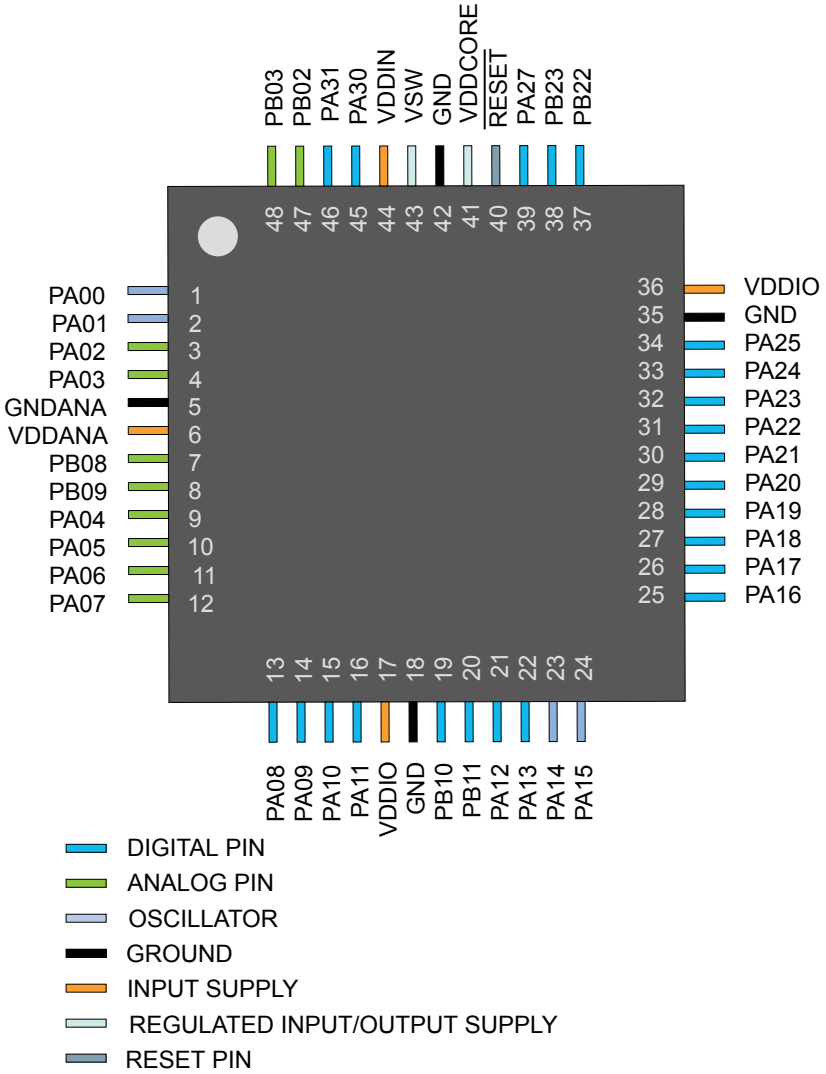
5.1. SAM L21J



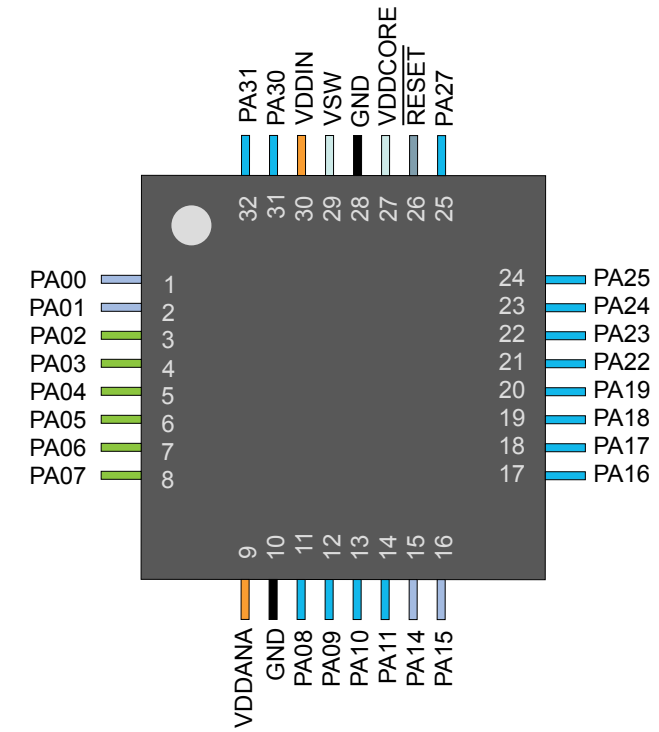
5.2. SAM L21J WLCSP64



5.3. SAM L21G


PB03
PB02
PA31
PA30
VDDIN
VSW
GND
VDDCORE
RESET
PA27
PB23
PB22
48
47
46
45
44
43
42
41
40
39
38
37
PA00
PA01
PA02
PA03
GNDANA
VDDANA
PB08
PB09
PA04
PA05
PA06
PA07
1
2
3
4
5
6
7
8
9
10
11
12
36
35
34
33
32
31
30
29
28
27
26
25
VDDIO
GND
PA25
PA24
PA23
PA22
PA21
PA20
PA19
PA18
PA17
PA16
13
14
15
16
17
18
19
20
21
22
23
24
PA08
PA09
PA10
PA11
VDDIO
GND
PB10
PB11
PA12
PA13
PA14
PA15
DIGITAL PIN
ANALOG PIN
OSCILLATOR
GROUND
INPUT SUPPLY
REGULATED INPUT/OUTPUT SUPPLY
RESET PIN

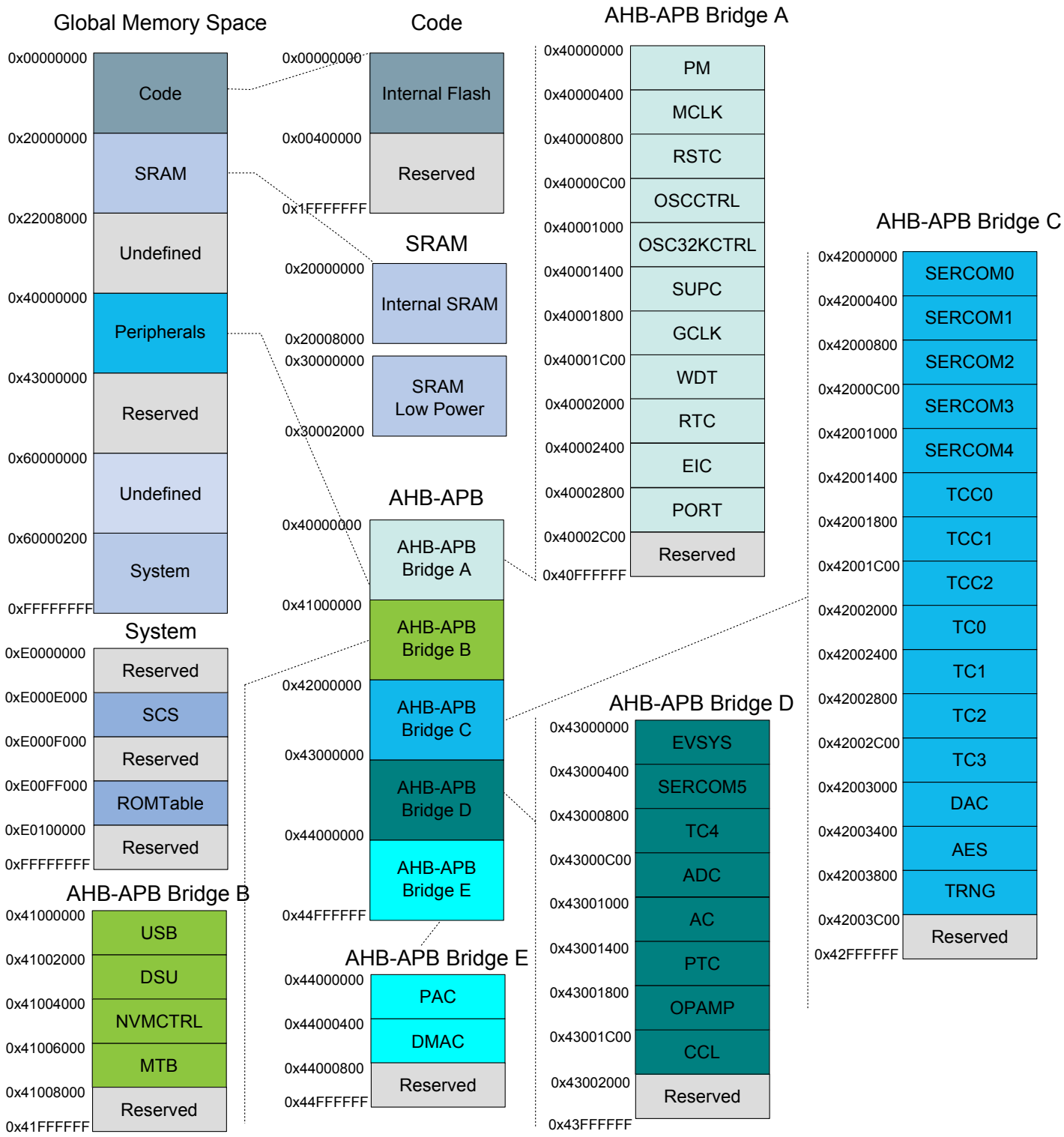
5.4. SAM L21E



- DIGITAL PIN
- ANALOG PIN
- OSCILLATOR
- GROUND
- INPUT SUPPLY
- REGULATED INPUT/OUTPUT SUPPLY
- RESET PIN

6. Product Mapping

Figure 6-1. Atmel SAM L21 Product Mapping



7. Processor and Architecture

7.1. Cortex M0+ Processor

The Atmel SAM L21 implements the ARM®Cortex™-M0+ processor, based on the ARMv6 Architecture and Thumb®-2 ISA. The Cortex M0+ is 100% instruction set compatible with its predecessor, the Cortex-M0 core, and upward compatible to Cortex-M3 and M4 cores. The implemented ARM Cortex-M0+ is revision r0p1. For more information refer to http://www.arm.com

7.1.1. Cortex M0+ Configuration

Table 7-1. Cortex M0+ Configuration in Atmel SAM L21

Features	Cortex M0+ options	Atmel SAM L21 configuration
Interrupts	External interrupts 0-32	29
Data endianness	Little-endian or big-endian	Little-endian
SysTick timer	Present or absent	Present
Number of watchpoint comparators	0, 1, 2	2
Number of breakpoint comparators	0, 1, 2, 3, 4	4
Halting debug support	Present or absent	Present
Multiplier	Fast or small	Fast (single cycle)
Single-cycle I/O port	Present or absent	Present
Wake-up interrupt controller	Supported or not supported	Not supported
Vector Table Offset Register	Present or absent	Present
Unprivileged/Privileged support	Present or absent	Absent - All software run in privileged mode only
Memory Protection Unit	Not present or 8-region	Not present
Reset all registers	Present or absent	Absent
Instruction fetch width	16-bit only or mostly 32-bit	32-bit

The ARM Cortex-M0+ core has two bus interfaces:

- Single 32-bit AMBA-3 AHB-Lite system interface that provides connections to peripherals and all system memory including Flash memory and RAM
- Single 32-bit I/O port bus interfacing to the PORT with 1-cycle loads and stores

7.1.1.1. Cortex M0+ Peripherals

- System Control Space (SCS)
  - The processor provides debug through registers in the SCS. Refer to the Cortex-M0+ Technical Reference Manual for details (http://www.arm.com)
- Nested Vectored Interrupt Controller (NVIC)

- External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC and the Cortex-M0+ processor core are closely coupled, providing low latency interrupt processing and efficient processing of late arriving interrupts. Refer to the Cortex-M0+ Technical Reference Manual for details (http://www.arm.com).
  Note: When the CPU frequency is much higher than the APB frequency it is recommended to insert a memory read barrier after each CPU write to registers mapped on the APB. Failing to do so in such conditions may lead to unexpected behavior such as e.g. re-entering a peripheral interrupt handler just after leaving it.

- System Timer (SysTick)
  - The System Timer is a 24-bit timer clocked by CLK_CPU that extends the functionality of both the processor and the NVIC. Refer to the Cortex-M0+ Technical Reference Manual for details (http://www.arm.com).
- System Control Block (SCB)
  - The System Control Block provides system implementation information, and system control. This includes configuration, control, and reporting of the system exceptions. Refer to the Cortex-M0+ Devices Generic User Guide for details (http://www.arm.com)
- Micro Trace Buffer (MTB)
  - The CoreSight MTB-M0+ (MTB) provides a simple execution trace capability to the Cortex-M0+ processor. Refer to section MTB-Micro Trace Buffer and the CoreSight MTB-M0+ Technical Reference Manual for details (http://www.arm.com).

Related Links

Nested Vector Interrupt Controller on page 21

7.1.1.2. Cortex M0+ Address Map

Table 7-2. Cortex-M0+ Address Map

Address	Peripheral
0xE000E000	System Control Space (SCS)
0xE000E010	System Timer (SysTick)
0xE000E100	Nested Vectored Interrupt Controller (NVIC)
0xE000ED00	System Control Block (SCB)
0x41006000	Micro Trace Buffer (MTB)

7.1.1.3. I/O Interface

The device allows direct access to PORT registers. Accesses to the AMBA® AHB-Lite™ and the single cycle I/O interface can be made concurrently, so the Cortex M0+ processor can fetch the next instructions while accessing the I/Os. This enables single cycle I/O access to be sustained for as long as necessary.

7.2. Nested Vector Interrupt Controller

7.2.1. Overview

The Nested Vectored Interrupt Controller (NVIC) in the SAM L21 supports 32 interrupt lines with four different priority levels. For more details, refer to the Cortex-M0+ Technical Reference Manual (http://www.arm.com).

7.2.2. Interrupt Line Mapping

Each of the 28 interrupt lines is connected to one peripheral instance, as shown in the table below. Each peripheral can have one or more interrupt flags, located in the peripheral's Interrupt Flag Status and Clear (INTFLAG) register.

An interrupt flag is set when the interrupt condition occurs. Each interrupt in the peripheral can be individually enabled by writing a 1 to the corresponding bit in the peripheral's Interrupt Enable Set (INTENSET) register, and disabled by writing 1 to the corresponding bit in the peripheral's Interrupt Enable Clear (INTENCLR) register.

An interrupt request is generated from the peripheral when the interrupt flag is set and the corresponding interrupt is enabled.

The interrupt requests for one peripheral are ORed together on system level, generating one interrupt request for each peripheral. An interrupt request will set the corresponding interrupt pending bit in the NVIC interrupt pending registers (SETPEND/CLRPEND bits in ISPR/ICPR).

For the NVIC to activate the interrupt, it must be enabled in the NVIC interrupt enable register (SETENA/CLRENA bits in ISER/ICER). The NVIC interrupt priority registers IPR0-IPR7 provide a priority field for each interrupt.

Table 7-3. Interrupt Line Mapping

Peripheral source	NVIC line
EIC NMI – External Interrupt Controller	NMI
PM – Power Manager MCLK - Main Clock OSCCTRL - Oscillators Controller OSC32KCTRL - 32KHz Oscillators Controller SUPC - Supply Controller PAC - Protecion Access Controller	0
WDT – Watchdog Timer	1
RTC – Real Time Counter	2
EIC – External Interrupt Controller	3
NVMCTRL – Non-Volatile Memory Controller	4
DMAC - Direct Memory Access Controller	5
USB - Universal Serial Bus	6
EVSYS – Event System	7
SERCOM0 – Serial Communication Interface 0	8
SERCOM1 – Serial Communication Interface 1	9
SERCOM2 – Serial Communication Interface 2	10
SERCOM3 – Serial Communication Interface 3	11
SERCOM4 – Serial Communication Interface 4	12

Peripheral source	NVIC line
SERCOM5 – Serial Communication Interface 5	13
TCC0 – Timer Counter for Control 0	14
TCC1 – Timer Counter for Control 1	15
TCC2 – Timer Counter for Control 2	16
TC0 – Timer Counter 0	17
TC1 – Timer Counter 1	18
TC2 – Timer Counter 2	19
TC3 – Timer Counter 3	20
TC4 – Timer Counter 4	21
ADC – Analog-to-Digital Converter	22
AC – Analog Comparator	23
DAC – Digital-to-Analog Converter	24
PTC – Peripheral Touch Controller	25
AES - Advanced Encrytpion Standard module	26
TRNG - True Random Number Generator	27

7.3. Micro Trace Buffer

7.3.1. Features

- Program flow tracing for the Cortex-M0+ processor
- MTB SRAM can be used for both trace and general purpose storage by the processor
- The position and size of the trace buffer in SRAM is configurable by software
- CoreSight compliant

7.3.2. Overview

When enabled, the MTB records the changes in program flow that are reported by the Cortex-M0+ processor over the execution trace interface. This interface is shared between the Cortex-M0+ processor and the CoreSight MTB-M0+. The information is stored by the MTB in the SRAM as trace packets. An off-chip debugger can extract the trace information using the Debug Access Port to read the trace information from the SRAM. The debugger can then reconstruct the program flow from this information.

The MTB stores trace information into the SRAM and gives the processor access to the SRAM simultaneously. The MTB ensures that trace write accesses have priority over processor accesses.

An execution trace packet consists of a pair of 32-bit words that the MTB generates when it detects a non-sequential change of the program pounter (PC) value. A non-sequential PC change can occur during branch instructions or during exception entry. See the CoreSight MTB-M0+ Technical Reference Manual for more details on the MTB execution trace packet format.

Tracing is enabled when the MASTER.EN bit in the Master Trace Control Register is 1. There are various ways to set the bit to 1 to start tracing, or to 0 to stop tracing. See the CoreSight Cortex-M0+ Technical Reference Manual for more details on the Trace start and stop and for a detailed description of the MTB's

MASTER register. The MTB can be programmed to stop tracing automatically when the memory fills to a specified watermark level or to start or stop tracing by writing directly to the MASTER.EN bit. If the watermark mechanism is not being used and the trace buffer overflows, then the buffer wraps around overwriting previous trace packets.

The base address of the MTB registers is 0x41006000; this address is also written in the CoreSight ROM Table. The offset of each register from the base address is fixed and as defined by the CoreSight MTB-M0+ Technical Reference Manual. The MTB has four programmable registers to control the behavior of the trace features:

- POSITION: Contains the trace write pointer and the wrap bit
- MASTER: Contains the main trace enable bit and other trace control fields
- FLOW: Contains the WATERMARK address and the AUTOSTOP and AUTOHALT control bits
- BASE: Indicates where the SRAM is located in the processor memory map. This register is provided to enable auto discovery of the MTB SRAM location by a debug agent

See the CoreSight MTB-M0+ Technical Reference Manual for a detailed description of these registers.

7.4. High-Speed Bus System

7.4.1. Features

High-Speed Bus Matrix has the following features:

- Symmetric crossbar bus switch implementation
- Allows concurrent accesses from different masters to different slaves
- 32-bit data bus
- Operation at a one-to-one clock frequency with the bus masters

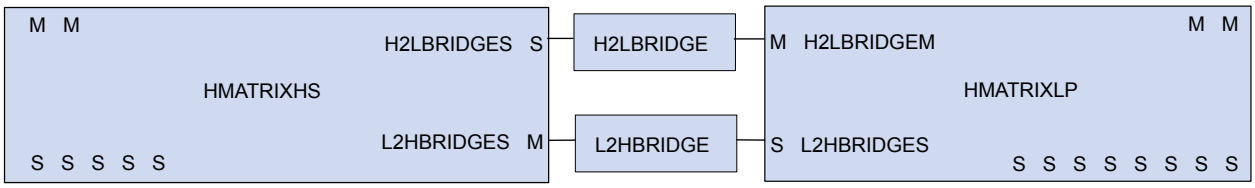
H2LBRIDGE has the following features:

- LP clock division support
- Write: Posted-write FIFO of 3 words, no bus stall until it is full
- Write: 1 cycle bus stall when full when LP clock is not divided
- 2 stall cycles on read when LP clock is not divided
- Ultra low latency mode:
  - Suitable when the HS clock frequency is not above half the maximum device clock frequency
  - Removes all intrinsic bridge stall cycles (except those needed for LP clock ratio adaptation)
  - Enabled by writing a '1' in 0x41008120 using a 32-bit write access

L2HBRIDGE has the following features:

- LP clock division support
- Write: Posted-write FIFO of 1 word, no bus stall until it is full
- Write: 1 cycle bus stall when full when LP clock is not divided
- 2 stall cycles on read when LP clock is not divided
- ultra low latency mode:
  - Suitable when the HS clock frequency is not above half the maximum device clock frequency
  - Removes all intrinsic bridge stall cycles (except those needed for LP clock ratio adaptation)
  - Enabled by writing a '1' in 0x41008120 using a 32-bit write access

Figure 7-1. High-Speed Bus System Components



7.4.2. Configuration

Figure 7-2. Master-Slave Relations High-Speed Bus Matrix

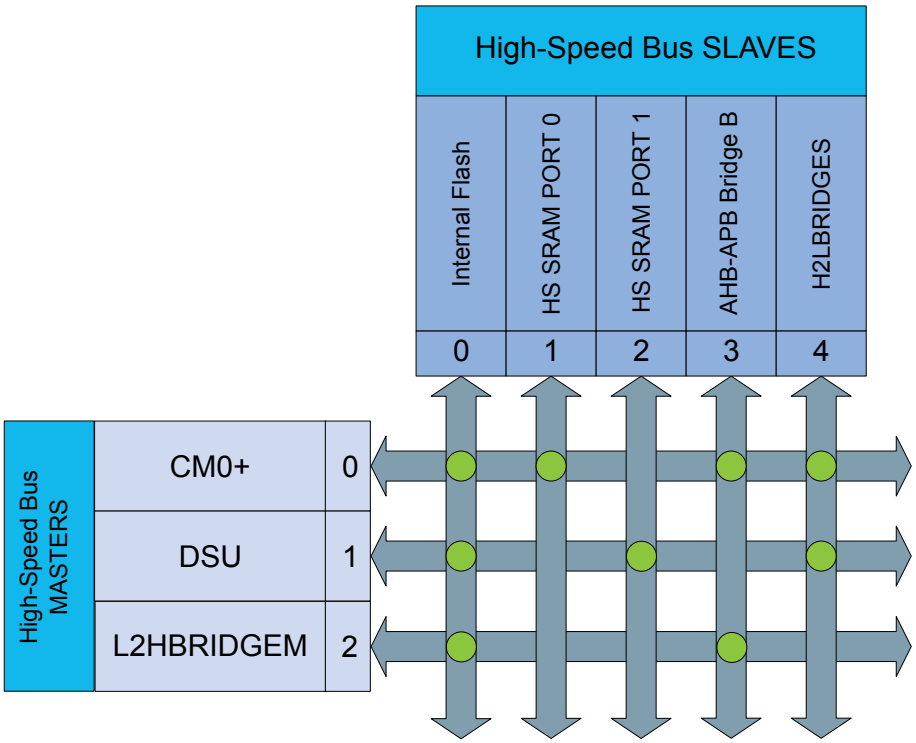


Figure 7-3. Master-Slave Relations Low-Power Bus Matrix

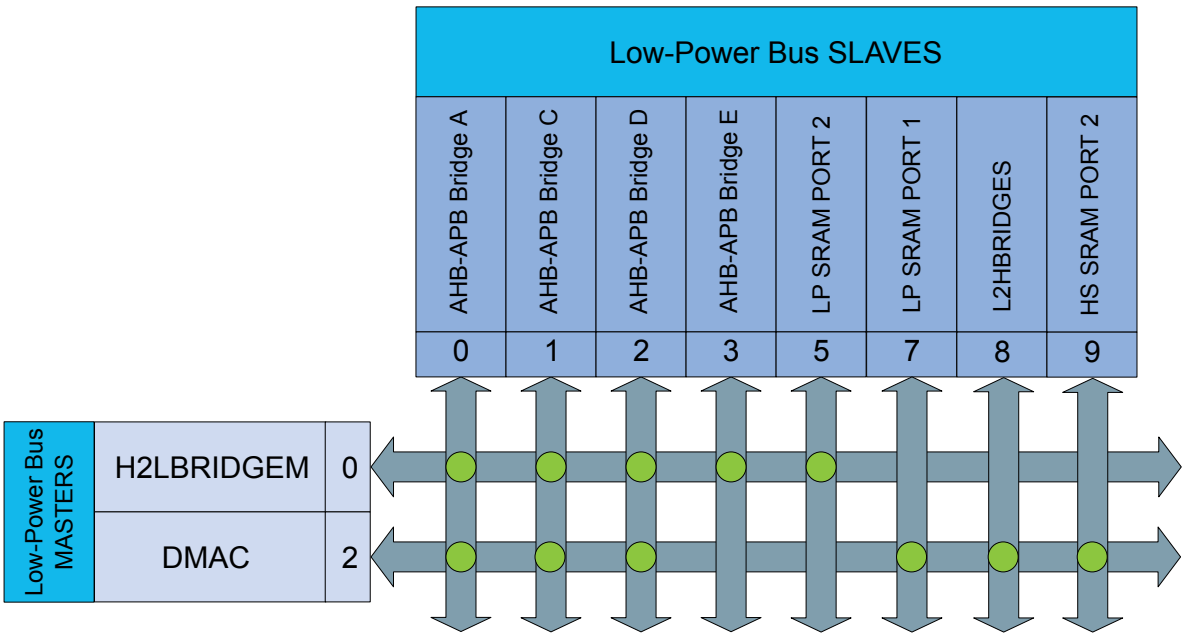


Table 7-4. High-Speed Bus Matrix Masters

High-Speed Bus Matrix Masters	Master ID
CM0+ - Cortex M0+ Processor	0
DSU - Device Service Unit	1
L2HBRIDGEM - Low-Power to High-Speed bus matrix AHB to AHB bridge	2

Table 7-5. High-Speed Bus Matrix Slaves

High-Speed Bus Matrix Slaves	Slave ID
Internal Flash Memory	0
HS SRAM Port 0 - CM0+ Access	1
HS SRAM Port 1 - DSU Access	2
AHB-APB Bridge B	3
H2LBRIDGES - High-Speed to Low-Power bus matrix AHB to AHB bridge	4

Table 7-6. Low-Power Bus Matrix Masters

Low-Power Bus Matrix Masters	Master ID
H2LBRIDGEM - High-Speed to Low-Power bus matrix AHB to AHB bridge	0
DMAC - Direct Memory Access Controller - Data Access	2

Table 7-7. Low-Power Bus Matrix Slaves

Low-Power Bus Matrix Slaves	Slave ID
AHB-APB Bridge A	0
AHB-APB Bridge C	1
AHB-APB Bridge D	2
AHB-APB Bridge E	3
LP SRAM Port 2- H2LBRIDGEM access	5
LP SRAM Port 1- DMAC access	7
L2HBRIDGES - Low-Power to High-Speed bus matrix AHB to AHB bridge	8
HS SRAM Port 2- HMATRIXLP access	9

7.4.3. SRAM Quality of Service

To ensure that masters with latency requirements get sufficient priority when accessing RAM, priority levels can be assigned to the masters for different types of access.

The Quality of Service (QoS) level is independently selected for each master accessing the RAM. For any access to the RAM, the RAM also receives the QoS level. The QoS levels and their corresponding bit values for the QoS level configuration are shown in the following table.

Table 7-8. Quality of Service

Value	Name	Description
0x0	DISABLE	Background (no sensitive operation)
0x1	LOW	Sensitive Bandwidth
0x2	MEDIUM	Sensitive Latency
0x3	HIGH	Critical Latency

If a master is configured with QoS level DISABLE (0x0) or LOW (0x1) there will be a minimum latency of one cycle for the RAM access.

The priority order for concurrent accesses are decided by two factors. First, the QoS level for the master and second, a static priority given by the port ID. The lowest port ID has the highest static priority. See the tables below for details.

The MTB has a fixed QoS level HIGH (0x3).

The CPU QoS level can be written/read, using 32-bit access only, at address 0x41008114 bits [1:0]. Its reset value is 0x3.

Refer to different master QOSCTRL registers for configuring QoS for the other masters (USB, DMAC).

Table 7-9. HS SRAM Port Connections QoS

HS SRAM Port Connection	Port ID	Connection Type	QoS	default QoS
MTB - Micro Trace Buffer	4	Direct	STATIC-3	0x3
USB - Universal Serial Bus	3	Direct	IP-QOSCTRL	0x3
HMATRIXLP - Low-Power Bus Matrix	2	Bus Matrix	0x44000934(1), bits[1:0]	0x2
DSU - Device Service Unit	1	Bus Matrix	0x4100201C(1)	0x2
CM0+ - Cortex M0+ Processor	0	Bus Matrix	0x41008114(1), bits[1:0]	0x3

Note:

1. Using 32-bit access only.

Table 7-10. LP SRAM Port Connections QoS

LP SRAM Port Connection	Port ID	Connection Type	QoS	default QoS
DMAC - Direct Memory Access Controller - Write-Back Access	5, 6	Direct	IP-QOSCTRL.WRBQOS	0x2
DMAC - Direct Memory Access Controller - Fetch Access	3, 4	Direct	IP-QOSCTRL.FQOS	0x2

LP SRAM Port Connection	Port ID	Connection Type	QoS	default QoS
H2LBRIDGEM - HS to LP bus matrix AHB to AHB bridge	2	Bus Matrix	0x44000924(1), bits[1:0]	0x2
DMAC - Direct Memory Access Controller - Data Access	1	Bus Matrix	IP-QOSCTRL.DQOS	0x2

Note:

1. Using 32-bit access only.

8. Packaging Information

8.1. Thermal Considerations

8.1.1. Thermal Resistance Data

The following table summarizes the thermal resistance data depending on the package.

Table 8-1. Thermal Resistance Data

Package Type	θ_{JA}	θ_{JC}
32-pin TQFP	68°C/W	25.8°C/W
48-pin TQFP	78.8°C/W	12.3°C/W
64-pin TQFP	66.7°C/W	11.9°C/W
32-pin QFN	37.2°C/W	3.1°C/W
48-pin QFN	31.6°C/W	10.3°C/W
64-pin QFN	32.2°C/W	10.1°C/W
64-pin WLCSP	36.8°C/W	5.0°C/W

Related Links

Junction Temperature on page 29

8.1.2. Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

where:

- θ_{JA} = Package thermal resistance, Junction-to-ambient (°C/W), see Thermal Resistance Data
- θ_{JC} = Package thermal resistance, Junction-to-case thermal resistance (°C/W), see Thermal Resistance Data
- $\theta_{HEATSINK}$ = Thermal resistance (°C/W) specification of the external cooling device
- P_D = Device power consumption (W)
- T_A = Ambient temperature (°C)

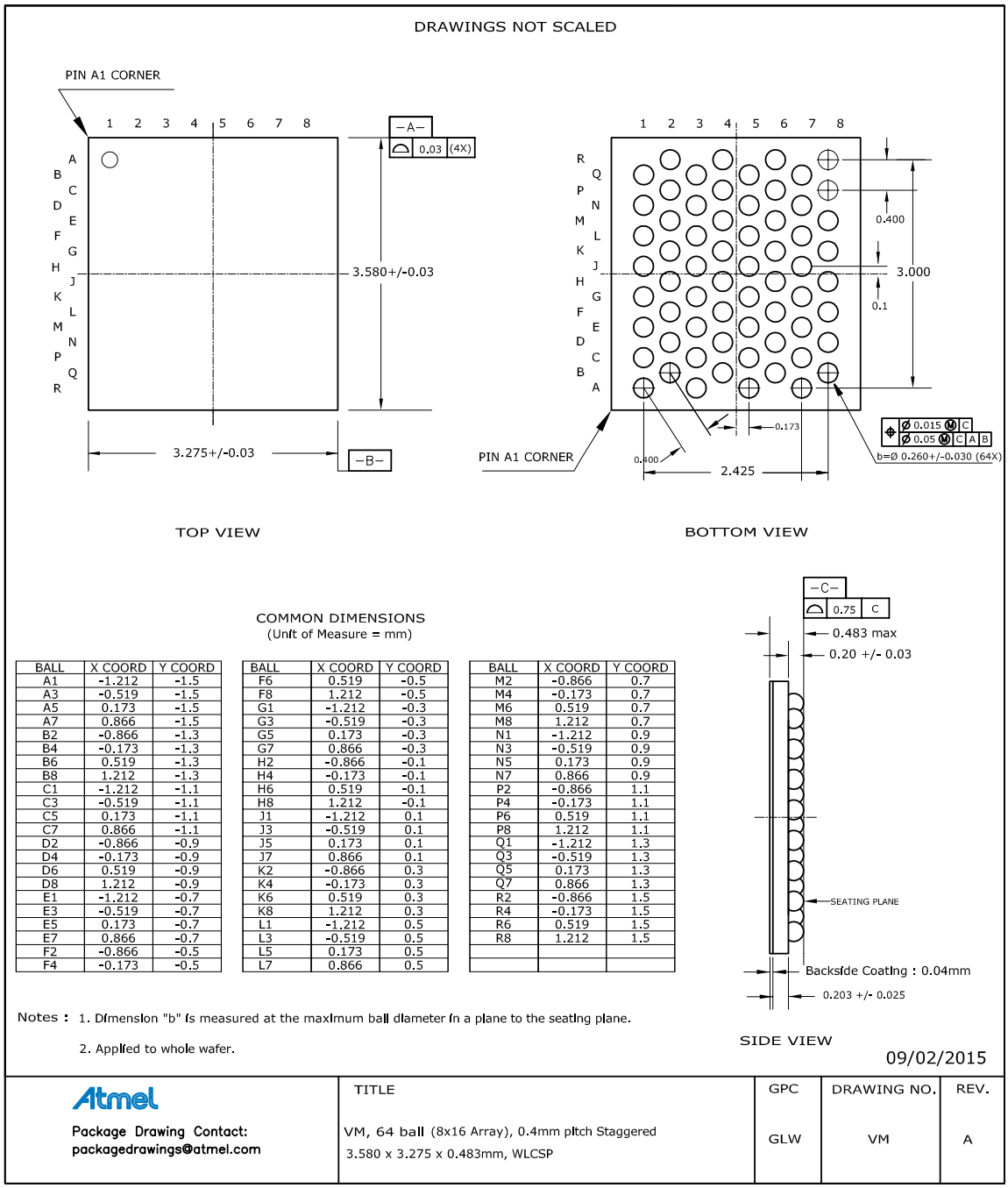
From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

Related Links

Thermal Resistance Data on page 29

8.2. Package Drawings

8.2.1. 64-Ball WLCSP



BALL	X COORD	Y COORD
A1	-1.212	-1.5
A3	-0.519	-1.5
A5	0.173	-1.5
A7	0.866	-1.5
B2	-0.866	-1.3
B4	-0.173	-1.3
B6	0.519	-1.3
B8	1.212	-1.3
C1	-1.212	-1.1
C3	-0.519	-1.1
C5	0.173	-1.1
C7	0.866	-1.1
D2	-0.866	-0.9
D4	-0.173	-0.9
D6	0.519	-0.9
D8	1.212	-0.9
E1	-1.212	-0.7
E3	-0.519	-0.7
E5	0.173	-0.7
E7	0.866	-0.7
F2	-0.866	-0.5
F4	-0.173	-0.5

BALL	X COORD	Y COORD
F6	0.519	-0.5
F8	1.212	-0.5
G1	-1.212	-0.3
G3	-0.519	-0.3
G5	0.173	-0.3
G7	0.866	-0.3
H2	-0.866	-0.1
H4	-0.173	-0.1
H6	0.519	-0.1
H8	1.212	-0.1
J1	-1.212	0.1
J3	-0.519	0.1
J5	0.173	0.1
J7	0.866	0.1
K2	-0.866	0.3
K4	-0.173	0.3
K6	0.519	0.3
K8	1.212	0.3
L1	-1.212	0.5
L3	-0.519	0.5
L5	0.173	0.5
L7	0.866	0.5

BALL	X COORD	Y COORD
M2	-0.866	0.7
M4	-0.173	0.7
M6	0.519	0.7
M8	1.212	0.7
N1	-1.212	0.9
N3	-0.519	0.9
N5	0.173	0.9
N7	0.866	0.9
P2	-0.866	1.1
P4	-0.173	1.1
P6	0.519	1.1
P8	1.212	1.1
Q1	-1.212	1.3
Q3	-0.519	1.3
Q5	0.173	1.3
Q7	0.866	1.3
R2	-0.866	1.5
R4	-0.173	1.5
R6	0.519	1.5
R8	1.212	1.5

Table 8-2. Device and Package Maximum Weight

10	mg

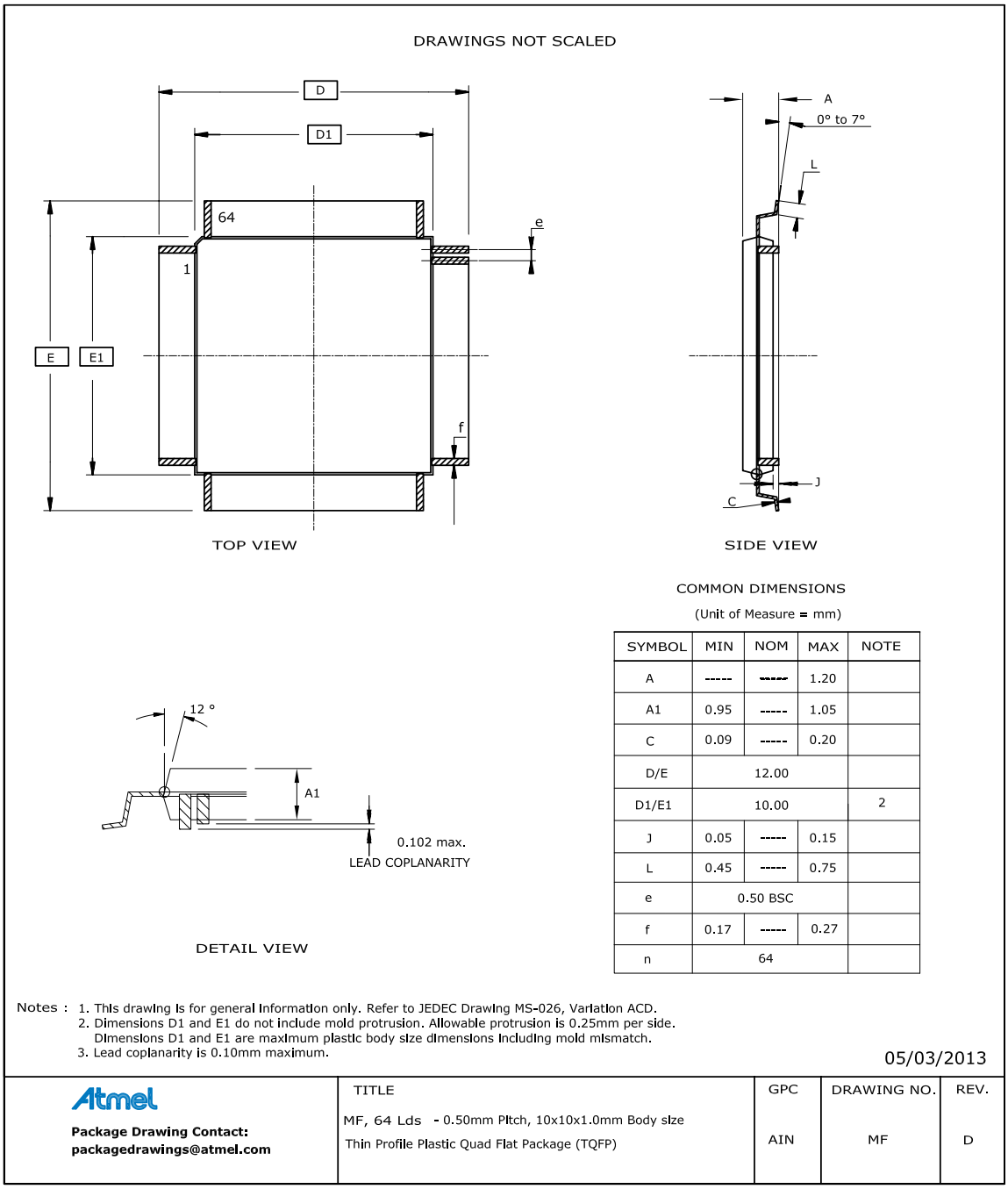
Table 8-3. Package Characteristics

Moisture Sensitivity Level	MSL1

Table 8-4. Package Reference

JEDEC Drawing Reference	N/A
JESD97 Classification	E1

8.2.2. 64 pin TQFP



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.95	-----	1.05	
C	0.09	-----	0.20	
D/E		12.00		
D1/E1		10.00		2
J	0.05	-----	0.15	
L	0.45	-----	0.75	
e		0.50 BSC		
f	0.17	-----	0.27	
n		64		

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ACD.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

05/03/2013

	TITLE	GPC	DRAWING NO.	REV.
Atmel **Package Drawing Contact:** **packagedrawings@atmel.com**	MF, 64 Lds - 0.50mm Pitch, 10x10x1.0mm Body size Thin Profile Plastic Quad Flat Package (TQFP)	AIN	MF	D

Table 8-5. Device and Package Maximum Weight

300	mg

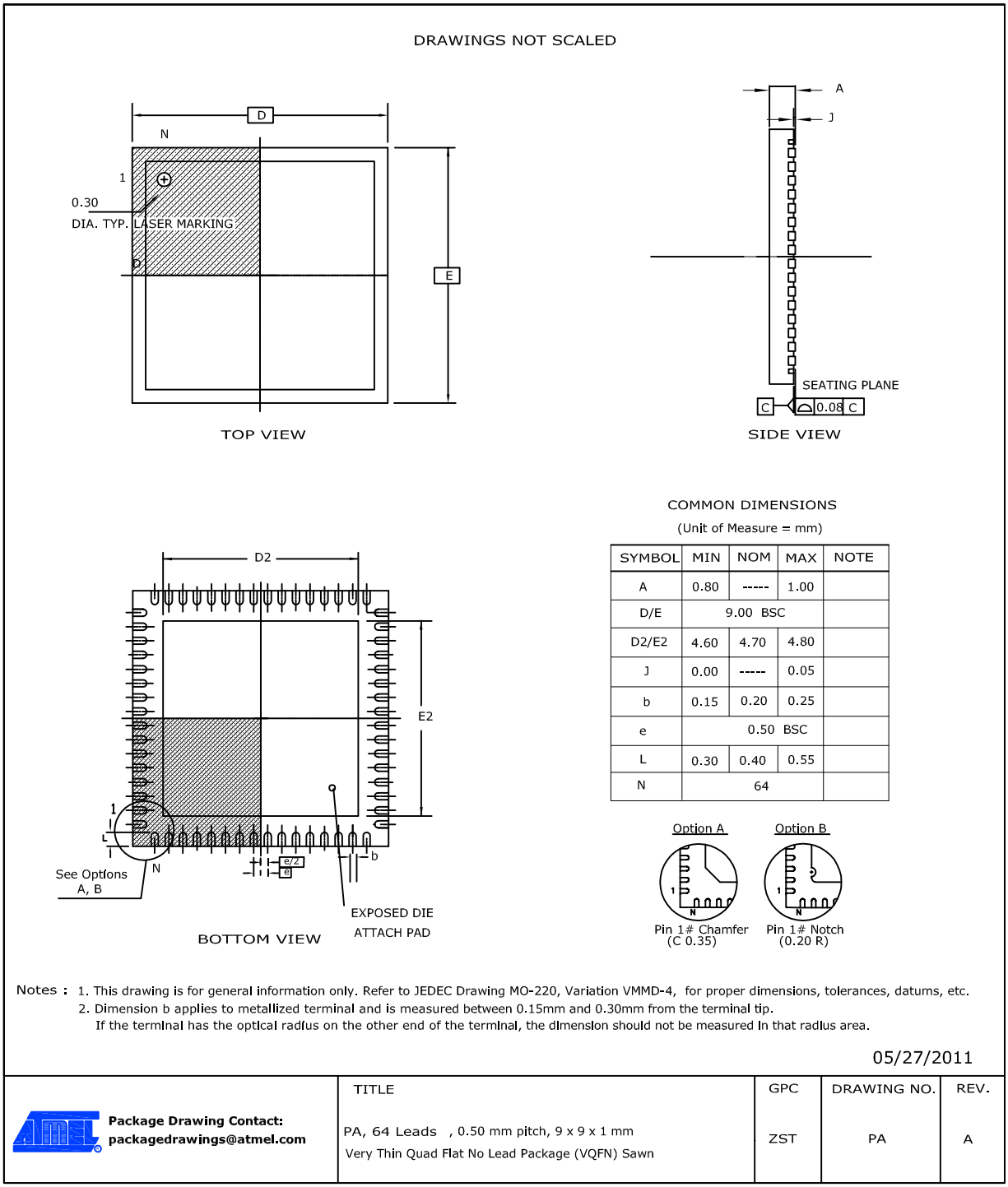
Table 8-6. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 8-7. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

8.2.3. 64 pin QFN



SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	-----	1.00	
D/E		9.00 BSC		
D2/E2	4.60	4.70	4.80	
J	0.00	-----	0.05	
b	0.15	0.20	0.25	
e		0.50 BSC		
L	0.30	0.40	0.55	
N		64		

Note: The exposed die attach pad is not connected electrically inside the device.

Table 8-8. Device and Package Maximum Weight

200	mg

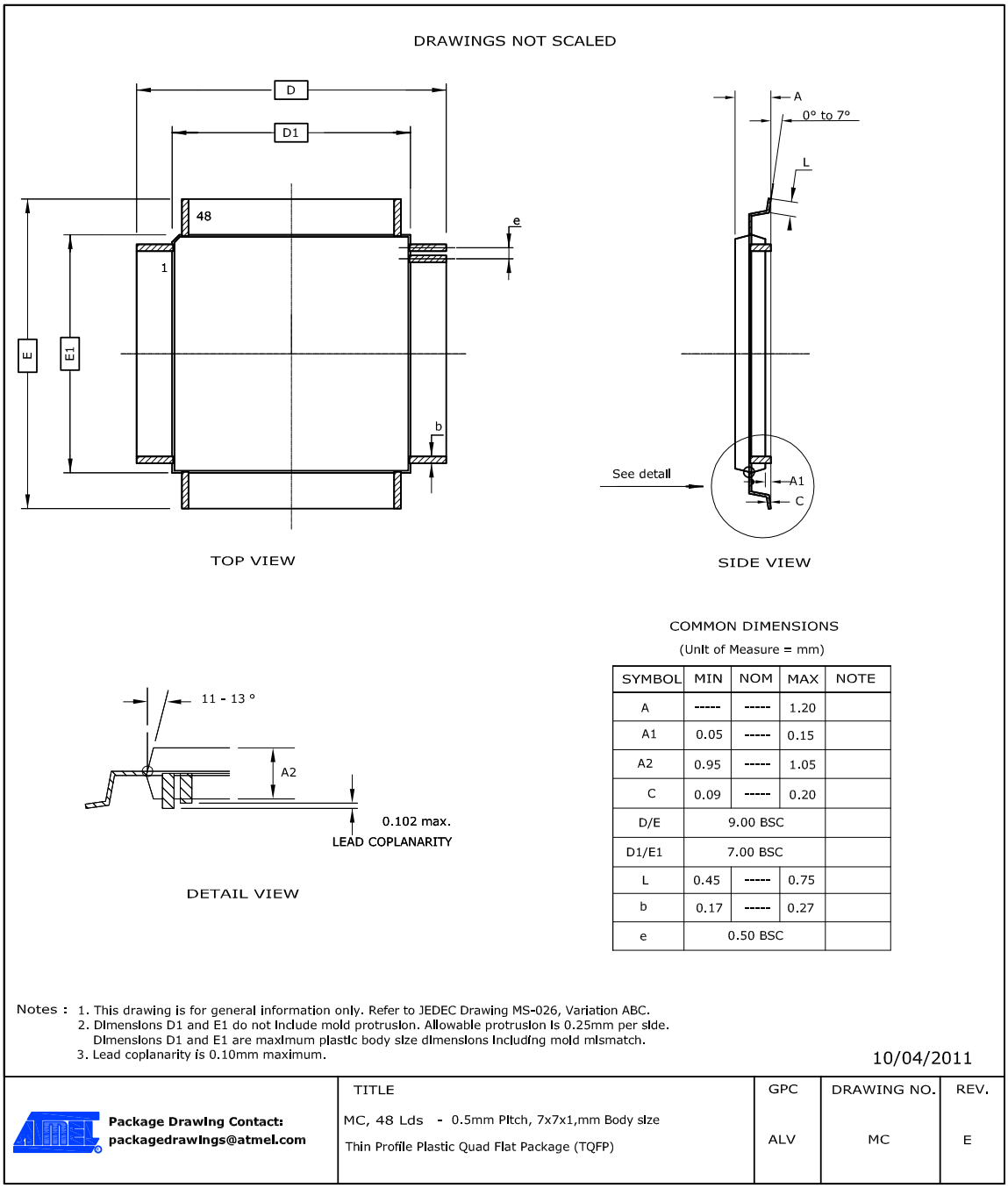
Table 8-9. Package Charateristics

Moisture Sensitivity Level	MSL3

Table 8-10. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

8.2.4. 48 pin TQFP



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.05	-----	0.15	
A2	0.95	-----	1.05	
C	0.09	-----	0.20	
D/E	9.00 BSC			
D1/E1	7.00 BSC			
L	0.45	-----	0.75	
b	0.17	-----	0.27	
e	0.50 BSC			

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ABC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

10/04/2011

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	MC, 48 Lds - 0.5mm Pitch, 7x7x1,mm Body size Thin Profile Plastic Quad Flat Package (TQFP)	ALV	MC	E

Table 8-11. Device and Package Maximum Weight

140	mg

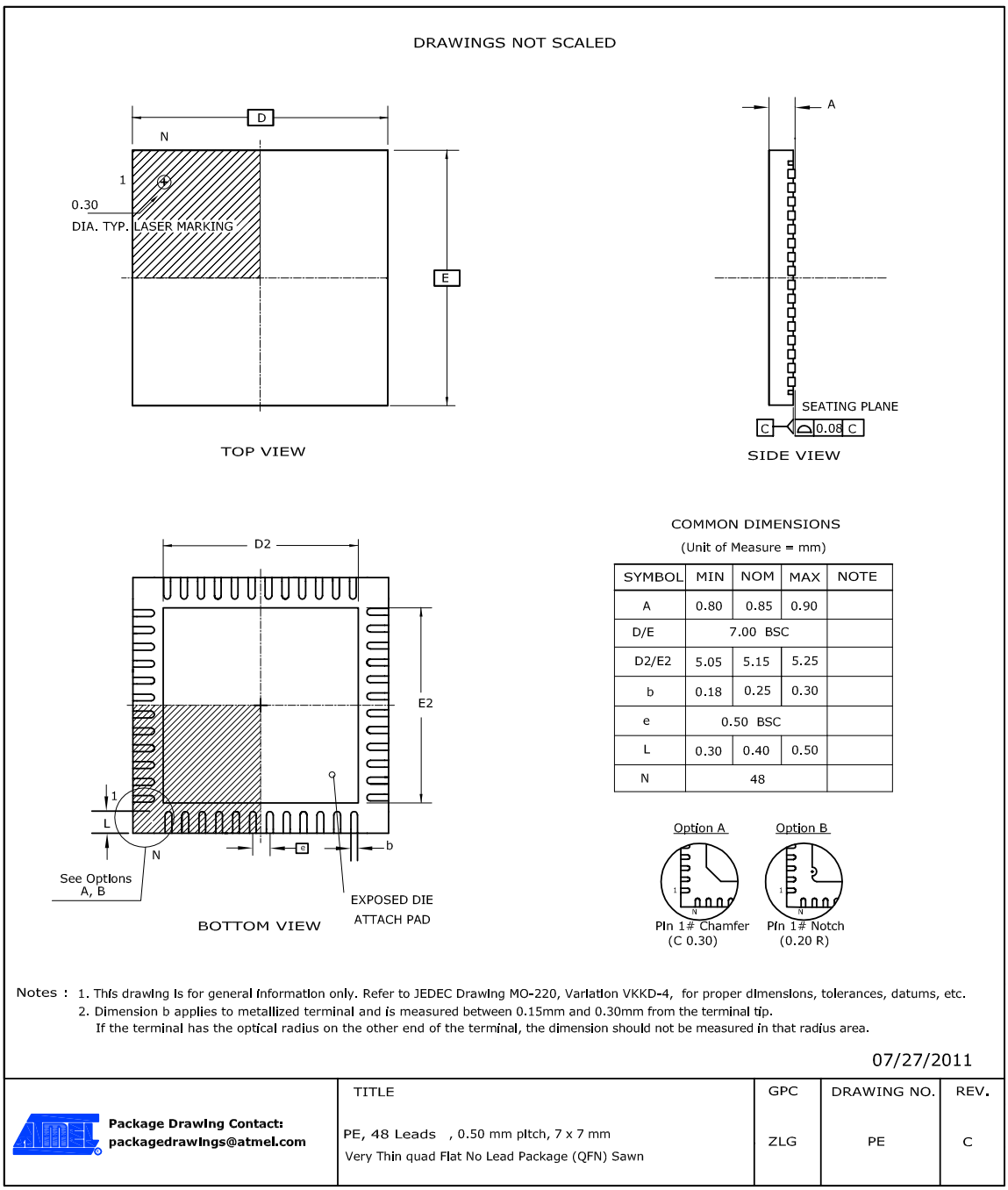
Table 8-12. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 8-13. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

8.2.5. 48 pin QFN



Note: The exposed die attach pad is not connected electrically inside the device.

Table 8-14. Device and Package Maximum Weight

140	mg

Table 8-15. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 8-16. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

8.2.6. 32 pin TQFP

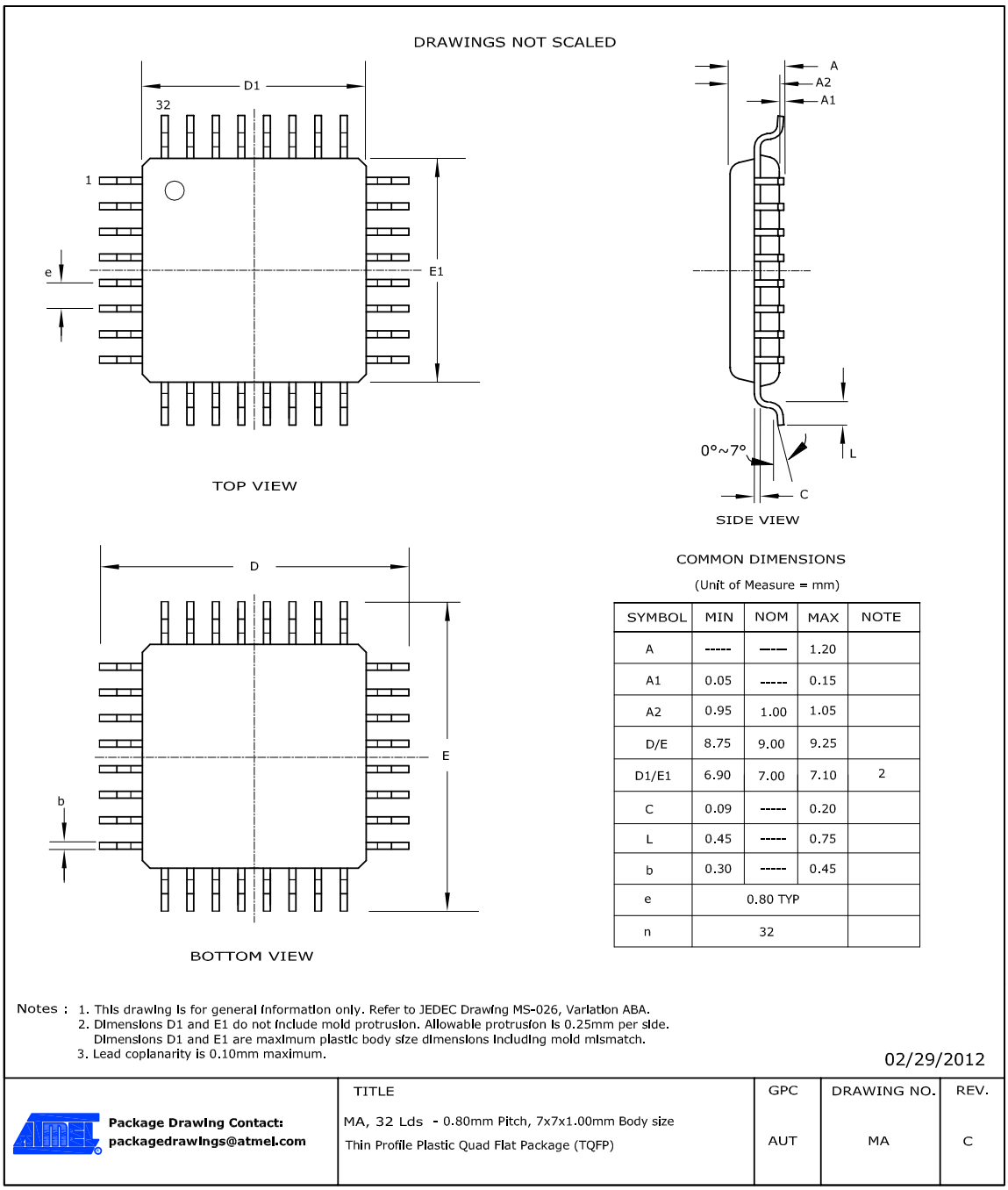


Table 8-17. Device and Package Maximum Weight

100	mg

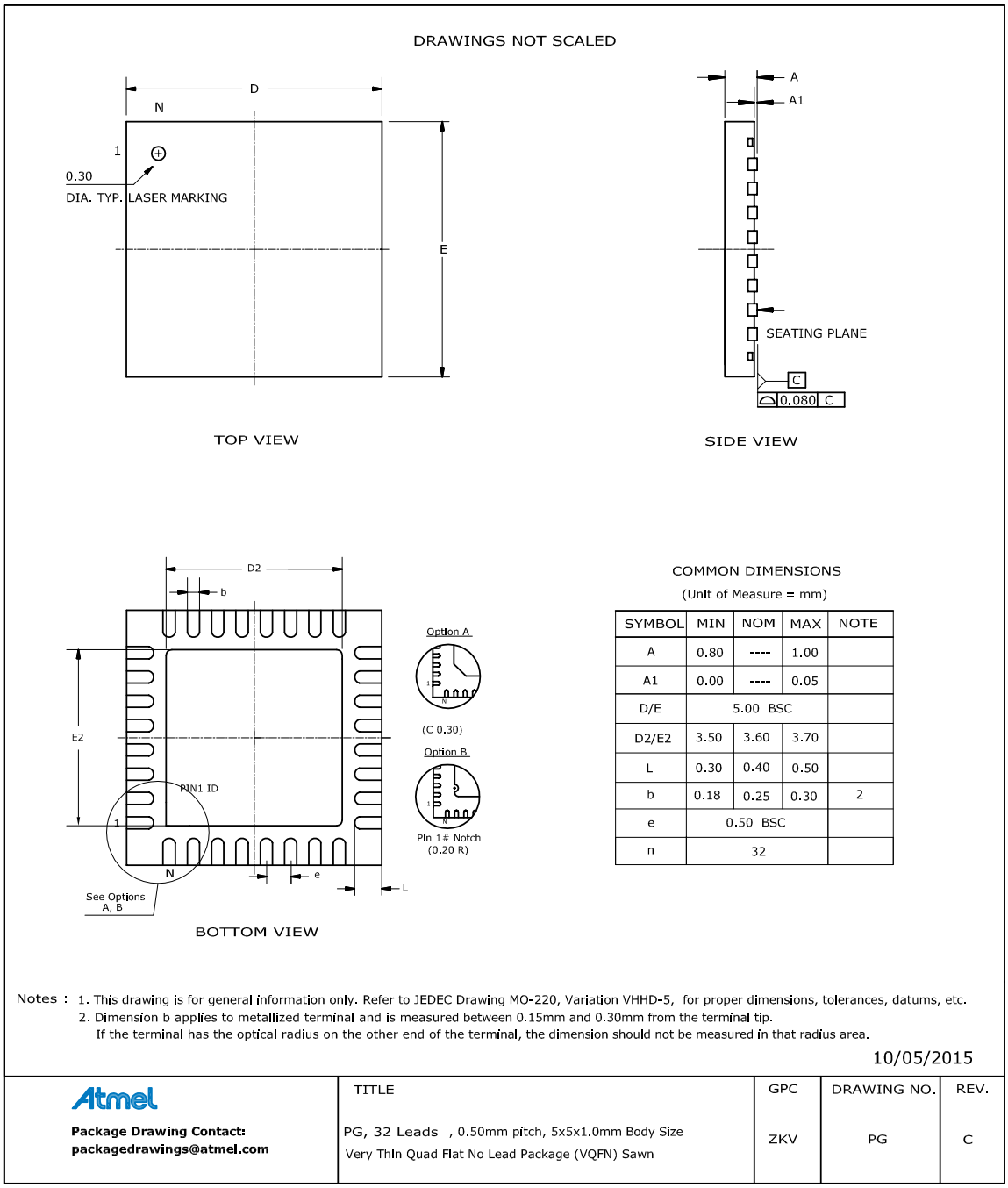
Table 8-18. Package Charateristics

Moisture Sensitivity Level	MSL3

Table 8-19. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

8.2.7. 32 pin QFN



Note: The exposed die attach pad is connected inside the device to GND and GNDANA.

Table 8-20. Device and Package Maximum Weight

90	mg

Table 8-21. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 8-22. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

8.3. Soldering Profile

The following table gives the recommended soldering profile from J-STD-20.

Table 8-23.

Profile Feature	Green Package
Average Ramp-up Rate (217°C to peak)	3°C/s max.
Preheat Temperature 175°C ±25°C	150-200°C
Time Maintained Above 217°C	60-150s
Time within 5°C of Actual Peak Temperature	30s
Peak Temperature Range	260°C
Ramp-down Rate	6°C/s max.
Time 25°C to Peak Temperature	8 minutes max.

A maximum of three reflow passes is allowed per component.

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Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**

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