AT91SAM ARM-based Embedded MPU

SAM9263

Description

The AT91SAM9263 32-bit microcontroller, based on the ARM926EJ-S processor, is architectured on a 9-layer matrix, allowing a maximum internal bandwidth of nine 32-bit buses. It also features two independent external memory buses, EBI0 and EBI1, capable of interfacing with a wide range of memory devices and an IDE hard disk. Two external buses prevent bottlenecks, thus guaranteeing maximum performance.

The AT91SAM9263 embeds an LCD Controller supported by a Two D Graphics Controller and a 2-channel DMA Controller, and one Image Sensor Interface. It also integrates several standard peripherals, such as USART, SPI, TWI, Timer Counters, PWM Generators, Multimedia Card interface and one CAN Controller.

When coupled with an external GPS engine, the AT91SAM9263 provides the ideal solution for navigation systems.

This is a summary document. The complete document is available on the Atmel website at www.atmel.com.

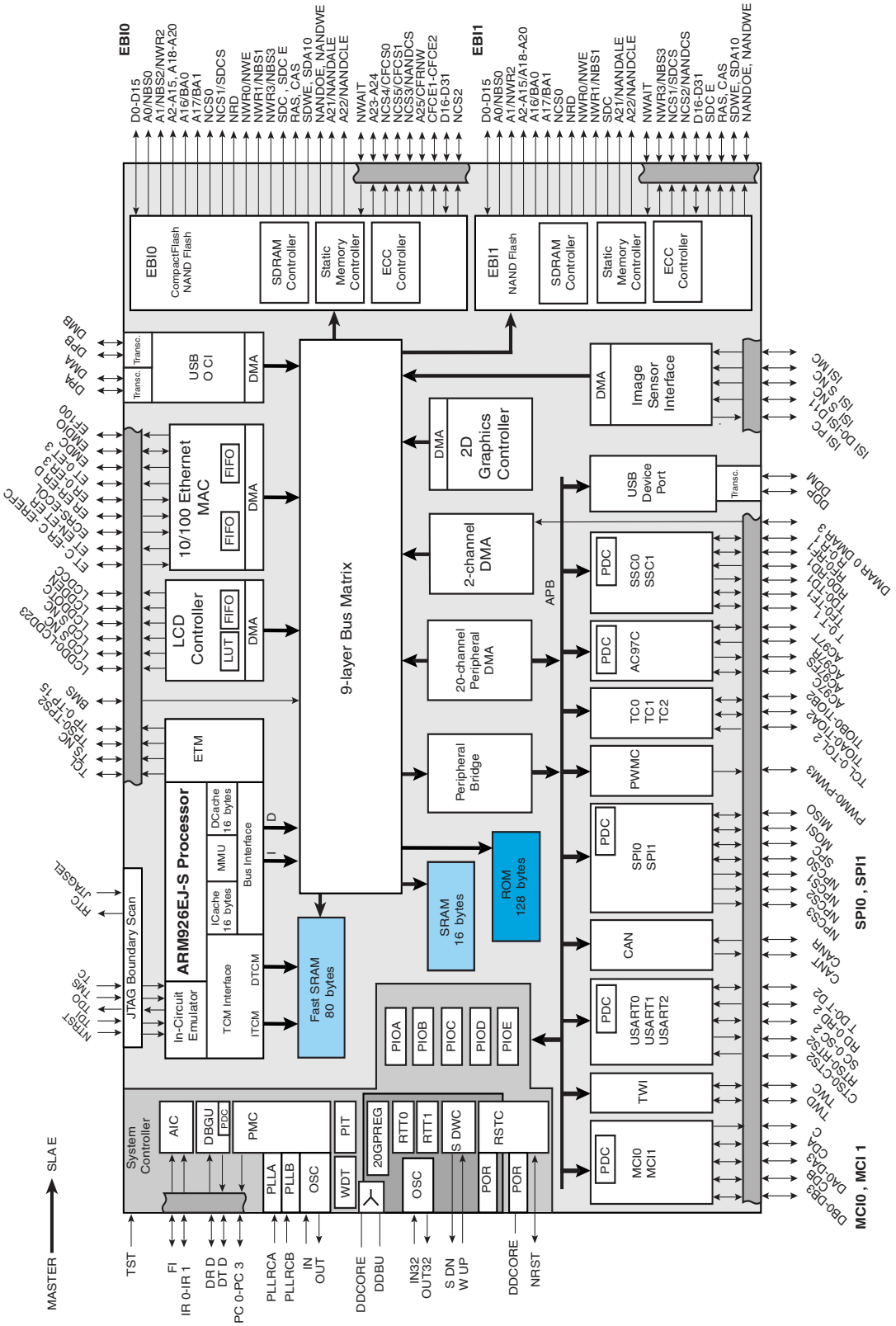
1. Features

- Incorporates the ARM926EJ-S™ ARM® Thumb® Processor
  - DSP Instruction Extensions, Jazelle® Technology for Java® Acceleration
  - 16 Kbyte Data Cache, 16 Kbyte Instruction Cache, Write Buffer
  - 220 MIPS at 200 MHz
  - Memory Management Unit
  - EmbeddedICE™, Debug Communication Channel Support
  - Mid-level Implementation Embedded Trace Macrocell™
- Bus Matrix
  - Nine 32-bit-layer Matrix, Allowing a Total of 28.8 Gbps of On-chip Bus Bandwidth
  - Boot Mode Select Option, Remap Command
- Embedded Memories
  - One 128 Kbyte Internal ROM, Single-cycle Access at Maximum Bus Matrix Speed
  - One 80 Kbyte Internal SRAM, Single-cycle Access at Maximum Processor or Bus Matrix Speed
  - One 16 Kbyte Internal SRAM, Single-cycle Access at Maximum Bus Matrix Speed
- Dual External Bus Interface (EBI0 and EBI1)
  - EBI0 Supports SDRAM, Static Memory, ECC-enabled NAND Flash and CompactFlash®
  - EBI1 Supports SDRAM, Static Memory and ECC-enabled NAND Flash
- DMA Controller (DMAC)
  - Acts as one Bus Matrix Master
  - Embeds 2 Unidirectional Channels with Programmable Priority, Address Generation, Channel Buffering and Control
- Twenty Peripheral DMA Controller Channels (PDC)
- LCD Controller
  - Supports Passive or Active Displays
  - Up to 24 bits per Pixel in TFT Mode, Up to 16 bits per Pixel in STN Color Mode
  - Up to 16M Colors in TFT Mode, Resolution Up to 2048x2048, Supports Virtual Screen Buffers
- Two D Graphics Accelerator
  - Line Draw, Block Transfer, Clipping, Commands Queuing
- Image Sensor Interface
  - ITU-R BT. 601/656 External Interface, Programmable Frame Capture Rate
  - 12-bit Data Interface for Support of High Sensibility Sensors
  - SAV and EAV Synchronization, Preview Path with Scaler, YCbCr Format
- USB 2.0 Full Speed (12 Mbits per second) Host Double Port
  - Dual On-chip Transceivers
  - Integrated FIFOs and Dedicated DMA Channels
- USB 2.0 Full Speed (12 Mbits per second) Device Port
  - On-chip Transceiver, 2,432-byte Configurable Integrated DPRAM
- Ethernet MAC 10/100 Base-T
  - Media Independent Interface or Reduced Media Independent Interface
  - 28-byte FIFOs and Dedicated DMA Channels for Receive and Transmit
- Fully-featured System Controller, including
  - Reset Controller, Shutdown Controller
  - Twenty 32-bit Battery Backup Registers for a Total of 80 Bytes
  - Clock Generator and Power Management Controller
  - Advanced Interrupt Controller and Debug Unit
  - Periodic Interval Timer, Watchdog Timer and Double Real-time Timer
- Reset Controller (RSTC)
  - Based on Two Power-on Reset Cells, Reset Source Identification and Reset Output Control
- Shutdown Controller (SHDWC)
  - Programmable Shutdown Pin Control and Wake-up Circuitry
- Clock Generator (CKGR)
  - 32768Hz Low-power Oscillator on Battery Backup Power Supply, Providing a Permanent Slow Clock

  - 3 to 20 MHz On-chip Oscillator and Two Up to 240 MHz PLLs
- Power Management Controller (PMC)
  - Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
  - Four Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - Two External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
  - 2-wire UART and Support for Debug Communication Channel, Programmable ICE Access Prevention
  - Mode for General Purpose Two-wire UART Serial Communication
- Periodic Interval Timer (PIT)
  - 20-bit Interval Timer plus 12-bit Interval Counter
- Watchdog Timer (WDT)
  - Key-protected, Programmable Only Once, Windowed 16-bit Counter Running at Slow Clock
- Two Real-time Timers (RTT)
  - 32-bit Free-running Backup Counter Running at Slow Clock with 16-bit Prescaler
- Five 32-bit Parallel Input/Output Controllers (PIOA, PIOB, PIOC, PIOD and PIOE)
  - 160 Programmable I/O Lines Multiplexed with Up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
- One Part 2.0A and Part 2.0B-compliant CAN Controller
  - 16 Fully-programmable Message Object Mailboxes, 16-bit Time Stamp Counter
- Two Multimedia Card Interface (MCI)
  - SDCard/SDIO and MultiMediaCard™ Compliant
  - Automatic Protocol Control and Fast Automatic Data Transfers with PDC
  - Two SDCard Slots Support on eAch Controller
- Two Synchronous Serial Controllers (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I²S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- One AC97 Controller (AC97C)
  - 6-channel Single AC97 Analog Front End Interface, Slot Assigner
- Three Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation, Manchester Encoding/Decoding
  - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
- Two Master/Slave Serial Peripheral Interface (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
- One Three-channel 16-bit Timer/Counters (TC)
  - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- One Four-channel 16-bit PWM Controller (PWMC)
- One Two-wire Interface (TWI)
  - Master Mode Support, All Two-wire Atmel® EEPROMs Supported
- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- Required Power Supplies
  - 1.08V to 1.32V for VDDCORE and VDDBU
  - 3.0V to 3.6V for VDDOSC and VDDPLL
  - 2.7V to 3.6V for VDDIOP0 (Peripheral I/Os)
  - 1.65V to 3.6V for VDDIOP1 (Peripheral I/Os)
  - Programmable 1.65V to 1.95V or 3.0V to 3.6V for VDDIOM0/VDDIOM1 (Memory I/Os)
- Available in a 324-ball TFBGA Green Package

2. AT91SAM9263 Block Diagram

Figure 2-1. AT91SAM9263 Block Diagram



3. Signal Description

Table 3-1 gives details on the signal name classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
Power Supplies				
VDDIOM0	EBI0 I/O Lines Power Supply	Power		1.65V to 3.6V
VDDIOM1	EBI1 I/O Lines Power Supply	Power		1.65V to 3.6V
VDDIOP0	Peripherals I/O Lines Power Supply	Power		2.7V to 3.6V
VDDIOP1	Peripherals I/O Lines Power Supply	Power		1.65V to 3.6V
VDDBU	Backup I/O Lines Power Supply	Power		1.08V to 1.32V
VDDPLL	PLL Power Supply	Power		3.0V to 3.6V
VDDOSC	Oscillator Power Supply	Power		3.0V to 3.6V
VDDCORE	Core Chip Power Supply	Power		1.08V to 1.32V
GND	Ground	Ground		
GNDPLL	PLL Ground	Ground		
GNDBU	Backup Ground	Ground		
Clocks, Oscillators and PLLs				
XIN	Main Oscillator Input	Input		
XOUT	Main Oscillator Output	Output		
XIN32	Slow Clock Oscillator Input	Input		
XOUT32	Slow Clock Oscillator Output	Output		
PLLRCA	PLL A Filter	Input		
PLLRCB	PLL B Filter	Input		
PCK0 - PCK3	Programmable Clock Output	Output		
Shutdown, Wakeup Logic				
SHDN	Shutdown Control	Output		Driven at 0V only. Do not tie over VDDBU.
WKUP	Wake-up Input	Input		Accepts between 0V and VDDBU.
ICE and JTAG				
NTRST	Test Reset Signal	Input	Low	Pull-up resistor
TCK	Test Clock	Input		No pull-up resistor
TDI	Test Data In	Input		No pull-up resistor
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		No pull-up resistor
JTAGSEL	JTAG Selection	Input		Pull-down resistor. Accepts between 0V and VDDBU.
RTCK	Return Test Clock	Output		

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
Embedded Trace Module - ETM				
TSYNC	Trace Synchronization Signal	Output		
TCLK	Trace Clock	Output		
TPS0 - TPS2	Trace ARM Pipeline Status	Output		
TPK0 - TPK15	Trace Packet Port	Output		
Reset/Test				
NRST	Microcontroller Reset	I/O	Low	Pull-up resistor
TST	Test Mode Select	Input		Pull-down resistor
BMS	Boot Mode Select	Input		
Debug Unit - DBGU				
DRXD	Debug Receive Data	Input		
DTXD	Debug Transmit Data	Output		
Advanced Interrupt Controller - AIC				
IRQ0 - IRQ1	External Interrupt Inputs	Input		
FIQ	Fast Interrupt Input	Input		
PIO Controller - PIOA - PIOB - PIOC - PIOD - PIOE				
PA0 - PA31	Parallel IO Controller A	I/O		Pulled-up input at reset
PB0 - PB31	Parallel IO Controller B	I/O		Pulled-up input at reset
PC0 - PC31	Parallel IO Controller C	I/O		Pulled-up input at reset
PD0 - PD31	Parallel IO Controller D	I/O		Pulled-up input at reset
PE0 - PE31	Parallel IO Controller E	I/O		Pulled-up input at reset
Direct Memory Access Controller - DMA				
DMARQ0-DMARQ3	DMA Requests	Input		
External Bus Interface - EBI0 - EBI1				
EBIx_D0 - EBIx_D31	Data Bus	I/O		Pulled-up input at reset
EBIx_A0 - EBIx_A25	Address Bus	Output		0 at reset
EBIx_NWAIT	External Wait Signal	Input	Low	
Static Memory Controller - SMC				
EBI0_NCS0 - EBI0_NCS5, EBI1_NCS0 - EBI1_NCS2	Chip Select Lines	Output	Low	
EBIx_NWR0 -EBIx_NWR3	Write Signal	Output	Low	
EBIx_NRD	Read Signal	Output	Low	
EBIx_NWE	Write Enable	Output	Low	
EBIx_NBS0 - EBIx_NBS3	Byte Mask Signal	Output	Low	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
CompactFlash Support				
EBI0_CFCE1 - EBI0_CFCE2	CompactFlash Chip Enable	Output	Low	
EBI0_CFOE	CompactFlash Output Enable	Output	Low	
EBI0_CFWE	CompactFlash Write Enable	Output	Low	
EBI0_CFIOR	CompactFlash IO Read	Output	Low	
EBI0_CFIOW	CompactFlash IO Write	Output	Low	
EBI0_CFRNW	CompactFlash Read Not Write	Output		
EBI0_CFCS0 - EBI0_CFCS1	CompactFlash Chip Select Lines	Output	Low	
NAND Flash Support				
EBIx_NANDCS	NAND Flash Chip Select	Output	Low	
EBIx_NANDOE	NAND Flash Output Enable	Output	Low	
EBIx_NANDWE	NAND Flash Write Enable	Output	Low	
SDRAM Controller				
EBIx_SDCK	SDRAM Clock	Output		
EBIx_SDCKE	SDRAM Clock Enable	Output	High	
EBIx_SDCS	SDRAM Controller Chip Select	Output	Low	
EBIx_BA0 - EBIx_BA1	Bank Select	Output		
EBIx_SDWE	SDRAM Write Enable	Output	Low	
EBIx_RAS - EBIx_CAS	Row and Column Signal	Output	Low	
EBIx_SDA10	SDRAM Address 10 Line	Output		
Multimedia Card Interface				
MCIx_CK	Multimedia Card Clock	Output		
MCIx_CDA	Multimedia Card Slot A Command	I/O		
MCIx_CDB	Multimedia Card Slot B Command	I/O		
MCIx_DA0 - MCIx_DA3	Multimedia Card Slot A Data	I/O		
MCIx_DB0 - MCIx_DB3	Multimedia Card Slot B Data	I/O		
Universal Synchronous Asynchronous Receiver Transmitter USART				
SCKx	USARTx Serial Clock	I/O		
TXDx	USARTx Transmit Data	I/O		
RXDx	USARTx Receive Data	Input		
RTSx	USARTx Request To Send	Output		
CTSx	USARTx Clear To Send	Input		
Synchronous Serial Controller SSC				
TDx	SSCx Transmit Data	Output		
RDx	SSCx Receive Data	Input		
TKx	SSCx Transmit Clock	I/O		

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
RKx	SSCx Receive Clock	I/O		
TFx	SSCx Transmit Frame Sync	I/O		
RFx	SSCx Receive Frame Sync	I/O		
AC97 Controller - AC97C				
AC97RX	AC97 Receive Signal	Input		
AC97TX	AC97 Transmit Signal	Output		
AC97FS	AC97 Frame Synchronization Signal	Output		
AC97CK	AC97 Clock signal	Input		
Timer/Counter - TC				
TCLKx	TC Channel x External Clock Input	Input		
TIOAx	TC Channel x I/O Line A	I/O		
TIOBx	TC Channel x I/O Line B	I/O		
Pulse Width Modulation Controller- PWMC				
PWMx	Pulse Width Modulation Output	Output		
Serial Peripheral Interface - SPI				
SPIx_MISO	Master In Slave Out	I/O		
SPIx_MOSI	Master Out Slave In	I/O		
SPIx_SPCK	SPI Serial Clock	I/O		
SPIx_NPCS0	SPI Peripheral Chip Select 0	I/O	Low	
SPIx_NPCS1 - SPIx_NPCS3	SPI Peripheral Chip Select	Output	Low	
Two-Wire Interface				
TWD	Two-wire Serial Data	I/O		
TWCK	Two-wire Serial Clock	I/O		
CAN Controllers				
CANRX	CAN Input	Input		
CANTX	CAN Output	Output		
LCD Controller - LCDC				
LCDD0 - LCDD23	LCD Data Bus	Output		
LCDVSYNC	LCD Vertical Synchronization	Output		
LCDHSYNC	LCD Horizontal Synchronization	Output		
LCDDOTCK	LCD Dot Clock	Output		
LCDDEN	LCD Data Enable	Output		
LCDCC	LCD Contrast Control	Output		

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
Ethernet 10/100				
ETXCK	Transmit Clock or Reference Clock	Input		MII only, REFCK in RMII
ERXCK	Receive Clock	Input		MII only
ETXEN	Transmit Enable	Output		
ETX0-ETX3	Transmit Data	Output		ETX0-ETX1 only in RMII
ETXER	Transmit Coding Error	Output		MII only
ERXDV	Receive Data Valid	Input		RXDV in MII, CRSDV in RMII
ERX0-ERX3	Receive Data	Input		ERX0-ERX1 only in RMII
ERXER	Receive Error	Input		
ECRS	Carrier Sense and Data Valid	Input		MII only
ECOL	Collision Detect	Input		MII only
EMDC	Management Data Clock	Output		
EMDIO	Management Data Input/Output	I/O		
EF100	Force 100Mbit/sec.	Output	High	RMII only
USB Device Port				
DDM	USB Device Port Data -	Analog		
DDP	USB Device Port Data +	Analog		
USB Host Port				
HDPA	USB Host Port A Data +	Analog		
HDMA	USB Host Port A Data -	Analog		
HDPB	USB Host Port B Data +	Analog		
HDMB	USB Host Port B Data -	Analog		
Image Sensor Interface - ISI				
ISI_D0-ISI_D11	Image Sensor Data	Input		
ISI_MCK	Image Sensor Reference Clock	Output		Provided by PCK3
ISI_HSYNC	Image Sensor Horizontal Synchro	Input		
ISI_VSYNC	Image Sensor Vertical Synchro	Input		
ISI_PCK	Image Sensor Data Clock	Input		

4. Package and Pinout

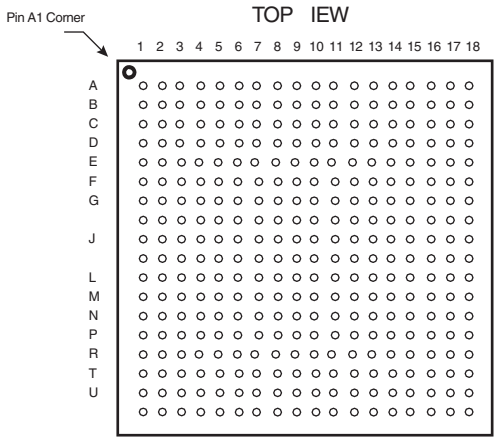
The AT91SAM9263 is available in a 324-ball TFBGA Green package, 15 x 15 mm, 0.8mm ball pitch.

4.1 324-ball TFBGA Package Outline

Figure 4-1 shows the orientation of the 324-ball TFBGA package.

A detailed mechanical description is given in the section “AT91SAM9263 Mechanical Characteristics” in the product datasheet.

Figure 4-1. 324-ball TFBGA Pinout (Top View)



4.2 324-ball TFBGA Package Pinout

Table 4-1. AT91SAM9263 Pinout for 324-ball TFBGA Package

Pin	Signal Name
A1	EBI0_D2
A2	EBI0_SDCKE
A3	EBI0_NWE_NWR0
A4	EBI0_NCS1_SDCS
A5	EBI0_A19
A6	EBI0_A11
A7	EBI0_A10
A8	EBI0_A5
A9	EBI0_A1_NBS2_NWR2
A10	PD4
A11	PC30
A12	PC26
A13	PC24
A14	PC19
A15	PC12
A16	VDDCORE
A17	VDDIOP0
A18	DDP
B1	EBI0_D4
B2	EBI0_NANDOE
B3	EBI0_CAS
B4	EBI0_RAS
B5	EBI0_NBS3_NWR3
B6	EBI0_A22
B7	EBI0_A15
B8	EBI0_A7
B9	EBI0_A4
B10	PD0
B11	PC28
B12	PC21
B13	PC17
B14	PC9
B15	PC7
B16	PC5
B17	PB16
B18	DDM
C1	EBI0_D6
C2	EBI0_D0
C3	EBI0_NANDWE
C4	EBI0_SDWE
C5	EBI0_SDCK
C6	EBI0_A21
C7	EBI0_A13
C8	EBI0_A8
C9	EBI0_A3
C10	PD2
C11	PC29
C12	PC23
C13	PC14
C14	PC8
C15	PC3
E10	PC31
E11	PC22
E12	PC15
E13	PC11
E14	PC4
E15	PB30
E16	PC0
E17	PB31
E18	HDPA
F1	PD7
F2	EBI0_D13
F3	EBI0_D9
F4	EBI0_D11
F5	EBI0_D12
F6	EBI0_NCS0
F7	EBI0_A16_BA0
F8	EBI0_A12
F9	EBI0_A6
F10	PD3
F11	PC27
F12	PC18
F13	PC13
F14	PB26
F15	PB25
F16	PB29
F17	PB27
F18	HDMA
G1	PD17
G2	PD12
G3	PD6
G4	EBI0_D14
G5	PD5
G6	PD8
G7	PD10
G8	GND
G9	NC[1]
G10	GND
G11	GND
G12	GND
G13	PB21
G14	PB20
G15	PB23
G16	PB28
G17	PB22
G18	PB18
H1	PD24
H2	PD13
H3	PD15
H4	PD9
H5	PD11
H6	PD14
K1	PE6
K2	PD28
K3	PE0
K4	PE1
K5	PD27
K6	PD31
K7	PD29
K8	PD25
K9	GND
K10	VDDIOM0
K11	GND
K12	VDDIOM0
K13	PB3/BMS
K14	PA14
K15	PA15
K16	PB1
K17	PB0
K18	PB2
L1	PE10
L2	PE4
L3	PE9
L4	PE7
L5	PE5
L6	PE2
L7	PE3
L8	VDDIOP1
L9	VDDIOM1
L10	VDDIOM0
L11	VDDIOP0
L12	GNDBU
L13	PA13
L14	PB4
L15	PA9
L16	PA12
L17	PA10
L18	PA11
M1	PE18
M2	PE14
M3	PE15
M4	PE11
M5	PE13
M6	PE12
M7	PE8
M8	VDDBU
M9	EBI1_A21
M10	VDDIOM1
M11	GND
M12	GND
M13	VDDIOM1
M14	PA6
M15	PA4
P10	EBI1_NCS0
P11	EBI1_NWE_NWR0
P12	EBI1_D4
P13	EBI1_D10
P14	PA3
P15	PA2
P16	PE28
P17	TDI
P18	PLLRCB
R1	XOUT32
R2	TST
R3	PA18
R4	PA25
R5	PA30
R6	EBI1_A2
R7	EBI1_A14
R8	EBI1_A13
R9	EBI1_A17_BA1
R10	EBI1_D1
R11	EBI1_D8
R12	EBI1_D12
R13	EBI1_D15
R14	PE26
R15	EBI1_SDCK
R16	PE30
R17	TCK
R18	XOUT
T1	VDDOSC
T2	VDDIOM1
T3	PA19
T4	PA21
T5	PA26
T6	PA31
T7	EBI1_A7
T8	EBI1_A12
T9	EBI1_A18
T10	EBI1_D0
T11	EBI1_D7
T12	EBI1_D14
T13	PE23
T14	PE25
T15	PE29
T16	PE31
T17	GNDPLL
T18	XIN
U1	PA17
U2	PA20
U3	PA23
U4	PA24
U5	PA28
U6	EBI1_A0_NBS0

Table 4-1. AT91SAM9263 Pinout for 324-ball TFBGA Package (Continued)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
C16	GND	H7	PD16	M16	PA7	U7	EBI1_A5
C17	VDDIOP0	H8	VDDIOM0	M17	PA5	U8	EBI1_A10
C18	HDPB	H9	GND	M18	PA8	U9	EBI1_A16_BA0
D1	EBI0_D10	H10	VDDCORE	N1	NC	U10	EBI1_NRD
D2	EBI0_D3	H11	GND	N2	NC	U11	EBI1_D3
D3	NC(1)	H12	PB19	N3	PE19	U12	EBI1_D13
D4	EBI0_D1	H13	PB17	N4	NC(1)	U13	PE22
D5	EBI0_A20	H14	PB15	N5	PE17	U14	PE27
D6	EBI0_A17_BA1	H15	PB13	N6	PE16	U15	RTCK
D7	EBI0_A18	H16	PB24	N7	EBI1_A6	U16	NTRST
D8	EBI0_A9	H17	PB14	N8	EBI1_A11	U17	VDDPLLA
D9	EBI0_A2	H18	PB12	N9	EBI1_A22	U18	PLLRCA
D10	PD1	J1	PD30	N10	EBI1_D2	V1	VDDCORE
D11	PC25	J2	PD26	N11	EBI1_D6	V2	PA22
D12	PC20	J3	PD22	N12	EBI1_D9	V3	PA27
D13	PC6	J4	PD19	N13	GND	V4	PA29
D14	PC16	J5	PD18	N14	GNDPLL	V5	EBI1_A1_NWR2
D15	PC10	J6	PD23	N15	PA1	V6	EBI1_A3
D16	PC2	J7	PD21	N16	PA0	V7	EBI1_A9
D17	PC1	J8	PD20	N17	TMS	V8	EBI1_A15
D18	HDMB	J9	GND	N18	TDO	V9	EBI1_A20
E1	EBI0_D15	J10	GND	P1	XIN32	V10	EBI1_NBS1_NWR1
E2	EBI0_D7	J11	GND	P2	SHDN	V11	EBI1_D5
E3	EBI0_D5	J12	PB11	P3	PA16	V12	EBI1_D11
E4	EBI0_D8	J13	PB9	P4	WKUP	V13	PE21
E5	EBI0_NBS1_NWR1	J14	PB10	P5	JTAGSEL	V14	PE24
E6	EBI0_NRD	J15	PB5	P6	PE20	V15	NRST
E7	EBI0_A14	J16	PB6	P7	EBI1_A8	V16	GND
E8	EBI0_SDA10	J17	PB7	P8	EBI1_A4	V17	GND
E9	EBI0_A0_NBS0	J18	PB8	P9	EBI1_A19	V18	VDDPLLB

Note: 1. NC pins must be left unconnected.

5. Power Considerations

5.1 Power Supplies

AT91SAM9263 has several types of power supply pins:

- VDDCORE pins: Power the core, including the processor, the embedded memories and the peripherals; voltage ranges from 1.08V to 1.32V, 1.2V nominal.
- VDDIOM0 and VDDIOM1 pins: Power the External Bus Interface 0 I/O lines and the External Bus Interface 1 I/O lines, respectively; voltage ranges between 1.65V and 1.95V (1.8V nominal) or between 3.0V and 3.6V (3.3V nominal).
- VDDIOP0 pins: Power the Peripheral I/O lines and the USB transceivers; voltage ranges from 2.7V to 3.6V, 3.3V nominal.
- VDDIOP1 pins: Power the Peripheral I/O lines involving the Image Sensor Interface; voltage ranges from 1.65V to 3.6V, 1.8V, 2.5V, 3V or 3.3V nominal.
- VDDBU pin: Powers the Slow Clock oscillator and a part of the System Controller; voltage ranges from 1.08V to 1.32V, 1.2V nominal.
- VDDPLL pin: Powers the PLL cells; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDOSC pin: Powers the Main Oscillator cells; voltage ranges from 3.0V to 3.6V, L3.3V nominal.

The power supplies VDDIOM0, VDDIOM1 and VDDIOP0, VDDIOP1 are identified in the pinout table and the multiplexing tables. These supplies enable the user to power the device differently for interfacing with memories and for interfacing with peripherals.

Ground pins GND are common to VDDOSC, VDDCORE, VDDIOM0, VDDIOM1, VDDIOP0 and VDDIOP1 pins power supplies. Separated ground pins are provided for VDDBU and VDDPLL. These ground pins are respectively GNDBU and GNDPLL.

5.2 Power Consumption

The AT91SAM9263 consumes about 700 µA (worst case) of static current on VDDCORE at 25°C. This static current rises at up to 7 mA if the temperature increases to 85°C.

On VDDBU, the current does not exceed 3 µA @25°C, but can rise at up to 20 µA @85°C. An automatic switch to VDDCORE guarantees low power consumption on the battery when the system is on.

For dynamic power consumption, the AT91SAM9263 consumes a maximum of 70 mA on VDDCORE at maximum conditions (1.2V, 25°C, processor running full-performance algorithm).

5.3 Programmable I/O Lines Power Supplies

The power supply pins VDDIOM0 and VDDIOM1 accept two voltage ranges. This allows the device to reach its maximum speed, either out of 1.8V or 3.0V external memories.

The maximum speed is 100 MHz on the pin SDCK (SDRAM Clock) loaded with 10 pF. The other signals (control, address and data signals) do not go over 50 MHz, loaded with 30 pF for power supply at 1.8V and 50 pF for power supply at 3.3V.

The voltage ranges are determined by programming registers in the Chip Configuration registers located in the Matrix User Interface.

At reset, the selected voltage defaults to 3.3V nominal and power supply pins can accept either 1.8V or 3.3V. However, the device cannot reach its maximum speed if the voltage supplied to the pins is only 1.8V without reprogramming the EBI0 voltage range. The user must be sure to program the EBI0 voltage range before getting the device out of its Slow Clock Mode.

6. I/O Line Considerations

6.1 JTAG Port Pins

TMS, TDI and TCK are Schmitt trigger inputs and have no pull-up resistors.

TDO and RTCK are outputs, driven at up to VDDIOP0, and have no pull-up resistors.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level (VDDBU). It integrates a permanent pull-down resistor of about 15 kΩ to GNDBU, so that it can be left unconnected for normal operations.

The NTRST signal is described in Section 6.3.

All JTAG signals except JTAGSEL (VDDBU) are supplied with VDDIOP0.

6.2 Test Pin

The TST pin is used for manufacturing test purposes when asserted high. It integrates a permanent pull-down resistor of about 15 kΩ to GNDBU, so that it can be left unconnected for normal operations. Driving this line at a high level leads to unpredictable results.

This pin is supplied with VDDBU.

6.3 Reset Pins

NRST is an open-drain output integrating a non-programmable pull-up resistor. It can be driven with voltage at up to VDDIOP0.

NTRST is an input which allows reset of the JTAG Test Access port. It has no action on the processor.

As the product integrates power-on reset cells, which manage the processor and the JTAG reset, the NRST and NTRST pins can be left unconnected.

The NRST and NTRST pins both integrate a permanent pull-up resistor of 100 kΩ minimum to VDDIOP0.

The NRST signal is inserted in the Boundary Scan.

6.4 PIO Controllers

All the I/O lines managed by the PIO Controllers integrate a programmable pull-up resistor of 100 kΩ typical. Programming of this pull-up resistor is performed independently for each I/O line through the PIO Controllers.

After reset, all the I/O lines default as inputs with pull-up resistors enabled, except those which are multiplexed with the External Bus Interface signals that require to be enabled as Peripheral at reset. This is explicitly indicated in the column “Reset State” of the PIO Controller multiplexing tables on page 33 and following.

6.5 Shutdown Logic Pins

The SHDN pin is a tri-state output only pin, which is driven by the Shutdown Controller. There is no internal pull-up. An external pull-up to VDDBU is needed and its value must be higher than 1 MΩ. The resistor value is calculated according to the regulator enable implementation and the SHDN level.

The pin WKUP is an input-only. It can accept voltages only between 0V and VDDBU.

7. Processor and Architecture

7.1 ARM926EJ-S Processor

- RISC Processor based on ARM v5TEJ Harvard Architecture with Jazelle technology for Java acceleration
- Two Instruction Sets
  - ARM High-performance 32-bit Instruction Set
  - Thumb High Code Density 16-bit Instruction Set
- DSP Instruction Extensions
- 5-stage Pipeline Architecture
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)
  - Data Memory (M)
  - Register Write (W)
- 16 Kbyte Data Cache, 16 Kbyte Instruction Cache
  - Virtually-addressed 4-way Associative Cache
  - Eight words per line
  - Write-through and Write-back Operation
  - Pseudo-random or Round-robin Replacement
- Write Buffer
  - Main Write Buffer with 16-word Data Buffer and 4-address Buffer
  - DCache Write-back Buffer with 8-word Entries and a Single Address Entry
  - Software Control Drain
- Standard ARM v4 and v5 Memory Management Unit (MMU)
  - Access Permission for Sections
  - Access Permission for large pages and small pages can be specified separately for each quarter of the page
  - 16 embedded domains
- Bus Interface Unit (BIU)
  - Arbitrates and Schedules AHB Requests
  - Separate Masters for both instruction and data access providing complete Matrix system flexibility
  - Separate Address and Data Buses for both the 32-bit instruction interface and the 32-bit data interface
  - On Address and Data Buses, data can be 8-bit (Bytes), 16-bit (Half-words) or 32-bit (Words)

7.2 Bus Matrix

- 9-layer Matrix, handling requests from 9 masters
- Programmable Arbitration strategy
  - Fixed-priority Arbitration
  - Round-Robin Arbitration, either with no default master, last accessed default master or fixed default master
- Burst Management
  - Breaking with Slot Cycle Limit Support
  - Undefined Burst Length Support
- One Address Decoder provided per Master
  - Three different slaves may be assigned to each decoded memory area: one for internal boot, one for external boot, one after remap

- Boot Mode Select
  - Non-volatile Boot Memory can be internal or external
  - Selection is made by BMS pin sampled at reset
- Remap Command
  - Allows Remapping of an Internal SRAM in Place of the Boot Non-Volatile Memory
  - Allows Handling of Dynamic Exception Vectors

7.3 Matrix Masters

The Bus Matrix of the AT91SAM9263 manages nine masters, thus each master can perform an access concurrently with others to an available slave peripheral or memory.

Each master has its own decoder, which is defined specifically for each master.

Table 7-1. List of Bus Matrix Masters

Master 0	OHCI USB Host Controller
Master 1	Image Sensor Interface
Master 2	Two D Graphic Controller
Master 3	DMA Controller
Master 4	Ethernet MAC
Master 5	LCD Controller
Master 6	Peripheral DMA Controller
Master 7	ARM926 Data
Master 8	ARM926™ Instruction

7.4 Matrix Slaves

The Bus Matrix of the AT91SAM9263 manages eight slaves. Each slave has its own arbiter, thus allowing to program a different arbitration per slave.

The LCD Controller, the DMA Controller, the USB OTG and the USB Host have a user interface mapped as a slave on the Matrix. They share the same layer, as programming them does not require a high bandwidth.

Table 7-2. List of Bus Matrix Slaves

Slave 0	Internal ROM
Slave 1	Internal 80 Kbyte SRAM
Slave 2	Internal 16 Kbyte SRAM
Slave 3	LCD Controller User Interface
	DMA Controller User Interface
	USB Host User Interface
Slave 4	External Bus Interface 0
Slave 5	External Bus Interface 1
Slave 6	Peripheral Bridge

7.5 Master to Slave Access

In most cases, all the masters can access all the slaves. However, some paths do not make sense, for example, allowing access from the Ethernet MAC to the Internal Peripherals. Thus, these paths are forbidden or simply not wired, and are shown as "-" in Table 7-3.

Table 7-3. Masters to Slaves Access

Master		0	1	2	3	4	5	6	7&8
Slave		OHCI USB Host Controller	Image Sensor Interface	Two D Graphics Controller	DMA Controller	Ethernet MAC	LCD Controller	Peripheral DMA Controller	ARM926 Data & Instruction
0	Internal ROM	X	X	X	X	X	X	X	X
1	Internal 80 Kbyte SRAM	X	X	X	X	X	X	X	X
2	Internal 16 Kbyte SRAM Bank	X	X	X	X	X	X	X	X
3	LCD Controller User Interface	-	-	-	-	-	-	-	X
	DMA Controller User Interface	-	-	-	-	-	-	-	X
	USB Host User Interface	-	-	-	-	-	-	-	X
4	External Bus Interface 0	X	X	X	X	X	X	X	X
5	External Bus Interface 1	X	X	X	X	X	X	X	X
6	Peripheral Bridge	-	-	-	X	-	-	X	X

7.6 Peripheral DMA Controller

- Acts as one Matrix Master
- Allows data transfers between a peripheral and memory without any intervention of the processor
- Next Pointer support, removes heavy real-time constraints on buffer management.
- Twenty channels
  - Two for each USART
  - Two for the Debug Unit
  - Two for each Serial Synchronous Controller
  - Two for each Serial Peripheral Interface
  - Two for the AC97 Controller
  - One for each Multimedia Card Interface

The Peripheral DMA Controller handles transfer requests from the channel according to the following priorities (low to high priorities):

- DBGU Transmit Channel
- USART2 Transmit Channel
- USART1 Transmit Channel
- USART0 Transmit Channel
- AC97 Transmit Channel

- SPI1 Transmit Channel
- SPI0 Transmit Channel
- SSC1 Transmit Channel
- SSC0 Transmit Channel
- DBGU Receive Channel
- USART2 Receive Channel
- USART1 Receive Channel
- USART0 Receive Channel
- AC97 Receive Channel
- SPI1 Receive Channel
- SPI0 Receive Channel
- SSC1 Receive Channel
- SSC0 Receive Channel
- MCI1 Transmit/Receive Channel
- MCI0 Transmit/Receive Channel

7.7 DMA Controller

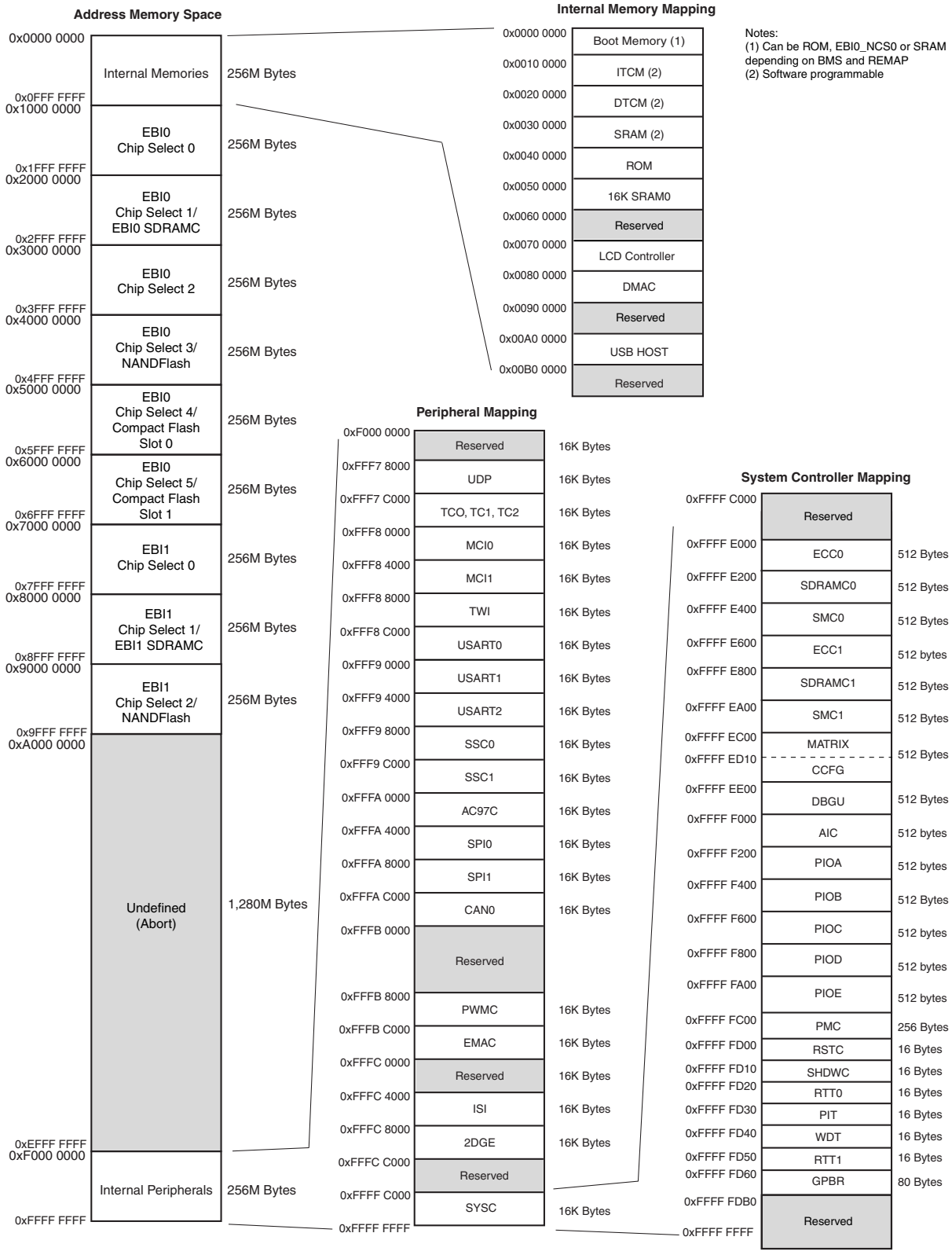
- Acts as one Matrix Master
- Embeds 2 unidirectional channels with programmable priority
- Address Generation
  - Source/destination address programming
  - Address increment, decrement or no change
  - DMA chaining support for multiple non-contiguous data blocks through use of linked lists
  - Scatter support for placing fields into a system memory area from a contiguous transfer. Writing a stream of data into non-contiguous fields in system memory.
  - Gather support for extracting fields from a system memory area into a contiguous transfer
  - User enabled auto-reloading of source, destination and control registers from initially programmed values at the end of a block transfer
  - Auto-loading of source, destination and control registers from system memory at end of block transfer in block chaining mode
  - Unaligned system address to data transfer width supported in hardware
- Channel Buffering
  - Two 8-word FIFOs
  - Automatic packing/unpacking of data to fit FIFO width
- Channel Control
  - Programmable multiple transaction size for each channel
  - Support for cleanly disabling a channel without data loss
  - Suspend DMA operation
  - Programmable DMA lock transfer support.
- Transfer Initiation
  - Supports four external DMA Requests
  - Support for software handshaking interface. Memory mapped registers can be used to control the flow of a DMA transfer in place of a hardware handshaking interface
- Interrupt
  - Programmable interrupt generation on DMA transfer completion, Block transfer completion, Single/Multiple transaction completion or Error condition

7.8 Debug and Test Features

- ARM926 Real-time In-circuit Emulator
  - Two real-time Watchpoint Units
  - Two Independent Registers: Debug Control Register and Debug Status Register
  - Test Access Port Accessible through JTAG Protocol
  - Debug Communications Channel
- Debug Unit
  - Two-pin UART
  - Debug Communication Channel Interrupt Handling
  - Chip ID Register
- Embedded Trace Macrocell: ETM9™
  - Medium+ Level Implementation
  - Half-rate Clock Mode
  - Four Pairs of Address Comparators
  - Two Data Comparators
  - Eight Memory Map Decoder Inputs
  - Two 16-bit Counters
  - One 3-stage Sequencer
  - One 45-byte FIFO
- IEEE1149.1 JTAG Boundary-scan on All Digital Pins

8. Memories

Figure 8-1. AT91SAM9263 Memory Mapping



A first level of address decoding is performed by the Bus Matrix, i.e., the implementation of the Advanced High Performance Bus (AHB) for its master and slave interfaces with additional features.

Decoding breaks up the 4G bytes of address space into 16 banks of 256M bytes. The banks 1 to 9 are directed to the EBI0 that associates these banks to the external chip selects EBI0_NCS0 to EBI0_NCS5 and EBI1_NCS0 to EBI1_NCS2. The bank 0 is reserved for the addressing of the internal memories, and a second level of decoding provides 1M bytes of internal memory area. Bank 15 is reserved for the peripherals and provides access to the Advanced Peripheral Bus (APB).

Other areas are unused and performing an access within them provides an abort to the master requesting such an access.

Each master has its own bus and its own decoder, thus allowing a different memory mapping for each master. However, in order to simplify the mappings, all the masters have a similar address decoding.

Regarding Master 0 and Master 1 (ARM926 Instruction and Data), three different slaves are assigned to the memory space decoded at address 0x0: one for internal boot, one for external boot and one after remap. Refer to Table 8-1, “Internal Memory Mapping,” on page 21 for details.

A complete memory map is presented in Figure 8-1 on page 20.

8.1 Embedded Memories

- 128 Kbyte ROM
  - Single Cycle Access at full matrix speed
- One 80 Kbyte Fast SRAM
  - Single Cycle Access at full matrix speed
  - Supports ARM926EJ-S TCM interface at full processor speed
  - Allows internal Frame Buffer for up to 1/4 VGA 8 bpp screen
- 16 Kbyte Fast SRAM
  - Single Cycle Access at full matrix speed

8.1.1 Internal Memory Mapping

Table 8-1 summarizes the Internal Memory Mapping, depending on the Remap status and the BMS state at reset.

Table 8-1. Internal Memory Mapping

Address	REMAP = 0		REMAP = 1
	BMS = 1	BMS = 0	
0x0000 0000	ROM	EBI0_NCS0	SRAM C

8.1.1.1 Internal 80 Kbyte Fast SRAM

The AT91SAM9263 device embeds a high-speed 80 Kbyte SRAM. This internal SRAM is split into three areas. Its memory mapping is presented in Figure 8-1 on page 20.

- Internal SRAM A is the ARM926EJ-S Instruction TCM. The user can map this SRAM block anywhere in the ARM926 instruction memory space using CP15 instructions and the TCR configuration register located in the Chip Configuration User Interface. This SRAM block is also accessible by the ARM926 Data Master and by the AHB Masters through the AHB bus at address 0x0010 0000.
- Internal SRAM B is the ARM926EJ-S Data TCM. The user can map this SRAM block anywhere in the ARM926 data memory space using CP15 instructions. This SRAM block is also accessible by the ARM926 Data Master and by the AHB Masters through the AHB bus at address 0x0020 0000.
- Internal SRAM C is only accessible by all the AHB Masters. After reset and until the Remap Command is performed, this SRAM block is accessible through the AHB bus at address 0x0030 0000 by all the AHB Masters. After Remap, this SRAM block also becomes accessible through the AHB bus at address 0x0 by the ARM926 Instruction and the ARM926 Data Masters.

Within the 80 Kbytes of SRAM available, the amount of memory assigned to each block is software programmable as a multiple of 16 Kbytes as shown in Table 8-2. This table provides the size of the Internal SRAM C according to the size of the internal SRAM A and the internal SRAM B.

Table 8-2. Internal SRAM Block Size

Internal SRAM C		Internal SRAM A (ITCM) Size		
		0	16 Kbytes	32 Kbytes
Internal SRAM B (DTCM) size	0	80 Kbytes	64 Kbytes	48 Kbytes
	16 Kbytes	64 Kbytes	48 Kbytes	32 Kbytes
	32 Kbytes	48 Kbytes	32 Kbytes	16 Kbytes

Note that among the five 16 Kbyte blocks making up the Internal SRAM, one is permanently assigned to Internal SRAM C.

At reset, the whole memory (80 Kbytes) is assigned to Internal SRAM C.

The memory blocks assigned to SRAM A, SRAM B and SRAM C areas are not contiguous and when the user dynamically changes the Internal SRAM configuration, the new 16 Kbyte block organization may affect the previous configuration from a software point of view.

Table 8-3 illustrates different configurations and the related 16 Kbyte blocks assignments (RB0 to RB4).

Table 8-3. 16 Kbyte Block Allocation

Decoded Area	Address	Configuration examples and related 16 Kbyte block assignments				
		ITCM = 0 Kbyte DTCM = 0 Kbyte AHB = 80 Kbytes (1)	ITCM = 32 Kbytes DTCM = 32 Kbytes AHB = 16 Kbytes	ITCM = 16 Kbytes DTCM = 32 Kbytes AHB = 32 Kbytes	ITCM = 32 Kbytes DTCM = 16 Kbytes AHB = 32 Kbytes	ITCM = 16 Kbytes DTCM = 16 Kbytes AHB = 48 Kbytes
Internal SRAM A (ITCM)	0x0010 0000		RB1	RB1	RB1	RB1
	0x0010 4000		RB0		RB0	
Internal SRAM B (DTCM)	0x0020 0000		RB3	RB3	RB3	RB3
	0x0020 4000		RB2	RB2		
Internal SRAM C (AHB)	0x0030 0000	RB4	RB4	RB4	RB4	RB4
	0x0030 4000	RB3		RB0	RB2	RB2
	0x0030 8000	RB2				RB0
	0x0030 C000	RB1				
	0x0031 0000	RB0				

Note: 1. Configuration after reset.

When accessed from the Bus Matrix, the internal 80 Kbytes of Fast SRAM is single cycle accessible at full matrix speed (MCK). When accessed from the processor's TCM Interface, they are also single cycle accessible at full processor speed.

8.1.1.2 Internal 16 Kbyte Fast SRAM

The AT91SAM9263 integrates a 16 Kbyte SRAM, mapped at address 0x0050 0000. This SRAM is single cycle accessible at full Bus Matrix speed.

8.1.2 Boot Strategies

The system always boots at address 0x0. To ensure maximum boot possibilities, the memory layout can be changed with two parameters.

REMAP allows the user to layout the internal SRAM bank to 0x0. This is done by software once the system has booted. Refer to the section “AT91SAM9263 Bus Matrix” in the product datasheet for more details.

When REMAP = 0, BMS allows the user to layout at address 0x0 either the ROM or an external memory. This is done via hardware at reset.

Note: Memory blocks not affected by these parameters can always be seen at their specified base addresses. See the complete memory map presented in Figure 8-1 on page 20.

The AT91SAM9263 Bus Matrix manages a boot memory that depends on the level on the pin BMS at reset. The internal memory area mapped between address 0x0 and 0x000F FFFF is reserved to this effect.

If BMS is detected at 1, the boot memory is the embedded ROM.

If BMS is detected at 0, the boot memory is the memory connected on the Chip Select 0 of the External Bus Interface.

8.1.2.1 BMS = 1, Boot on Embedded ROM

The system boots on Boot Program.

- Boot at slow clock
- Auto baudrate detection
- Downloads and runs an application from external storage media into internal SRAM
- Downloaded code size depends on embedded SRAM size
- Automatic detection of valid application
- Bootloader on a non-volatile memory
  - SD Card
  - NAND Flash
  - SPI DataFlash® and Serial Flash connected on NPCS0 of the SPI0
- Interface with SAM-BA® Graphic User Interface to enable code loading via:
  - Serial communication on a DBGU
  - USB Bulk Device Port

8.1.2.2 BMS = 0, Boot on External Memory

- Boot at slow clock
- Boot with the default configuration for the Static Memory Controller, byte select mode, 16-bit data bus, Read/Write controlled by Chip Select, allows boot on 16-bit non-volatile memory.

The customer-programmed software must perform a complete configuration.

To speed up the boot sequence when booting at 32 kHz EBI0 CS0 (BMS=0) the user must:

1. Program the PMC (main oscillator enable or bypass mode).
2. Program and Start the PLL.
3. Reprogram the SMC setup, cycle, hold, mode timings registers for CS0 to adapt them to the new clock.
4. Switch the main clock to the new value.

8.2 External Memories

The external memories are accessed through the External Bus Interfaces 0 and 1. Each Chip Select line has a 256 Mbyte memory area assigned.

Refer to Figure 8-1 on page 20.

8.2.1 External Bus Interfaces

The AT91SAM9263 features two External Bus Interfaces to offer more bandwidth to the system and to prevent bottlenecks while accessing external memories.

8.2.1.1 External Bus Interface 0

- Integrates three External Memory Controllers:
  - Static Memory Controller
  - SDRAM Controller
  - ECC Controller
- Additional logic for NAND Flash and CompactFlash
- Optional Full 32-bit External Data Bus
- Up to 26-bit Address Bus (up to 64 Mbytes linear per chip select)
- Up to 6 Chip Selects, Configurable Assignment:
  - Static Memory Controller on NCS0
  - SDRAM Controller or Static Memory Controller on NCS1
  - Static Memory Controller on NCS2
  - Static Memory Controller on NCS3, Optional NAND Flash support
  - Static Memory Controller on NCS4 - NCS5, Optional CompactFlash support
- Optimized for Application Memory Space

8.2.1.2 External Bus Interface 1

- Integrates three External Memory Controllers:
  - Static Memory Controller
  - SDRAM Controller
  - ECC Controller
- Additional logic for NAND Flash
- Optional Full 32-bit External Data Bus
- Up to 23-bit Address Bus (up to 8 Mbytes linear)
- Up to 3 Chip Selects, Configurable Assignment:
  - Static Memory Controller on NCS0
  - SDRAM Controller or Static Memory Controller on NCS1
  - Static Memory Controller on NCS2, Optional NAND Flash support
- Allows supporting an external Frame Buffer for the embedded LCD Controller without impacting processor performance.

8.2.2 Static Memory Controller

- 8-, 16- or 32-bit Data Bus
- Multiple Access Modes supported
  - Byte Write or Byte Select Lines
  - Asynchronous read in Page Mode supported (4- up to 32-byte page size)
- Multiple device adaptability
  - Compliant with LCD Module
  - Control signals programmable setup, pulse and hold time for each Memory Bank
- Multiple Wait State Management
  - Programmable Wait State Generation
  - External Wait Request
  - Programmable Data Float Time
- Slow Clock mode supported

8.2.3 SDRAM Controller

- Supported devices

    - Standard and Low-power SDRAM (Mobile SDRAM)
- Numerous configurations supported
    - **2K, 4K, 8K Row Address Memory Parts**
    - **SDRAM with two or four Internal Banks**
    - **SDRAM with 16- or 32-bit Data Path**
- Programming facilities
    - **Word, half-word, byte access**
    - **Automatic page break when Memory Boundary has been reached**
    - **Multibank Ping-pong Access**
    - **Timing parameters specified by software**
    - **Automatic refresh operation, refresh rate is programmable**
- **Energy-saving capabilities**
    - **Self-refresh, power down and deep power down modes supported**
- Error detection
    - **Refresh Error Interrupt**
- **SDRAM Power-up Initialization by software**
- **CAS Latency of 1, 2 and 3 supported**
- **Auto Precharge Command not used**

8.2.4 Error Corrected Code Controller

- Tracking the accesses to a NAND Flash device by triggering on the corresponding chip select
- Single-bit error correction and two-bit random detection
- Automatic Hamming Code Calculation while writing
    - ECC value available in a register
- Automatic Hamming Code Calculation while reading
    - Error Report, including error flag, correctable error flag and word address being detected erroneous
    - Support 8- or 16-bit NAND Flash devices with 512-, 1024-, 2048- or 4096-byte pages

9. System Controller

The System Controller is a set of peripherals that allow handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc.

The System Controller User Interface also embeds registers that are used to configure the Bus Matrix and a set of registers for the chip configuration. The chip configuration registers can be used to configure:

- EBI0 and EBI1 chip select assignment and voltage range for external memories
- ARM Processor Tightly Coupled Memories

The System Controller peripherals are all mapped within the highest 16 Kbytes of address space, between addresses 0xFFFF C000 and 0xFFFF FFFF.

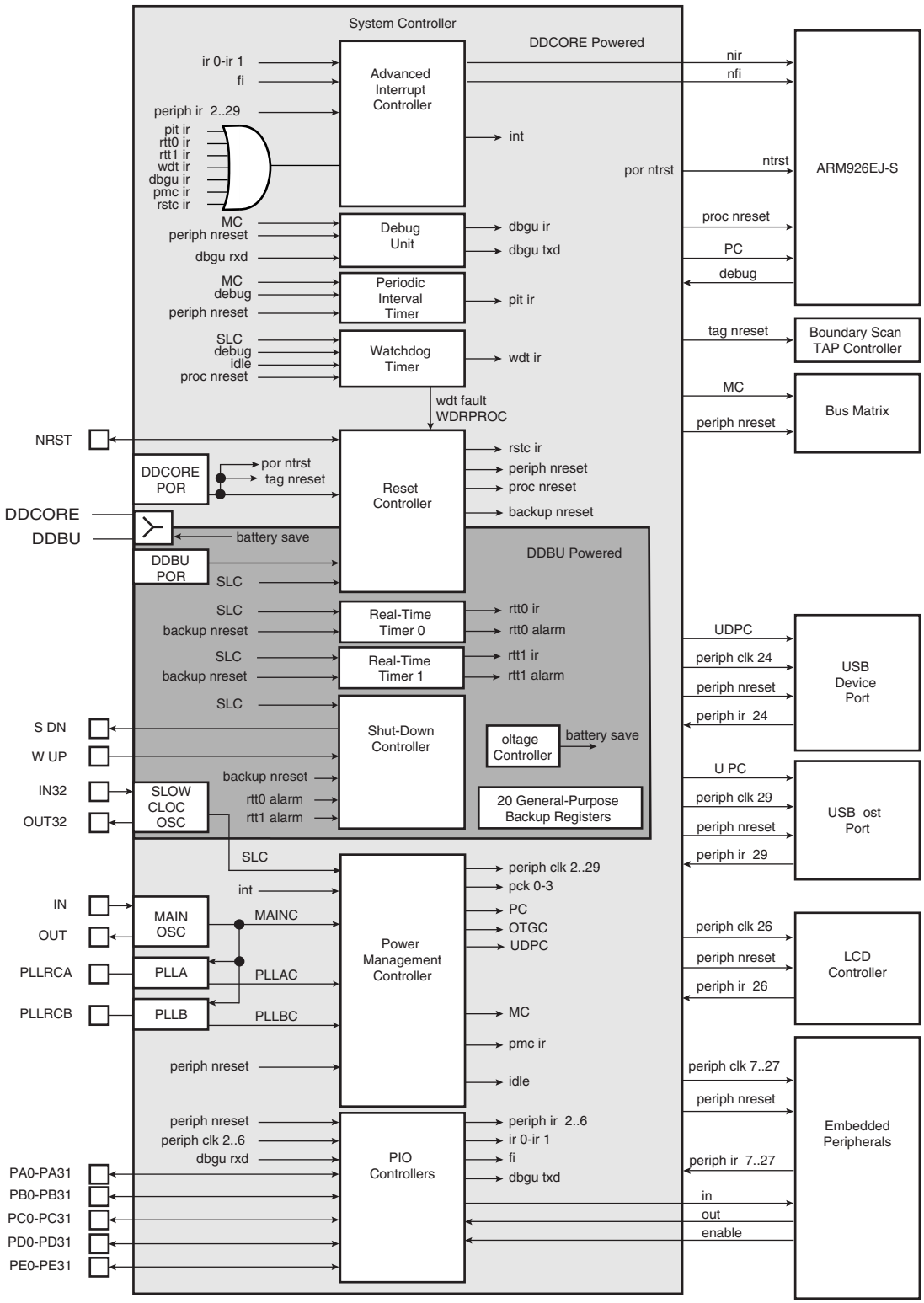
However, all the registers of the System Controller are mapped on the top of the address space. This allows all the registers of the System Controller to be addressed from a single pointer by using the standard ARM instruction set, as the Load/Store instructions have an indexing mode of ± 4 Kbytes.

Figure 9-1 on page 26 shows the System Controller block diagram.

Figure 8-1 on page 20 shows the mapping of the User Interfaces of the System Controller peripherals.

9.1 System Controller Block Diagram

Figure 9-1. AT91SAM9263 System Controller Block Diagram



9.2 Reset Controller

- Based on two Power-on-Reset cells
  - One on VDDBU and one on VDDCORE
- Status of the last reset
  - Either general reset (VDDBU rising), wake-up reset (VDDCORE rising), software reset, user reset or watchdog reset
- Controls the internal resets and the NRST pin output
  - Allows shaping a reset signal for the external devices

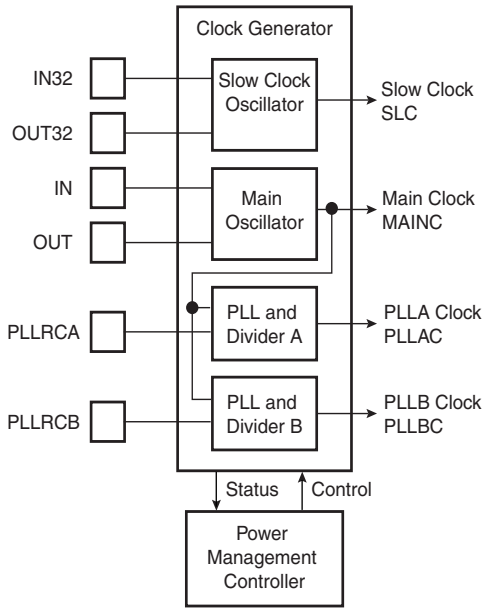
9.3 Shutdown Controller

- Shutdown and Wake-up logic
  - Software programmable assertion of the SHDN pin (SHDN is push-pull)
  - Deassertion programmable on a WKUP pin level change or on alarm

9.4 Clock Generator

- Embeds the low-power 32768 Hz Slow Clock Oscillator
  - Provides the permanent Slow Clock SLCK to the system
- Embeds the Main Oscillator
  - Oscillator bypass feature
  - Supports 3 to 20 MHz crystals
- Embeds 2 PLLs
  - Output 80 to 240 MHz clocks
  - Integrates an input divider to increase output accuracy
  - 1 MHz Minimum input frequency

Figure 9-2. Clock Generator Block Diagram



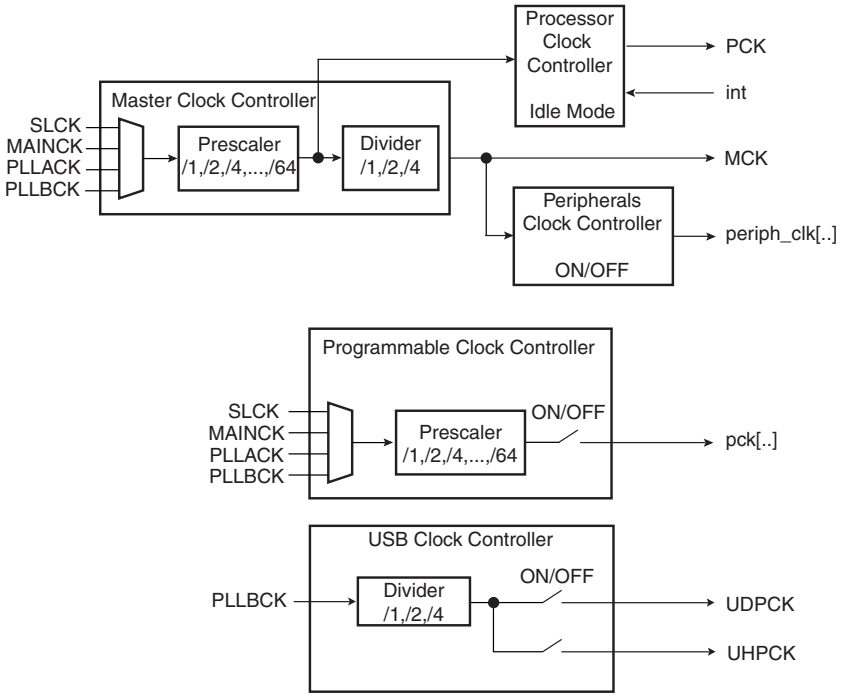
9.5 Power Management Controller

- Provides:

- the Processor Clock PCK
- the Master Clock MCK, in particular to the Matrix and the memory interfaces
- the USB Device Clock UDPCK
- the USB Host Clock UHPCK
- independent peripheral clocks, typically at the frequency of MCK
- four programmable clock outputs: PCK0 to PCK3

- Five flexible operating modes:
  - Normal Mode with processor and peripherals running at a programmable frequency
  - Idle Mode with processor stopped while waiting for an interrupt
  - Slow Clock Mode with processor and peripherals running at low frequency
  - Standby Mode, mix of Idle and Backup Mode, with peripherals running at low frequency, processor stopped waiting for an interrupt
  - Backup Mode with Main Power Supplies off, VDDBU powered by a battery

Figure 9-3. AT91SAM9263 Power Management Controller Block Diagram



9.6 Periodic Interval Timer

- Includes a 20-bit Periodic Counter, with less than 1 µs accuracy
- Includes a 12-bit Interval Overlay Counter
- Real-time OS or Linux®/WindowsCE® compliant tick generator

9.7 Watchdog Timer

- 16-bit key-protected Counter, programmable only once
- Windowed, prevents the processor deadlocking on the watchdog access

9.8 Real-time Timer

- Two Real-time Timers, allowing backup of time with different accuracies
  - 32-bit Free-running back-up counter

- Integrates a 16-bit programmable prescaler running on the embedded 32.768Hz oscillator
- Alarm Register capable of generating a wake-up of the system through the Shutdown Controller

9.9 General-purpose Backup Registers

- Twenty 32-bit general-purpose backup registers

9.10 Backup Power Switch

- Automatic switch of VDDBU to VDDCORE guaranteeing very low power consumption on VDDBU while VDDCORE is present

9.11 Advanced Interrupt Controller

- Controls the interrupt lines (nIRQ and nFIQ) of the ARM Processor
- Thirty-two individually maskable and vectored interrupt sources
  - Source 0 is reserved for the Fast Interrupt Input (FIQ)
  - Source 1 is reserved for system peripherals (PIT, RTT, PMC, DBGU, etc.)
  - Programmable Edge-triggered or Level-sensitive Internal Sources
  - Programmable Positive/Negative Edge-triggered or High/Low Level-sensitive
- Four External Sources plus the Fast Interrupt signal
- 8-level Priority Controller
  - Drives the Normal Interrupt of the processor
  - Handles priority of the interrupt sources 1 to 31
  - Higher priority interrupts can be served during service of lower priority interrupt
- Vectoring
  - Optimizes Interrupt Service Routine Branch and Execution
  - One 32-bit Vector Register per interrupt source
  - Interrupt Vector Register reads the corresponding current Interrupt Vector
- Protect Mode
  - Easy debugging by preventing automatic operations when protect models are enabled
- Fast Forcing
  - Permits redirecting any normal interrupt source on the Fast Interrupt of the processor

9.12 Debug Unit

- Composed of two functions
- Two-pin UART
  - Implemented features are 100% compatible with the standard Atmel USART
  - Independent receiver and transmitter with a common programmable Baud Rate Generator
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
  - Support for two PDC channels with connection to receiver and transmitter
  - Mode for general purpose Two-wire UART serial communication
- Debug Communication Channel Support
  - Offers visibility of and interrupt trigger from COMMRX and COMMTX signals from the ARM Processor's ICE Interface

9.13 Chip Identification

- Chip ID: 0x019607A0
- JTAG ID: 0x05B0C03F
- ARM926 TAP ID: 0x0792603F

9.14 PIO Controllers

- Five PIO Controllers, PIOA to PIOE, controlling a total of 160 I/O Lines
- Each PIO Controller controls up to 32 programmable I/O Lines
  - PIOA has 32 I/O Lines
  - PIOB has 32 I/O Lines
  - PIOC has 32 I/O Lines
  - PIOD has 32 I/O Lines
  - PIOE has 32 I/O Lines
- Fully programmable through Set/Clear Registers
- Multiplexing of two peripheral functions per I/O Line
- For each I/O Line (whether assigned to a peripheral or used as general-purpose I/O)
  - Input change interrupt
  - Glitch filter
  - Multi-drive option enables driving in open drain
  - Programmable pull-up on each I/O line
  - Pin data status register, supplies visibility of the level on the pin at any time
- Synchronous output, provides Set and Clear of several I/O lines in a single write

10. Peripherals

10.1 User Interface

The Peripherals are mapped in the upper 256 Mbytes of the address space between the addresses 0xFFFA 0000 and 0xFFFC FFFF. Each User Peripheral is allocated 16 Kbytes of address space.

A complete memory map is presented in Figure 8-1 on page 20.

10.2 Identifiers

Table 10-1 defines the Peripheral Identifiers. A peripheral identifier is required for the control of the peripheral interrupt with the Advanced Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 10-1. AT91SAM9263 Peripheral Identifiers

Peripheral ID	Peripheral Mnemonic	Peripheral Name	External Interrupt
0	AIC	Advanced Interrupt Controller	FIQ
1	SYSC	System Controller Interrupt	
2	PIOA	Parallel I/O Controller A	
3	PIOB	Parallel I/O Controller B	
4	PIOC to PIOE	Parallel I/O Controller C, D and E	
5	reserved		
6	reserved		
7	US0	USART 0	
8	US1	USART 1	
9	US2	USART 2	
10	MCI0	Multimedia Card Interface 0	
11	MCI1	Multimedia Card Interface 1	
12	CAN	CAN Controller	
13	TWI	Two-Wire Interface	
14	SPI0	Serial Peripheral Interface 0	
15	SPI1	Serial Peripheral Interface 1	
16	SSC0	Synchronous Serial Controller 0	
17	SSC1	Synchronous Serial Controller 1	
18	AC97C	AC97 Controller	
19	TC0, TC1, TC2	Timer/Counter 0, 1 and 2	
20	PWMC	Pulse Width Modulation Controller	
21	EMAC	Ethernet MAC	
22	reserved		
23	2DGE	2D Graphic Engine	
24	UDP	USB Device Port	
25	ISI	Image Sensor Interface	
26	LCDC	LCD Controller	
27	DMA	DMA Controller	
28	reserved		
29	UHP	USB Host Port	
30	AIC	Advanced Interrupt Controller	IRQ0
31	AIC	Advanced Interrupt Controller	IRQ1

Note: Setting AIC, SYSC, UHP and IRQ0 - 1 bits in the clock set/clear registers of the PMC has no effect.

10.2.1 Peripheral Interrupts and Clock Control

10.2.1.1 System Interrupt

The System Interrupt in Source 1 is the wired-OR of the interrupt signals coming from:

- the SDRAM Controller
- the Debug Unit
- the Periodic Interval Timer
- the Real-Time Timer
- the Watchdog Timer
- the Reset Controller
- the Power Management Controller

The clock of these peripherals cannot be deactivated and Peripheral ID 1 can only be used within the Advanced Interrupt Controller.

10.2.1.2 External Interrupts

All external interrupt signals, i.e., the Fast Interrupt signal FIQ or the Interrupt signals IRQ0 to IRQ1, use a dedicated Peripheral ID. However, there is no clock control associated with these peripheral IDs.

10.2.1.3 Timer Counter Interrupts

The three Timer Counter channels interrupt signals are OR-wired together to provide the interrupt source 19 of the Advanced Interrupt Controller. This forces the programmer to read all Timer Counter status registers before branching the right Interrupt Service Routine.

The Timer Counter channels clocks cannot be deactivated independently. Switching off the clock of the Peripheral 19 disables the clock of the 3 channels.

10.3 Peripherals Signals Multiplexing on I/O Lines

The AT91SAM9263 device features 5 PIO controllers, PIOA, PIOB, PIOC, PIOD and PIOE, which multiplex the I/O lines of the peripheral set.

Each PIO Controller controls up to 32 lines. Each line can be assigned to one of two peripheral functions, A or B. The multiplexing tables define how the I/O lines of the peripherals A and B are multiplexed on the PIO Controllers. The two columns “Function” and “Comments” have been inserted in this table for the user’s own comments; they may be used to track how pins are defined in an application.

Note that some peripheral functions which are output only may be duplicated within both tables.

The column “Reset State” indicates whether the PIO Line resets in I/O mode or in peripheral mode. If I/O is specified, the PIO Line resets in input with the pull-up enabled, so that the device is maintained in a static state as soon as the reset is released. As a result, the bit corresponding to the PIO Line in the register PIO_PSR (Peripheral Status Register) resets low.

If a signal name is specified in the “Reset State” column, the PIO Line is assigned to this function and the corresponding bit in PIO_PSR resets high. This is the case of pins controlling memories, in particular the address lines, which require the pin to be driven as soon as the reset is released. Note that the pull-up resistor is also enabled in this case.

10.3.1 PIO Controller A Multiplexing

Table 10-2. Multiplexing on PIO Controller A

PIO Controller A					Application Usage	
I/O Line	Peripheral A	Peripheral B	Reset State	Power Supply	Function	Comments
PA0	MCI0_DA0	SPI0_MISO	I/O	VDDIOP0		
PA1	MCI0_CDA	SPI0_MOSI	I/O	VDDIOP0		
PA2		SPI0_SPCK	I/O	VDDIOP0		
PA3	MCI0_DA1	SPI0_NPCS1	I/O	VDDIOP0		
PA4	MCI0_DA2	SPI0_NPCS2	I/O	VDDIOP0		
PA5	MCI0_DA3	SPI0_NPCS0	I/O	VDDIOP0		
PA6	MCI1_CK	PCK2	I/O	VDDIOP0		
PA7	MCI1_CDA		I/O	VDDIOP0		
PA8	MCI1_DA0		I/O	VDDIOP0		
PA9	MCI1_DA1		I/O	VDDIOP0		
PA10	MCI1_DA2		I/O	VDDIOP0		
PA11	MCI1_DA3		I/O	VDDIOP0		
PA12	MCI0_CK		I/O	VDDIOP0		
PA13	CANTX	PCK0	I/O	VDDIOP0		
PA14	CANRX	IRQ0	I/O	VDDIOP0		
PA15	TCLK2	IRQ1	I/O	VDDIOP0		
PA16	MCI0_CDB	EBI1_D16	I/O	VDDIOM1		
PA17	MCI0_DB0	EBI1_D17	I/O	VDDIOM1		
PA18	MCI0_DB1	EBI1_D18	I/O	VDDIOM1		
PA19	MCI0_DB2	EBI1_D19	I/O	VDDIOM1		
PA20	MCI0_DB3	EBI1_D20	I/O	VDDIOM1		
PA21	MCI1_CDB	EBI1_D21	I/O	VDDIOM1		
PA22	MCI1_DB0	EBI1_D22	I/O	VDDIOM1		
PA23	MCI1_DB1	EBI1_D23	I/O	VDDIOM1		
PA24	MCI1_DB2	EBI1_D24	I/O	VDDIOM1		
PA25	MCI1_DB3	EBI1_D25	I/O	VDDIOM1		
PA26	TXD0	EBI1_D26	I/O	VDDIOM1		
PA27	RXD0	EBI1_D27	I/O	VDDIOM1		
PA28	RTS0	EBI1_D28	I/O	VDDIOM1		
PA29	CTS0	EBI1_D29	I/O	VDDIOM1		
PA30	SCK0	EBI1_D30	I/O	VDDIOM1		
PA31	DMARQ0	EBI1_D31	I/O	VDDIOM1		

10.3.2 PIO Controller B Multiplexing

Table 10-3. Multiplexing on PIO Controller B

PIO Controller B					Application Usage	
I/O Line	Peripheral A	Peripheral B	Reset State	Power Supply	Function	Comments
PB0	AC97FS	TF0	I/O	VDDIOP0		
PB1	AC97CK	TK0	I/O	VDDIOP0		
PB2	AC97TX	TD0	I/O	VDDIOP0		
PB3	AC97RX	RD0	I/O	VDDIOP0		
PB4	TWD	RK0	I/O	VDDIOP0		
PB5	TWCK	RF0	I/O	VDDIOP0		
PB6	TF1	DMARQ1	I/O	VDDIOP0		
PB7	TK1	PWM0	I/O	VDDIOP0		
PB8	TD1	PWM1	I/O	VDDIOP0		
PB9	RD1	LCDCC	I/O	VDDIOP0		
PB10	RK1	PCK1	I/O	VDDIOP0		
PB11	RF1	SPI0_NPCS3	I/O	VDDIOP0		
PB12	SPI1_MISO		I/O	VDDIOP0		
PB13	SPI1_MOSI		I/O	VDDIOP0		
PB14	SPI1_SPCK		I/O	VDDIOP0		
PB15	SPI1_NPCS0		I/O	VDDIOP0		
PB16	SPI1_NPCS1	PCK1	I/O	VDDIOP0		
PB17	SPI1_NPCS2	TIOA2	I/O	VDDIOP0		
PB18	SPI1_NPCS3	TIOB2	I/O	VDDIOP0		
PB19			I/O	VDDIOP0		
PB20			I/O	VDDIOP0		
PB21			I/O	VDDIOP0		
PB22			I/O	VDDIOP0		
PB23			I/O	VDDIOP0		
PB24		DMARQ3	I/O	VDDIOP0		
PB25			I/O	VDDIOP0		
PB26			I/O	VDDIOP0		
PB27		PWM2	I/O	VDDIOP0		
PB28		TCLK0	I/O	VDDIOP0		
PB29		PWM3	I/O	VDDIOP0		
PB30			I/O	VDDIOP0		
PB31			I/O	VDDIOP0		

10.3.3 PIO Controller C Multiplexing

Table 10-4. Multiplexing on PIO Controller C

PIO Controller C					Application Usage	
I/O Line	Peripheral A	Peripheral B	Reset State	Power Supply	Function	Comments
PC0	LCDVSYNC		I/O	VDDIOP0		
PC1	LCDHSYNC		I/O	VDDIOP0		
PC2	LCDDOTCK		I/O	VDDIOP0		
PC3	LCDDEN	PWM1	I/O	VDDIOP0		
PC4	LCDD0	LCDD3	I/O	VDDIOP0		
PC5	LCDD1	LCDD4	I/O	VDDIOP0		
PC6	LCDD2	LCDD5	I/O	VDDIOP0		
PC7	LCDD3	LCDD6	I/O	VDDIOP0		
PC8	LCDD4	LCDD7	I/O	VDDIOP0		
PC9	LCDD5	LCDD10	I/O	VDDIOP0		
PC10	LCDD6	LCDD11	I/O	VDDIOP0		
PC11	LCDD7	LCDD12	I/O	VDDIOP0		
PC12	LCDD8	LCDD13	I/O	VDDIOP0		
PC13	LCDD9	LCDD14	I/O	VDDIOP0		
PC14	LCDD10	LCDD15	I/O	VDDIOP0		
PC15	LCDD11	LCDD19	I/O	VDDIOP0		
PC16	LCDD12	LCDD20	I/O	VDDIOP0		
PC17	LCDD13	LCDD21	I/O	VDDIOP0		
PC18	LCDD14	LCDD22	I/O	VDDIOP0		
PC19	LCDD15	LCDD23	I/O	VDDIOP0		
PC20	LCDD16	ETX2	I/O	VDDIOP0		
PC21	LCDD17	ETX3	I/O	VDDIOP0		
PC22	LCDD18	ERX2	I/O	VDDIOP0		
PC23	LCDD19	ERX3	I/O	VDDIOP0		
PC24	LCDD20	ETXER	I/O	VDDIOP0		
PC25	LCDD21	ERXDV	I/O	VDDIOP0		
PC26	LCDD22	ECOL	I/O	VDDIOP0		
PC27	LCDD23	ERXCK	I/O	VDDIOP0		
PC28	PWM0	TCLK1	I/O	VDDIOP0		
PC29	PCK0	PWM2	I/O	VDDIOP0		
PC30	DRXD		I/O	VDDIOP0		
PC31	DTXD		I/O	VDDIOP0		

10.3.4 PIO Controller D Multiplexing

Table 10-5. Multiplexing on PIO Controller D

PIO Controller D					Application Usage	
I/O Line	Peripheral A	Peripheral B	Reset State	Power Supply	Function	Comments
PD0	TXD1	SPI0_NPCS2	I/O	VDDIOP0		
PD1	RXD1	SPI0_NPCS3	I/O	VDDIOP0		
PD2	TXD2	SPI1_NPCS2	I/O	VDDIOP0		
PD3	RXD2	SPI1_NPCS3	I/O	VDDIOP0		
PD4	FIQ	DMARQ2	I/O	VDDIOP0		
PD5	EBI0_NWAIT	RTS2	I/O	VDDIOM0		
PD6	EBI0_NCS4/CFCS0	CTS2	I/O	VDDIOM0		
PD7	EBI0_NCS5/CFCS1	RTS1	I/O	VDDIOM0		
PD8	EBI0_CFCE1	CTS1	I/O	VDDIOM0		
PD9	EBI0_CFCE2	SCK2	I/O	VDDIOM0		
PD10		SCK1	I/O	VDDIOM0		
PD11	EBI0_NCS2	TSYNC	I/O	VDDIOM0		
PD12	EBI0_A23	TCLK	A23	VDDIOM0		
PD13	EBI0_A24	TPS0	A24	VDDIOM0		
PD14	EBI0_A25_CFRNW	TPS1	A25	VDDIOM0		
PD15	EBI0_NCS3/NANDCS	TPS2	I/O	VDDIOM0		
PD16	EBI0_D16	TPK0	I/O	VDDIOM0		
PD17	EBI0_D17	TPK1	I/O	VDDIOM0		
PD18	EBI0_D18	TPK2	I/O	VDDIOM0		
PD19	EBI0_D19	TPK3	I/O	VDDIOM0		
PD20	EBI0_D20	TPK4	I/O	VDDIOM0		
PD21	EBI0_D21	TPK5	I/O	VDDIOM0		
PD22	EBI0_D22	TPK6	I/O	VDDIOM0		
PD23	EBI0_D23	TPK7	I/O	VDDIOM0		
PD24	EBI0_D24	TPK8	I/O	VDDIOM0		
PD25	EBI0_D25	TPK9	I/O	VDDIOM0		
PD26	EBI0_D26	TPK10	I/O	VDDIOM0		
PD27	EBI0_D27	TPK11	I/O	VDDIOM0		
PD28	EBI0_D28	TPK12	I/O	VDDIOM0		
PD29	EBI0_D29	TPK13	I/O	VDDIOM0		
PD30	EBI0_D30	TPK14	I/O	VDDIOM0		
PD31	EBI0_D31	TPK15	I/O	VDDIOM0		

10.3.5 PIO Controller E Multiplexing

Table 10-6. Multiplexing on PIO Controller E

PIO Controller E					Application Usage	
I/O Line	Peripheral A	Peripheral B	Reset State	Power Supply	Function	Comments
PE0	ISI_D0		I/O	VDDIOP1		
PE1	ISI_D1		I/O	VDDIOP1		
PE2	ISI_D2		I/O	VDDIOP1		
PE3	ISI_D3		I/O	VDDIOP1		
PE4	ISI_D4		I/O	VDDIOP1		
PE5	ISI_D5		I/O	VDDIOP1		
PE6	ISI_D6		I/O	VDDIOP1		
PE7	ISI_D7		I/O	VDDIOP1		
PE8	ISI_PCK	TIOA1	I/O	VDDIOP1		
PE9	ISI_HSYNC	TIOB1	I/O	VDDIOP1		
PE10	ISI_VSYNC	PWM3	I/O	VDDIOP1		
PE11		PCK3	I/O	VDDIOP1		
PE12		ISI_D8	I/O	VDDIOP1		
PE13		ISI_D9	I/O	VDDIOP1		
PE14		ISI_D10	I/O	VDDIOP1		
PE15		ISI_D11	I/O	VDDIOP1		
PE16			I/O	VDDIOP1		
PE17			I/O	VDDIOP1		
PE18		TIOA0	I/O	VDDIOP1		
PE19		TIOB0	I/O	VDDIOP1		
PE20		EBI1_NWAIT	I/O	VDDIOM1		
PE21	ETXCK	EBI1_NANDWE	I/O	VDDIOM1		
PE22	ECRS	EBI1_NCS2/NANDCS	I/O	VDDIOM1		
PE23	ETX0	EB1_NANDOE	I/O	VDDIOM1		
PE24	ETX1	EBI1_NWR3/NBS3	I/O	VDDIOM1		
PE25	ERX0	EBI1_NCS1/SDCS	I/O	VDDIOM1		
PE26	ERX1		I/O	VDDIOM1		
PE27	ERXER	EBI1_SDCKE	I/O	VDDIOM1		
PE28	ETXEN	EBI1_RAS	I/O	VDDIOM1		
PE29	EMDC	EBI1_CAS	I/O	VDDIOM1		
PE30	EMDIO	EBI1_SDWE	I/O	VDDIOM1		
PE31	EF100	EBI1_SDA10	I/O	VDDIOM1		

10.4 System Resource Multiplexing

10.4.1 LCD Controller

The LCD Controller can interface with several LCD panels. It supports 4 bits per pixel (bpp), 8 bpp or 16 bpp without limitation. Interfacing 24 bpp TFT panels prevents using the Ethernet MAC. 16 bpp TFT panels are interfaced through peripheral B functions, as color data is output on LCDD3 to LCDD7, LCDD11 to LCDD15 and LCDD19 to LCDD23. Intensity bit is output on LCDD10. Using the peripheral B does not prevent using MAC lines. 16 bpp STN panels are interfaced through peripheral A and color data is output on LCDD0 to LCDD15, thus MAC lines can be used on peripheral B.

Mapping the LCD signals on peripheral A and peripheral B makes is possible to use 24 bpp TFT panels in 24 bits (peripheral A) or 16 bits (peripheral B) by reprogramming the PIO controller and thus without hardware modification.

10.4.2 ETM™

Using the ETM prevents the use of the EBI0 in 32-bit mode. Only 16-bit mode (EBI0_D0 to EBI0_D15) is available, makes EBI0 unable to interface CompactFlash and NAND Flash cards, reduces EBI0's address bus width which makes it unable to address memory ranges bigger than 0x7FFFFF and finally it makes impossible to use EBI0_NCS2 and EBI0_NCS3.

10.4.3 EBI1

Using the following features prevents using EBI1 in 32-bit mode:

- the second slots of MCI0 and/or MCI1
- USART0
- DMA request 0 (DMARQ0)

10.4.4 Ethernet 10/100MAC

Using the following features of EBI1 prevents using Ethernet 10/100MAC:

- SDRAM
- NAND (unless NANDCS, NANDOE and NANDWE are managed by PIO)
- SMC 32 bits (SMC 16 bits is still available)
- NCS1, NCS2 are not available in SMC mode

10.4.5 SSC

Using SSC0 prevents using the AC97 Controller and Two-wire Interface.

Using SSC1 prevents using DMA Request 1, PWM0, PWM1, LCDCC and PCK1.

10.4.6 USART

Using USART2 prevents using EBI0's NWAIT signal, Chip Select 4 and CompactFlash Chip Enable 2.

Using USART1 prevents using EBI0's Chip Select 5 and CompactFlash Chip Enable1.

10.4.7 NAND Flash

Using the NAND Flash interface on EBI1 prevents using Ethernet MAC.

10.4.8 CompactFlash

Using the CompactFlash interface prevents using NCS4 and/or NCS5 to access other parallel devices.

10.4.9 SPI0 and MCI Interface

SPI0 signals and MCI0 signals are multiplexed, as the DataFlash Card is hardware-compatible with the SDCard. Only one can be used at a time.

10.4.10 Interrupts

Using IRQ0 prevents using the CAN controller.

Using FIQ prevents using DMA Request 2.

10.4.11 Image Sensor Interface

Using ISI in 8-bit data mode prevents using timers TIOA1, TIOB1.

10.4.12 Timers

Using TIOA2 and TIOB2, in this order, prevents using SPI1's Chip Selects [2-3].

10.5 Embedded Peripherals Overview

10.5.1 Serial Peripheral Interface

- Supports communication with serial external devices
  - Four chip selects with external decoder support allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
- Very fast transfers supported
  - Transfers with baud rates up to MCK
  - The chip select line may be left active to speed up transfers on the same device

10.5.2 Two-wire Interface

- Master Mode only
- Compatibility with standard two-wire serial memory
- One, two or three bytes for slave address
- Sequential read/write operations

10.5.3 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB- or LSB-first
  - Optional break generation and detection

- By 8 or by-16 over-sampling receiver frequency
- Hardware handshaking RTS-CTS
- Receiver time-out and transmitter timeguard
- Optional Multi-drop Mode with address generation and detection
- Optional Manchester Encoding

- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit
- IrDA modulation and demodulation
  - Communication at up to 115.2 Kbps
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo

10.5.4 Serial Synchronous Controller

- Provides serial synchronous communication links used in audio and telecom applications (with CODECs in Master or Slave Modes, I^2S, TDM Buses, Magnetic Card Reader, etc.)
- Contains an independent receiver and transmitter and a common clock divider
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

10.5.5 AC97 Controller

- Compatible with AC97 Component Specification V2.2
- Can interface with a single analog front end
- Three independent RX Channels and three independent TX Channels
  - One RX and one TX channel dedicated to the AC97 analog front end control
  - One RX and one TX channel for data transfers, associated with a PDC
  - One RX and one TX channel for data transfers with no PDC
- Time Slot Assigner that can assign up to 12 time slots to a channel
- Channels support mono or stereo up to 20-bit sample length
  - Variable sampling rate AC97 Codec Interface (48 kHz and below)

10.5.6 Timer Counter

- Three 16-bit Timer Counter Channels
- Wide range of functions including:
  - Frequency Measurement
  - Event Counting
  - Interval Measurement
  - Pulse Generation
  - Delay Timing
  - Pulse Width Modulation
  - Up/down Capabilities
- Each channel is user-configurable and contains:
  - Three external clock inputs
  - Five internal clock inputs
  - Two multi-purpose input/output signals

- Two global registers that act on all three TC Channels

10.5.7 Pulse Width Modulation Controller

- 4 channels, one 16-bit counter per channel
- Common clock generator, providing thirteen different clocks
  - Modulo n counter providing eleven clocks
  - Two independent Linear Dividers working on modulo n counter outputs
- Independent channel programming
  - Independent Enable Disable commands
  - Independent clock selection
  - Independent period and duty cycle, with double bufferization
  - Programmable selection of the output waveform polarity
  - Programmable center or left aligned output waveform

10.5.8 Multimedia Card Interface

- Two double-channel Multimedia Card Interfaces, allowing concurrent transfers with 2 cards
- Compatibility with MultiMediaCard Specification Version 3.31
- Compatibility with SD Memory Card Specification Version 1.0
- Compatibility with SDIO Specification Version V1.1
- Cards clock rate up to Master Clock divided by 2
- Embedded power management to slow down clock rate when not used
- Each MCI has two slots, each supporting
  - One slot for one MultiMediaCard bus (up to 30 cards) or
  - One SD Memory Card
- Support for stream, block and multi-block data read and write

10.5.9 CAN Controller

- Fully compliant with 16-mailbox CAN 2.0A and 2.0B CAN Controllers
- Bit rates up to 1Mbit/s.
- Object-oriented mailboxes, each with the following properties:
  - CAN Specification 2.0 Part A or 2.0 Part B programmable for each message
  - Object Configurable as receive (with overwrite or not) or transmit
  - Local Tag and Mask Filters up to 29-bit Identifier/Channel
  - 32 bits access to Data registers for each mailbox data object
  - Uses a 16-bit time stamp on receive and transmit message
  - Hardware concatenation of ID unmasked bitfields to speedup family ID processing
  - 16-bit internal timer for Time Stamping and Network synchronization
  - Programmable reception buffer length up to 16 mailbox object
  - Priority Management between transmission mailboxes
  - Autobaud and listening mode
  - Low power mode and programmable wake-up on bus activity or by the application
  - Data, Remote, Error and Overload Frame handling

10.5.10 USB Host Port

- Compliant with Open HCI Rev 1.0 Specification
- Compliant with USB V2.0 full-speed and low-speed specification

- Supports both low-speed 1.5 Mbps and full-speed 12 Mbps devices
- Root hub integrated with two downstream USB ports
- Two embedded USB transceivers
- Supports power management
- Operates as a master on the matrix

10.5.11 USB Device Port

- USB V2.0 full-speed compliant, 12 Mbits per second
- Embedded USB V2.0 full-speed transceiver
- Embedded 2,432-byte dual-port RAM for endpoints
- Suspend/Resume logic
- Ping-pong mode (two memory banks) for isochronous and bulk endpoints
- Six general-purpose endpoints
  - Endpoint 0 and 3: 64 bytes, no ping-pong mode
  - Endpoint 1 and 2: 64 bytes, ping-pong mode
  - Endpoint 4 and 5: 512 bytes, ping-pong mode

10.5.12 LCD Controller

- Single and Dual scan color and monochrome passive STN LCD panels supported
- Single scan active TFT LCD panels supported
- 4-bit single scan, 8-bit single or dual scan, 16-bit dual scan STN interfaces supported
- Up to 24-bit single scan TFT interfaces supported
- Up to 16 gray levels for mono STN and up to 4096 colors for color STN displays
- 1, 2 bits per pixel (palletized), 4 bits per pixel (non-palletized) for mono STN
- 1, 2, 4, 8 bits per pixel (palletized), 16 bits per pixel (non-palletized) for color STN
- 1, 2, 4, 8 bits per pixel (palletized), 16, 24 bits per pixel (non-palletized) for TFT
- Single clock domain architecture
- Resolution supported up to 2048x2048
- 2D DMA Controller for management of virtual Frame Buffer
  - Allows management of frame buffer larger than the screen size and moving the view over this virtual frame buffer
- Automatic resynchronization of the frame buffer pointer to prevent flickering

10.5.13 Two D Graphics Controller

- Acts as one Matrix Master
- Commands are passed through the APB User Interface
- Operates directly in the frame buffer of the LCD Controller
  - Line draw
  - Block transfer
  - Clipping
- Commands queuing through a FIFO

10.5.14 Ethernet 10/100 MAC

- Compatibility with IEEE Standard 802.3
- 10 and 100 Mbits per second data throughput capability
- Full- and half-duplex operations
- MII or RMII interface to the physical layer

- Register Interface to address, data, status and control registers
- DMA Interface, operating as a master on the Memory Controller
- Interrupt generation to signal receive and transmit completion
- 28-byte transmit and 28-byte receive FIFOs
- Automatic pad and CRC generation on transmitted frames
- Address checking logic to recognize four 48-bit addresses
- Support promiscuous mode where all valid frames are copied to memory
- Support physical layer management through MDIO interface control of alarm and update time/calendar data in

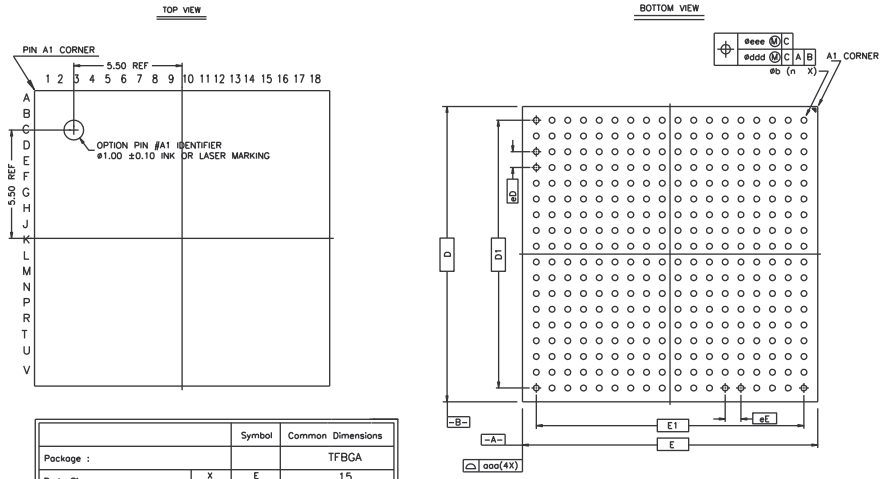
10.5.15 Image Sensor Interface

- ITU-R BT. 601/656 8-bit mode external interface support
- Support for ITU-R BT.656-4 SAV and EAV synchronization
- Vertical and horizontal resolutions up to 2048 x 2048
- Preview Path up to 640*480
- Support for packed data formatting for YCbCr 4:2:2 formats
- Preview scaler to generate smaller size image
- Programmable frame capture rate

11. Package Drawings

11.1 Package Drawing AT91SAM9263B-CU

Figure 11-1. 324-ball TFBGA Package Drawing



		Symbol	Common Dimensions
Package :			TFBGA
Body Size:	X	E	15
	Y	D	15
Ball Pitch :	X	eE	0.80
	Y	eD	0.80
Total Thickness :		A	1.20 MAX
Mold Thickness :		M	0.53 Ref.
Substrate Thickness :		S	0.26 Ref.
Ball Diameter :			0.30
Stand Off :		A1	0.16 ~ 0.26
Ball Width :		b	0.40 ~ 0.40
Package Edge Tolerance :		aaa	1.20
Mold Flatness :		bbb	0.53
Coplanarity:		ccc	0.08
Ball Offset (Package) :		ddd	0.15
Ball Offset (Ball) :		eee	0.08
Ball Count :		n	324
Edge Ball Center to Center :	X	E1	13.60
	Y	D1	13.60

Table 11-1. Soldering Information

Ball Land	0.4 mm +/- 0.05
Soldering Mask Opening	0.275 mm +/- 0.03

Table 11-2. Device and 324-ball TFBGA Package Maximum Weight

572	mg

Table 11-3. 324-ball TFBGA Package Characteristics

Moisture Sensitivity Level	3

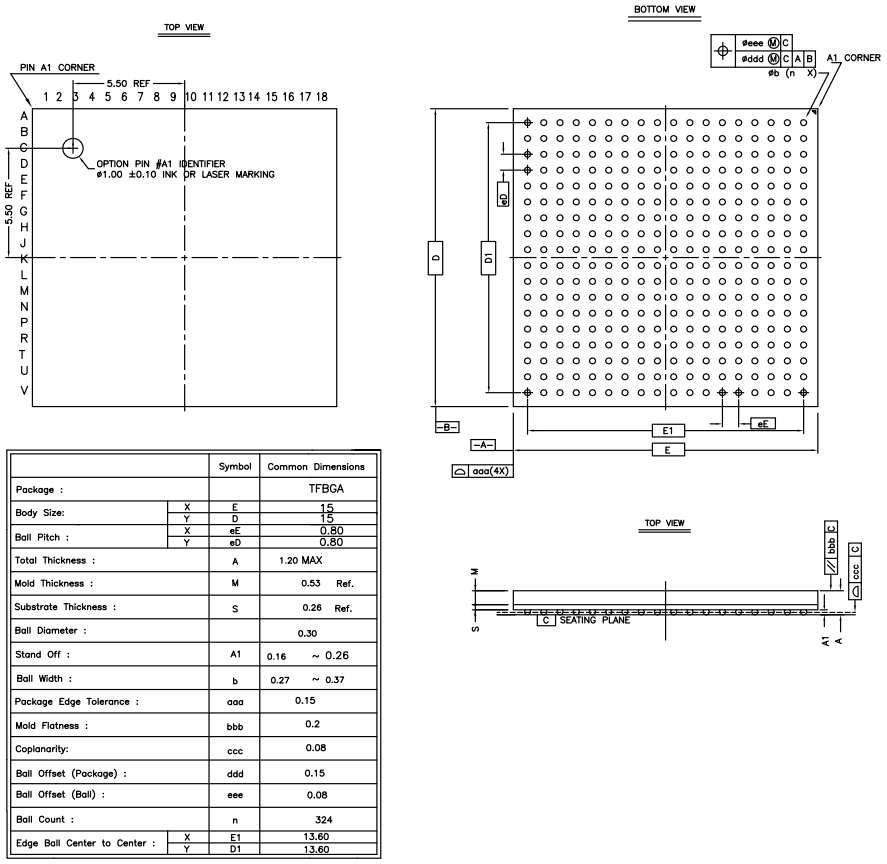
Table 11-4. Package Reference

JEDEC Drawing Reference	MO-210
JESD97 Classification	e1

This package respects the recommendations of the NEMI User Group.

11.2 Package Drawing (AT91SAM9263B-CU-100)

Figure 11-2. 324-ball TFBGA Package Drawing



		Symbol	Common Dimensions
Package :			TFBGA
Body Size:	X	E	15
	Y	D	15
Ball Pitch :	X	eE	0.80
	Y	eD	0.80
Total Thickness :		A	1.20 MAX
Mold Thickness :		M	0.53 Ref.
Substrate Thickness :		S	0.26 Ref.
Ball Diameter :			0.30
Stand Off :		A1	0.16 ~ 0.26
Ball Width :		b	0.27 ~ 0.37
Package Edge Tolerance :		aaa	0.15
Mold Flatness :		bbb	0.2
Coplanarity:		ccc	0.08
Ball Offset (Package) :		ddd	0.15
Ball Offset (Ball) :		eee	0.08
Ball Count :		n	324
Edge Ball Center to Center :	X	E1	13.60
	Y	D1	13.60

Table 11-5. Soldering Information

Ball Land	0.4 mm +/- 0.05
Solder Mask Opening	0.275 mm +/- 0.03

Table 11-6. Device and 324-ball TFBGA Package Maximum Weight

572	mg

Table 11-7. 324-ball TFBGA Package Characteristics

Moisture Sensitivity Level	3

Table 11-8. Package Reference

JEDEC Drawing Reference	MO-275
JESD97 Classification	e8

This package respects the recommendations of the NEMI User Group.

12. AT91SAM9263 Ordering Information

Table 12-1. AT91SAM9263 Ordering Information

Marketing Revision Level B Ordering Code	Package	Package Type	Temperature Operating Range
AT91SAM9263B-CU	TFBGA 324	Green	Industrial -40°C to 85°C
AT91SAM9263B-CU-100	TFBGA 324	Green	Industrial -40°C to 85°C

13. Revision History

Table 13-1. Revision History

Document Ref.	Comments	Change Request Ref.
6459IS	**Ordering Code:** Table 12-1, "AT91SAM9263 Ordering Information", Removed all reference to Marketing Revision Level A, AT91SAM9263-CU Added AT91SAM9263B-CU-100 to Marketing Revision Level B Ordering Code.	8456 (msg3)
	Package Drawings: Section 11. "Package Drawings" Old Package Drawing removed. Existing package described in: Section 11.1 "Package Drawing AT91SAM9263B-CU" Package drawings and related information added for SAM9263B-CU-100. Section 11.2 "Package Drawing (AT91SAM9263B-CU-100)" Document format updated with subsequent change to pagination.	8456 (msg3)
6249HS	EBI0_NCS3 restriction added to Section 10.4.2 "ETM™" on page 38	6053
	Second paragraph in Section 5.3 "Programmable I/O Lines Power Supplies" on page 13 edited.	6395
6249GS	Overview: "Features" Debug Unit (DBGU) updated. Section 10.4.3 "EBI1", updated Section 10.4.4 "Ethernet 10/100MAC", added to datasheet Section 6.5 "Shutdown Logic Pins", updated, "SHDN pin is tri state output....."	5846 5903 rfo
6249FS	Section 5.1 "Power Supplies", VDDCORE and VDDBU updated. Section 5.2, "Power Sequence Requirements removed from datasheet.	5791/5793
6249ES	New Ordering Code: **AT91SAM9263B-CU** added to Table 12-1, "AT91SAM9263 Ordering Information".	5560
	Section 8.1.2.1 "BMS = 1, Boot on Embedded ROM", changes to list under "Bootloader on a non-volatile memory"	5425
	Section 5.2 "Power Sequence Requirements", section added to datasheet.	5643
	Section 10.4.3 "EBI1", System Resource Multiplexing, Ethernet 10/100 MAC limitation on EBI1 updated.	5713
	Section 10.5.8 "Multimedia Card Interface", protocol specification compatibilities updated.	5282
	Section 10.5.13 "Two D Graphics Controller", removed reference to Polygon Fill, removed from Features also.	5206
	Table 3-1, "Signal Description List", Image Sensor Interface, ISI_MCK is provided by PCK3. Table 10-6, "Multiplexing on PIO Controller E", ISI_MCK removed from PE11 line of the table.	5329

Table 13-1. Revision History

Document Ref.	Comments	Change Request Ref.
6249DS	”Features”, SPI: Synchronous Communications feature removed.	4910
	Section 5.1 ”Power Supplies”, VDDIO and VDDBU slope alignment described.	4967
	Section 5.2 ”Power Consumption”, paragraph beginning with “On VDDBU...” updated.	4505
	Section 10.5.8 ”Multimedia Card Interface”, “When REMAP = 1.....” removed from 2nd paragraph.	5029
	Section 10.5.8 ”Multimedia Card Interface”, MMC and SDMC compatibility updated.	4945
	Section 8.2.1.1 ”External Bus Interface 0”, feature added.	4146
	Section 8.2.1.1 ”External Bus Interface 0”, feature added.	
	“Package and Pinout” , references to package are “324-TFBGA.	4664
	Figure 9-3 ”AT91SAM9263 Power Management Controller Block Diagram” on page 28, /3 divider removed.	4834
	Figure 11-1 ”324-ball TFBGA Package Drawing” on page 44, updated.	4668

Table 13-1. Revision History

Document Ref.	Comments	Change Request Ref.
6249CS	In Section 4.1 “324-ball TFBGA Package Outline” on page 10 corrected package top view.	4463
	All new information for Table 7-1, “List of Bus Matrix Masters,” on page 16, Table 7-2, “List of Bus Matrix Slaves,” on page 16 and Table 7-3, “Masters to Slaves Access,” on page 17.	4466
	In Section 9.3 “Shutdown Controller” on page 27, corrected reference to shutdown pin.	3870
	In Section 5.2 “Power Consumption” on page 13, specified static current consumption as worst case. Corrected Section 10.4.7 “NAND Flash” on page 38, with information on EMAC.	3825
	In Section 10.4.3 “EBI1” on page 38, added Ethernet 10/100 MAC to the System Resource Multiplexing list of EBI1.	4064
	In Section 10.4.11 “Image Sensor Interface” on page 39 and Section 10.4.12 “Timers” on page 39, removed mention of keyboard interfaces.	4407
6249BS	Corrected typo to IDE hard disk in Section “Description” on page 1.	3804
	Corrected ordering code in Section “” on page 46.	3805
6249AS	First issue.	



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