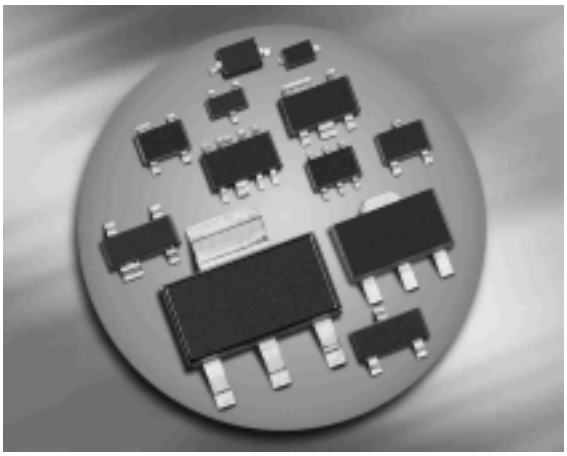
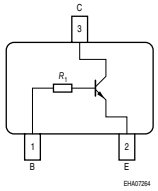
**NPN Silicon Digital Transistor**

- Switching circuit, inverter, interface circuit, driver circuit
- Built in bias resistor ($R_1$ = 47 kΩ)



**BCR149F/L3**
**BCR149T**




| Type | Marking | Pin Configuration | | | | | | Package |
|---|---|---|---|---|---|---|---|---|
| BCR149F* | UAs | 1=B | 2=E | 3=C | - | - | - | TSFP-3 |
| BCR149L3* | UA | 1=B | 2=E | 3=C | - | - | - | TSLP-3-4 |
| BCR149T* | UA | 1=B | 2=E | 3=C | - | - | - | SC75 |

* Preliminary

**Maximum Ratings**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Collector-emitter voltage | $V_{CEO}$ | 50 | V |
| Collector-base voltage | $V_{CBO}$ | 50 | |
| Input forward voltage | $V_{i(fwd)}$ | 80 | |
| Input reverse voltage | $V_{i(rev)}$ | 5 | |
| Collector current | $I_C$ | 70 | mA |
| Total power dissipation- | $P_{tot}$ | | mW |
| BCR149F, $T_S \leq 128°C$ | | 250 | |
| BCR149L3, $T_S \leq 135°C$ | | 250 | |
| BCR149T, $T_S \leq 109°C$ | | 250 | |
| Junction temperature | $T_j$ | 150 | °C |
| Storage temperature | $T_{stg}$ | -65 ... 150 | |

**Thermal Resistance**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Junction - soldering point[1)] | $R_{thJS}$ | | K/W |
| BCR149F | | ≤ 90 | |
| BCR149L3 | | ≤ 60 | |
| BCR149T | | ≤ 165 | |

**Electrical Characteristics** at $T_A$ = 25°C, unless otherwise specified

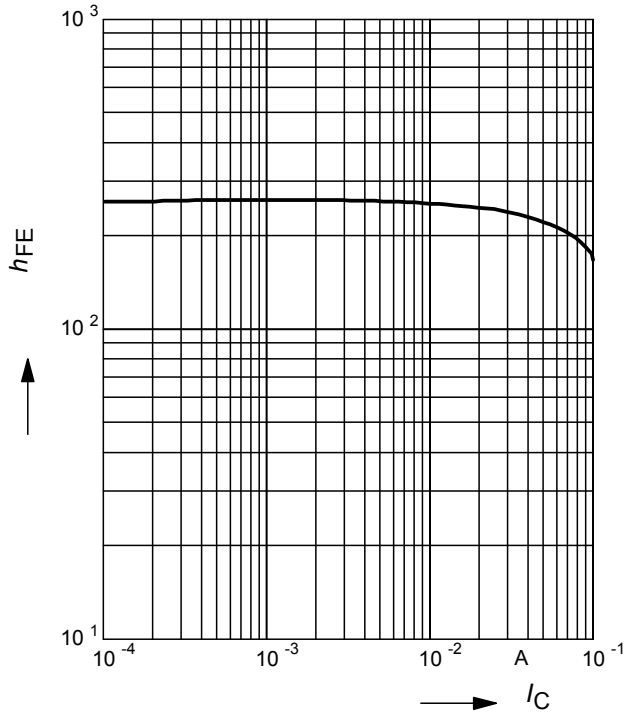
| Parameter | Symbol | Values | | | Unit |
|---|---|---|---|---|---|
| | | min. | typ. | max. | |
| **DC Characteristics** | | | | | |
| Collector-emitter breakdown voltage<br>$I_C$ = 100 µA, $I_B$ = 0 | $V_{(BR)CEO}$ | 50 | - | - | V |
| Collector-base breakdown voltage<br>$I_C$ = 10 µA, $I_E$ = 0 | $V_{(BR)CBO}$ | 50 | - | - | |
| Collector-base cutoff current<br>$V_{CB}$ = 40 V, $I_E$ = 0 | $I_{CBO}$ | - | - | 100 | nA |
| Emitter-base cutoff current<br>$V_{EB}$ = 5 V, $I_C$ = 0 | $I_{EBO}$ | - | - | 100 | nA |
| DC current gain[2)]<br>$I_C$ = 5 mA, $V_{CE}$ = 5 V | $h_{FE}$ | 120 | - | 630 | - |
| Collector-emitter saturation voltage[2)]<br>$I_C$ = 10 mA, $I_B$ = 0.5 mA | $V_{CEsat}$ | - | - | 0.3 | V |
| Input off voltage<br>$I_C$ = 100 µA, $V_{CE}$ = 5 V | $V_{i(off)}$ | 0.4 | - | 0.8 | |
| Input on voltage<br>$I_C$ = 2 mA, $V_{CE}$ = 0.3 V | $V_{i(on)}$ | 0.5 | - | 1.5 | |
| Input resistor | $R_1$ | 32 | 47 | 62 | kΩ |
| **AC Characteristics** | | | | | |
| Transition frequency<br>$I_C$ = 10 mA, $V_{CE}$ = 5 V, $f$ = 100 MHz | $f_T$ | - | 150 | - | MHz |
| Collector-base capacitance<br>$V_{CB}$ = 10 V, $f$ = 1 MHz | $C_{cb}$ | - | 3 | - | pF |

[1]For calculation of $R_{thJA}$ please refer to Application Note Thermal Resistance

[2]Pulse test: t < 300µs; D < 2%

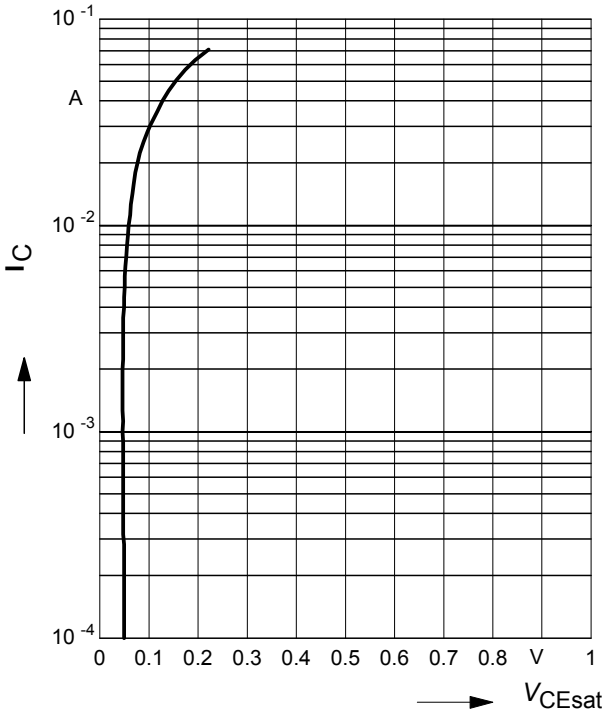
**DC current gain** $h_{FE} = f(I_C)$

$V_{CE}$ = 5 V (common emitter configuration)



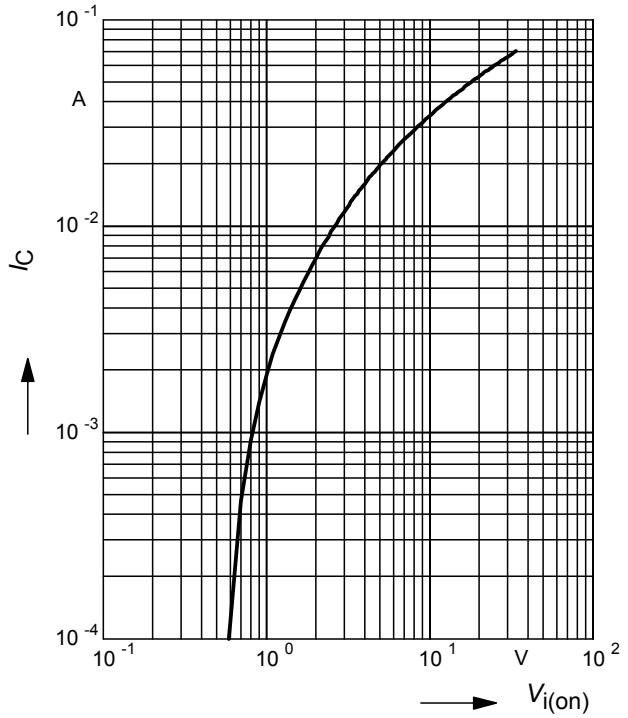

**Collector-emitter saturation voltage**

$V_{CEsat} = f(I_C)$, $h_{FE}$ = 20



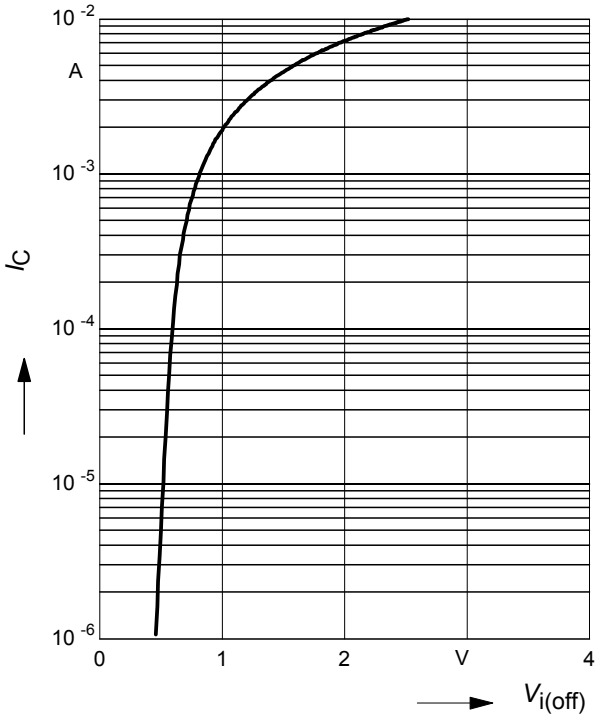

**Input on Voltage** $V_{i(on)} = f(I_C)$

$V_{CE}$ = 0.3V (common emitter configuration)



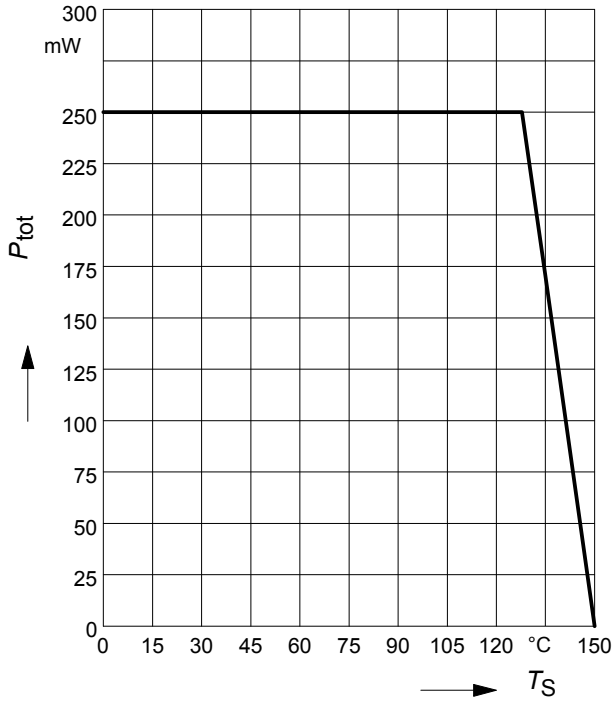

**Input off voltage** $V_{i(off)} = f(I_C)$

$V_{CE}$ = 5V (common emitter configuration)



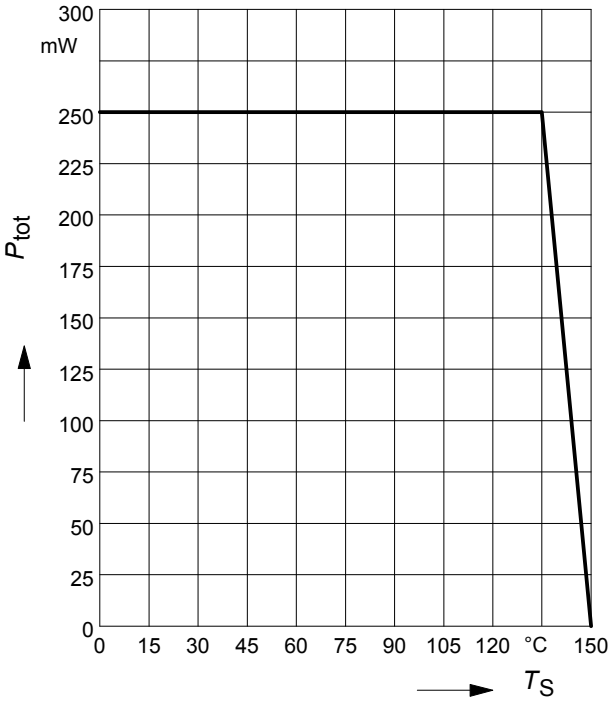
**Total power dissipation $P_{tot} = f(T_S)$**

BCR149F



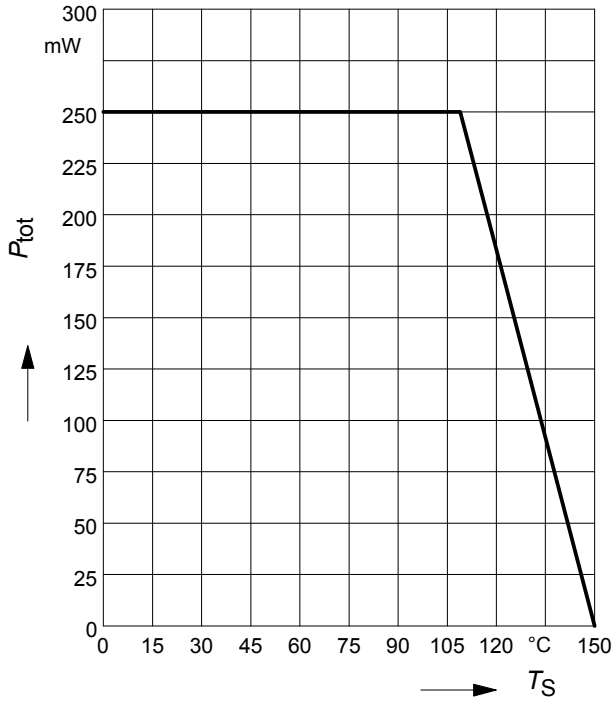

**Total power dissipation $P_{tot} = f(T_S)$**

BCR149L3



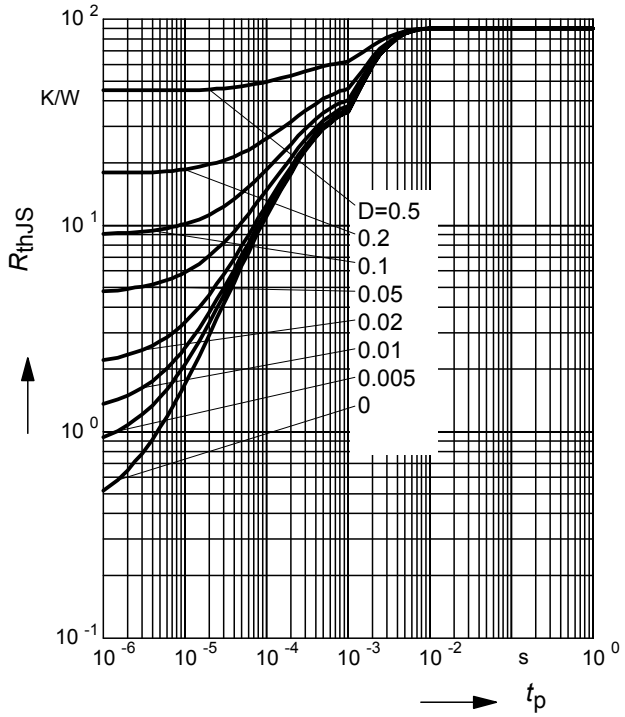

**Total power dissipation $P_{tot} = f(T_S)$**

BCR149T



**Permissible Puls Load** $R_{thJS} = f(t_p)$

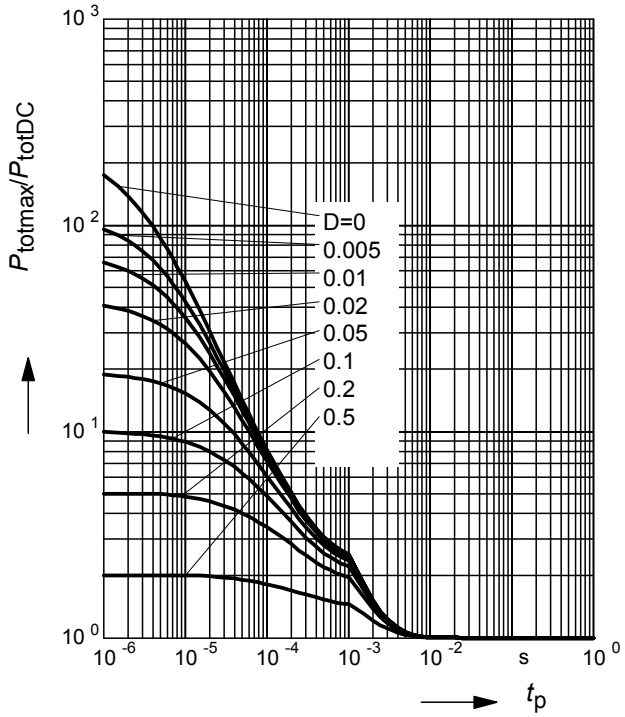
BCR149F




**Permissible Pulse Load**

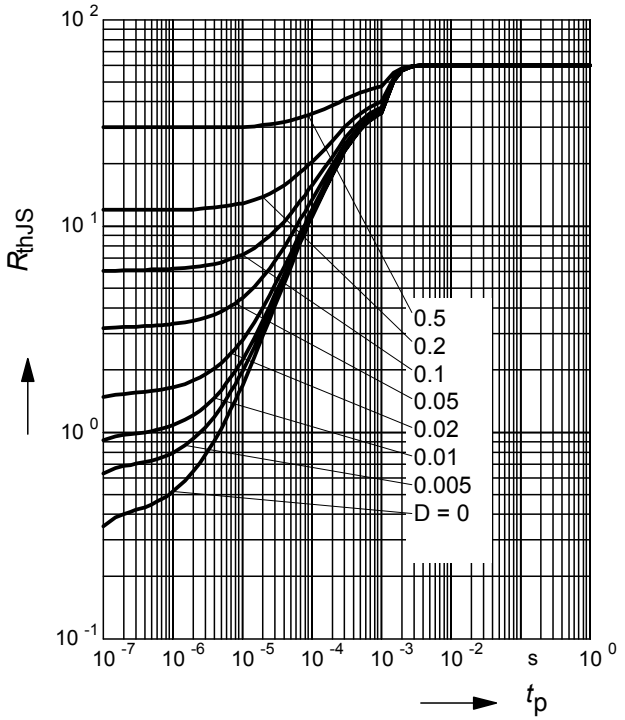
$P_{totmax}/P_{totDC} = f(t_p)$

BCR149F




**Permissible Puls Load** $R_{thJS} = f(t_p)$

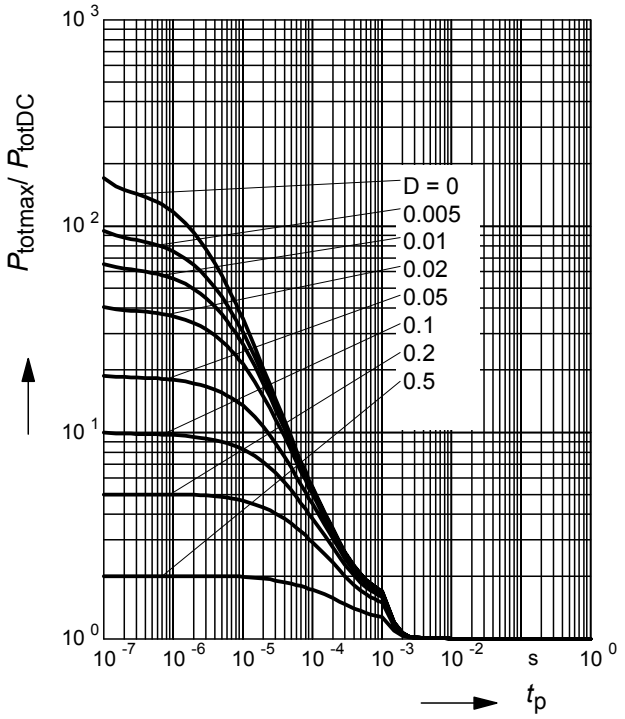
BCR149L3




**Permissible Pulse Load**

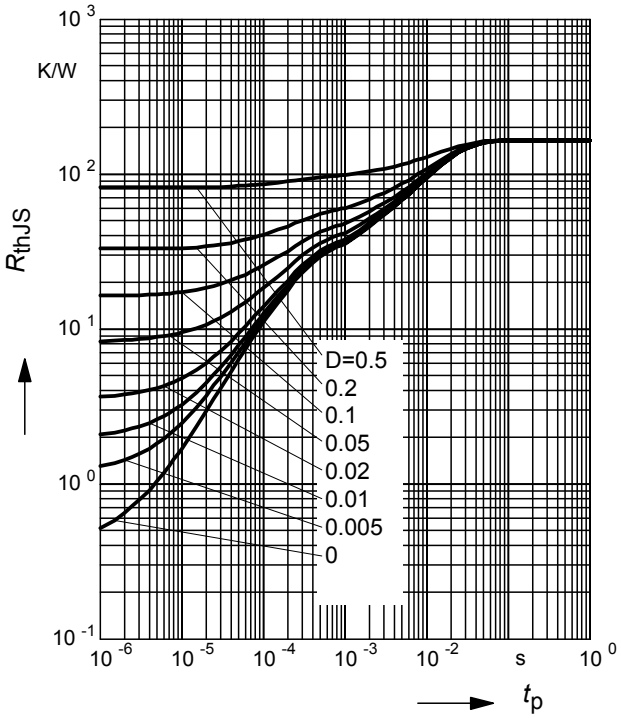
$P_{totmax}/P_{totDC} = f(t_p)$

BCR149L3



**Permissible Puls Load** $R_{thJS} = f(t_p)$

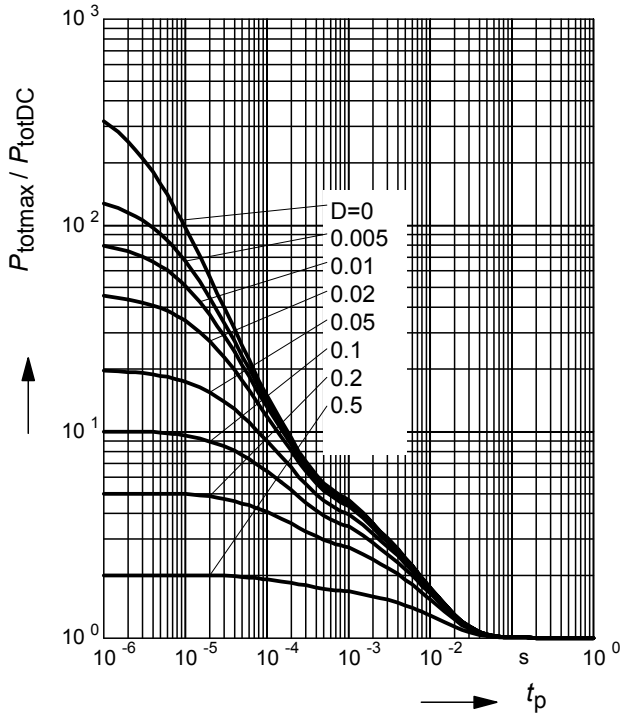
BCR149T



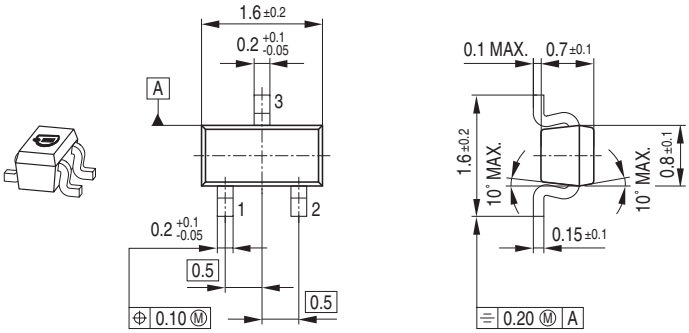

**Permissible Pulse Load**

$P_{totmax}/P_{totDC} = f(t_p)$

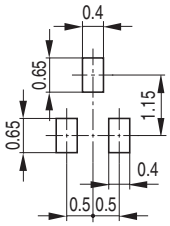
BCR149T



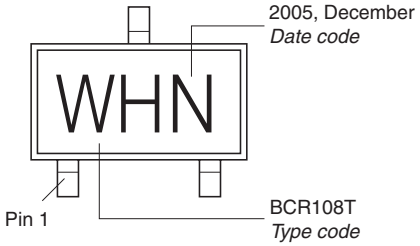
## Package Outline




## Foot Print

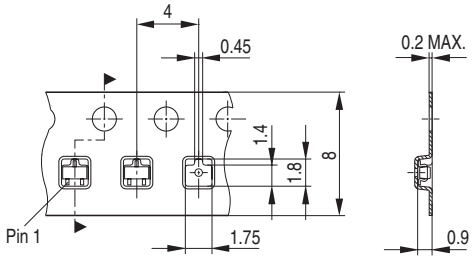



## Marking Layout (Example)




## Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel
Reel ø330 mm = 10.000 Pieces/Reel

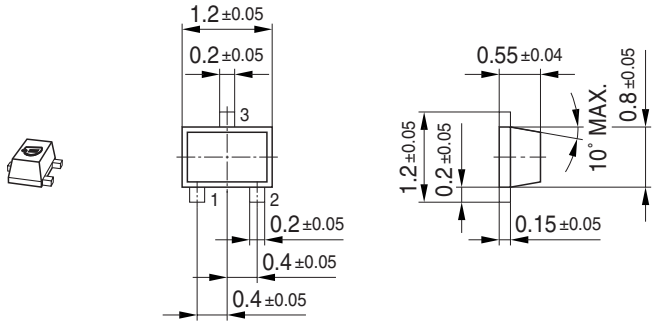


## Date Code marking for discrete packages with one digit (SCD80, SC79, SC75[1)]) CES-Code

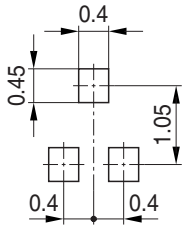
| Month | 2003 | 2004 | 2005 | 2006 | 2007 | 2008 | 2009 | 2010 | 2011 | 2012 | 2013 | 2014 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 01 | a | p | A | P | a | p | A | P | a | p | A | P |
| 02 | b | q | B | Q | b | q | B | Q | b | q | B | Q |
| 03 | c | r | C | R | c | r | C | R | c | r | C | R |
| 04 | d | s | D | S | d | s | D | S | d | s | D | S |
| 05 | e | t | E | T | e | t | E | T | e | t | E | T |
| 06 | f | u | F | U | f | u | F | U | f | u | F | U |
| 07 | g | v | G | V | g | v | G | V | g | v | G | V |
| 08 | h | x | H | X | h | x | H | X | h | x | H | X |
| 09 | j | y | J | Y | j | y | J | Y | j | y | J | Y |
| 10 | k | z | K | Z | k | z | K | Z | k | z | K | Z |
| 11 | l | 2 | L | 4 | l | 2 | L | 4 | l | 2 | L | 4 |
| 12 | n | 3 | N | 5 | n | 3 | N | 5 | n | 3 | N | 5 |

1) New Marking Layout for SC75, implemented at October 2005.

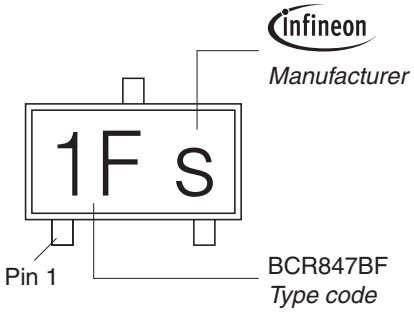
## Package Outline




## Foot Print

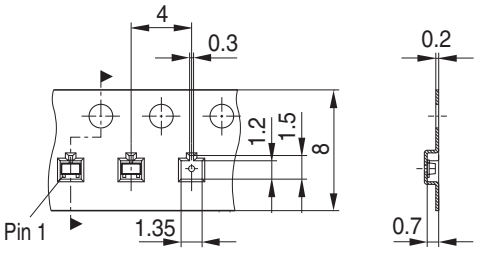



## Marking Layout (Example)

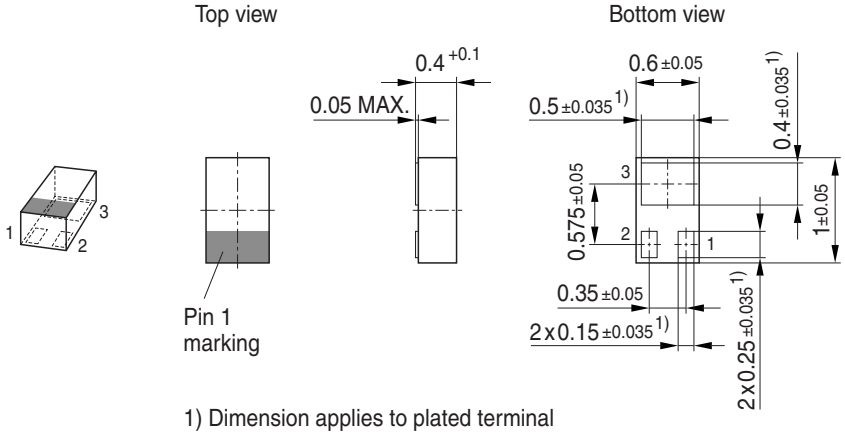



## Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel
Reel ø330 mm = 10.000 Pieces/Reel



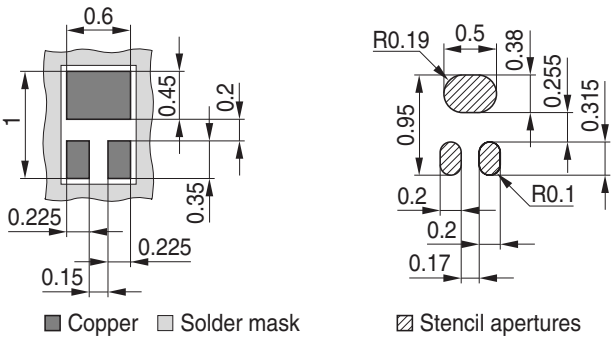
## Package Outline



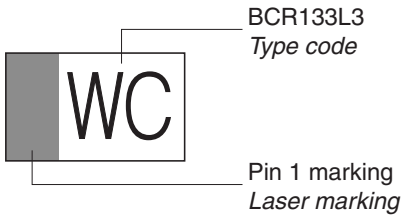

1) Dimension applies to plated terminal

## Foot Print

For board assembly information please refer to Infineon website "Packages"

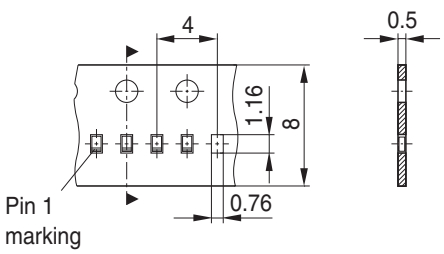



## Marking Layout




## Standard Packing

Reel ø180 mm = 15.000 Pieces/Reel



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