



# BGA7351

50 MHz to 500 MHz high linearity Si variable gain amplifier;  
28 dB gain range

Rev. 3 — 11 June 2014

Product data sheet

## 1. Product profile

### 1.1 General description

The BGA7351 MMIC is a dual independently digitally controlled IF Variable Gain Amplifier (VGA) operating from 50 MHz to 500 MHz. Each IF VGA amplifies with a gain range of 28 dB and at its maximum gain setting delivers 16.5 dBm output power at 1 dB gain compression and a superior linear performance.

The BGA7351 Dual IF VGA is optimized for a differential gain error of less than  $\pm 0.1$  dB for accurate gain control and has a total integrated gain error of less than  $\pm 0.3$  dB. Moreover it meets the demanding phase error requirements for GSM. BGA7351 has less than  $3.0^\circ$  phase error over the full gain range of 28 dB.

The gain controls of each amplifier are separate digital gain-control word, which is provided externally through two sets of 5 bits.

The BGA7351 is housed in a 32 pins 5 mm  $\times$  5 mm leadless HVQFN32 package.

### 1.2 Features and benefits

- Dual independent digitally controlled 28 dB gain range VGAs, with 5-bit control interface
- 50 MHz to 500 MHz frequency operating range
- Gain step size: 1 dB  $\pm$  0.1 dB
- 22 dB power gain
- Fast gain stage switching capability
- 16.5 dBm output power at 1 dB gain compression
- 46 dBm third order intercept point
- Constant third order intercept point over output power
- $-85$  dBc second harmonic level
- Excellent noise figure of 6 dB
- 5 V single supply operation with power-down control
- Logic-level shutdown control pin reduces supply current
- Excellent ESD protection at all pins
- Moisture sensitivity level 1
- Unconditionally stable
- Excellent differential integrated gain and phase error
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)



### 1.3 Applications

- Compatible with GSM / W-CDMA / WiMAX / LTE base-station infrastructure / multi carrier systems
- Multi channel receivers
- General use for ADC driver applications

### 1.4 Quick reference data

**Table 1. Quick reference data**

$A\_EN = "1"$ ;  $B\_EN = "1"$  (VGA enabled). Typical values at  $V_{CC} = 5\text{ V}$ ;  $I_{CC} = 280\text{ mA}$ ; Tuned for  $f_{IF} = 172\text{ MHz}$ ;  $B = 60\text{ MHz}$ ;  $T_{case} = 25\text{ }^{\circ}\text{C}$ ; Differential input resistance matched to  $150\text{ }\Omega$ ; Differential output resistance matched to  $200\text{ }\Omega$ ; unless otherwise specified; see [Section 11](#) "Application information".

| Symbol          | Parameter                             | Conditions                                     | Min  | Typ       | Max  | Unit     |
|-----------------|---------------------------------------|------------------------------------------------|------|-----------|------|----------|
| $V_{CC}$        | supply voltage                        | $V_{CC(A)} + V_{CC(B)}$                        | 4.75 | 5         | 5.25 | V        |
| $I_{CC}$        | supply current                        | $I_{CC(A)} + I_{CC(B)}$                        |      |           |      |          |
|                 |                                       | $A\_EN = "0"$ ; $B\_EN = "0"$                  | -    | 3         | 5    | mA       |
|                 |                                       | $A\_EN = "1"$ ; $B\_EN = "1"$                  | -    | 280       | 300  | mA       |
| $G_p$           | power gain                            | maximum gain <a href="#">[1]</a>               | 21   | 22        | 23   | dB       |
|                 |                                       | minimum gain <a href="#">[2]</a>               | -7   | -6        | -5   | dB       |
| $R_{i(dif)}$    | differential input resistance         |                                                | 120  | 150       | 180  | $\Omega$ |
| $R_{o(dif)}$    | differential output resistance        |                                                | 140  | 180       | 220  | $\Omega$ |
| NF              | noise figure                          | maximum gain <a href="#">[1]</a>               | -    | 6         | 7    | dB       |
|                 |                                       | increased rate per gain step                   | -    | 0.8       | 1    | dB       |
| $IP3_O$         | output third-order intercept point    | gain step 14 <a href="#">[3][4]</a>            | -    | 46        | -    | dBm      |
| $P_{L(1dB)}$    | output power at 1 dB gain compression | upper 5 gain steps <a href="#">[1][5]</a>      | -    | 16.5      | -    | dBm      |
| $\alpha_{2H}$   | second harmonic level                 | gain step 14 <a href="#">[4][6]</a>            | -    | -85       | -    | dBc      |
| $E_{G(dif)}$    | differential gain error               |                                                | -    | $\pm 0.1$ | -    | dB       |
| $E_{\phi(dif)}$ | differential phase error              | upper 12 dB gain range                         | -    | 1.0       | -    | deg      |
|                 |                                       | per gain step (for all consecutive gain steps) | -    | 0.5       | -    | deg      |

[1] Maximum gain; gain code = 00000.

[2] Minimum gain; gain code = 11100.

[3]  $P_L = 2\text{ dBm}$  per tone; spacing = 2 MHz ( $f_1 = 171\text{ MHz}$ ;  $f_2 = 173\text{ MHz}$ )

[4] Gain code = 01110.

[5] Gain code = 00000, 00001, 00010, 00011, 00100.

[6]  $P_L = 2\text{ dBm}$  one tone ( $f = 86\text{ MHz}$ ;  $f_{meas} = 172\text{ MHz}$ )

## 2. Pinning information

### 2.1 Pinning

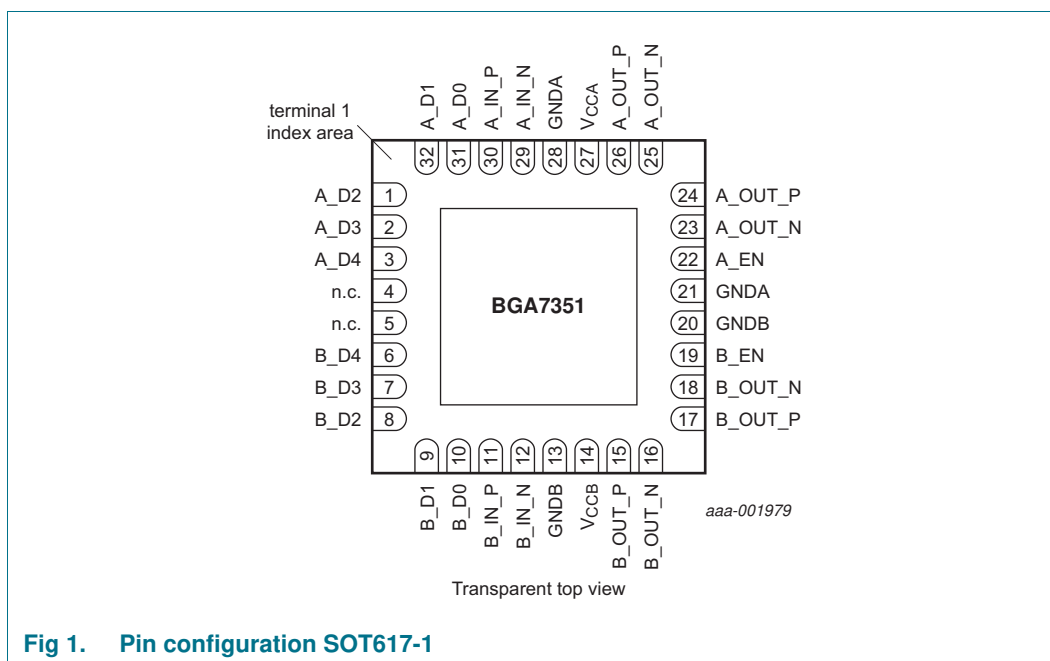


Fig 1. Pin configuration SOT617-1

### 2.2 Pin description

Table 2. Pin description

| Symbol           | Pin    | Description                                     |
|------------------|--------|-------------------------------------------------|
| A_D2             | 1      | MSB – 2 for gain control interface of channel A |
| A_D3             | 2      | MSB – 1 for gain control interface of channel A |
| A_D4             | 3      | MSB for gain control interface of channel A     |
| n.c.             | 4      | not connected <a href="#">[1]</a>               |
| n.c.             | 5      | not connected <a href="#">[1]</a>               |
| B_D4             | 6      | MSB for gain control interface of channel B     |
| B_D3             | 7      | MSB – 1 for gain control interface of channel B |
| B_D2             | 8      | MSB – 2 for gain control interface of channel B |
| B_D1             | 9      | LSB + 1 for gain control interface of channel B |
| B_D0             | 10     | LSB for gain control interface of channel B     |
| B_IN_P           | 11     | channel B positive input <a href="#">[2]</a>    |
| B_IN_N           | 12     | channel B negative input <a href="#">[2]</a>    |
| GNDB             | 13, 20 | ground for channel B                            |
| V <sub>CCB</sub> | 14     | supply voltage for channel B                    |
| B_OUT_P          | 15, 17 | channel B positive output <a href="#">[2]</a>   |
| B_OUT_N          | 16, 18 | channel B negative output <a href="#">[2]</a>   |
| B_EN             | 19     | power enable pin for channel B                  |
| GNDA             | 21, 28 | ground for channel A                            |

Table 2. Pin description ...continued

| Symbol           | Pin        | Description                                     |
|------------------|------------|-------------------------------------------------|
| A_EN             | 22         | power enable pin for channel A                  |
| A_OUT_N          | 23, 25     | channel A negative output [2]                   |
| A_OUT_P          | 24, 26     | channel A positive output [2]                   |
| V <sub>CCA</sub> | 27         | supply voltage for channel A                    |
| A_IN_N           | 29         | channel A negative input [2]                    |
| A_IN_P           | 30         | channel A positive input [2]                    |
| A_D0             | 31         | LSB for gain control interface of channel A     |
| A_D1             | 32         | LSB + 1 for gain control interface of channel A |
| GND              | GND paddle | RF ground and DC ground [3]                     |

[1] Pin to be left open.

[2] Each channel should be independently enabled with logic HIGH and disabled with logic LOW.

[3] The center metal base of the SOT617-1 also functions as heatsink for the VGA.

### 3. Ordering information

Table 3. Ordering information

| Type number | Package |                                                                                                    |          |
|-------------|---------|----------------------------------------------------------------------------------------------------|----------|
|             | Name    | Description                                                                                        | Version  |
| BGA7351     | HVQFN32 | plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm | SOT617-1 |

4. Functional diagram

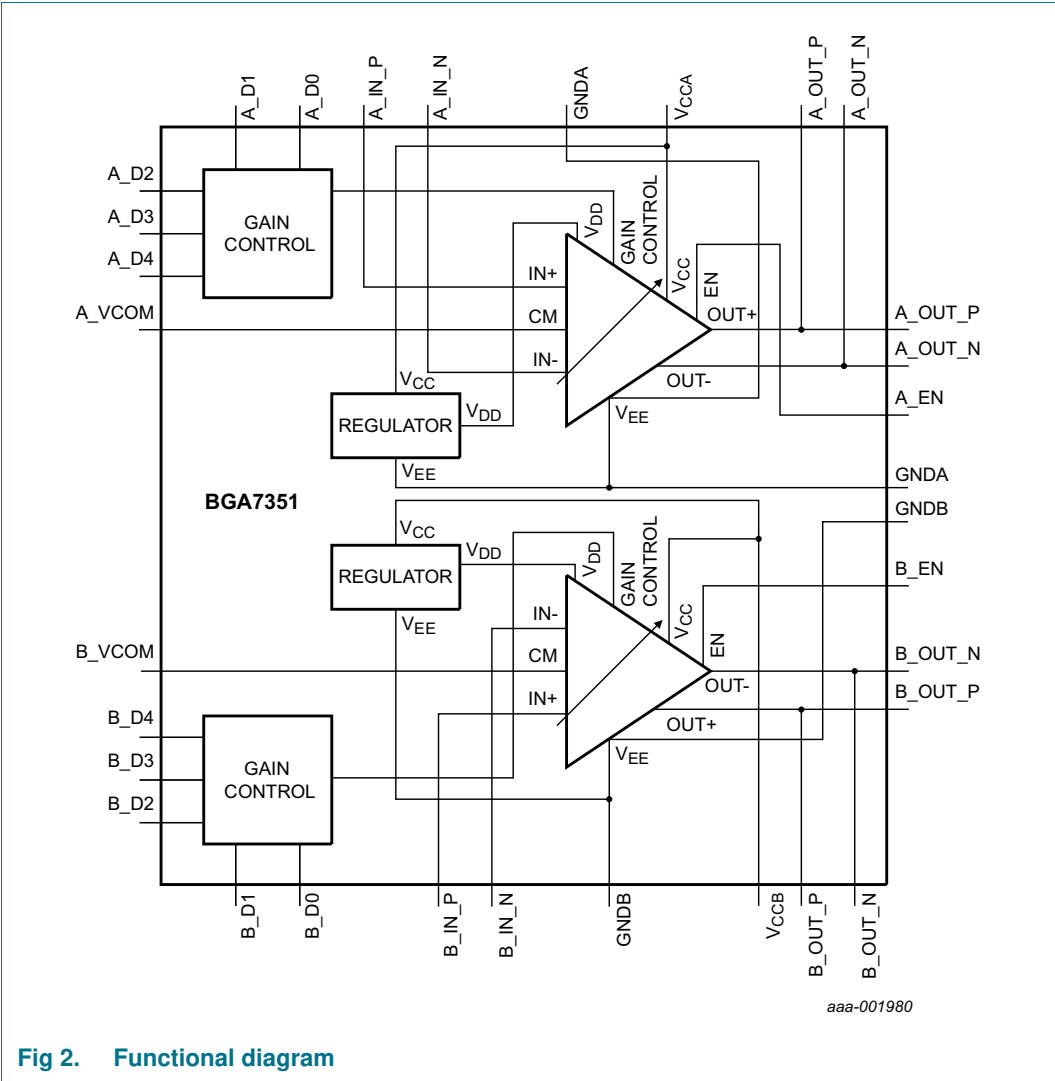


Fig 2. Functional diagram

5. Enable control

Table 4. Enable / disable control settings

| Mode       | Function description  | Mode description | Enable |      | V <sub>EN</sub> (V) |      | I <sub>EN</sub> (μA) |     |
|------------|-----------------------|------------------|--------|------|---------------------|------|----------------------|-----|
|            |                       |                  | A_EN   | B_EN | Min                 | Max  | Min                  | Max |
| A_EN, B_EN | VGA function off      | disable          | "0"    | "0"  | 0                   | 0.8  | -                    | 1   |
| A_EN, B_EN | VGA in operating mode | enable           | "1"    | "1"  | 1.6                 | 5.25 | -                    | 1   |

## 6. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol      | Parameter                       | Conditions                                                       | Min  | Max  | Unit |
|-------------|---------------------------------|------------------------------------------------------------------|------|------|------|
| $V_{CC(A)}$ | supply voltage (A)              | [1]                                                              | -    | 6    | V    |
| $V_{CC(B)}$ | supply voltage (B)              | [1]                                                              | -    | 6    | V    |
| $V_{AEN}$   | voltage on pin A_EN             |                                                                  | -0.6 | +6   | V    |
| $V_{BEN}$   | voltage on pin B_EN             |                                                                  | -0.6 | +6   | V    |
| $V_{AD0}$   | voltage on pin A_D0             |                                                                  | -0.6 | +6   | V    |
| $V_{AD1}$   | voltage on pin A_D1             |                                                                  | -0.6 | +6   | V    |
| $V_{AD2}$   | voltage on pin A_D2             |                                                                  | -0.6 | +6   | V    |
| $V_{AD3}$   | voltage on pin A_D3             |                                                                  | -0.6 | +6   | V    |
| $V_{AD4}$   | voltage on pin A_D4             |                                                                  | -0.6 | +6   | V    |
| $V_{BD0}$   | voltage on pin B_D0             |                                                                  | -0.6 | +6   | V    |
| $V_{BD1}$   | voltage on pin B_D1             |                                                                  | -0.6 | +6   | V    |
| $V_{BD2}$   | voltage on pin B_D2             |                                                                  | -0.6 | +6   | V    |
| $V_{BD3}$   | voltage on pin B_D3             |                                                                  | -0.6 | +6   | V    |
| $V_{BD4}$   | voltage on pin B_D4             |                                                                  | -0.6 | +6   | V    |
| $V_{AIN}$   | voltage on pin A_IN             |                                                                  | -0.6 | +6   | V    |
| $V_{BIN}$   | voltage on pin B_IN             |                                                                  | -0.6 | +6   | V    |
| $P_{i(RF)}$ | RF input power                  |                                                                  | -    | 20   | dBm  |
| $T_{case}$  | case temperature                |                                                                  | -40  | +85  | °C   |
| $T_j$       | junction temperature            |                                                                  | -    | 150  | °C   |
| $V_{ESD}$   | electrostatic discharge voltage | Human Body Model (HBM);<br>According JEDEC standard 22-A114E     | -    | 4000 | V    |
|             |                                 | Charged Device Model (CDM);<br>According JEDEC standard 22-C101B | -    | 2000 | V    |
|             |                                 | Machine Model (MM);<br>According JEDEC standard 22-A115          | -    | 400  | V    |

[1] Caution: All digital pins may not exceed  $V_{CC}$  as the internal ESD circuit can be damaged. To prevent this it is recommended that  $V_{AEN}$  and  $V_{BEN}$  are limited to a maximum of 5 mA.

## 7. Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol           | Parameter                                | Conditions                                                                      | Typ | Unit |
|------------------|------------------------------------------|---------------------------------------------------------------------------------|-----|------|
| $R_{th(j-case)}$ | thermal resistance from junction to case | $T_{case} = 85\text{ °C}$ ; $V_{CC} = 5\text{ V}$ ;<br>$I_{CC} = 280\text{ mA}$ | 7   | K/W  |

## 8. Static characteristics

**Table 7. Characteristics**

$A\_EN = "1"$ ;  $B\_EN = "1"$  (both channels enabled). Typical values at  $V_{CC} = 5\text{ V}$ ;  $T_{case} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

| Symbol   | Parameter                | Conditions                    | Min  | Typ | Max  | Unit |
|----------|--------------------------|-------------------------------|------|-----|------|------|
| $V_{CC}$ | supply voltage           | $V_{CC(A)} + V_{CC(B)}$       | 4.75 | 5   | 5.25 | V    |
| $I_{CC}$ | supply current           | $I_{CC(A)} + I_{CC(B)}$       |      |     |      |      |
|          |                          | $A\_EN = "0"$ ; $B\_EN = "0"$ | -    | 3   | 5    | mA   |
|          |                          | $A\_EN = "1"$ ; $B\_EN = "1"$ | -    | 280 | 300  | mA   |
| $V_{IH}$ | HIGH-level input voltage | [1]                           | 1.6  | -   | 5.25 | V    |
| $V_{IL}$ | LOW-level input voltage  | [1]                           | -    | -   | 0.8  | V    |
| P        | power dissipation        |                               | -    | 1.4 | 1.6  | W    |

[1] Voltage on the control pins.

## 9. Dynamic characteristics

**Table 8. Characteristics**

$A\_EN = "1"$ ;  $B\_EN = "1"$  (VGA enabled). Typical values at  $V_{CC} = 5\text{ V}$ ;  $I_{CC} = 280\text{ mA}$ ; Tuned for  $f_{IF} = 172\text{ MHz}$ ;  $B = 60\text{ MHz}$ ;  $T_{case} = 25\text{ }^{\circ}\text{C}$ ; Differential input resistance matched to  $150\text{ }\Omega$ ; Differential output resistance matched to  $200\text{ }\Omega$ ; unless otherwise specified; see [Section 11 "Application information"](#).

| Symbol           | Parameter                | Conditions                                     | Min | Typ       | Max | Unit |
|------------------|--------------------------|------------------------------------------------|-----|-----------|-----|------|
| $G_p$            | power gain               | maximum gain [1]                               |     |           |     |      |
|                  |                          | $f = 50\text{ MHz}$ ; $B = 30\text{ MHz}$      | -   | 22.5      | -   | dB   |
|                  |                          | $f = 172\text{ MHz}$ ; $B = 60\text{ MHz}$     | 21  | 22        | 23  | dB   |
|                  |                          | $f = 250\text{ MHz}$ ; $B = 60\text{ MHz}$     | -   | 21.5      | -   | dB   |
|                  |                          | $f = 450\text{ MHz}$ ; $B = 100\text{ MHz}$    | -   | 21.5      | -   | dB   |
|                  |                          | minimum gain [2]                               |     |           |     |      |
|                  |                          | $f = 50\text{ MHz}$ ; $B = 30\text{ MHz}$      | -   | -5.5      | -   | dB   |
|                  |                          | $f = 172\text{ MHz}$ ; $B = 60\text{ MHz}$     | -7  | -6        | -5  | dB   |
|                  |                          | $f = 250\text{ MHz}$ ; $B = 60\text{ MHz}$     | -   | -6.5      | -   | dB   |
|                  |                          | $f = 450\text{ MHz}$ ; $B = 100\text{ MHz}$    | -   | -8        | -   | dB   |
| $\Delta G_{adj}$ | gain adjustment range    | [1]                                            | -   | 28        | -   | dB   |
| $G_{step}$       | gain step                |                                                | -   | 1         | -   |      |
| $G_{flat}$       | gain flatness            | [1]                                            | -   | $\pm 0.5$ | -   | dB   |
| $E_{G(dif)}$     | differential gain error  |                                                | -   | $\pm 0.1$ | -   | dB   |
| $E_{G(itg)}$     | integrated gain error    | upper 12 dB gain range                         | -   | $\pm 0.2$ | -   | dB   |
|                  |                          | full gain range                                | -   | $\pm 0.3$ | -   | dB   |
| $E_{\phi(dif)}$  | differential phase error | upper 12 dB gain range                         | -   | 1.0       | -   | deg  |
|                  |                          | per gain step (for all consecutive gain steps) | -   | 0.5       | -   | deg  |
|                  |                          | full gain range                                | -   | 3.0       | -   | deg  |
| $t_{s(step)G}$   | gain step settling time  | per 1.5 dB of steady state                     | -   | 5         | 15  | ns   |
|                  |                          | per 0.1 dB of steady state                     | -   | 20        | 40  | ns   |

**Table 8. Characteristics ...continued**

$A\_EN = "1"$ ;  $B\_EN = "1"$  (VGA enabled). Typical values at  $V_{CC} = 5\text{ V}$ ;  $I_{CC} = 280\text{ mA}$ ; Tuned for  $f_{IF} = 172\text{ MHz}$ ;  $B = 60\text{ MHz}$ ;  $T_{case} = 25\text{ }^{\circ}\text{C}$ ; Differential input resistance matched to  $150\text{ }\Omega$ ; Differential output resistance matched to  $200\text{ }\Omega$ ; unless otherwise specified; see [Section 11](#) "Application information".

| Symbol                 | Parameter                             | Conditions                                  | Min | Typ  | Max | Unit          |
|------------------------|---------------------------------------|---------------------------------------------|-----|------|-----|---------------|
| $\Delta t_{d(grp)}$    | group delay time variation            | $B = 30\text{ MHz}$                         | -   | 86   | -   | ps            |
| $t_{pu}$               | power-up time                         |                                             | -   | -    | 1   | $\mu\text{s}$ |
| $R_{i(dif)}$           | differential input resistance         |                                             | 120 | 150  | 180 | $\Omega$      |
| $R_{o(dif)}$           | differential output resistance        |                                             | 140 | 180  | 220 | $\Omega$      |
| $\alpha_{isol(ch-ch)}$ | isolation between channels            | $f \leq 250\text{ MHz}$                     | 50  | -    | -   | dB            |
|                        |                                       | $250\text{ MHz} < f < 400\text{ MHz}$       | 47  | -    | -   | dB            |
|                        |                                       | $400\text{ MHz} \leq f \leq 500\text{ MHz}$ | 45  | -    | -   | dB            |
| CMRR                   | common-mode rejection ratio           |                                             | 40  | -    | -   | dB            |
| IP3 <sub>O</sub>       | output third-order intercept point    | gain step 14 <a href="#">[3]</a>            |     |      |     |               |
|                        |                                       | $f = 50\text{ MHz}$ <a href="#">[4]</a>     | -   | 47   | -   | dBm           |
|                        |                                       | $f = 172\text{ MHz}$ <a href="#">[5]</a>    | -   | 46   | -   | dBm           |
|                        |                                       | $f = 250\text{ MHz}$ <a href="#">[6]</a>    | -   | 41   | -   | dBm           |
|                        |                                       | $f = 450\text{ MHz}$ <a href="#">[7]</a>    | -   | 34   | -   | dBm           |
|                        |                                       | upper 5 gain steps <a href="#">[8]</a>      |     |      |     |               |
|                        |                                       | $f = 50\text{ MHz}$ <a href="#">[4]</a>     | -   | 48   | -   | dBm           |
|                        |                                       | $f = 172\text{ MHz}$ <a href="#">[5]</a>    | -   | 44   | -   | dBm           |
|                        |                                       | $f = 250\text{ MHz}$ <a href="#">[6]</a>    | -   | 41   | -   | dBm           |
|                        |                                       | $f = 450\text{ MHz}$ <a href="#">[7]</a>    | -   | 33   | -   | dBm           |
| IP2 <sub>O</sub>       | output second-order intercept point   | upper 5 gain steps <a href="#">[8]</a>      |     |      |     |               |
|                        |                                       | $f = 50\text{ MHz}$ <a href="#">[9]</a>     | -   | 78   | -   | dBm           |
|                        |                                       | $f = 172\text{ MHz}$ <a href="#">[10]</a>   | -   | 73   | -   | dBm           |
|                        |                                       | $f = 250\text{ MHz}$ <a href="#">[11]</a>   | -   | 65   | -   | dBm           |
| P <sub>L(1dB)</sub>    | output power at 1 dB gain compression | upper 5 gain steps <a href="#">[8]</a>      |     |      |     |               |
|                        |                                       | $f = 50\text{ MHz}$                         | -   | 16.8 | -   | dBm           |
|                        |                                       | $f = 172\text{ MHz}$                        | -   | 16.5 | -   | dBm           |
|                        |                                       | $f = 250\text{ MHz}$                        | -   | 15.8 | -   | dBm           |
|                        |                                       | $f = 450\text{ MHz}$                        | -   | 15.1 | -   | dBm           |

**Table 8. Characteristics ...continued**

$A\_EN = "1"$ ;  $B\_EN = "1"$  (VGA enabled). Typical values at  $V_{CC} = 5\text{ V}$ ;  $I_{CC} = 280\text{ mA}$ ; Tuned for  $f_{IF} = 172\text{ MHz}$ ;  $B = 60\text{ MHz}$ ;  $T_{case} = 25\text{ }^{\circ}\text{C}$ ; Differential input resistance matched to  $150\text{ }\Omega$ ; Differential output resistance matched to  $200\text{ }\Omega$ ; unless otherwise specified; see [Section 11](#) "Application information".

| Symbol        | Parameter             | Conditions                                                       | Min | Typ | Max | Unit |
|---------------|-----------------------|------------------------------------------------------------------|-----|-----|-----|------|
| $\alpha_{2H}$ | second harmonic level | gain step 14 <a href="#">[3]</a>                                 |     |     |     |      |
|               |                       | $P_L = 2\text{ dBm}$ , $f = 172\text{ MHz}$ <a href="#">[12]</a> | -   | -85 | -   | dBc  |
|               |                       | $P_L = 5\text{ dBm}$ , $f = 172\text{ MHz}$ <a href="#">[13]</a> | -   | -82 | -   | dBc  |
|               |                       | $P_L = 2\text{ dBm}$ , $f = 450\text{ MHz}$ <a href="#">[14]</a> | -   | -67 | -   | dBc  |
|               |                       | $P_L = 5\text{ dBm}$ , $f = 450\text{ MHz}$ <a href="#">[15]</a> | -   | -64 | -   | dBc  |
|               |                       | upper 5 gain steps <a href="#">[8]</a>                           |     |     |     |      |
|               |                       | $P_L = 2\text{ dBm}$ , $f = 172\text{ MHz}$ <a href="#">[12]</a> | -   | -83 | -   | dBc  |
|               |                       | $P_L = 5\text{ dBm}$ , $f = 172\text{ MHz}$ <a href="#">[13]</a> | -   | -80 | -   | dBc  |
|               |                       | $P_L = 2\text{ dBm}$ , $f = 450\text{ MHz}$ <a href="#">[14]</a> | -   | -59 | -   | dBc  |
|               |                       | $P_L = 5\text{ dBm}$ , $f = 450\text{ MHz}$ <a href="#">[15]</a> | -   | -54 | -   | dBc  |
| NF            | noise figure          | maximum gain <a href="#">[1]</a>                                 | -   | 6   | 7   | dB   |
|               |                       | increase rate per gain step                                      | -   | 0.8 | 1   | dB   |

[1] Maximum gain; gain code = 00000.

[2] Minimum gain; gain code = 11100.

[3] Gain code = 01110.

[4]  $P_L = 2\text{ dBm}$  per tone; spacing =  $2\text{ MHz}$  ( $f_1 = 49\text{ MHz}$ ;  $f_2 = 51\text{ MHz}$ )

[5]  $P_L = 2\text{ dBm}$  per tone; spacing =  $2\text{ MHz}$  ( $f_1 = 171\text{ MHz}$ ;  $f_2 = 173\text{ MHz}$ )

[6]  $P_L = 2\text{ dBm}$  per tone; spacing =  $2\text{ MHz}$  ( $f_1 = 249\text{ MHz}$ ;  $f_2 = 251\text{ MHz}$ )

[7]  $P_L = 2\text{ dBm}$  per tone; spacing =  $2\text{ MHz}$  ( $f_1 = 449\text{ MHz}$ ;  $f_2 = 451\text{ MHz}$ )

[8] Gain code = 00000, 00001, 00010, 00011, 00100.

[9]  $P_L = 2\text{ dBm}$  per tone ( $f_1 = 24\text{ MHz}$ ;  $f_2 = 74\text{ MHz}$ ;  $f_{meas} = 50\text{ MHz}$ )

[10]  $P_L = 2\text{ dBm}$  per tone ( $f_1 = 82\text{ MHz}$ ;  $f_2 = 90\text{ MHz}$ ;  $f_{meas} = 172\text{ MHz}$ )

[11]  $P_L = 2\text{ dBm}$  per tone ( $f_1 = 120\text{ MHz}$ ;  $f_2 = 130\text{ MHz}$ ;  $f_{meas} = 250\text{ MHz}$ )

[12]  $P_L = 2\text{ dBm}$  one tone ( $f = 86\text{ MHz}$ ;  $f_{meas} = 172\text{ MHz}$ )

[13]  $P_L = 5\text{ dBm}$  one tone ( $f = 86\text{ MHz}$ ;  $f_{meas} = 172\text{ MHz}$ )

[14]  $P_L = 2\text{ dBm}$  one tone ( $f = 225\text{ MHz}$ ;  $f_{meas} = 450\text{ MHz}$ )

[15]  $P_L = 5\text{ dBm}$  one tone ( $f = 225\text{ MHz}$ ;  $f_{meas} = 450\text{ MHz}$ )

Table 9. Gain control

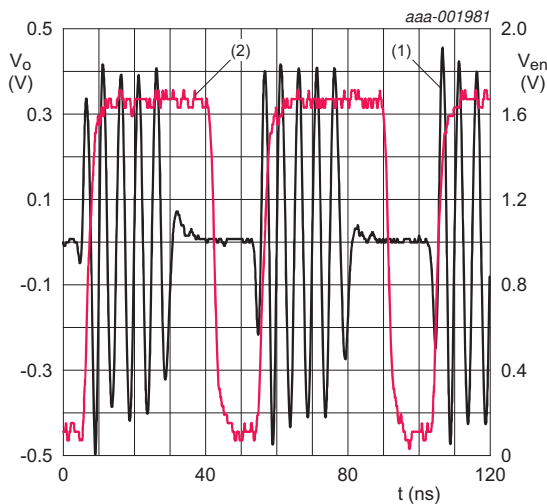
| gain step | input to either A_D0 to A_D4 pins<br>or B_D0 to B_D4 pins | nominal power gain (dB) |
|-----------|-----------------------------------------------------------|-------------------------|
| 0         | 00000                                                     | 22                      |
| 1         | 00001                                                     | 21                      |
| 2         | 00010                                                     | 20                      |
| 3         | 00011                                                     | 19                      |
| 4         | 00100                                                     | 18                      |
| 5         | 00101                                                     | 17                      |
| 6         | 00110                                                     | 16                      |
| 7         | 00111                                                     | 15                      |
| 8         | 01000                                                     | 14                      |
| 9         | 01001                                                     | 13                      |
| 10        | 01010                                                     | 12                      |
| 11        | 01011                                                     | 11                      |
| 12        | 01100                                                     | 10                      |
| 13        | 01101                                                     | 9                       |
| 14        | 01110                                                     | 8                       |
| 15        | 01111                                                     | 7                       |
| 16        | 10000                                                     | 6                       |
| 17        | 10001                                                     | 5                       |
| 18        | 10010                                                     | 4                       |
| 19        | 10011                                                     | 3                       |
| 20        | 10100                                                     | 2                       |
| 21        | 10101                                                     | 1                       |
| 22        | 10110                                                     | 0                       |
| 23        | 10111                                                     | -1                      |
| 24        | 11000                                                     | -2                      |
| 25        | 11001                                                     | -3                      |
| 26        | 11010                                                     | -4                      |
| 27        | 11011                                                     | -5                      |
| 28        | 11100                                                     | -6                      |
| -         | > 11100                                                   | -6                      |

## 10. Moisture sensitivity

Table 10. Moisture sensitivity level

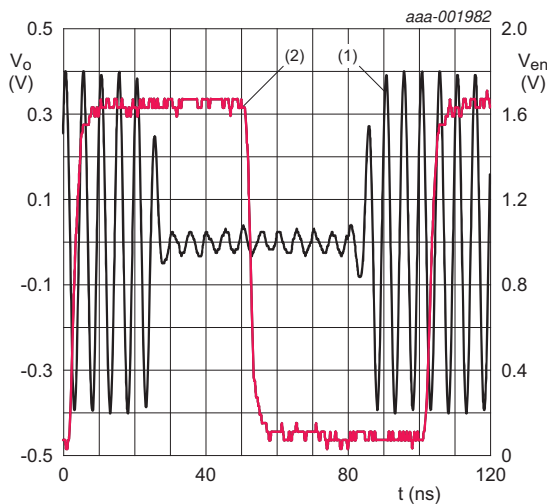
| Test methodology | Class |
|------------------|-------|
| JESD-22-A113     | 1     |

11. Application information



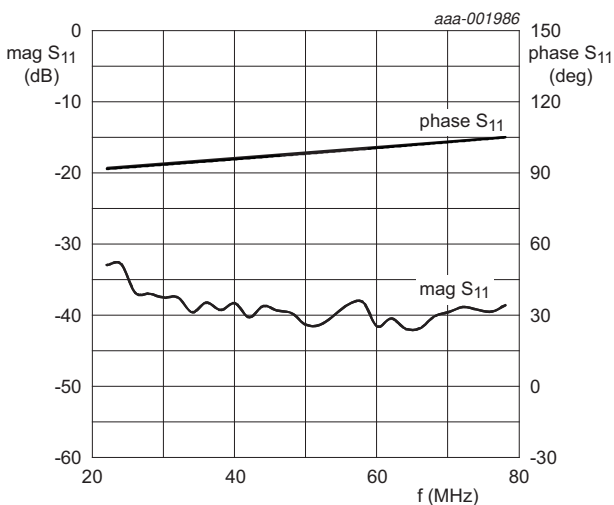
- (1)  $V_O$
- (2)  $V_{en}$

Fig 3. Enable time response



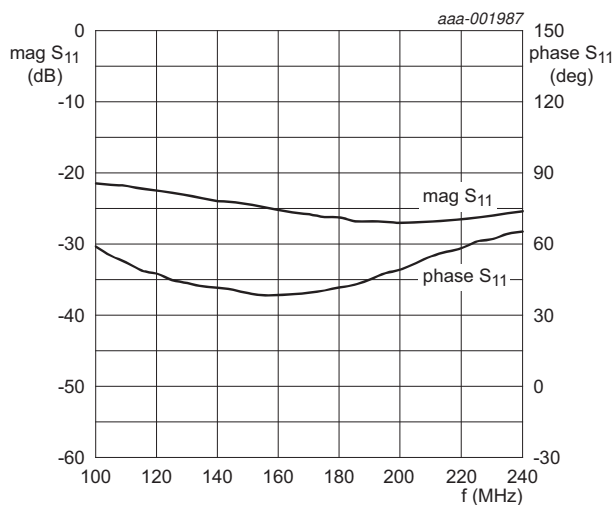
- (1)  $V_O$
- (2)  $V_{en}$

Fig 4. Gain step response from min. to max. gain



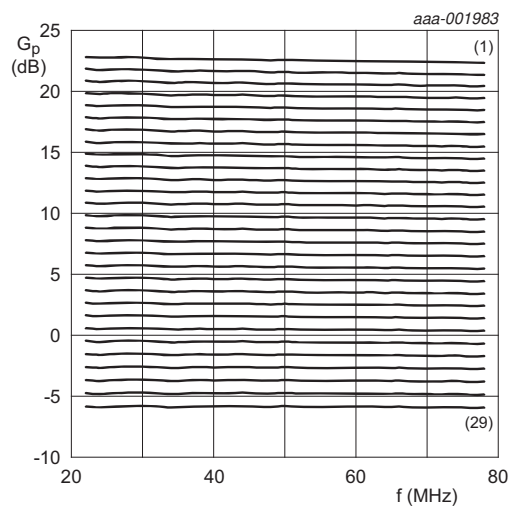
Tuned for  $f_{IF} = 50$  MHz; measured at gain step 0 (maximum gain).

Fig 5.  $S_{11}$  as a function of frequency



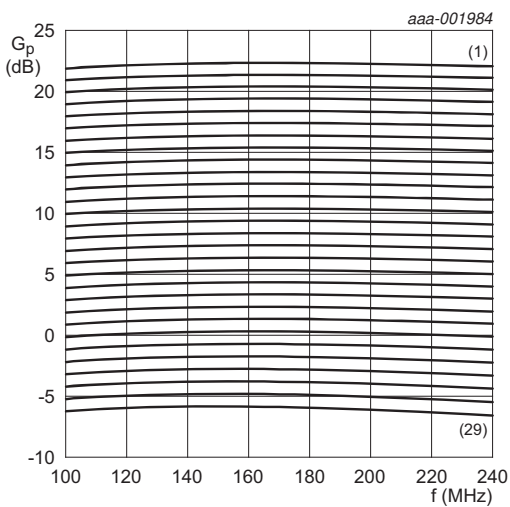
Tuned for  $f_{IF} = 172$  MHz; measured at gain step 0 (maximum gain).

Fig 6.  $S_{11}$  as a function of frequency



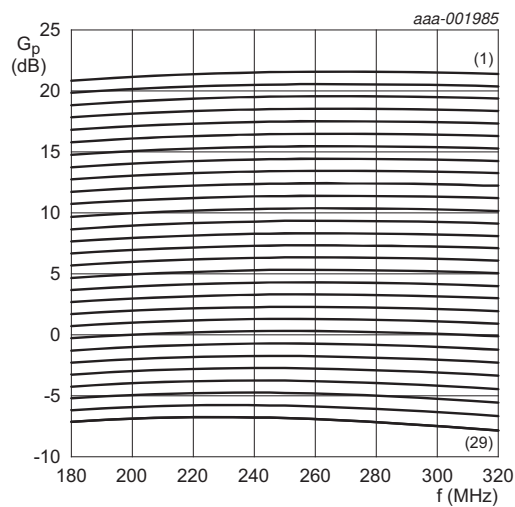
Tuned for  $f_{IF} = 50$  MHz;  $P_L = 5$  dBm; step size 1 dB.  
(1) gain step 0 (maximum gain)  
(29) gain step 28 (minimum gain)

Fig 7. Power gain as a function of frequency



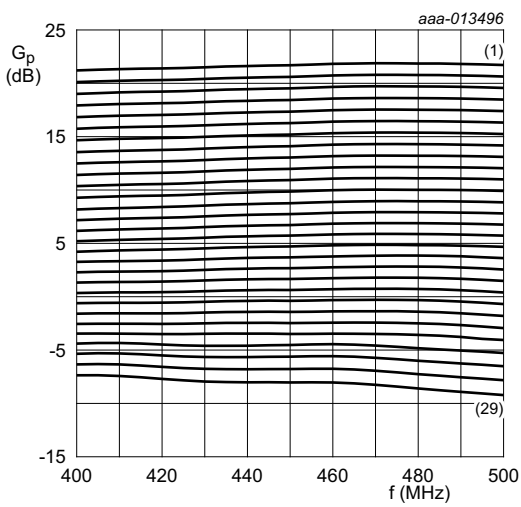
Tuned for  $f_{IF} = 172$  MHz;  $P_L = 5$  dBm; step size 1 dB.  
(1) gain step 0 (maximum gain)  
(29) gain step 28 (minimum gain)

Fig 8. Power gain as a function of frequency



Tuned for  $f_{IF} = 250$  MHz;  $P_L = 5$  dBm; step size 1 dB.  
(1) gain step 0 (maximum gain)  
(29) gain step 28 (minimum gain)

Fig 9. Power gain as a function of frequency



Tuned for  $f_{IF} = 450$  MHz;  $P_L = 5$  dBm; step size 1 dB.  
(1) gain step 0 (maximum gain)  
(29) gain step 28 (minimum gain)

Fig 10. Power gain as a function of frequency

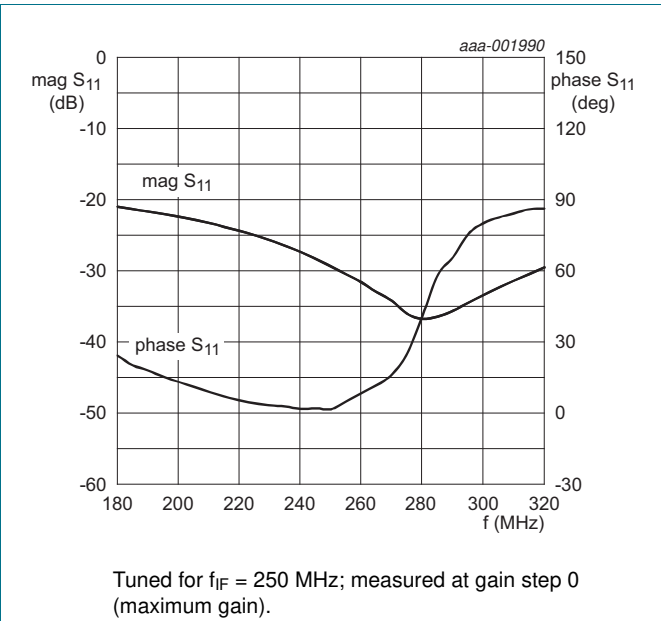


Fig 11.  $S_{11}$  as a function of frequency

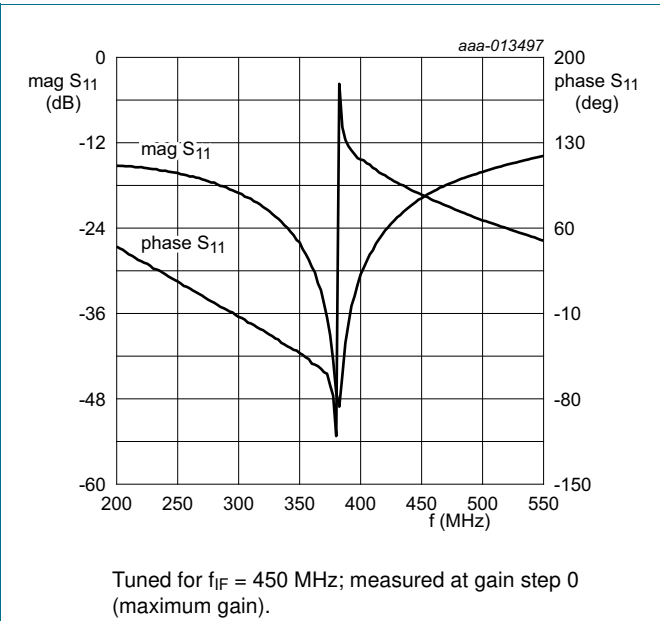


Fig 12.  $S_{11}$  as a function of frequency

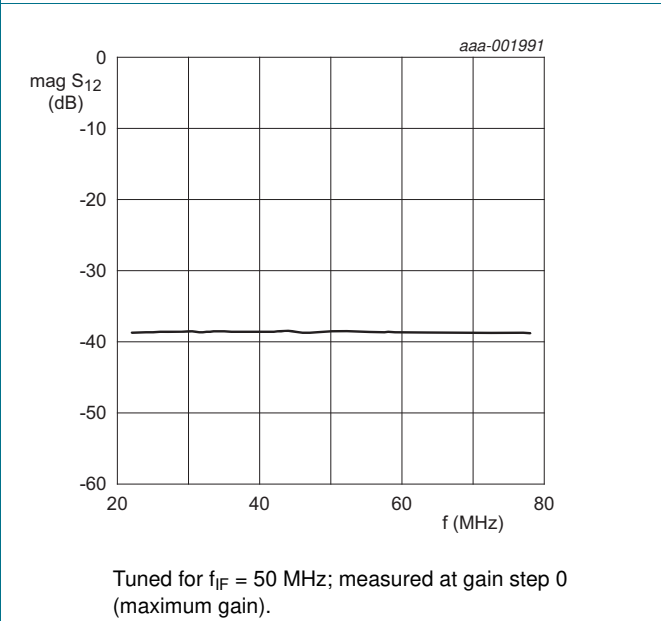


Fig 13.  $S_{12}$  as a function of frequency

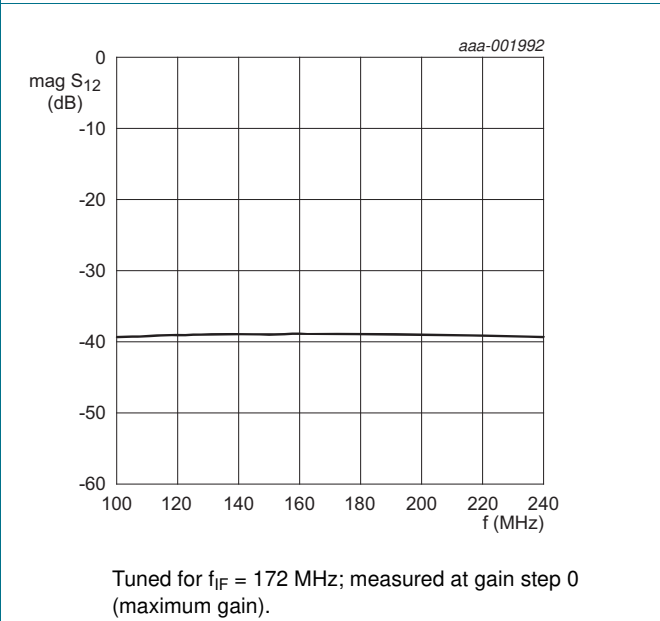
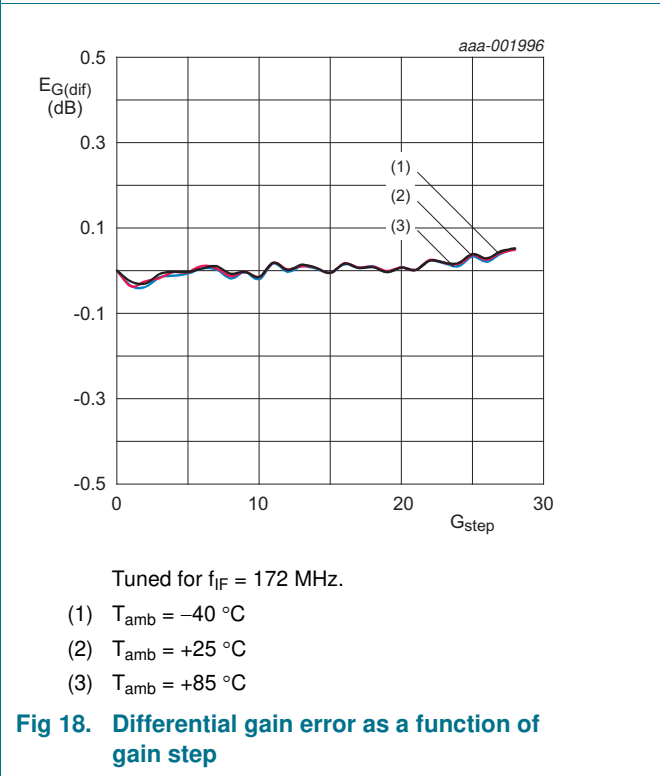
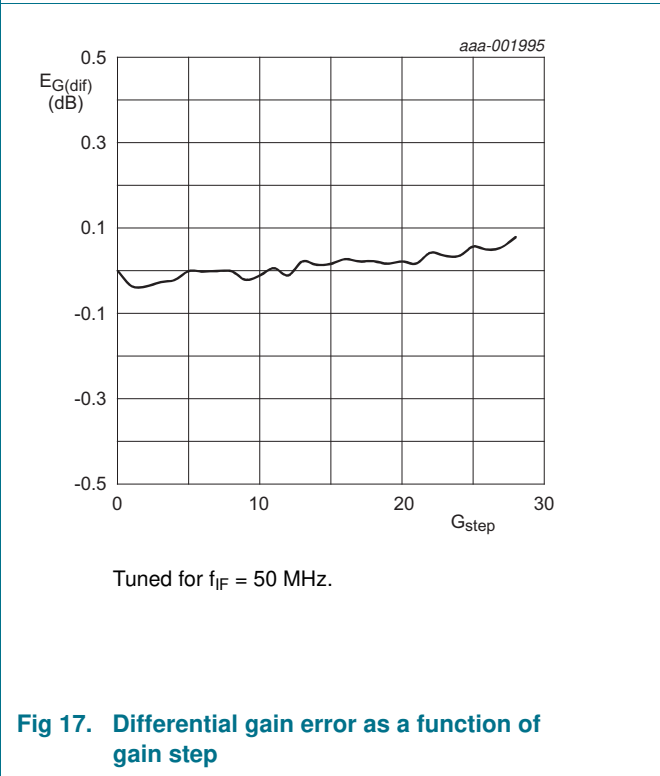
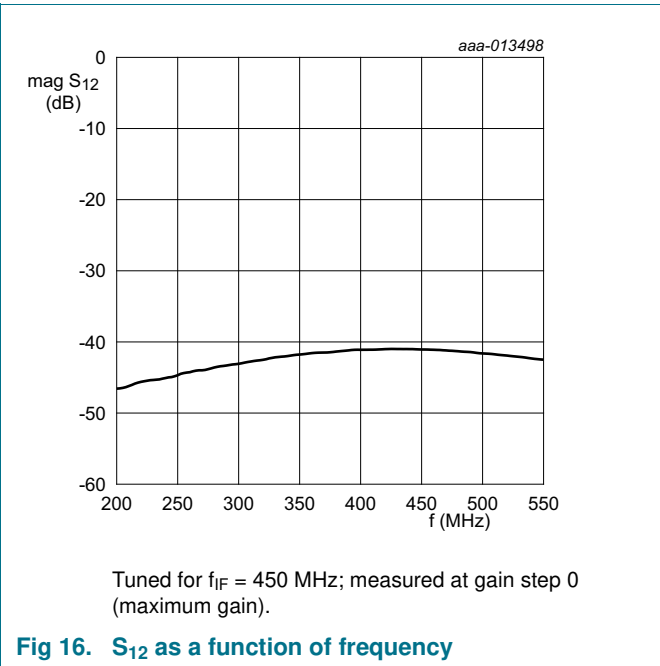
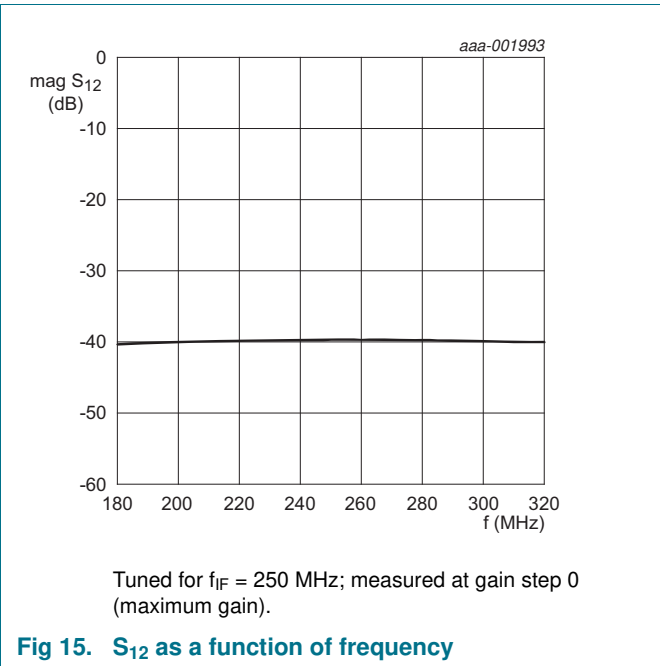
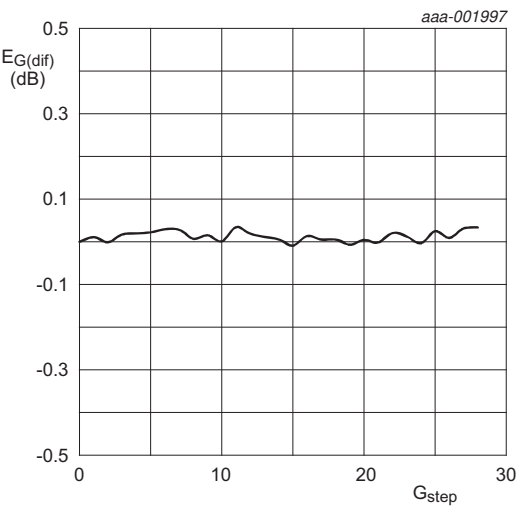


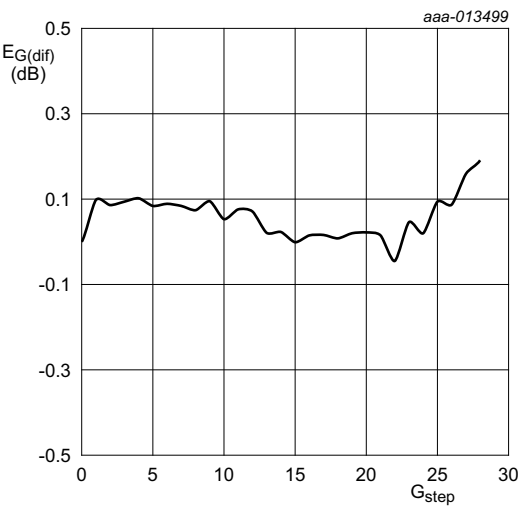
Fig 14.  $S_{12}$  as a function of frequency





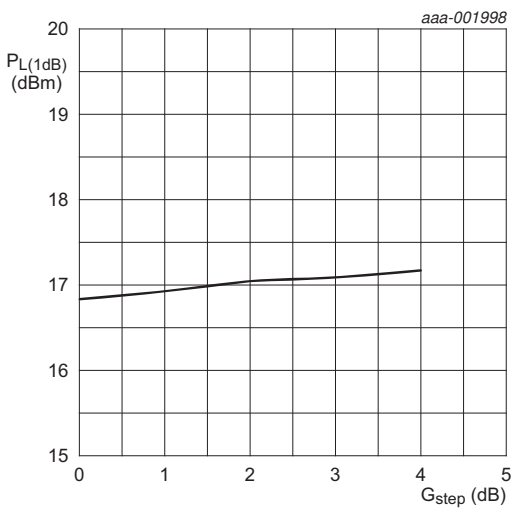
Tuned for  $f_{IF} = 250$  MHz.

Fig 19. Differential gain error as a function of gain step



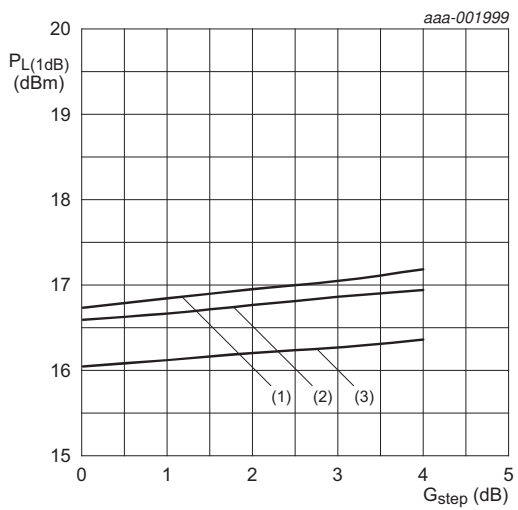
Tuned for  $f_{IF} = 450$  MHz.

Fig 20. Differential gain error as a function of gain step



Tuned for  $f_{IF} = 50$  MHz.

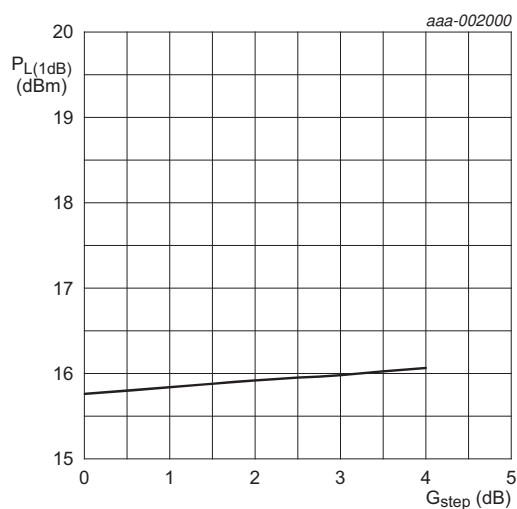
Fig 21. output power at 1 dB gain compression as a function of gain step



Tuned for  $f_{IF} = 172$  MHz.

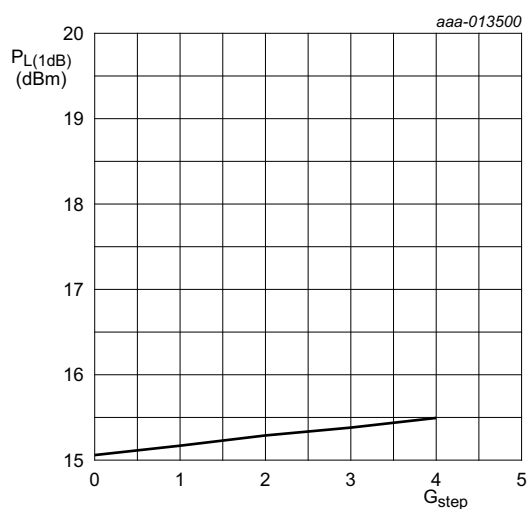
- (1)  $T_{\text{amb}} = -40$  °C
- (2)  $T_{\text{amb}} = +25$  °C
- (3)  $T_{\text{amb}} = +85$  °C

Fig 22. output power at 1 dB gain compression as a function of gain step



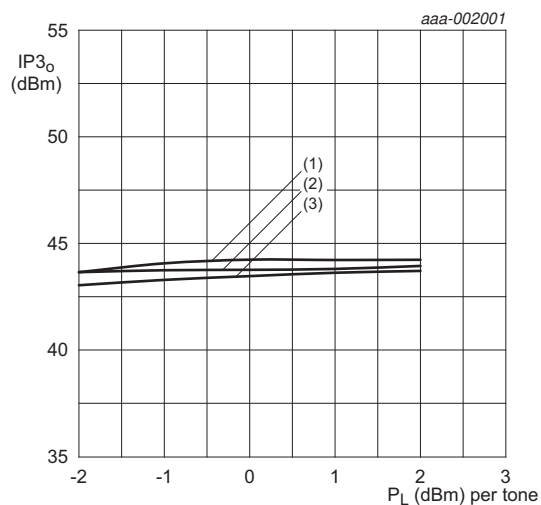
Tuned for  $f_{IF} = 250$  MHz.

**Fig 23.** output power at 1 dB gain compression as a function of gain step



Tuned for  $f_{IF} = 450$  MHz.

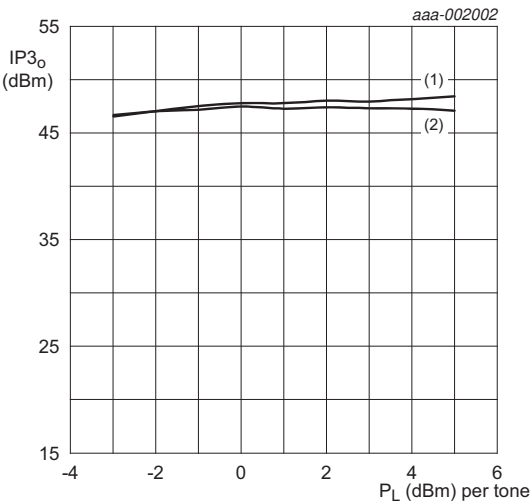
**Fig 24.** output power at 1 dB gain compression as a function of gain step



Tuned for  $f_{IF} = 172$  MHz; measured at gain step 0 (maximum gain).

- (1)  $T_{amb} = -40$  °C
- (2)  $T_{amb} = +25$  °C
- (3)  $T_{amb} = +85$  °C

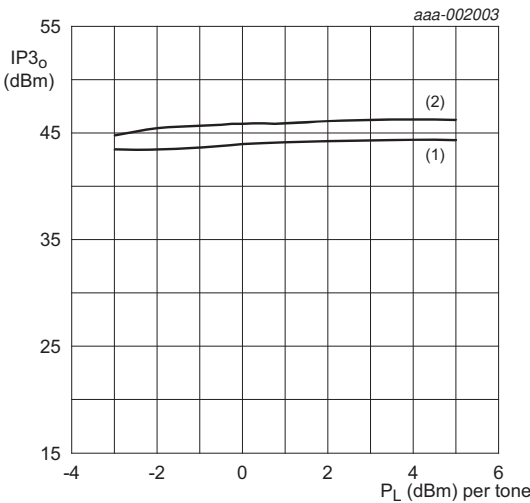
**Fig 25.** Output third order intercept point as a function of output power per tone



Tuned for  $f_{IF} = 50$  MHz.

(1) gain step 0  
(2) gain step 14

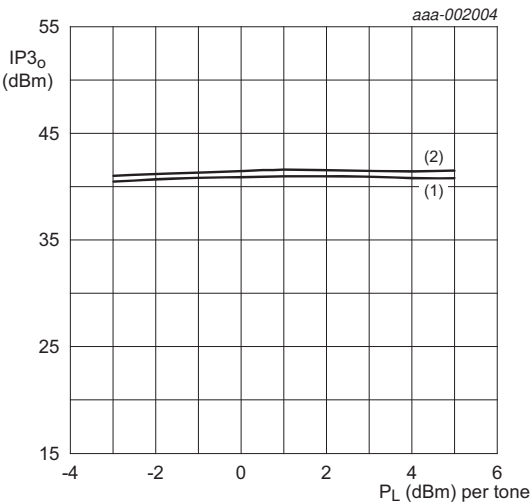
Fig 26. Output third order intercept point as a function of output power per tone



Tuned for  $f_{IF} = 172$  MHz.

(1) gain step 0  
(2) gain step 14

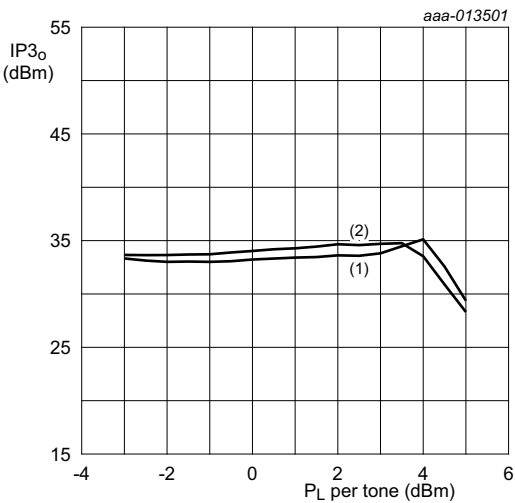
Fig 27. Output third order intercept point as a function of output power per tone



Tuned for  $f_{IF} = 250$  MHz.

(1) gain step 0  
(2) gain step 14

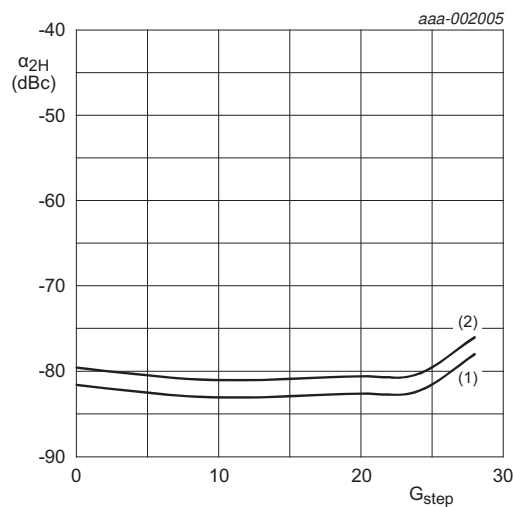
Fig 28. Output third order intercept point as a function of output power per tone



Tuned for  $f_{IF} = 450$  MHz.

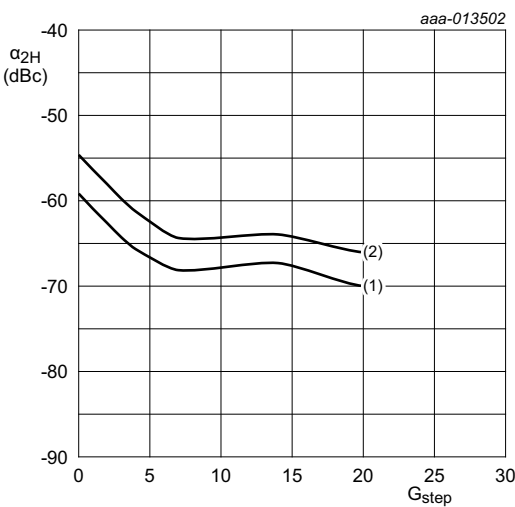
(1) gain step 0  
(2) gain step 14

Fig 29. Output third order intercept point as a function of output power per tone



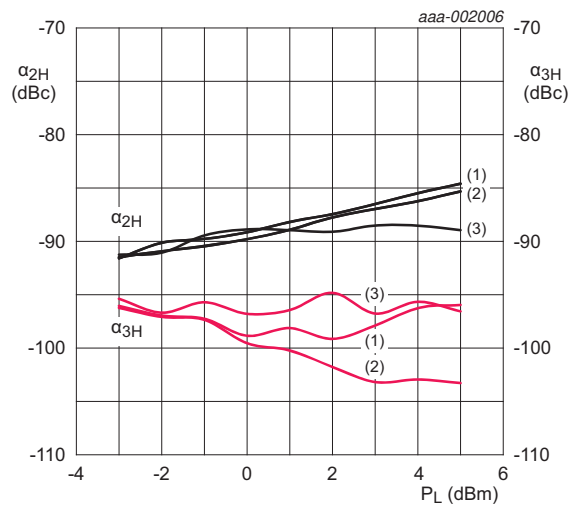
Tuned for  $f_{IF} = 86$  MHz;  $f_{2H} = 172$  MHz;  $f_{3H} = 258$  MHz.  
(1)  $P_L = 2$  dBm  
(2)  $P_L = 5$  dBm

Fig 30. Second harmonic level as a function of gain step



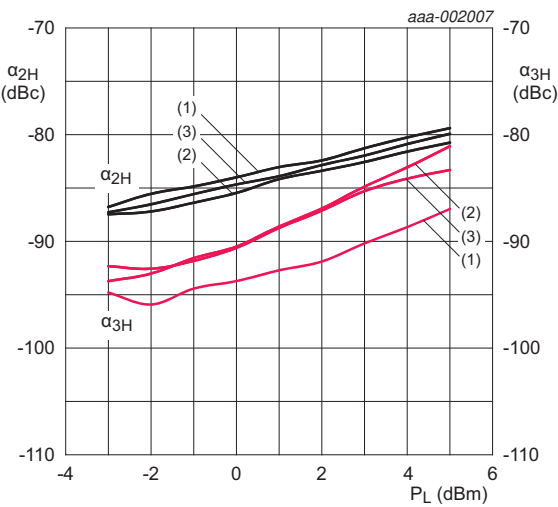
Tuned for  $f_{IF} = 225$  MHz;  $f_{2H} = 450$  MHz;  $f_{3H} = 675$  MHz.  
(1)  $P_L = 2$  dBm  
(2)  $P_L = 5$  dBm

Fig 31. Second harmonic level as a function of gain step



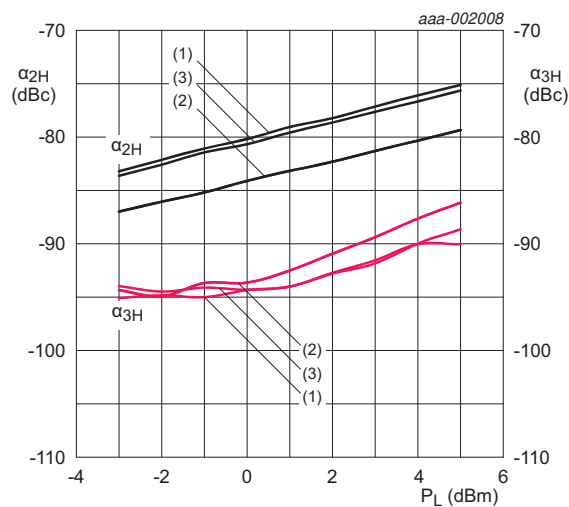
Tuned for  $f_{IF} = 50$  MHz;  $f_{2H} = 100$  MHz;  $f_{3H} = 150$  MHz;  
 $T_{amb} = 25$  °C.  
(1) gain step 0  
(2) gain step 14  
(3) gain step 24

Fig 32. Second harmonic level and third harmonic level as a function of output power



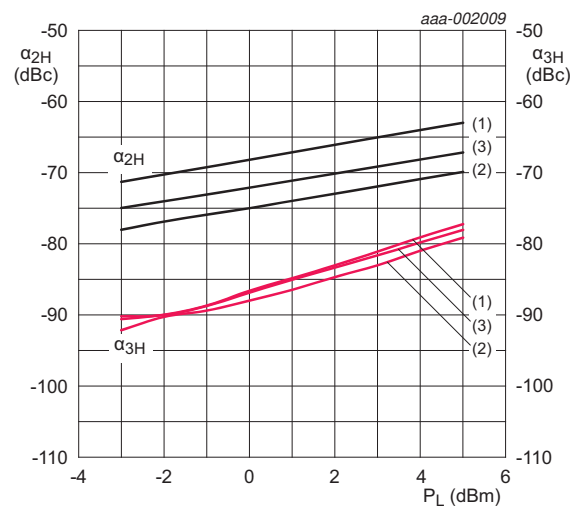
Tuned for  $f_{IF} = 86$  MHz;  $f_{2H} = 172$  MHz;  $f_{3H} = 258$  MHz;  
 $T_{amb} = 25$  °C.  
(1) gain step 0  
(2) gain step 14  
(3) gain step 24

Fig 33. Second harmonic level and third harmonic level as a function of output power



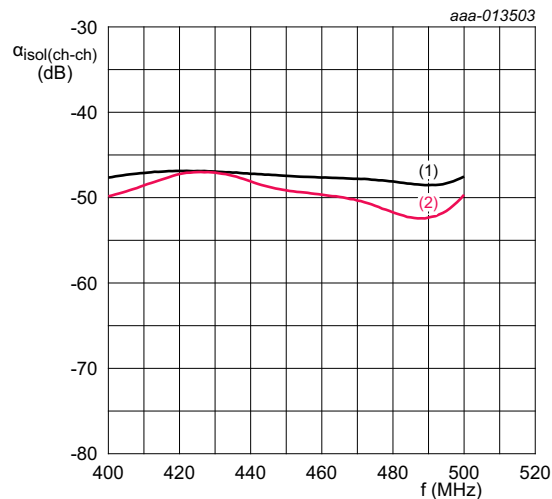
Tuned for  $f_{IF} = 172$  MHz;  $f_{2H} = 358$  MHz;  $f_{3H} = 530$  MHz;  $T_{amb} = 25$  °C.  
(1) gain step 0  
(2) gain step 14  
(3) gain step 24

Fig 34. Second harmonic level and third harmonic level as a function of output power



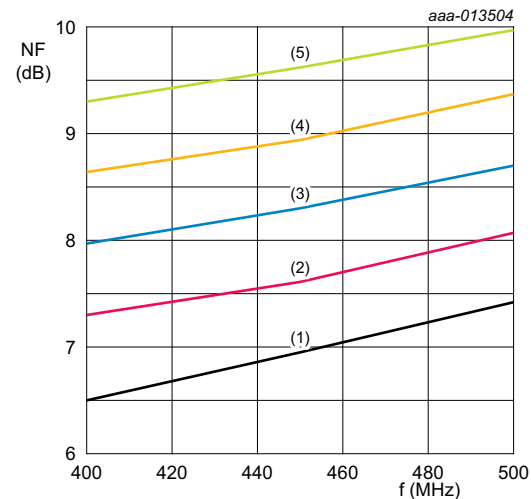
Tuned for  $f_{IF} = 250$  MHz;  $f_{2H} = 500$  MHz;  $f_{3H} = 750$  MHz;  $T_{amb} = 25$  °C.  
(1) gain step 0  
(2) gain step 14  
(3) gain step 24

Fig 35. Second harmonic level and third harmonic level as a function of output power



Tuned for  $f_{IF} = 450$  MHz  
(1) channel A at gain step 0 (maximum gain); channel B at gain step 28 (minimum gain)  
(2) channel A at gain step 0 (maximum gain); channel B at gain step 0 (maximum gain)

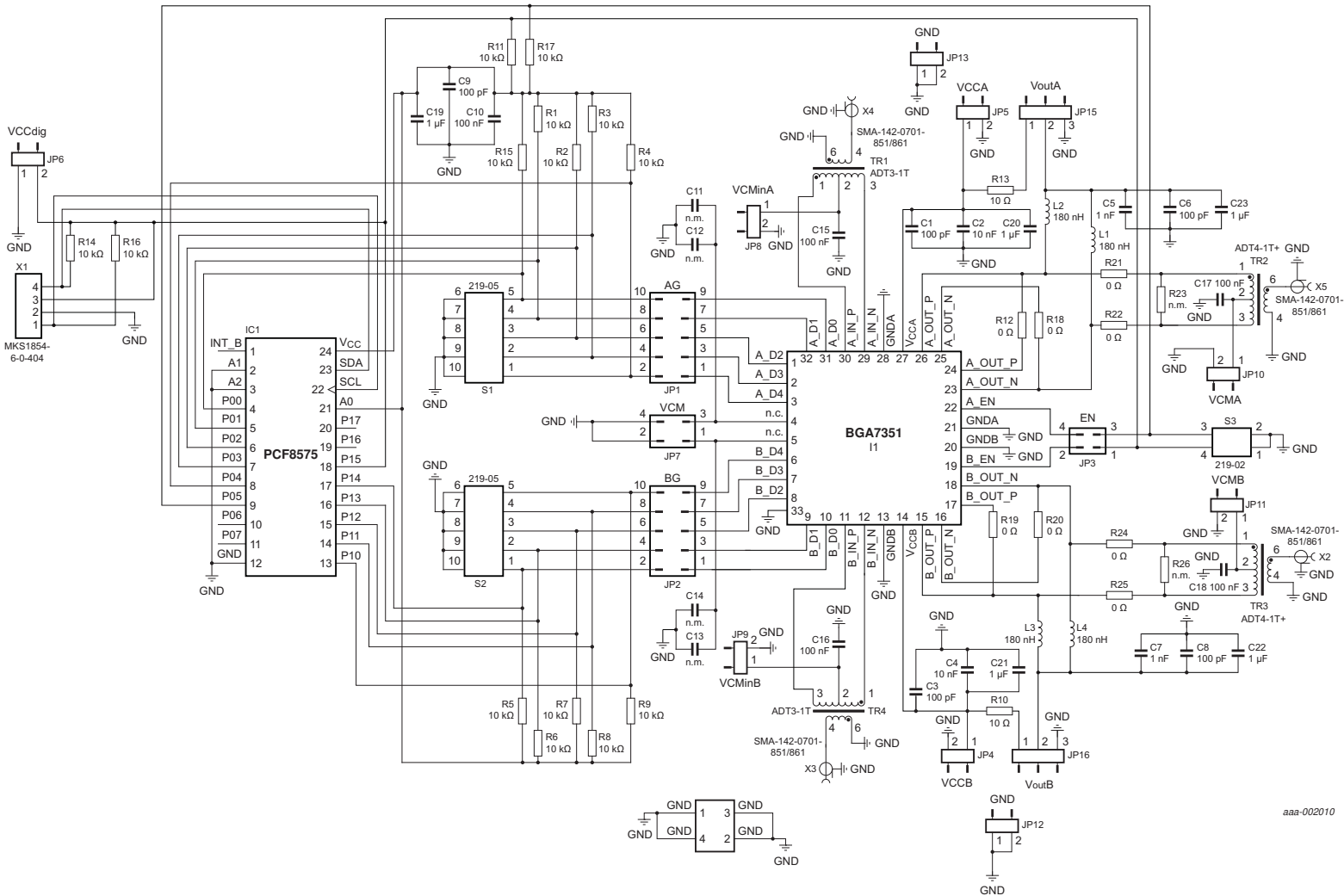
Fig 36. Isolation between channels as a function of frequency



Tuned for  $f_{IF} = 450$  MHz  
(1) gain step 0  
(2) gain step 1  
(3) gain step 2  
(4) gain step 3  
(5) gain step 4

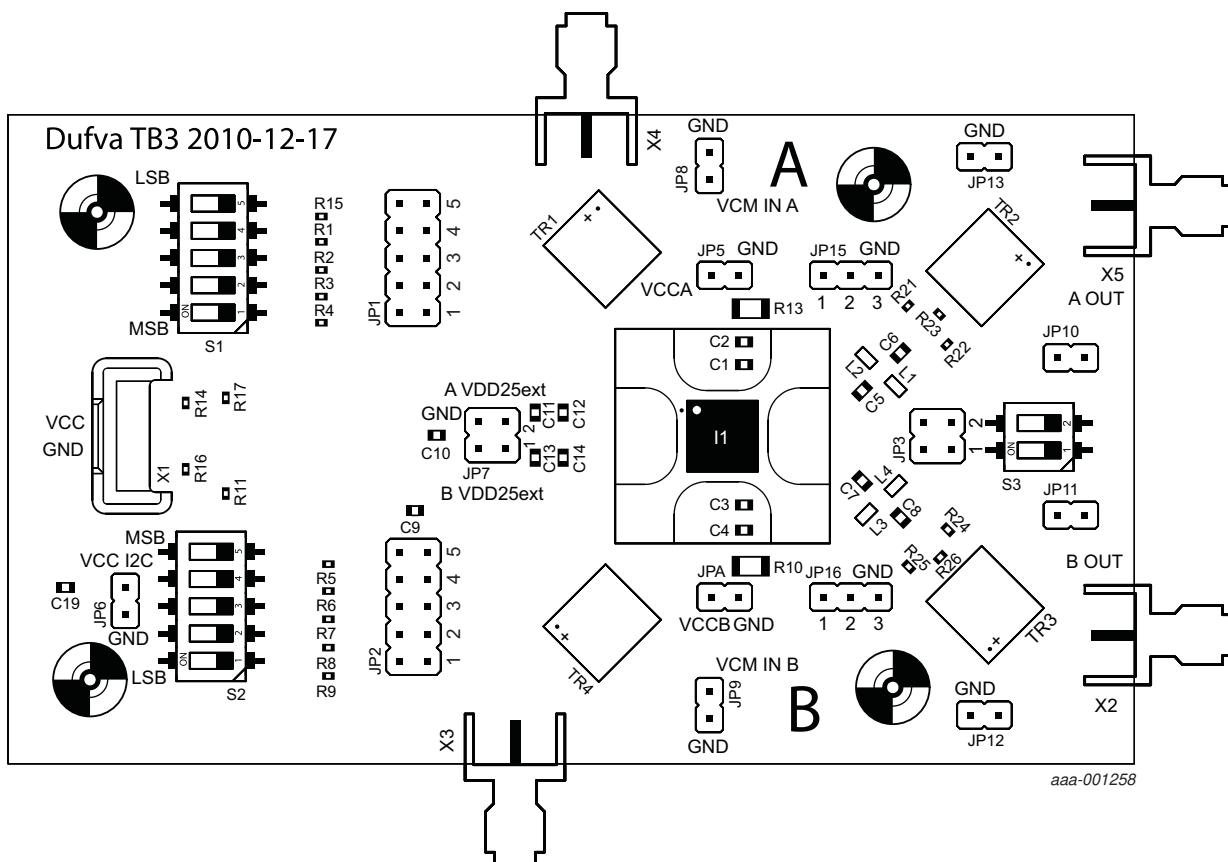
Fig 37. Noise figure as a function of frequency

## 11.1 Application PCB



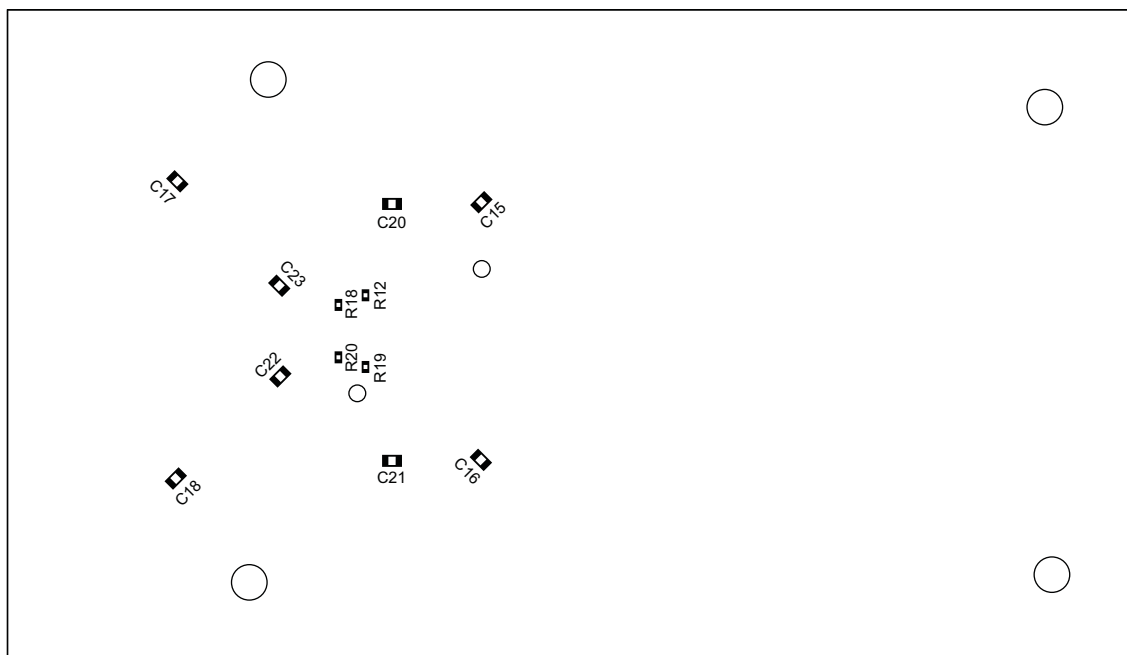
For a list of components see [Table 11](#).

**Fig 38. Schematic**



For a list of components see [Table 11](#).

**Fig 39. Components top side**



aaa-001259

For a list of components see [Table 11](#).

**Fig 40. Components bottom side**

**Table 11. List of components**

See [Figure 38](#), [Figure 39](#) and [Figure 40](#).

| Component               | Description | Conditions | Value     | Size | Remarks     |
|-------------------------|-------------|------------|-----------|------|-------------|
| C1, C3, C6, C8, C9      | capacitor   |            | 100 pF    | 0603 |             |
| C2, C4                  | capacitor   |            | 10 nF     | 0603 |             |
| C5, C7                  | capacitor   |            | 1 nF      | 0603 |             |
| C10, C15, C16, C17, C18 | capacitor   |            | 100 nF    | 0603 |             |
| C11                     | capacitor   |            | -         | 0603 | not mounted |
| C12                     | capacitor   |            | -         | 0603 | not mounted |
| C13                     | capacitor   |            | -         | 0603 | not mounted |
| C14                     | capacitor   |            | -         | 0603 | not mounted |
| C19, C20, C21, C22, C23 | capacitor   |            | 1 $\mu$ F | 0603 |             |
| I1                      | BGA7351     |            | -         |      |             |
| JP1                     | jumper      |            | -         | JP5  | AG          |
| JP2                     | jumper      |            | -         | JP5  | BG          |
| JP3                     | jumper      |            | -         | JP2  | EN          |
| JP4                     | jumper      |            | -         | JP2  | VCCB        |
| JP5                     | jumper      |            | -         | JP2  | VCCA        |
| JP6                     | jumper      |            | -         | JP2  | VCCdig      |
| JP7                     | jumper      |            | -         | JP2  | VCM         |
| JP8                     | jumper      |            | -         | JP2  | VCMInA      |

Table 11. List of components

See [Figure 38](#), [Figure 39](#) and [Figure 40](#).

| Component                                                   | Description     | Conditions                 | Value         | Size | Remarks                 |
|-------------------------------------------------------------|-----------------|----------------------------|---------------|------|-------------------------|
| JP9                                                         | jumper          |                            | -             | JP2  | VCMInB                  |
| JP10                                                        | jumper          |                            | -             | JP2  | VCMA                    |
| JP11                                                        | jumper          |                            | -             | JP2  | VCMB                    |
| JP12                                                        | jumper          |                            | -             | JP2  | GND                     |
| JP13                                                        | jumper          |                            | -             | JP2  | GND                     |
| JP15                                                        | jumper          |                            | -             | JP3  | VoutA                   |
| JP16                                                        | jumper          |                            | -             | JP3  | VoutB                   |
| L1, L2, L3, L4                                              | inductor        | $f_{IF} = 50 \text{ MHz}$  | 1200 nH       | 0603 | dependent on PCB layout |
|                                                             |                 | $f_{IF} = 172 \text{ MHz}$ | 150 nH        | 0603 | dependent on PCB layout |
|                                                             |                 | $f_{IF} = 250 \text{ MHz}$ | 56 nH         | 0603 | dependent on PCB layout |
|                                                             |                 | $f_{IF} = 450 \text{ MHz}$ | 27 nH         | 0603 | dependent on PCB layout |
| R1, R2, R3, R4, R5, R6, R7, R8, R9, R11, R14, R15, R16, R17 | resistor        |                            | 10 k $\Omega$ | 0402 |                         |
| R10, R13                                                    | resistor        |                            | 10 $\Omega$   | 1206 |                         |
| R12, R18, R19, R20, R21, R22, R24, R25                      | resistor        |                            | 0 $\Omega$    | 0402 |                         |
| R23, R26                                                    | resistor        |                            | -             | 0402 | not mounted             |
| S1, S2                                                      | DIP-switch      |                            | -             |      | CTS-219-05              |
| S3                                                          | DIP-switch      |                            | -             |      | CTS-219-02              |
| TR1                                                         | 1:3 transformer |                            | -             |      | Mini Circuits ADT3-1T+  |
| TR2                                                         | 1:4 transformer |                            | -             |      | Mini Circuits ADT4-1T+  |
| TR3                                                         | 1:3 transformer |                            | -             |      | Mini Circuits ADT4-1T+  |
| TR4                                                         | 1:4 transformer |                            | -             |      | Mini Circuits ADT3-1T+  |
| X1                                                          | -               |                            | -             |      | not mounted             |
| X2                                                          | SMA-connector   |                            | -             |      | BOUT_P                  |
| X3                                                          | SMA-connector   |                            | -             |      | BIN_P                   |
| X4                                                          | SMA-connector   |                            | -             |      | AIN_P                   |
| X5                                                          | SMA-connector   |                            | -             |      | AOUT_P                  |

12. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads;  
32 terminals; body 5 x 5 x 0.85 mm

SOT617-1

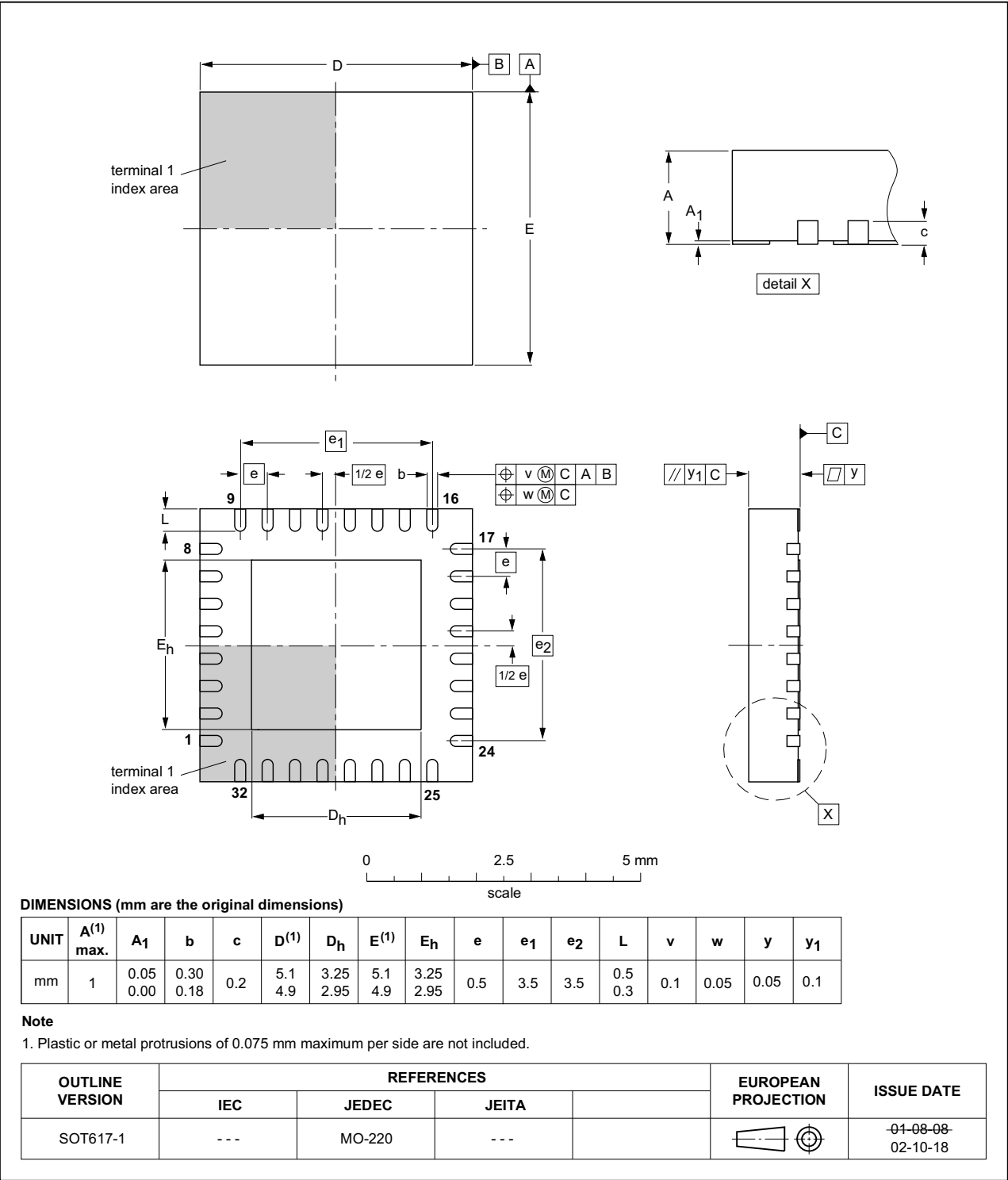


Fig 41. Package outline SOT617-1 (HVQFN32)

## 13. Abbreviations

Table 12. Abbreviations

| Acronym | Description                                     |
|---------|-------------------------------------------------|
| ADC     | Analog-to-Digital Converter                     |
| DIP     | Dual In-line Package                            |
| EMI     | ElectroMagnetic Interference                    |
| ESD     | ElectroStatic Discharge                         |
| GSM     | Global System for Mobile Communications         |
| HTOL    | High Temperature Operating Life                 |
| HVQFN   | Heatsink Very-thin Quad Flat-pack No-leads      |
| IF      | Intermediate Frequency                          |
| LSB     | Least Significant Bit                           |
| LTE     | Long Term Evolution                             |
| MMIC    | Monolithic Microwave Integrated Circuit         |
| MSB     | Most Significant Bit                            |
| PCB     | Printed-Circuit Board                           |
| SMA     | SubMiniature version A                          |
| WiMAX   | Worldwide Interoperability for Microwave Access |
| W-CDMA  | Wideband Code Division Multiple Access          |

## 14. Revision history

Table 13. Revision history

| Document ID    | Release date                                                                                                                                                                                                                                                                                                                           | Data sheet status  | Change notice | Supersedes  |
|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|---------------|-------------|
| BGA7351 v.3    | 20140611                                                                                                                                                                                                                                                                                                                               | Product data sheet | -             | BGA7351 v.2 |
| Modifications: | <ul style="list-style-type: none"> <li><a href="#">Table 8 on page 7</a>: some changes have been made</li> <li><a href="#">Section 11 on page 11</a>: some graphs have been added.</li> <li><a href="#">Table 11 on page 22</a>: the condition <math>f = 450</math> MHz has been added for the row containing the inductors</li> </ul> |                    |               |             |
| BGA7351 v.2    | 20121219                                                                                                                                                                                                                                                                                                                               | Product data sheet | -             | BGA7351 v.1 |
| BGA7351 v.1    | 20111228                                                                                                                                                                                                                                                                                                                               | Product data sheet | -             | -           |

## 15. Legal information

### 15.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition                                                                            |
|-----------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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