BLF7G20L-200; BLF7G20LS-200

Power LDMOS transistor

Rev. 5 — 1 September 2015

AMPLEON

Product data sheet

1. Product profile

1.1 General description

200 W LDMOS power transistor for base station applications at frequencies from 1805 MHz to 1990 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in a common source class-AB production test circuit.

Mode of operation	f (MHz)	I_{Dq} (mA)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	ACPR (dBc)
2-carrier W-CDMA	1805 to 1880	1620	28	55	18	33	–29 [1]

[1] Test signal: 3GPP; test model 1; 64 PDPCH; PAR = 8.4 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

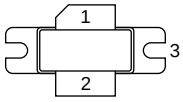
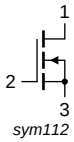
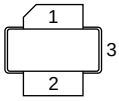
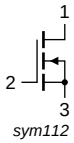
- Excellent ruggedness
- High efficiency
- Low R_{th} providing excellent thermal stability
- Designed for broadband operation (1805 MHz to 1990 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low-memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

1.3 Applications

- RF power amplifiers for W-CDMA base stations and multi-carrier applications in the 1805 MHz to 1990 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Graphic symbol
BLF7G20L-200 (SOT502A)				
1	drain			
2	gate			
3	source	[1]		
BLF7G20LS-200 (SOT502B)				
1	drain			
2	gate			
3	source	[1]		

[1] Connected to flange

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF7G20L-200	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A
BLF7G20LS-200	-	earless flanged LDMOST ceramic package; 2 leads	SOT502B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 55 W; V_{DS} = 28 V; I_{Dq} = 1620 mA	0.27	K/W

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6. Characteristics

Table 6. Characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.5 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 150 mA	1.5	1.9	2.3	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	4.2	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	42	50.6	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	−420	2.44	420	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 7.5 A	-	18.6	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 5.25 A	-	0.093	-	Ω

7. Test information

Table 7. Functional test information

Mode of operation: 2-carrier W-CDMA; PAR = 8.4 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 64 PDPCH; f_1 = 1807.5 MHz; f_2 = 1812.5 MHz; f_3 = 1872.5 MHz; f_4 = 1877.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 1620 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

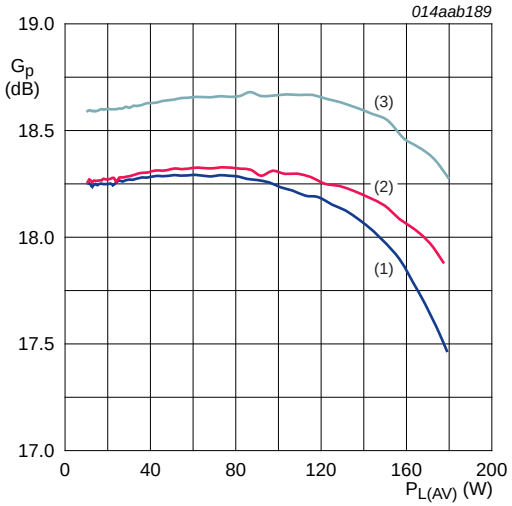
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(AV)}$	average output power		-	55	-	W
G_p	power gain	$P_{L(AV)}$ = 55 W	17	18	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 55 W	-	-	−10	dB
η_D	drain efficiency	$P_{L(AV)}$ = 55 W	30	33	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 55 W	-	−29	-	dBc

7.1 Ruggedness in class-AB operation

The BLF7G20L-200 and BLF7G20LS-200 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 30 V; I_{Dq} = 1620 mA; P_L = 185 W (CW); f = 1805 MHz to 1880 MHz.

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7.2 1 Tone CW



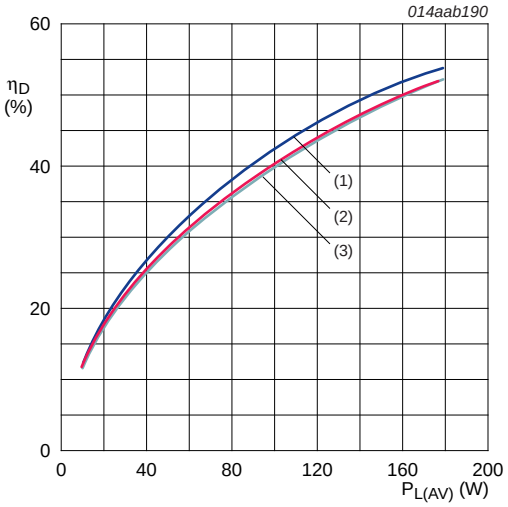
V_{DS} = 28 V; I_{Dq} = 1620 mA.

(1) f = 1805 MHz

(2) f = 1845 MHz

(3) f = 1880 MHz

Fig 1. Power gain as a function of average output power; typical values



V_{DS} = 28 V; I_{Dq} = 1620 mA.

(1) f = 1805 MHz

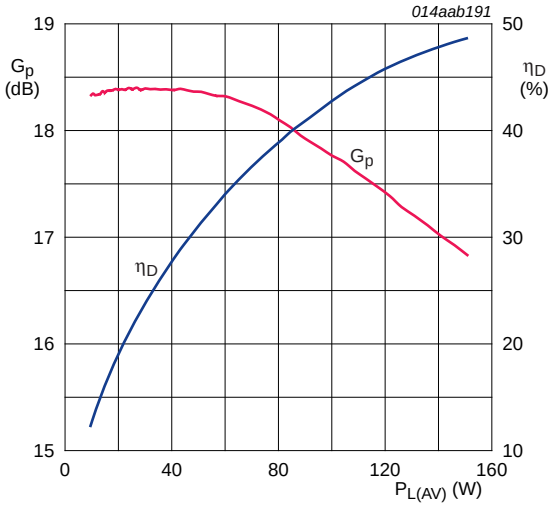
(2) f = 1845 MHz

(3) f = 1880 MHz

Fig 2. Drain efficiency as a function of average output power; typical values

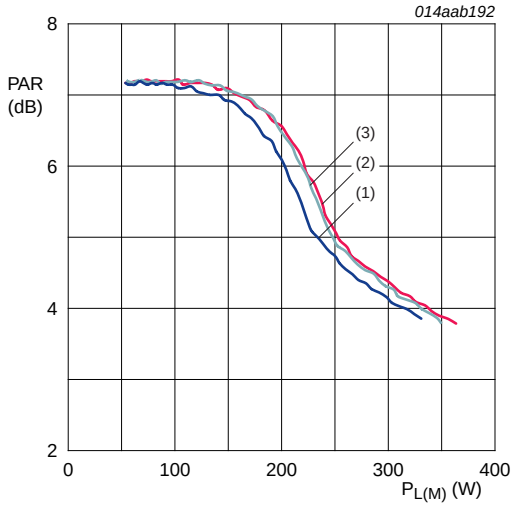
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7.3 1-carrier W-CDMA



V_{DS} = 28 V; I_{Dq} = 1620 mA; f = 1845 MHz; PAR = 7.2 dB at 0.01 % probability on the CCDF.

Fig 3. Power gain and drain efficiency as functions of average output power; typical values



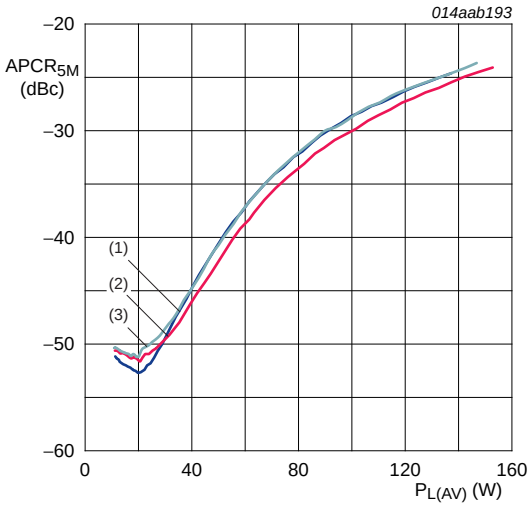
V_{DS} = 28 V; I_{Dq} = 1620 mA; PAR = 7.2 dB at 0.01 % probability on the CCDF.

(1) f = 1805 MHz

(2) f = 1845 MHz

(3) f = 1880 MHz

Fig 4. Peak-to-average power ratio as a function of peak power; typical values



V_{DS} = 28 V; I_{Dq} = 1620 mA; PAR = 7.2 dB at 0.01 % probability on the CCDF.

(1) f = 1805 MHz

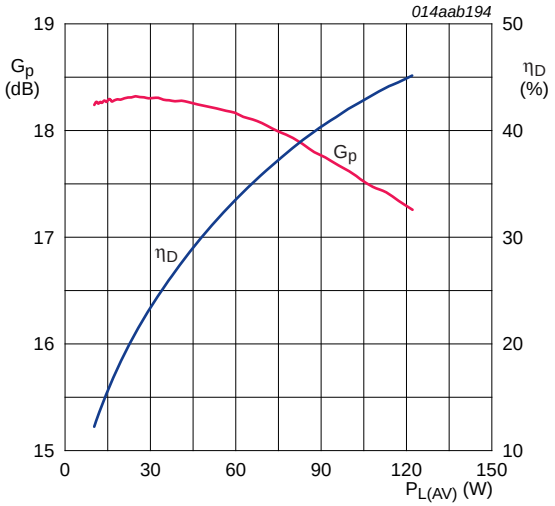
(2) f = 1845 MHz

(3) f = 1880 MHz

Fig 5. Adjacent power channel ratio (5 MHz) as function of average output power; typical values

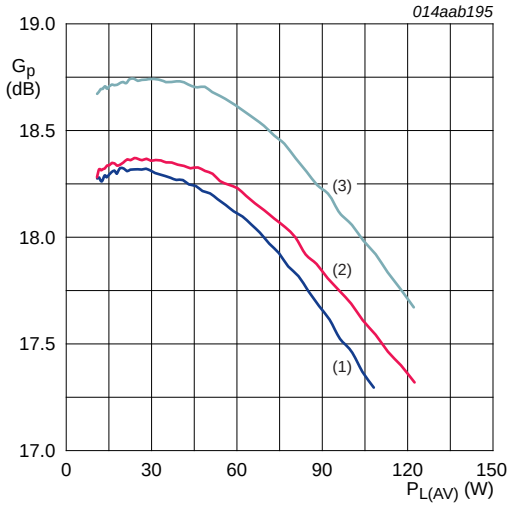
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7.4 2-carrier W-CDMA



V_{DS} = 28 V; I_{Dq} = 1620 mA; channel spacing = 5 MHz; PAR = 8.4 dB at 0.01 % probability on the CCDF.

Fig 6. Power gain and drain efficiency as functions of average output power; typical values



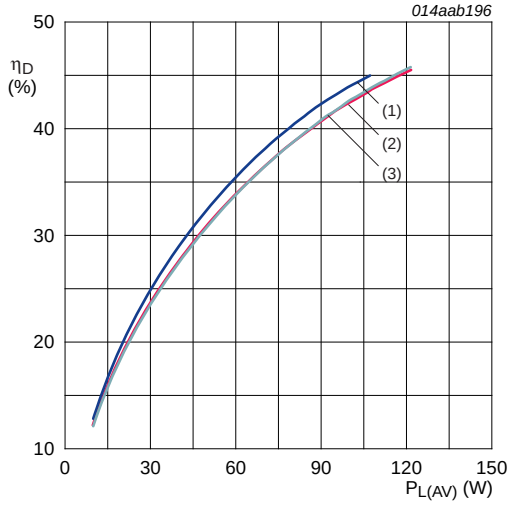
V_{DS} = 28 V; I_{Dq} = 1620 mA; channel spacing = 5 MHz; PAR = 8.4 dB at 0.01 % probability on the CCDF.

(1) f = 1805 MHz

(2) f = 1845 MHz

(3) f = 1880 MHz

Fig 7. Power gain as a function of average output power; typical values



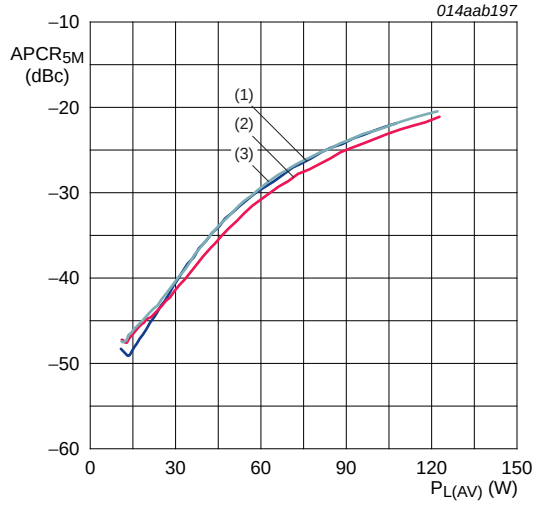
V_{DS} = 28 V; I_{Dq} = 1620 mA; channel spacing = 5 MHz; PAR = 8.4 dB at 0.01 % probability on the CCDF.

(1) f = 1805 MHz

(2) f = 1845 MHz

(3) f = 1880 MHz

Fig 8. Drain efficiency as a function of average output power; typical values



V_{DS} = 28 V; I_{Dq} = 1620 mA; channel spacing = 5 MHz; PAR = 8.4 dB at 0.01 % probability on the CCDF.

(1) f = 1805 MHz

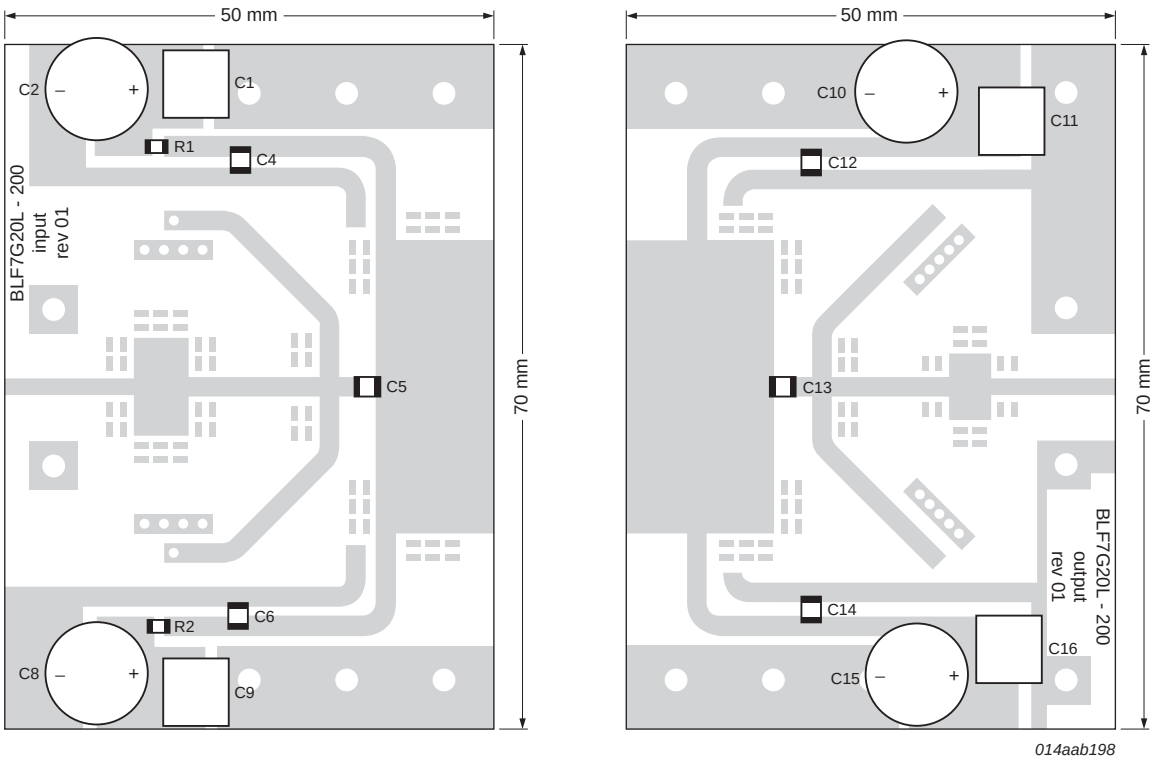
(2) f = 1845 MHz

(3) f = 1880 MHz

Fig 9. Adjacent power channel ratio (5 MHz) as a function of average output power; typical values

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7.5 Test circuit



See Table 8 for list of components. The drawing is not to scale.

Fig 10. Component layout

Table 8. List of components

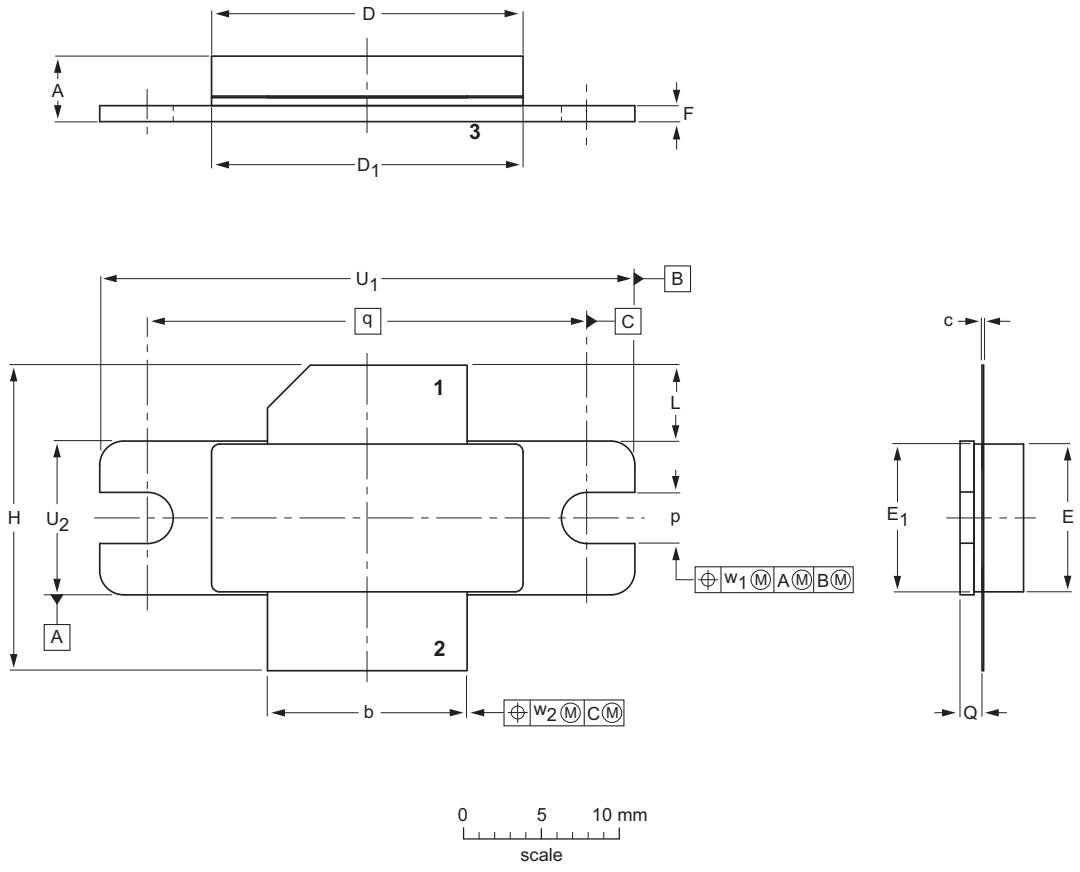
See Figure 10 for component layout.

Component	Description	Value	Remarks
C1, C9, C11, C16	multilayer ceramic chip capacitor	10 μF	TDK
C4, C6	multilayer ceramic chip capacitor	68 pF	ATC800B
C5	multilayer ceramic chip capacitor	2.0 pF	ATC800B
C12, C14	multilayer ceramic chip capacitor	100 pF	ATC800B
C13	multilayer ceramic chip capacitor	3.3 pF	ATC800B
C2, C8, C10, C15	electrolytic capacitor	470 μF; 63 V	
R1, R2	chip resistor	10 Ω	Philips 0603

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8. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads **SOT502A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

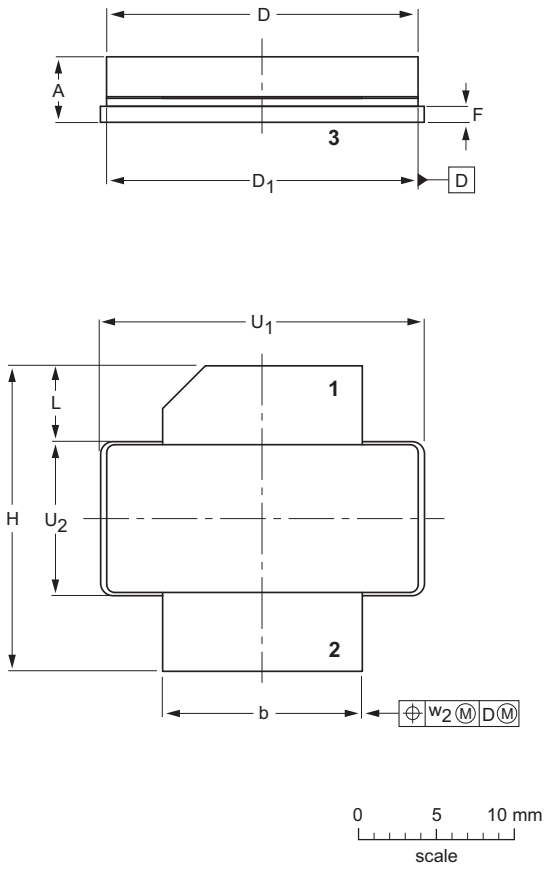
UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						~~03-01-10~~ 12-05-02

Fig 11. Package outline SOT502A

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Earless flanged ceramic package; 2 leads **SOT502B**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502B						~~07-05-09~~ 12-05-02

Fig 12. Package outline SOT502B

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9. Abbreviations

Table 9. Abbreviations

Acronym	Description
3GPP	Third Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
PDPCH	transmission Power of the Dedicated Physical CHannel
RF	Radio Frequency
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

10. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF7G20L-200_7G20LS-200#5	20150901	Product data sheet	-	BLF7G20L-200_7G20LS-200 v.4
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. • Legal texts have been adapted to the new company name where appropriate.			
BLF7G20L-200_7G20LS-200 v.4	20110722	Product data sheet	-	BLF7G20L-200_7G20LS-200 v.3
BLF7G20L-200_7G20LS-200 v.3	20110301	Preliminary data sheet	-	BLF7G20L-200_7G20LS-200 v.2
BLF7G20L-200_7G20LS-200 v.2	20100827	Preliminary data sheet	-	BLF7G20L-200_7G20LS-200 v.1
BLF7G20L-200_7G20LS-200 v.1	20100603	Objective data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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