I²C BUS compatible serial EEPROM

BR24C01A-W / BR24C01AF-W / BR24C01AFJ-W / BR24C01AFV-W / BR24C02-W / BR24C02F-W / BR24C02FJ-W / BR24C02FV-W / BR24C04-W / BR24C04F-W / BR24C04FJ-W / BR24C04FV-W

The BR24C01A-W, BR24C02-W, and BR24C04-W series are 2-wire (I²C BUS type) serial EEPROMs which are electrically programmable.

∗ I²C BUS is a registered trademark of Philips.

●Applications

VCRs, TVs, printers, car stereos, cordless telephones, short wave radios, programmable DIP switches

●Features

1) 128×8bits (1k) serial EEPROM.
(BR24C01A-W / AF-W / AFJ-W / AFV-W)
256×8bits (2k) serial EEPROM.
(BR24C02-W / F-W / FJ-W / FV-W)
512×8bits (4k) serial EEPROM.
(BR24C04-W / F-W / FJ-W / FV-W)
2) Two wire serial interface.
3) Operating voltage range : 2.7V~5.5V
4) Low current consumption
Active (at 5V) : 1.5mA (Typ.)
Standby (at 5V) : 0.1μA (Typ.)
5) Auto erase and auto complete functions can be used during write operations.
6) Page write function.
BR24C01A-W / AF-W / AFJ-W / AFV-W : 8 bytes
BR24C02-W / F-W / FJ-W / FV-W : 8 bytes
BR24C04-W / F-W / FJ-W / FV-W : 16 bytes
7) DATA security
Write protect feature
Inhibit to WRITE at low V_{CC}
8) Noise filters at SCL and SDA pins.
9) Address can be incremented automatically during read operations.
10) Compact packages.
11) Rewriting possible up to 100,000 times
12) Data can be stored for ten years without corruption.

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Applied voltage	V_{CC}	−0.3~+6.5	V
Power dissipation	Pd	300(SSOP−B8) ∗1	mW
		450(SOP8, SOP−J8) ∗2	
		800(DIP8) ∗3	
Storage temperature	Tstg	−65~+125	°C
Operating temperature	Topr	−40~+85	°C
Input voltage	−	−0.3~V_{CC}+0.3	V

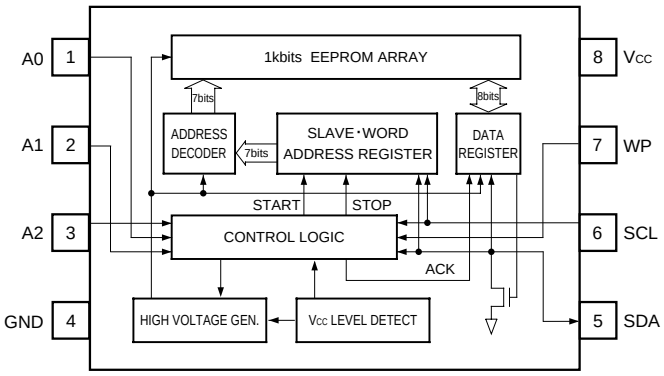
∗1 Reduced by 3.0mW for each increase in Ta of 1°C over 25°C.
∗2 Reduced by 4.5mW for each increase in Ta of 1°C over 25°C.
∗3 Reduced by 8.0mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	2.7~5.5 (WRITE)	V
		2.7~5.5 (READ)	V
Input voltage	V_{IN}	0~V_{CC}	V

●Block diagram

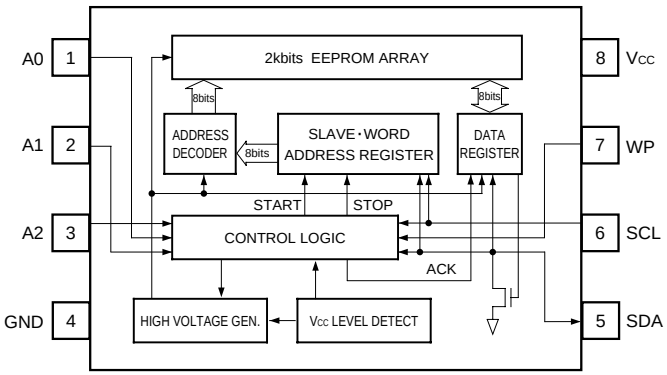
BR24C01A-W / AF-W / AFJ-W / AFV-W



●Pin descriptions

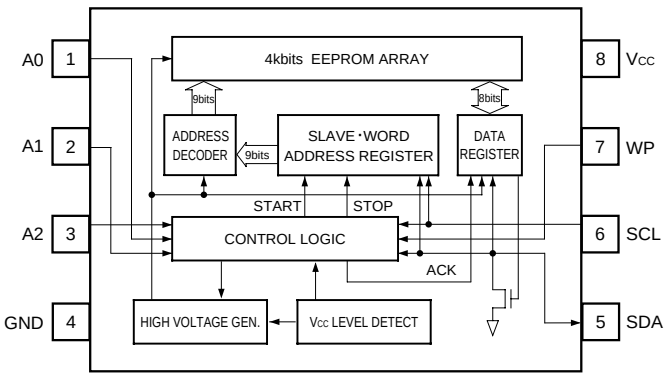
Pin name	Function
A0, A1, A2	Slave address setting pin
SCL	Serial data clock
SDA	Serial data input / output *
WP	Write protect pin
V_{CC}	Power supply
GND	Ground

* An open drain output requires a pull-up resistor.



Pin name	Function
A0, A1, A2	Slave address setting pin
SCL	Serial data clock
SDA	Serial data input / output *
WP	Write protect pin
V_{CC}	Power supply
GND	Ground

* An open drain output requires a pull-up resistor.



Pin name	Function
A0	N.C.
A1, A2	Slave address setting pin
SCL	Serial data clock
SDA	Serial data input / output *
WP	Write protect pin
V_{CC}	Power supply
GND	Ground

* An open drain output requires a pull-up resistor.

●Electrical characteristics

DC characteristics (unless otherwise noted, Ta = –40 to + 85 °C, V_{CC} = 2.7 to 5.5V)

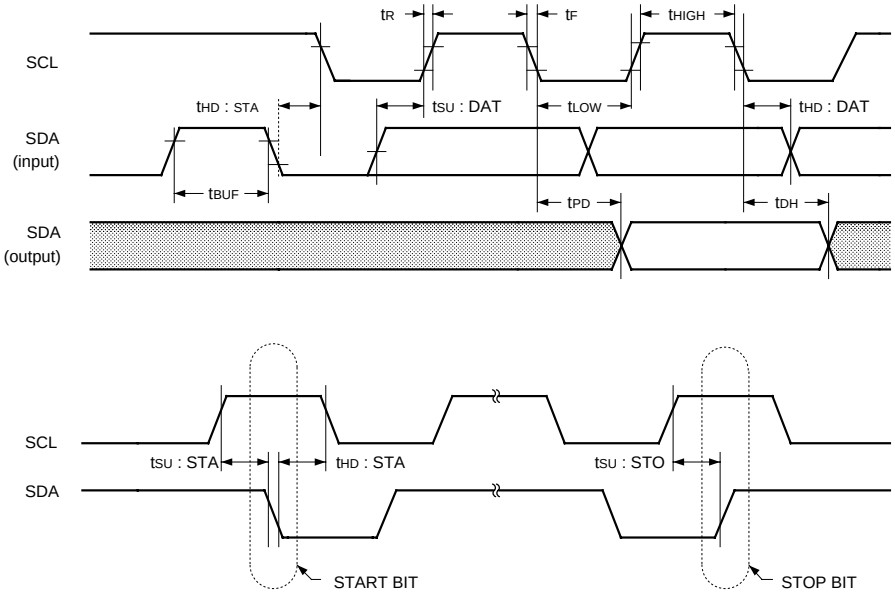
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input high level voltage	V_{IH}	0.7V_{CC}	–	–	V	–
Input low level voltage	V_{IL}	–	–	0.3V_{CC}	V	–
Output low level coltage	V_{OL}	–	–	0.4	V	I_{OL}=3.0mA(SDA)
Input leakage current	I_{LI}	–1	–	1	μA	V_{IN}=0V~V_{CC}
Output leakage current	I_{LO}	–1	–	1	μA	V_{OUT}=0V~V_{CC}
operatingcurrent dissipation	I_{CC}	–	–	2.0	mA	V_{CC}=5.5V, f_{SCL}=400kHz
Standby current	I_{SB}	–	–	2.0	μA	V_{CC}=5.5V, SDA·SCL=V_{CC} A0, A1, A2=GND, WP=GND

◎ Not designed for radiation resistance.

–40 to + 85 °C, V_{CC} = 2.7 to 5.5V)

Parameter	Symbol	Vcc=5V±10%			Vcc=3V±10%			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL frequency	f_{SCL}	–	–	400	–	–	100	kHz
Data clock HIGH time	t_{HIGH}	0.6	–	–	4.0	–	–	μs
Data clock LOW time	t_{LOW}	1.2	–	–	4.7	–	–	μs
SDA / SCL rise time	t_R	–	–	0.3	–	–	1.0	μs
SDA / SCL fall time	t_F	–	–	0.3	–	–	0.3	μs
Start condition hold time	t_{HD} : STA	0.6	–	–	4.0	–	–	μs
Start condition setup time	t_{SU} : STA	0.6	–	–	4.7	–	–	μs
Input data hold time	t_{HD} : DAT	0	–	–	0	–	–	ns
Input data setup time	t_{SU} : DAT	100	–	–	250	–	–	ns
Output data delay time	t_{PD}	0.1	–	0.9	0.2	–	3.5	μs
Output data hold time	t_{DH}	0.1	–	–	0.2	–	–	μs
Stop condition setup time	t_{SU} : STO	0.6	–	–	4.7	–	–	μs
Bus open time before start of transfer	t_{BUF}	1.2	–	–	4.7	–	–	μs
Internal write cycle time	t_{WR}	–	–	10	–	–	10	ms
Noise erase valid time (SCL / SDA pins)	t_I	–	–	0.05	–	–	0.1	μs

●Timing charts



· Data is read on the rising edge of SCL.

· Data is output in synchronization with the falling edge of SCL.

Fig.1 Synchronized data input / output timing

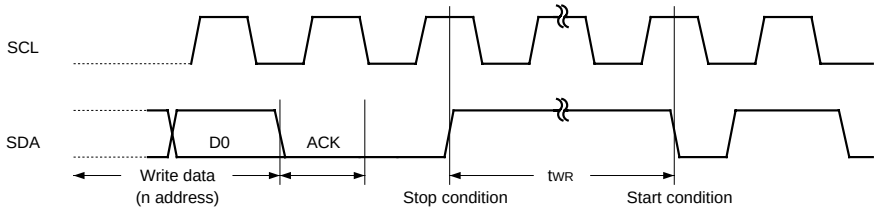


Fig.2 Write cycle timing

●Circuit operation

(1) Start condition (recognition of start bit)

Before executing any command, when SCL is HIGH, a start condition (start bit) is required to cause SDA to fall from HIGH to LOW. This IC is designed to constantly detect whether there is a start condition (start bit) for the SDA and SCL line, and no commands will be executed unless this condition is satisfied.
(See Fig.1 for the synchronized data input / output timing.)

(2) Stop condition (recognition of stop bit)

To stop any command, a stop condition (stop bit) is required. A stop condition is achieved when SDA goes from LOW to HIGH while SCL is HIGH. This enables commands to be completed.
(See Fig.1 for the synchronized data input / output timing.)

(3) Precautions concerning write commands

In the WRITE mode, the transferred data is not written to the memory unless the stop bit is executed.

(4) Device addressing

– BR24C01A-W / AF-W / AFJ-W / AFV-W, BR24C02-W / F-W / FJ-W / FV-W

1) Make sure the slave address is output from the master immediately after the start condition.
2) The upper four bits of the slave address are used to determine the device type. The device code for this IC is fixed at "1010".
3) The next three bits of the slave address (A2, A1, A0 … device address) are used to select the device. This IC can address up to eight devices on the same bus.
4) The lowermost bit of the slave address (R / $\overline{W}$ … READ / $\overline{WRITE}$) is used to set the write or read mode as follows.
   R / $\overline{W}$ set to 0 … Write
   (Random read word address setting is also 0)
   R / $\overline{W}$ set to 1 … Read

1010	A2	A1	A0	R / $\overline{W}$

1) Make sure the slave address is output from the master in continuation with the start condition.
2) The upper four bits of the slave address are used to determine the device type. The device code for this IC is fixed at "1010".
3) The next two bits of the slave address (A2, A1, … device address) are used to select the device. This IC can address up to four devices on the same bus.
4) The next bit of the slave address (PS … Page Select) is used to select the page. As shown below, it can write to or read from any of the 256 words in the two pages in memory.
   PS set to 0 … Page 1 (000 to 0FF)
   PS set to 1 … Page 2 (100 to 1FF)
5) The lowermost bit of the slave address (R / $\overline{W}$ … READ / $\overline{WRITE}$) is used to set the write or read mode as follows.
   R / $\overline{W}$ set to 0 … Write
   (Random read word address setting is also 0)
   R / $\overline{W}$ set to 1 … Read

1010	A2	A1	PS	R / $\overline{W}$

When WP pin set to V_{CC} (High level), write protect is set by all address. When WP pin set to GND (Low level), enable to write to all address. Either control this pin or connect to GND (or V_{CC}). It is inhibited from being left unconnected.

(6) ACK signal

The acknowledge signal (ACK signal) is determined by software and is used to indicate whether or not a data transfer is proceeding normally. The transmitting device, whether the master or slave, opens the bus after an 8-bit data output (μ-COM when a write or read command of the slave address input ; this IC when reading data).

For the receiving device during the ninth clock cycle, SDA is set to LOW and an acknowledge signal (ACK signal) is sent to indicate that it received the 8-bit data (this IC when a write command or a read command of the slave address input, μ-COM when a read command data output).

The ICs output a LOW acknowledge signal (ACK signal) after recognizing the start condition and slave address (8 bits).

When data is being write to the ICs, a LOW acknowledge signal (ACK signal) is output after the receipt of each eight bits of data (word address and write data).

When data is being read from the IC, eight bits of data (read data) are output and the IC waits for a returned LOW acknowledge signal (ACK signal). When an acknowledge signal (ACK signal) is detected and a stop condition is not sent from the master (μ-COM) side, the IC continues to output data. If an acknowledge signal (ACK signal) is not detected, the IC interrupts the data transfer and ceases reading operations after recognizing the stop condition (stop bit). The IC then enters the waiting or standby state.
(See Fig.3 for acknowledge signal (ACK signal) response.)

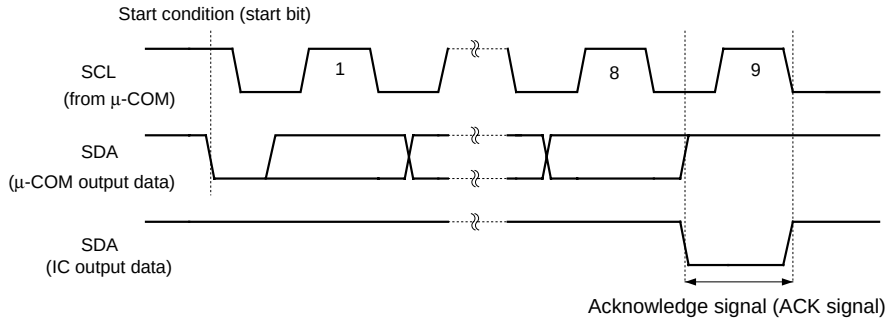


Fig.3 Acknowledge (ACK signal) response
(during write and read slave address input)

BR24C01A-W / AF-W / AFJ-W / AFV-W

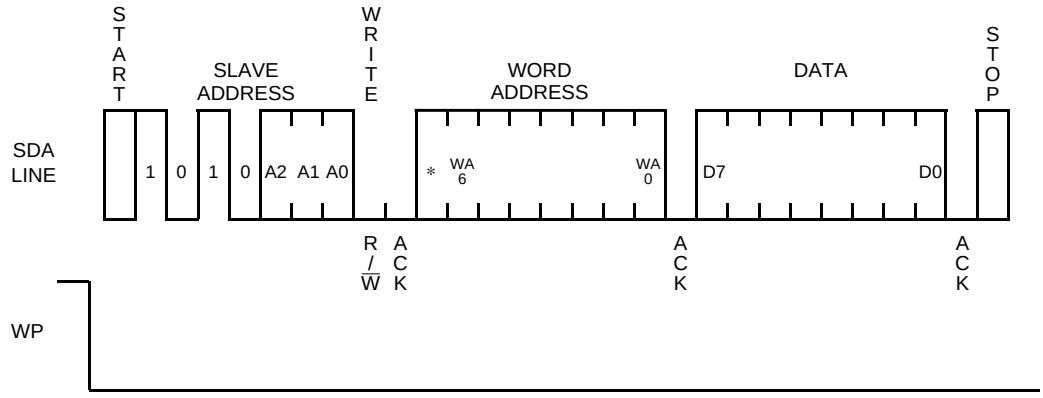


Fig.4

BR24C02-W / F-W / FJ-W / FV-W

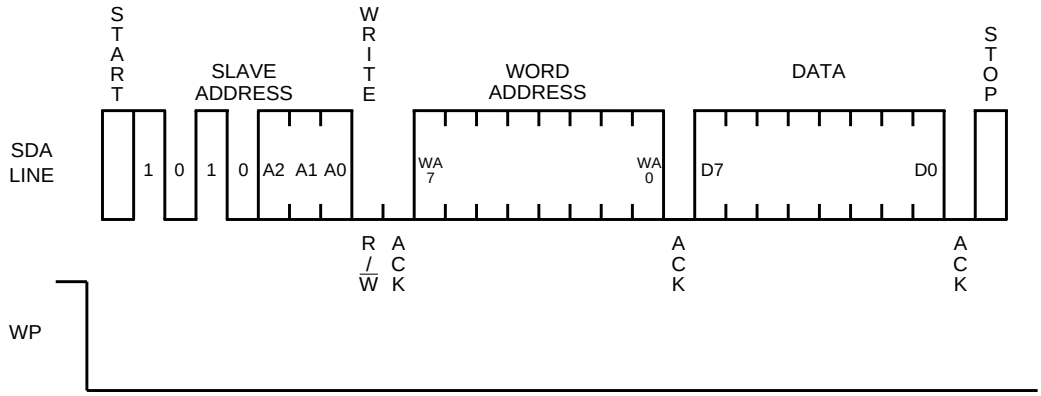


Fig.5

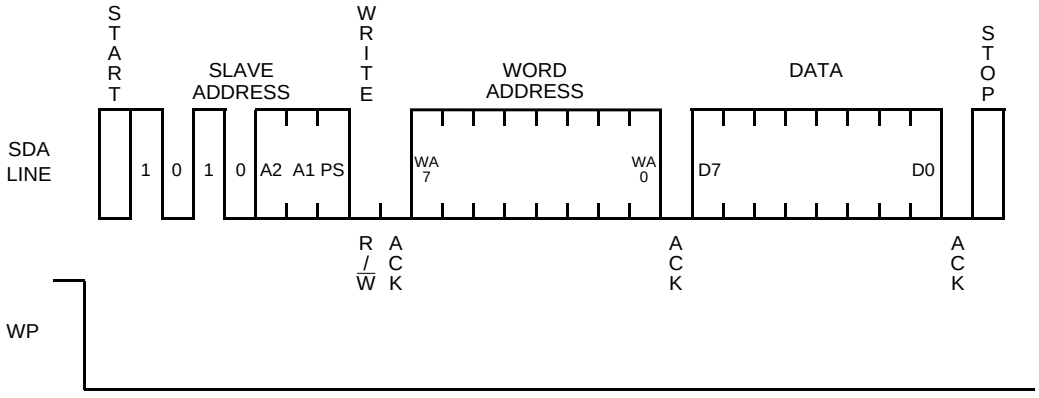


Fig.6

Data is written to the address designated by the word address (n address).

- After eight bits of data are input, the data is written to the memory cell by issuing the stop bit.

(8) Page write cycle

BR24C01A-W / AF-W / AFJ-W / AFV-W

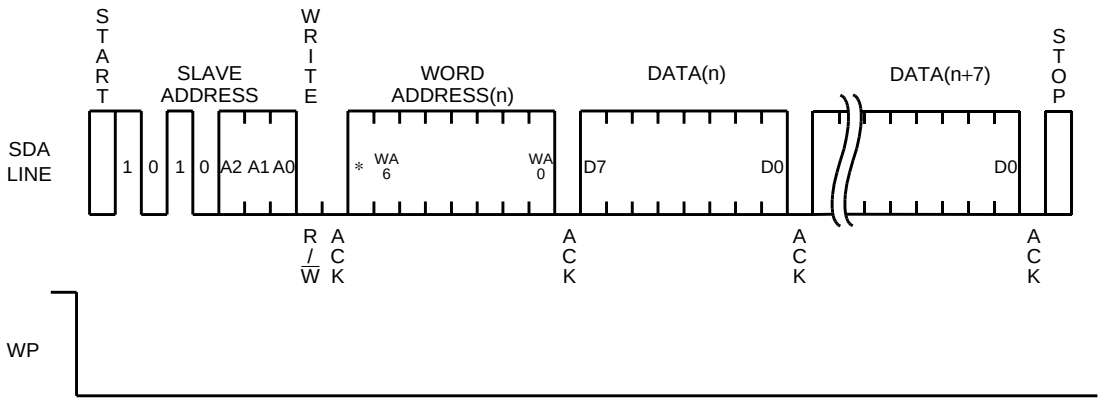


Fig.7

- A 8-byte write is possible using this command.
- Th page write command arbitrarily sets the upper four bits (WA6 to WA3) of the word address. The lower three bits (WA2 and WA0) can write up to eight bytes of data with the address being incremented internally.

BR24C02-W / F-W / FJ-W / FV-W

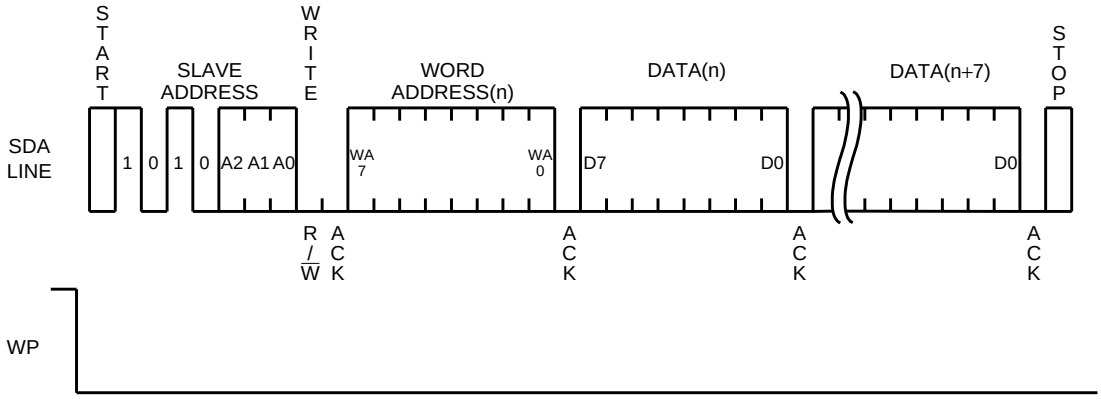


Fig.8

A 8-byte write is possible using this command.

- Th page write command arbitrarily sets the upper five bits (WA7 to WA3) of the word address. The lower three bits (WA2 and WA0) can write up to eight bytes of data with the address being incremented internally.

BR24C04-W / F-W / FJ-W / FV-W

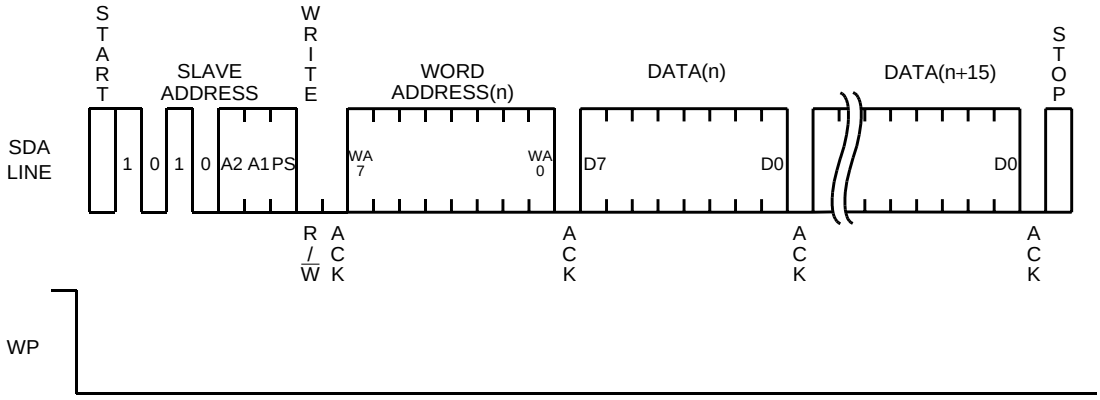


Fig.9

A 16-byte write is possible using this command.

- Th page write command arbitrarily sets the upper four bits (WA7 to WA4) of the word address. The lower four bits (WA3 and WA0) can write up to sixteen bytes of data with the address being incremented internally.

(9) Current read cycle

BR24C01A-W / AF-W / AFJ-W / AFV-W

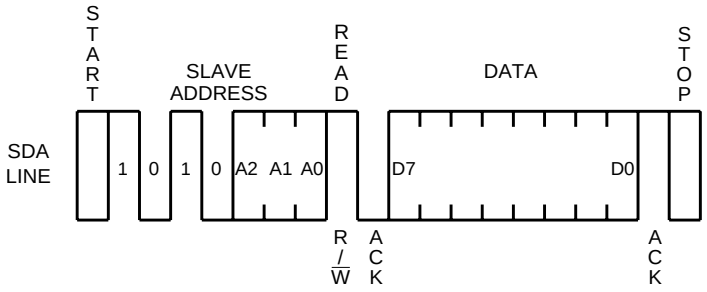


Fig.10

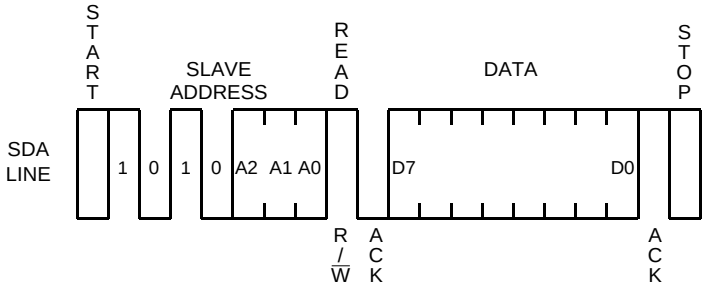


Fig.11

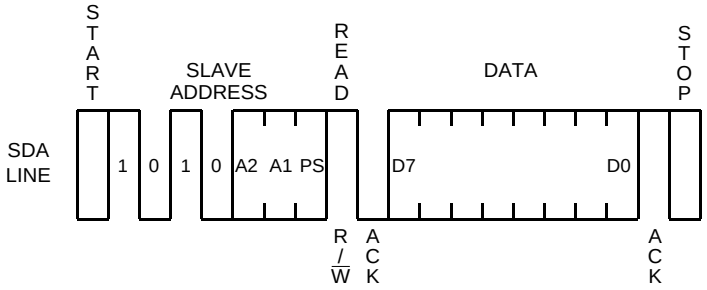


Fig.12

In case the previous operation is random or current read (which includes sequential read respectively), the internal address counter is increased by one from the last accessed address (n). Thus current read outputs the data of the next word address (n+1).

If the last command is byte or page write, the internal address counter stays at the last address (n). Thus current read outputs the data of the word address (n).

If the master does not transfer the acknowledge but does generate a stop condition, the current address read operation only provides s single byte of data.

At this point, this IC discontinues transmission.

- When an ACK signal LOW is detected after D0 and a stop condition is not sent from the master (μ-COM), the next word address data can be read. [All words all read enabled]
  (See Fig.16 to 18 for the sequential read cycles.)
- This command is ended by inputting HIGH to the ACK signal after D0 and raising the SDA signal (stop condition) by setting SCL to HIGH.

(10) Random read cycle

BR24C01A-W / AF-W / AFJ-W / AFV-W

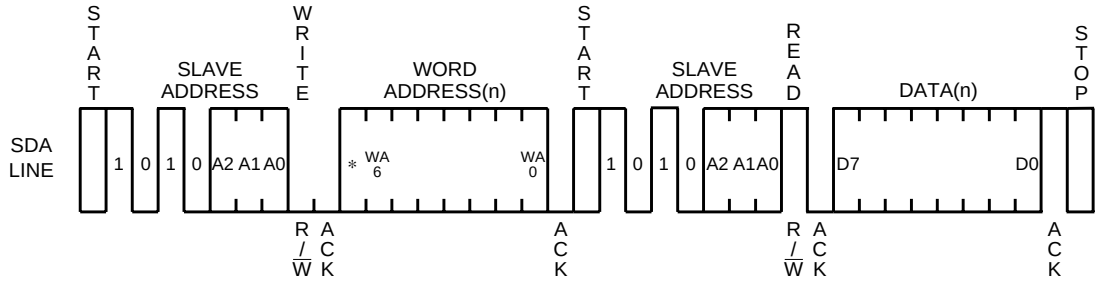


Fig.13

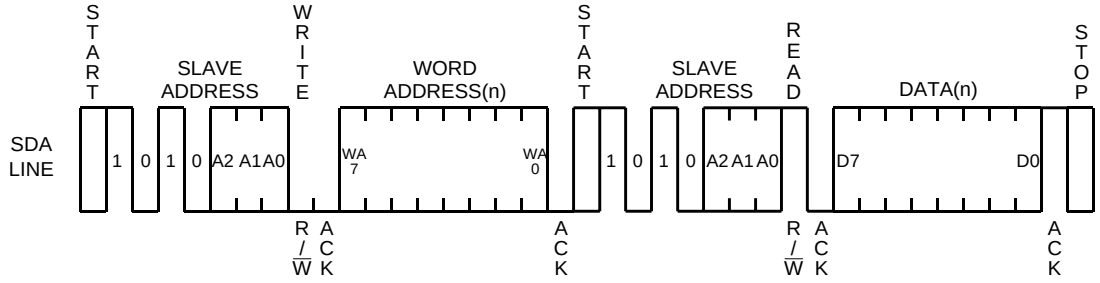


Fig.14

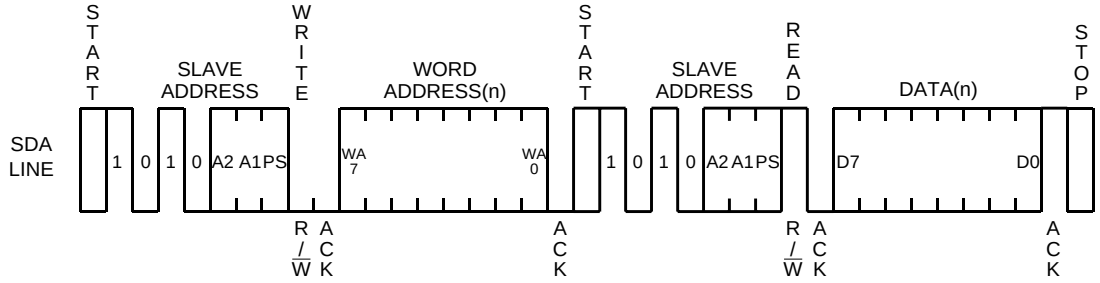


Fig.15

This command can read the designated word address data.

- When an ACK signal LOW is detected after D0 and a stop condition is not sent from the master (μ-COM), the next word address data can be read. [All words all read enabled]
  (See Fig.16 to 18 for the sequential read cycles.)
- This command is ended by inputting a HIGH signal to the ACK signal after D0 and raising the SDA signal (stop condition) by raising SCL to HIGH.

(11) Sequential read cycle (For a current read)

BR24C01A-W / AF-W / AFJ-W / AFV-W

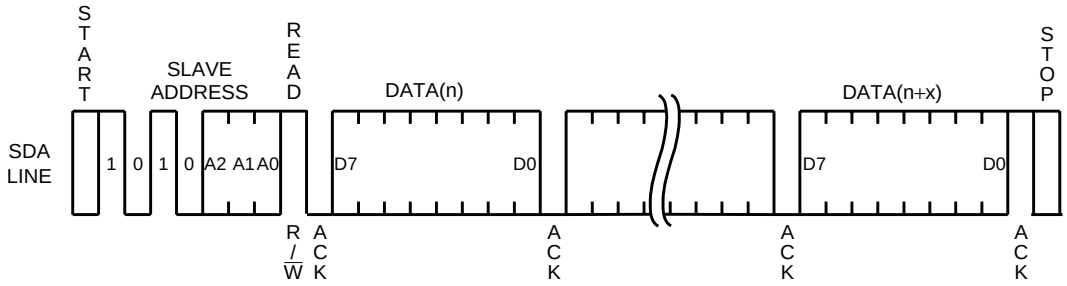


Fig.16

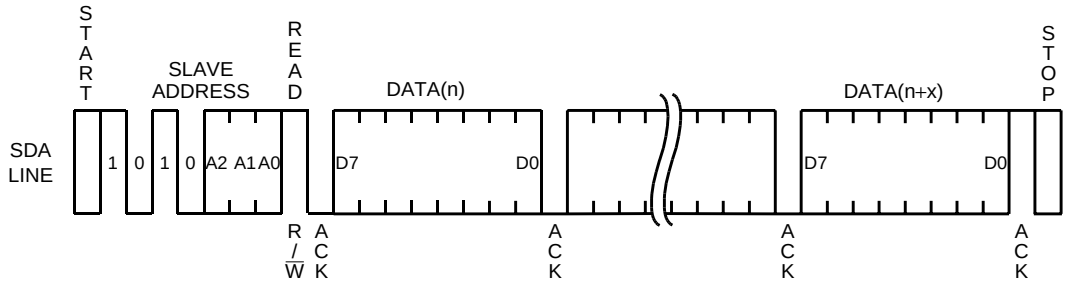


Fig.17

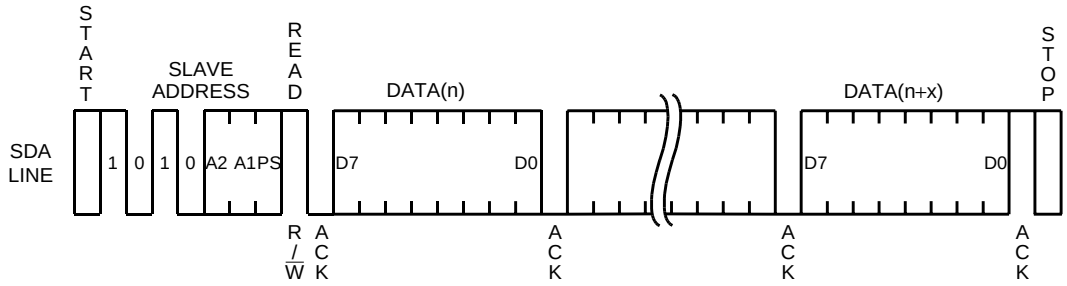


Fig.18

When an ACK signal LOW is detected after D0 and a stop condition is not sent from the master (μ-COM), the next word address data can be read. [All words can be read]

- This command is ended by inputting a HIGH signal to the ACK signal after D0 and raising the SDA signal (stop condition) using the SCL signal HIGH.
- Sequential reading can also be done with a random read.

●Operation notes

(1) During power rise

During power rise, the V_{CC} may rise passing though the low voltage domain in which the IC internal circuit does not work. For this reason, there is a risk of misoperation when the power rises without full IC internal reset.

To prevent this, pay attention to the following points during a power rise.

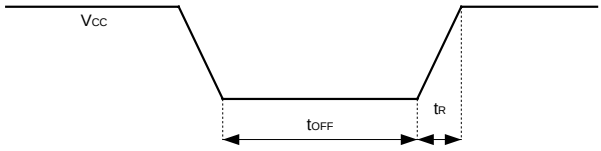
1) Set SCL = SDA = "HIGH"

2) Raise the power so as to active the Power On Reset (P. O. R) circuit.

Follow the steps below as to operate the P. O. R. circuit properly.

1) Set the power rise time (tR) to within 10ms.

2) Set the OFF domain for once power has been cut to 100mS minimum.



The SDA terminal is an open drain output. Consequently, it requires an external pull-up resistance. The appropriate pull-up resistance value is selected from the IC V_{OL}-I_{OL} features., which have been appended as measuring data, as well as V_{IL} and I_{LI} and other personal icons that control the IC in question.

Recommended values 2.0k to 10kW

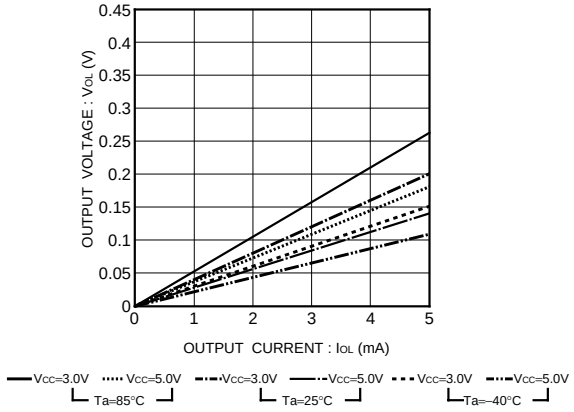
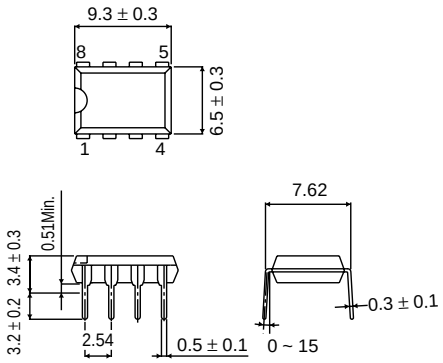


Fig.19 V_{OL}–I_{OL} features (Note : Typ.)

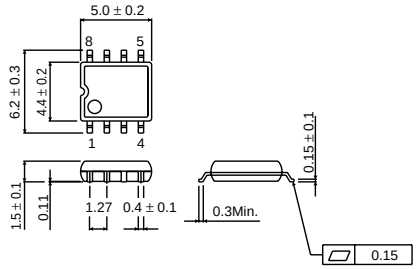
●**External dimensions** (Units : mm)

BR24C01A-W
BR24C02-W
BR24C04-W



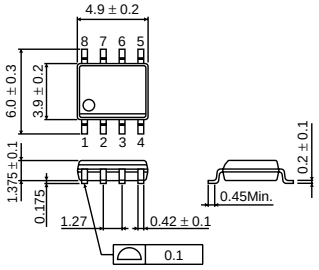
DIP8

BR24C01AF-W
BR24C02F-W
BR24C04F-W



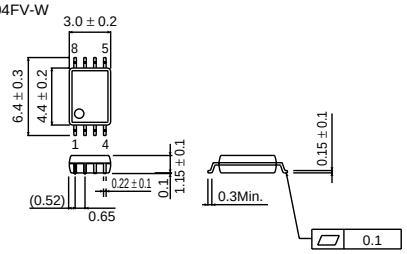
SOP8

BR24C01AFJ-W
BR24C02FJ-W
BR24C04FJ-W



SOP-J8

BR24C01AFV-W
BR24C02FV-W
BR24C04FV-W



SSOP-B8