OptiMOS™2 Power-Transistor

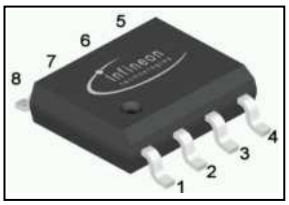
Features

- For fast switching converters and sync. rectification
- Qualified according to JEDEC[1] for target applications
- Super Logic level 2.5V rated; N-channel
- Dual n-channel
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Low on-resistance $R_{DS(on)}$
- Avalanche rated
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product Summary

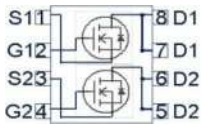
V_{DS}		20	V
$R_{DS(on),max}$	V_{GS}=4.5 V	30	mΩ
	V_{GS}=2.5 V	50	
I_D		6.5	A

PG-DSO-8



RoHS

Halogen-Free



Type	Package	Marking
BSO330N02K	PG-DSO-8	330N2K

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value		Unit
			10 secs	steady state	
Continuous drain current	I_D	V_{gs}=4.5V, T_C=25 °C[2]	6.5	5.4	A
		V_{gs}=4.5V, T_C=70 °C[2]	5.2	4.3	
		V_{gs}=2.5V, T_C=25 °C[2]	5.1	4.2	A
		V_{gs}=2.5V, T_C=70 °C[2]	4	3.3	
Pulsed drain current	$I_{D,pulse}$	T_C=25 °C[3]	26		
Avalanche energy, single pulse	E_{AS}	I_D=6.5 A, R_{GS}=25 Ω	19		mJ
Reverse diode dv/dt	dv/dt	I_D=6.5 A, V_{DS}=20 V, di/dt=200 A/µs, $T_{j,max}$=150 °C	6		kV/µs
Gate source voltage	V_{GS}		±12		V
Power dissipation	P_{tot}	T_A=25 °C[2]	2.0	1.4	W
		T_A=25 °C[1]	2.5		
Operating and storage temperature	T_j, T_{stg}		-55 ... 150		°C
ESD Class			0 (0V to 250V)		
IEC climatic category; DIN IEC 68-1			55/150/56		

Thermal characteristics

Thermal resistance, junction - soldering point	R_{thJS}		-	-	50	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint, t_p≤10 s	-	-	110	
		minimal footprint, steady state	-	-	150	
		6 cm^2 cooling area[2)], t_p≤10 s	-	-	63	
		6 cm^2 cooling area[2)], steady state	-	-	90	

Electrical characteristics, at T_j=25 °C, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	20	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=20 µA	0.7	0.95	1.2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=20 V, V_{GS}=0 V, T_j=25 °C	-	-	1	µA
		V_{DS}=20 V, V_{GS}=0 V, T_j=125 °C	-	-	100	
Gate-source leakage current	I_{GSS}	V_{GS}=12 V, V_{DS}=0 V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=2.5 V, I_D=5.1 A	-	38	50	mΩ
		V_{GS}=4.5 V, I_D=6.5 A	-	24	30	
Gate resistance	R_G		-	1.3	-	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=6.5 A	10	20	-	S

[1)] J-STD20 and JESD22

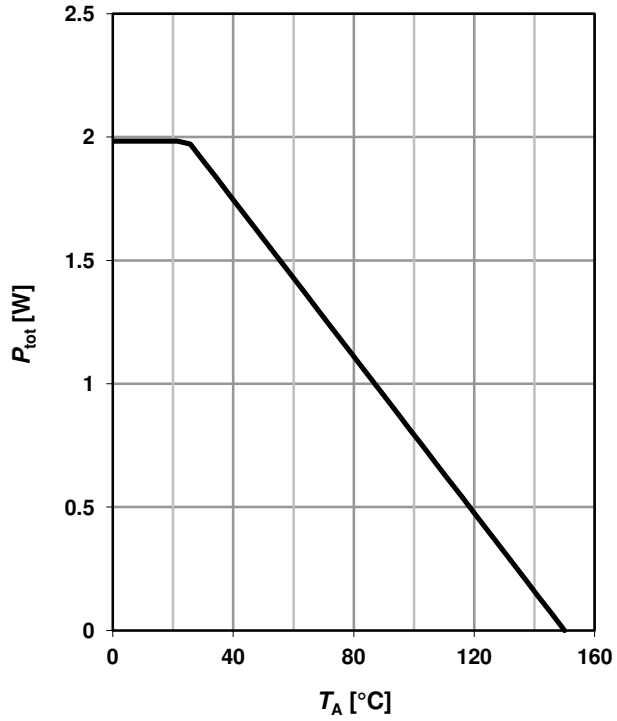
[2)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=10 V, f=1 MHz	-	550	730	pF
Output capacitance	C_{oss}		-	190	250	
Reverse transfer capacitance	C_{rss}		-	26	39	
Turn-on delay time	$t_{d(on)}$	V_{DD}=10 V, V_{GS}=4.5 V, I_D=6.5 A, $R_{G,ext}$=1.6 Ω	-	7.4	-	ns
Rise time	t_r		-	16.8	-	
Turn-off delay time	$t_{d(off)}$		-	13.4	-	
Fall time	t_f		-	2.8	-	
Gate Charge Characteristics[4)]						
Gate to source charge	Q_{gs}	V_{DD}=10 V, I_D=6.5 A, V_{GS}=0 to 4.5 V	-	1.2	1.6	nC
Gate charge at threshold	$Q_{g(th)}$		-	0.5	0.7	
Gate to drain charge	Q_{gd}		-	0.7	1.1	
Switching charge	Q_{sw}		-	1.4	2	
Gate charge total	Q_g		-	3.7	4.9	
Gate plateau voltage	$V_{plateau}$		-	2.2	-	V
Gate charge total, sync. FET	$Q_{g(sync)}$	V_{DS}=0.1 V, V_{GS}=0 to 4.5 V	-	3.4	4.5	nC
Output charge	Q_{oss}	V_{DD}=10 V, V_{GS}=0 V	-	2.6	3.4	
Reverse Diode						
Diode continuous forward current	I_S	T_C=25 °C	-	-	1.5	A
Diode pulse current	$I_{S,pulse}$		-	-	26	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=6.5 A, T_j=25 °C	-	0.88	1.2	V
Reverse recovery time	t_{rr}	V_R=10 V, I_F=6.5 A, di_F/dt=100 A/µs	-	14	-	ns
Reverse recovery charge	Q_{rr}	V_R=10 V, I_F=6.5 A, di_F/dt=100 A/µs	-	4.8	-	nC

[4)] See figure 16 for gate charge parameter definition

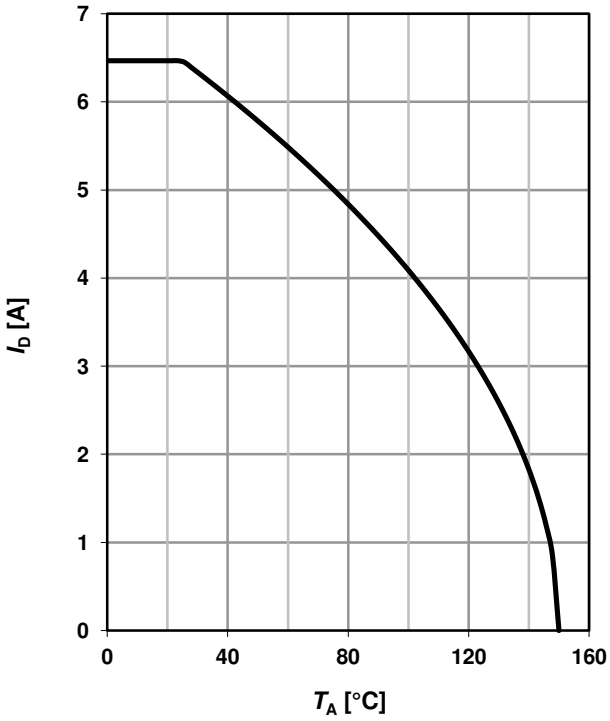
1 Power dissipation

P_{tot}=f(T_A); t_p≤10 s



2 Drain current

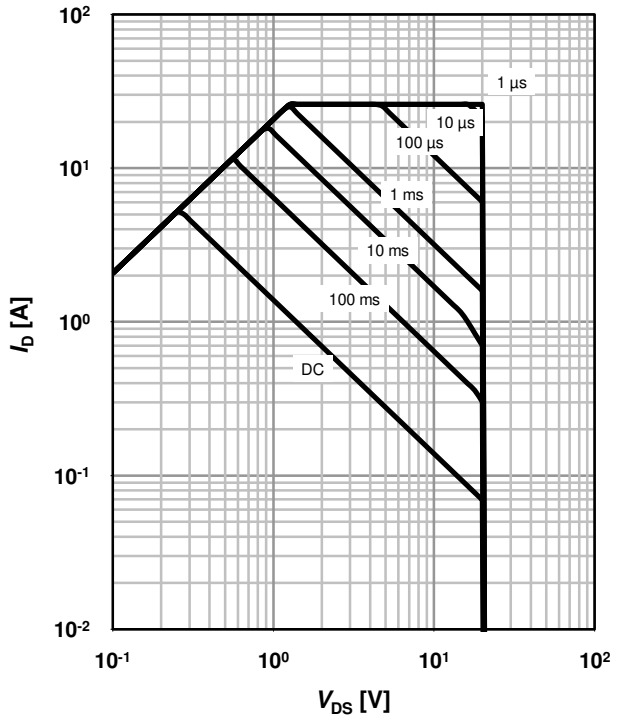
I_D=f(T_A); V_{GS}≥4.5 V; t_p≤10 s



3 Safe operating area

I_D=f(V_{DS}); T_A=25 °C[1]; D=0

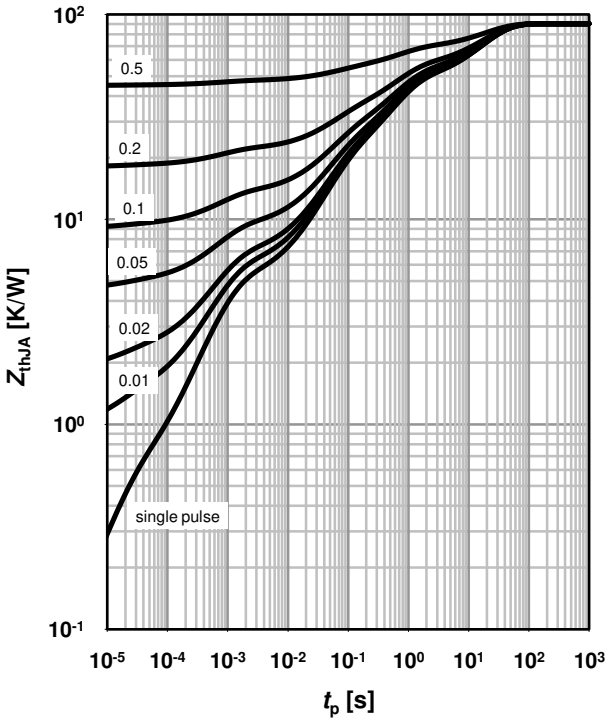
parameter: t_p



4 Max. transient thermal impedance

Z_{thJA}=f(t_p)[2]

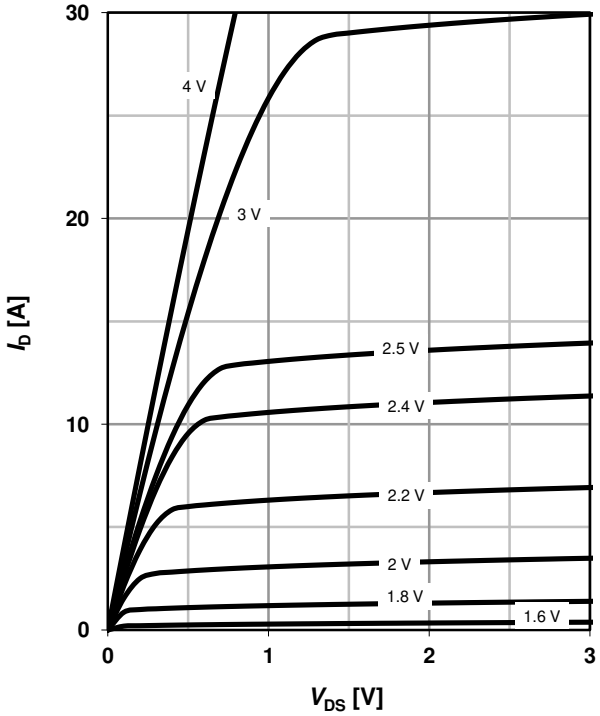
parameter: D=t_p/T



5 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

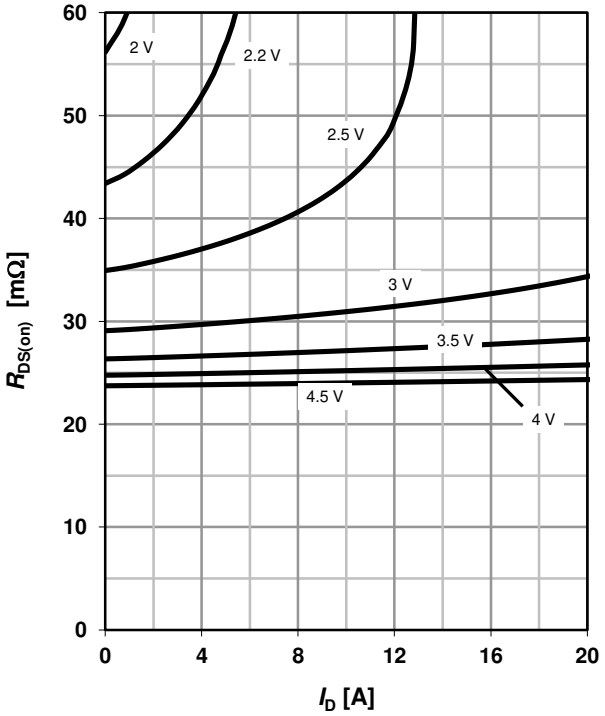
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}$=f(I_D); T_j=25 °C

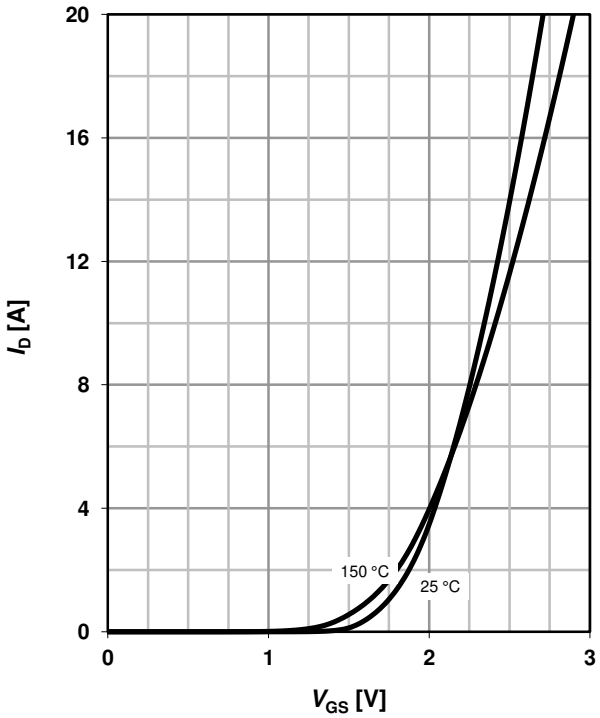
parameter: V_{GS}



7 Typ. transfer characteristics

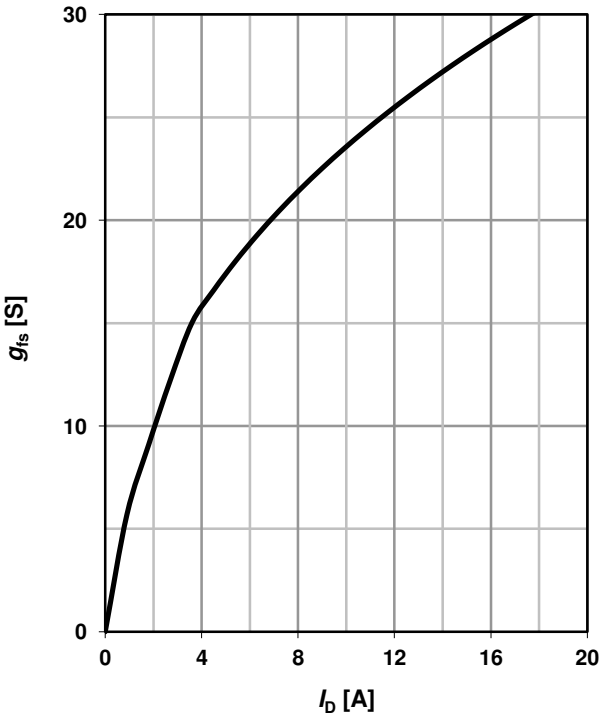
I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$

parameter: T_j



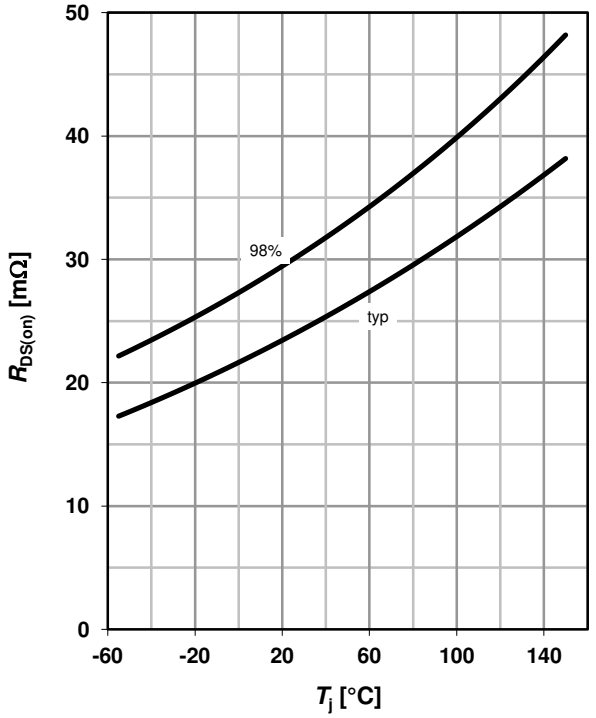
8 Typ. forward transconductance

g_{fs}=f(I_D); T_j=25 °C



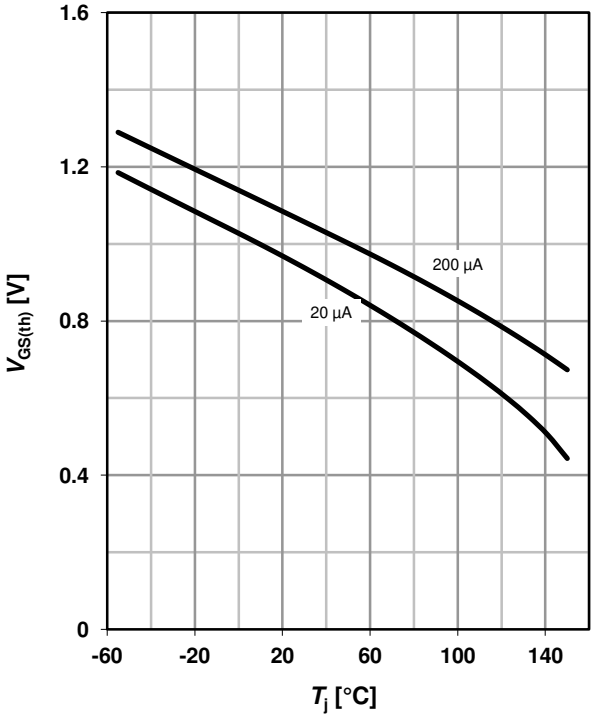
9 Drain-source on-state resistance

$R_{DS(on)}$=f(T_j); I_D=6.5 A; V_{GS}=4.5 V



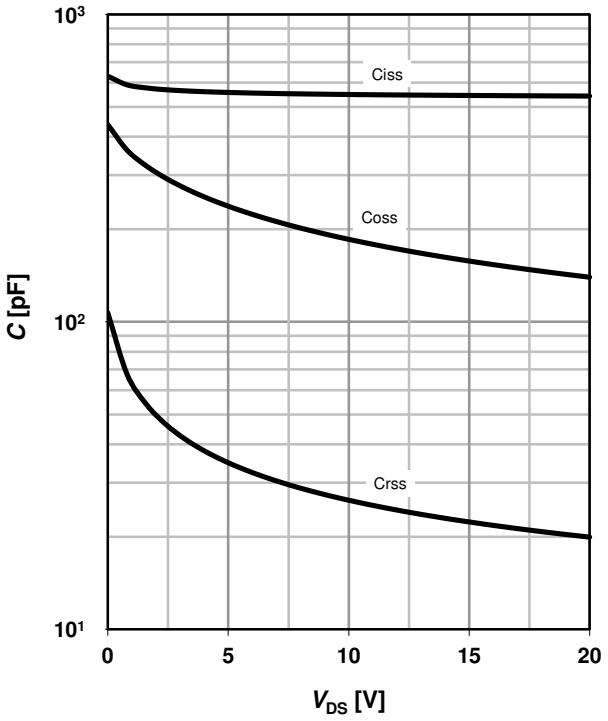
10 Typ. gate threshold voltage

$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}



11 Typ. capacitances

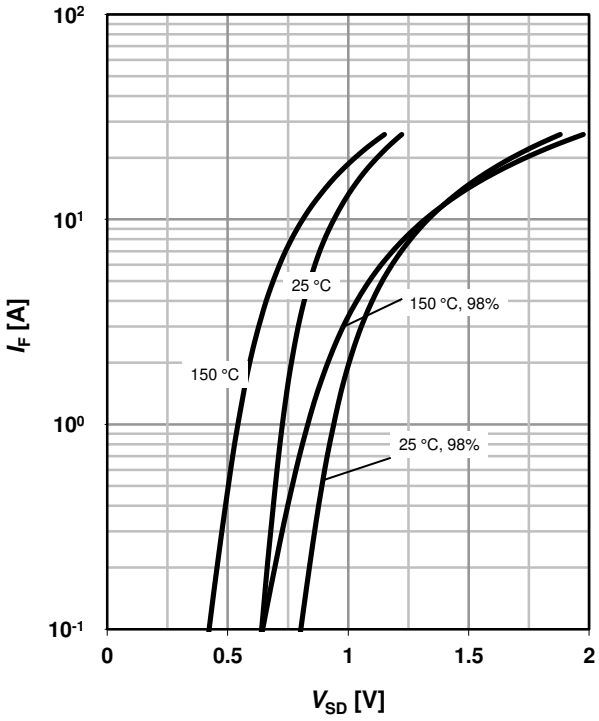
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

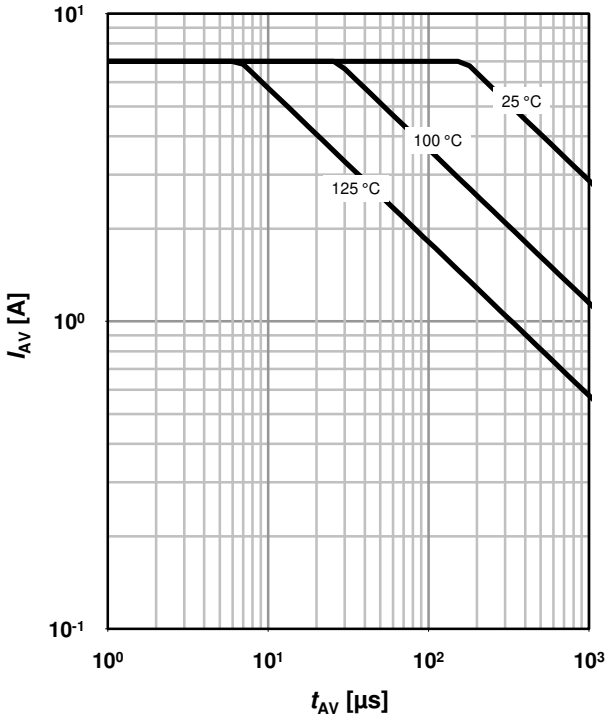
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

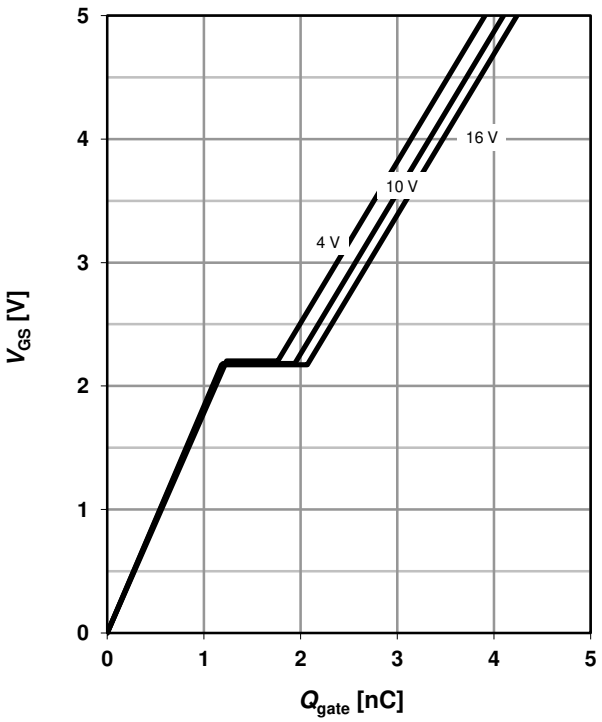
parameter: $T_{j(start)}$



14 Typ. gate charge

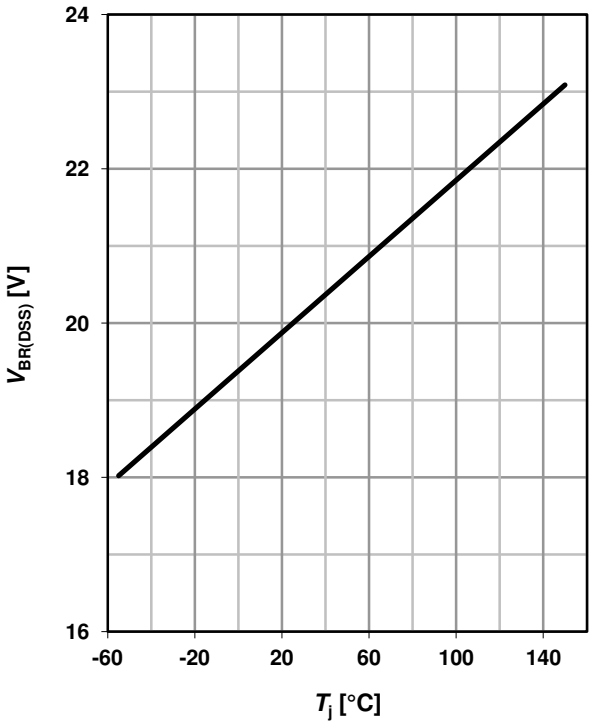
V_{GS}=f(Q_{gate}); I_D=6.5 A pulsed

parameter: V_{DD}

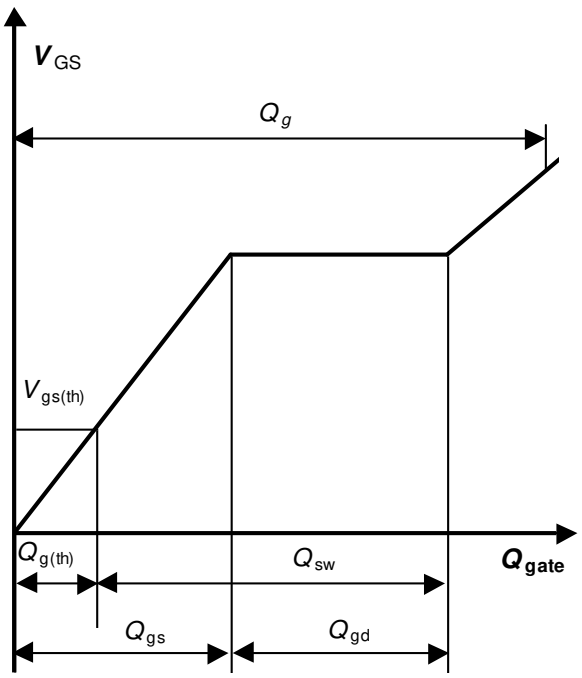


15 Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=1 mA

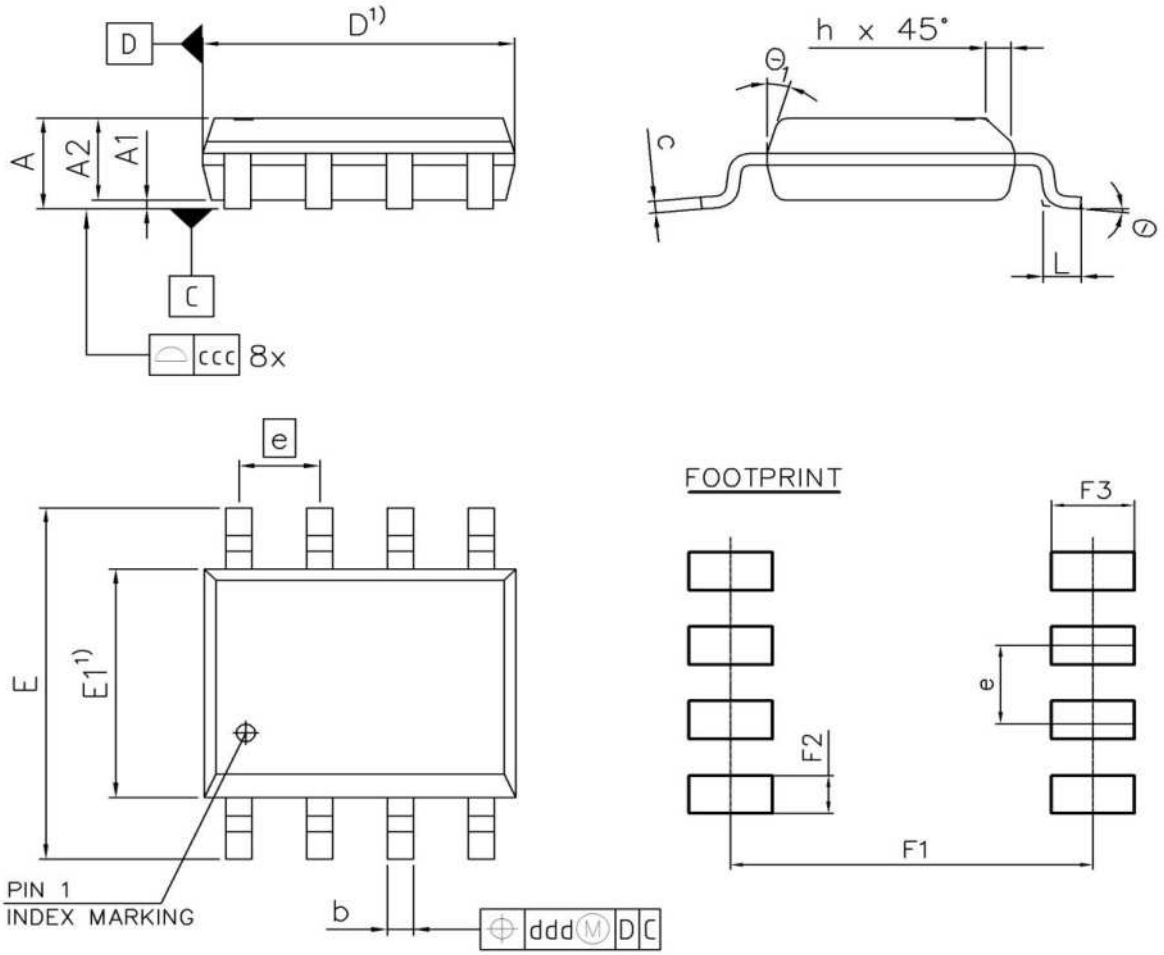


16 Gate charge waveforms



Package Outline **PG-TDSON-8**

PG-DSO-8: Outline



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.75	-	0.069
A1	0.10	-	0.004	-
A2	1.25	1.65	0.049	0.065
b	0.35	0.51	0.014	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27		0.050	
N	8		8	
L	0.39	0.89	0.015	0.035
h	0.23	0.50	0.009	0.020
Θ	0°	8°	0°	8°
Θ1	-	19°	-	19°
ccc	0.10		0.004	
ddd	0.25		0.010	
F1	5.59	5.79	0.220	0.228
F2	0.55	0.75	0.022	0.030
F3	1.21	1.41	0.048	0.056

DOCUMENT NO.
Z8B00003333

SCALE 0 1.0 0 1.0 2mm

EUROPEAN PROJECTION

ISSUE DATE
09.01.2008

REVISION
02

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Infineon Technologies AG
81726 Munich, Germany
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