BVA1761

High Linearity wideband DVGA with addressable function

50MHz - 6000MHz

Device Features

- Integrate DSA to AMP Functionality
- 50-6000MHz Broadband Performance
- Wide VDD Range
  AMP : 3.3V to 5.25V
  DSA : 2.7V to 5.5V
- Low current : 85mA @ 5V, 48mA @ 3.3V
- High Gain
  18.7dB @ 1.9GHz, 17dB @ 3.5GHz (VDD=5V)
  18.2dB @ 1.9GHz, 16.5dB @ 3.5GHz (VDD=3.3V)
- High OP1dB
  20.8dBm @ 1.9GHz, 20.0dBm @ 3.5GHz (VDD=5V)
  17.9dBm @ 1.9GHz, 16.8dBm @ 3.5GHz (VDD=3.3V)
- High OIP3
  36.9dBm @ 1.9GHz, 37.5dBm @ 3.5GHz (VDD=5V)
  33.3dBm @ 1.9GHz, 33.4dBm @ 3.5GHz (VDD=3.3V)
- Noise Figure at max gain setting
  2.1dB @ 1.9GHz, 2.8dB @ 3.5GHz
- Attenuation Range : Up to 31.75dB / 0.25dB step
- Safe attenuation state transitions
- Excellent attenuation accuracy
  ±(0.25 + 3% x ATT) @ 1.9GHz
  ±(0.25 + 5% x ATT) @ 3.5GHz
- Programming modes
  Serial mode only to minimize Control line
- 3bit Addressable function
  LE/DATA/CLK can be shared up to 8EA Chips
- Lead-free/RoHS2-compliant 24-lead 4mm x 4mm x 0.9mm QFN SMT package



24-lead 4mm x 4mm x 0.9mm QFN

Figure 1. Package Type

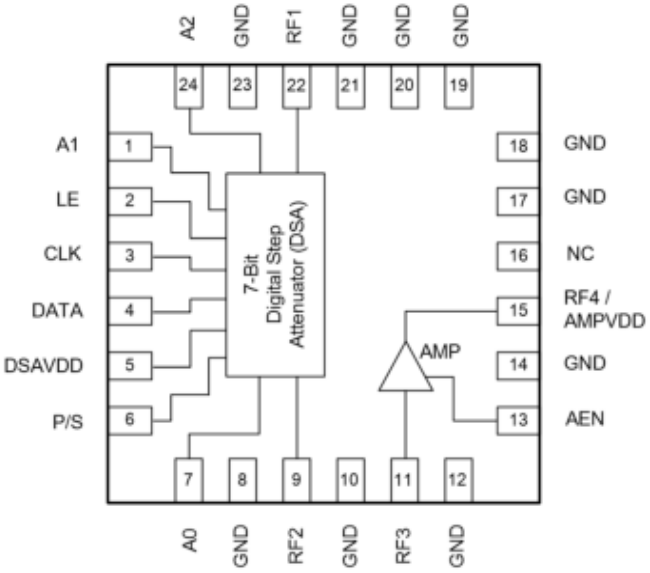


Figure 2. Functional Block Diagram

Product Description

The BVA1761 is a high performance, digitally controlled variable gain amplifier (DVGA) operating from 50MHz to 6GHz.

The BVA1761 integrates a high performance digital step attenuator (DSA) and a high linearity, broadband gain block amplifier operating voltage 3.3V to 5.25V DC within enable control using the small package (4x4mm QFN package).

Both DSA and gain block amplifier in BVA1761 are internally matched to 50 Ohms and It is easy to use with minimum external matching components required.

The BVA1761 can control 7bit attenuation to 0.25dB step up to 31.75dB and initialize to the maximum attenuation setting on power-up until next programming word is inputted.
In addition, Internal DSA has a 3-bit addressable function, so it can share up to 8 DSA's Latch Enable(LE), DATA and CLOCK(CLK) pin. This has the advantage of reducing the number of IO pins when using multiple DSA or DVGA chip with addressable function.

The BVA1761 is targeted for use in wireless infrastructure, point-to-point, or can be used for any general purpose wireless application.

Application

- 5G/4G/3G Wireless infrastructure and other high performance RF application
- Microwave and Satellite Radio
- General purpose Wireless

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Table 1. Electrical Specifications[1] @ VDD = 5V

Parameter		Condition	Min	Typ	Max	Unit
Operational Frequency Range			50		6000	MHz
Gain[2]		ATT = 0dB @ 3500MHz		17		dB
Attenuation Control range		0.25dB Step		0 - 31.75		dB
Attenuation Step				0.25		dB
Attenuation Accuracy	0.05GHz - 1GHz	Any bit or bit combination			±(0.25 + 2% of ATT setting)	dB
	1GHz - 2GHz				±(0.25 + 3% of ATT setting)	
	2GHz - 3GHz				±(0.25 + 3% of ATT setting)	
	3GHz - 4GHz				±(0.25 + 5% of ATT setting)	
	4GHz - 5GHz				±(0.25 + 5% of ATT setting)	
	5GHz - 6GHz				±(0.25 + 5% of ATT setting)	
Input Return loss	0.05GHz - 2GHz	ATT = 0dB	-9	-11		dB
	2GHz - 4GHz		-11	-14		
	4GHz - 6GHz		-12	-15		
Output Return loss	0.05GHz - 2GHz	ATT = 0dB	-12	-14		dB
	2GHz - 4GHz		-12	-15		
	4GHz - 6GHz		-8	-12		
Output Power for 1dB Compression		ATT = 0dB @ 3500MHz		20		dBm
Output Third Order Intercept Point[3]		ATT = 0dB @ 3500MHz		37.5		dBm
Noise Figure		ATT = 0dB @ 3500MHz		2.8		dB
DSA Switching time		50% CTRL to 90% or 10% RF		500	800	ns
AMP Switching time		50% CTRL to 90% or 10% RF		150		ns
Maximum Spurious level		Measured @ DSA RF1, RF2 ports		< -145		dBm
Impedance				50		Ω

1. Device performance _ measured on a BeRex Evaluation board at 25°C, 50 Ω system, VDD=+5.0V, measure on Evaluation Board (DSA to AMP)
2. Gain data has PCB & Connectors insertion loss de-embedded
3. OIP3 _ measured with two tones at an output of 0dBm per tone separated by 1MHz.

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Table 2. Electrical Specifications[1] @ VDD = 3.3V

Parameter		Condition	Min	Typ	Max	Unit
Operational Frequency Range			50		6000	MHz
Gain[2]		ATT = 0dB @ 3500MHz		16.5		dB
Attenuation Control range		0.25dB Step		0 - 31.75		dB
Attenuation Step				0.25		dB
Attenuation Accuracy	0.05GHz - 1GHz	Any bit or bit combination			±(0.25 + 2% of ATT setting)	dB
	1GHz - 2GHz				±(0.25 + 3% of ATT setting)	
	2GHz - 3GHz				±(0.25 + 3% of ATT setting)	
	3GHz - 4GHz				±(0.25 + 5% of ATT setting)	
	4GHz - 5GHz				±(0.25 + 5% of ATT setting)	
	5GHz - 6GHz				±(0.25 + 5% of ATT setting)	
Input Return loss	0.05GHz - 2GHz	ATT = 0dB	-9	-11		dB
	2GHz - 4GHz		-10	-14		
	4GHz - 6GHz		-12	-15		
Output Return loss	0.05GHz - 2GHz	ATT = 0dB	-12	-15		dB
	2GHz - 4GHz		-12	-15		
	4GHz - 6GHz		-8	-12		
Output Power for 1dB Compression		ATT = 0dB @ 3500MHz		16.8		dBm
Output Third Order Intercept Point[3]		ATT = 0dB @ 3500MHz		33.4		dBm
Noise Figure		ATT = 0dB @ 3500MHz		2.8		dB
DSA Switching time		50% CTRL to 90% or 10% RF		500	800	ns
AMP Switching time		50% CTRL to 90% or 10% RF		150		ns
Maximum Spurious level		Measured @ DSA RF1, RF2 ports		< -145		dBm
Impedance				50		Ω

1. Device performance _ measured on a BeRex Evaluation board at 25°C, 50 Ω system, VDD=+3.3V, measure on Evaluation Board (DSA to AMP)
2. Gain data has PCB & Connectors insertion loss de-embedded
3. OIP3 _ measured with two tones at an output of 0dBm per tone separated by 1MHz.

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Table 3. Typical RF Performance (VDD = 5.0V)[1]

Parameter	Frequency								Unit
	70[3]	900[4]	1800[5]	2140[5]	2650[5]	3500[6]	4650[7]	5800[8]	MHz
Gain[9]	20.9	20.0	18.7	18.6	18.0	17.0	16.0	15.3	dB
S11	-9.7	-14.1	-11.9	-14.6	-17.3	-11.0	-12.9	-16.4	dB
S22	-16.1	-15.9	-12.3	-17.8	-13.8	-13.3	-14.5	-9.9	dB
OIP3[10]	35.6	37.5	36.9	36.8	36.9	37.5	36.4	34.2	dBm
P1dB	20.8	21.8	20.9	20.6	20.6	20	19.2	17.4	dBm
Noise Figure	1.6	2.0	2.1	2.3	2.3	2.8	3.3	3.7	dB

Table 4. Typical RF Performance (VDD = 3.3V)[2]

Parameter	Frequency								Unit
	70[3]	900[4]	1800[5]	2140[5]	2650[5]	3500[6]	4650[7]	5800[8]	MHz
Gain[9]	20.4	19.6	18.2	18.1	17.5	16.5	15.4	14.8	dB
S11	-9.1	-13.1	-11.2	-13.4	-15.7	-10.5	-11.9	-15.3	dB
S22	-14.9	-15.4	-12.6	-17.1	-12.5	-14.0	-12.9	-7.5	dB
OIP3[10]	31.0	33.1	33.3	33.4	33.0	33.4	34.1	28.7	dBm
P1dB	17.5	18.6	18.0	17.5	17.8	16.8	16.6	14.2	dBm
Noise Figure	1.6	2.0	2.1	2.3	2.4	2.8	3.4	3.8	dB

1. Device performance _ measured on a BeRex evaluation board at 25°C, VDD=+5.0V, 50 Ω system. (DSA to AMP)
2. Device performance _ measured on a BeRex evaluation board at 25°C, VDD=+3.3V, 50 Ω system. (DSA to AMP)
3. 70MHz measured with application circuit refer to table 11.
4. 900MHz measured with application circuit refer to table 14.
5. 1800MHz, 2140MHz, 2650MHz measured with application circuit refer to table 17.
6. 3500MHz measured with application circuit refer to table 20.
7. 4650MHz measured with application circuit refer to table 23.
8. 5800MHz measured with application circuit refer to table 26.
9. Gain data has PCB & Connectors insertion loss de-embedded.
10. OIP3 measured with two tones at an output of 0dBm per tone separated by 1MHz

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Table 5. Absolute Maximum Ratings

Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage	AMP / DSA			5.5 / 5.5	V
Supply Current	AMP			190	mA
	DSA			1000	uA
Digital input voltage	AMP Control Pin (AEN)	-0.3		5.25	V
	DSA Control Pin (LE, DATA, CLK, P/S, A0, A1, A2)	-0.3		3.6	V
Maximum input power	AMP / DSA			0.5	dBm
Storage Temperature		-55		150	℃
Junction Temperature			150		℃

Operation of this device above any of these parameters may result in permanent damage.

Table 6. Recommended Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
Frequency Range	DSA + AMP	50		6000	MHz
Supply Voltage, VDD	AMP VDD	3.3	5	5.25	V
	DSA VDD	2.7		5.5	V
Current, IDD	AMP ON @ VDD=5V	66	83	100	mA
	AMP ON @ VDD=3.3V	39	48	57	mA
	AMP OFF			7	mA
	DSA	100	200	300	uA
AMP Control Voltage [AEN]	AMP ON	0		0.6	V
	AMP OFF	1.17		VDD	V
AEN pin Current	AMP OFF		150		uA
DSA Control Voltage	Digital Input High	1.17		3.6	V
	Digital Input Low	-0.3		0.6	V
DSA Control pin Current	Digital Input High			20	uA
Operating Temperature	DSA + AMP	-40		105	℃

Specifications are not guaranteed over all recommended operating conditions.

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Figure 3. Pin Configuration (Top View)

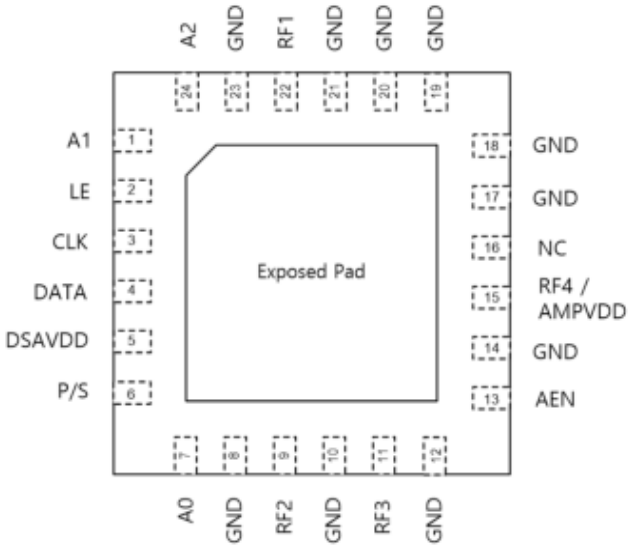


Table 7. Pin Description

Pin	Pin name	Description
1	A1	Address bit A1 connection.
2	LE	Latch Enable input
3	CLK	Serial interface clock input
4	DATA	Serial interface data input
5	DSAVDD	DSA Power Supply input
6	P/S	Serial Mode Select. This pin have to be set to HIGH.
7	A0	Address bit A0 connection.
9	RF2[1]	DSA output port (Attenuator RF Output) This pin should be connected to RF3(Pin 11) with DC blocking capacitor.
11	RF3	Amplifier RF Input This pin should be connected to RF2(Pin 9) with DC blocking capacitor.
13	AEN	Amplifier Enable input. Amplifier is enabled when this pin is set to Low .
15	RF4 / AMPVDD	Amplifier RF Output & Amplifier power supply input This pin is a final RF output port. (DSA + Amp structure)
22	RF1[1]	DSA input port (Attenuator RF Input) This pin is a main RF input port. (DSA + Amp structure)
24	A2	Address bit A2 connection.
8, 10, 12, 14, 17, 18, 19, 20, 21, 23	GND	Ground, These pins must be connected to ground
16	NC	

Note: 1. The RF pins do not require DC blocking capacitors for proper Operation if the 0V DC requirement is met.

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Programming Options

The BDA1761 is programmed to operate only in serial mode.
It operates in serial mode when the P/S pin is High, and when P/S pin is low, the internal DSA is fixed as Max attenuation(31.75dB), so the P/S pin must be set to High to use the serial mode.

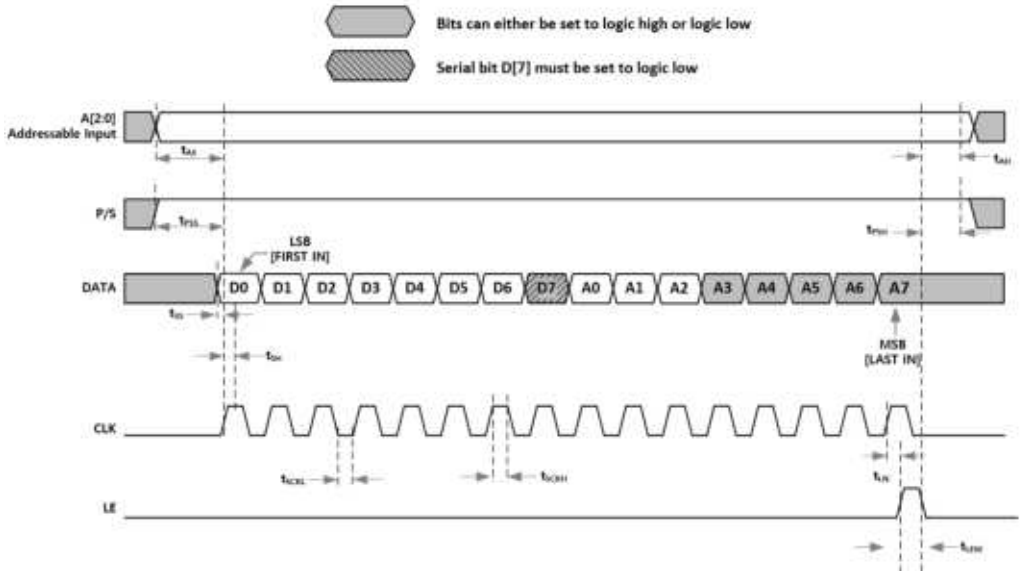
Serial Control Mode

The serial interface is a 7-bit shift register to shift in the data LSB (D0) first. It is controlled by three CMOS-compatible signals: DATA, CLK, and Latch Enable (LE).

Table 8. Truth Table for Serial Control Word

Digital Control Input								Attenuation state (dB)
D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	
LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	0
LOW	LOW	LOW	LOW	LOW	LOW	LOW	**HIGH**	0.25
LOW	LOW	LOW	LOW	LOW	LOW	**HIGH**	LOW	0.5
LOW	LOW	LOW	LOW	LOW	**HIGH**	LOW	LOW	1.0
LOW	LOW	LOW	LOW	**HIGH**	LOW	LOW	LOW	2.0
LOW	LOW	LOW	**HIGH**	LOW	LOW	LOW	LOW	4.0
LOW	LOW	**HIGH**	LOW	LOW	LOW	LOW	LOW	8.0
LOW	**HIGH**	LOW	LOW	LOW	LOW	LOW	LOW	16.0
LOW	**HIGH**	**HIGH**	**HIGH**	**HIGH**	**HIGH**	**HIGH**	**HIGH**	31.75

Figure 4. Serial Mode Timing Diagram



The serial interface is a 16-bit shift register made up of two words. The first 8-bit word is the Attenuation word, which controls the DSA state.

The second word is the address word, which uses only 3 of 8-bits that must match the hard wired A0-A2 programming in order to change the DSA state. If no external connections are made to A0 – A2 then internally they will default to 000 due to internal pull down resistors.

If these 3 external preset address bits are not matched with the SPI loaded address bits then the current attenuator state will remain unchanged.

This allows up to 8 serial-controlled devices to be used on a single board, which share a common DATA, CLK and LE**. (Figure 5)**

Table 9. Serial Interface Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{CLK}	Serial data clock frequency			10	MHz
t_{AS}	Address setup time	100			ns
t_{AH}	Address hold time	100			ns
t_{PSS}	P/S setup time	100			ns
t_{PSH}	P/S hold time	100			ns
t_{SS}	Serial Data setup time	10			ns
t_{SH}	Serial Data hold time	10			ns
t_{SCKH}	Serial clock high time	30			ns
t_{SCKL}	Serial clock low time	30			ns
t_{LN}	LE setup time	10			ns
t_{LEW}	Minimum LE pulse width	30			ns

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Figure 5. Multi Device Addressing Scheme using SPI

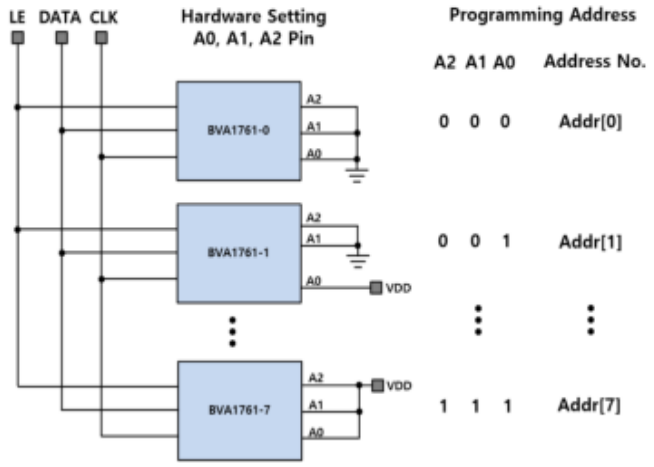


Table 10. Truth Table for Address Control Word

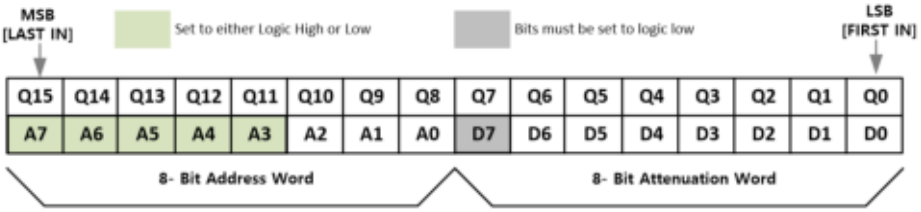
Address Digital Control Input								Address Setting	Addr No.
A7 (MSB)	A6	A5	A4	A3	A2	A1	A0 (LSB)		
X	X	X	X	X	LOW	LOW	LOW	000	Addr[0]
X	X	X	X	X	LOW	LOW	**HIGH**	001	Addr[1]
X	X	X	X	X	LOW	**HIGH**	LOW	010	Addr[2]
X	X	X	X	X	LOW	**HIGH**	**HIGH**	011	Addr[3]
X	X	X	X	X	**HIGH**	LOW	LOW	100	Addr[4]
X	X	X	X	X	**HIGH**	LOW	**HIGH**	101	Addr[5]
X	X	X	X	X	**HIGH**	**HIGH**	LOW	110	Addr[6]
X	X	X	X	X	**HIGH**	**HIGH**	**HIGH**	111	Addr[7]

Serial Register Map

The BVA1761 can be programmed via the serial control on the rising edge of Latch Enable (LE) which loads the last 8-bits attenuation word and 8-bits address word in the SHIFT Register. Data is clocked in LSB(D0) first.

The shift register must be loaded while LE is kept LOW to prevent changing the attenuation value during data is inputted.

Figure 6. Serial Register Map



The serial register consist of 16 bits as shown in Figure 6. First 8 bits from LSB are Attenuation word, 8 bits after that are Address word. The Attenuation word is DSA attenuation control bit and the Address word is static logical bit determined by A0, A1 and A2 digital inputs. The attenuation word is derived directly from the value of the attenuation state. To find the attenuation word, multiply the value of the state by four because of 0.25dB step up to 31.75dB (total 127 Attenuation state), then convert to binary.

For example, to program attenuation 15.75dB state of Addr[5] BVA1761 :

Attenuation State	Address state
4 x 15.75 = 63	Digital input of A2, A1, A0 pin = 101
63 -> 00111111	A7 - A0 : xxxxx101

Serial DATA Input : xxxxx10100111111

x	x	x	x	x	1	0	1	0	0	1	1	1	1	1	1
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

Power-Up state Settings

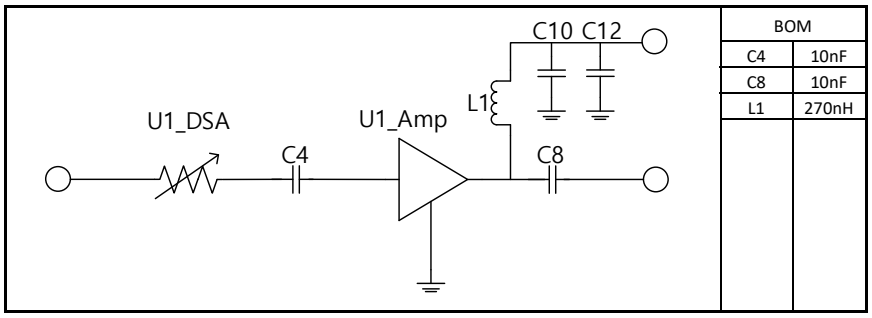
The BVA1761 will always initialize to the minimum Gain state (Max Attenuation = 31.75dB) on power-up and will remain in this setting until the user latches in the next programming word.

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Typical RF Performance Plot - BVA1761 EVK - PCB (Application Circuit : 50 ~ 500MHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 11

Table 11. 50 ~ 500MHz IF Application Circuit



This value can be changed little by little according to the frequency band and bandwidth.

Table 12. Typical IF Performance @ VDD = 5V

Parameter	Frequency			Unit
	70	200	500	MHz
Gain[1]	20.9	20.9	20.6	dB
S11	-9.7	-15.3	-15.2	dB
S22	-16.1	-22.5	-20.1	dB
OIP3[2]	35.6	37.2	37.0	dBm
P1dB	20.8	21.9	21.9	dBm
Noise Figure	1.6	1.7	1.7	dB

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 _ measured with two tones at an output of 0 dBm per tone separated by 1 MHz.

Table 13. Typical IF Performance @ VDD = 3.3V

Parameter	Frequency			Unit
	70	200	500	MHz
Gain[1]	20.4	20.5	20.2	dB
S11	-9.1	-14.1	-13.9	dB
S22	-14.9	-20.2	-17.9	dB
OIP3[2]	31.0	32.9	32.8	dBm
P1dB	17.5	18.7	18.7	dBm
Noise Figure	1.6	1.6	1.8	dB

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 _ measured with two tones at an output of 0 dBm per tone separated by 1 MHz.

Figure 7. Gain vs. Frequency @ VDD = 5V
over Temperature

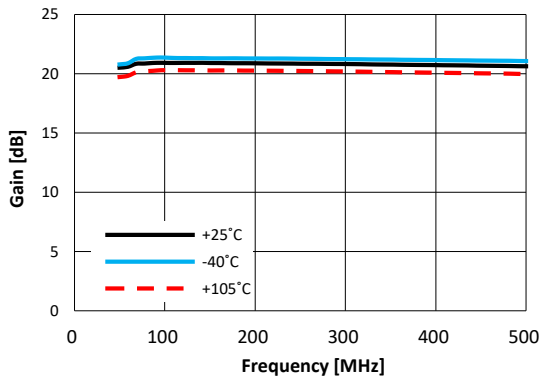
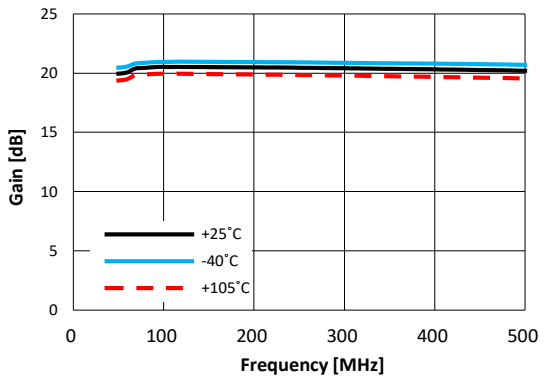


Figure 8. Gain vs. Frequency @ VDD = 3.3V
over Temperature



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Typical RF Performance Plot - BVA1761 EVK - PCB (Application Circuit:50 ~ 500MHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 11

Figure 9. Gain vs. Frequency
over Major Attenuation States

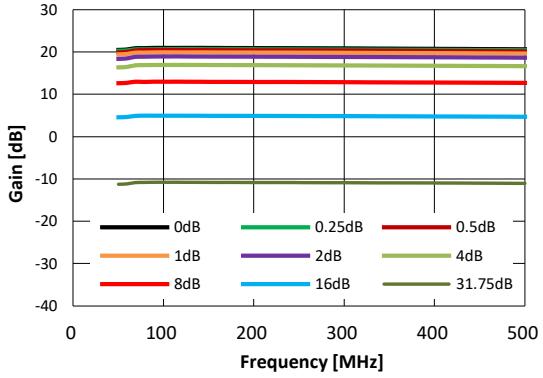


Figure 10. Gain vs. Frequency vs VDD
Max Gain States

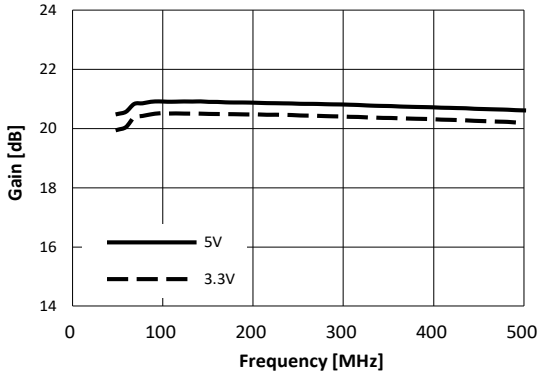


Figure 11. Input Return Loss vs. Frequency
over Temperature (Min[1] / Max Gain State)

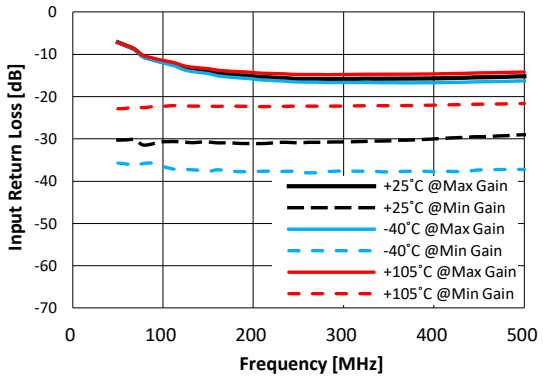
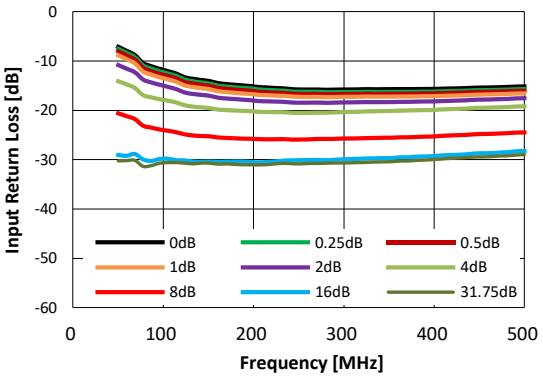


Figure 12. Input Return Loss vs. Frequency
Over Major Attenuation States



1.Min Gain was measured in the state is set with attenuation 31.75dB.

Figure 13. Output Return Loss vs. Frequency
over Temperature (Min[1] / Max Gain State)

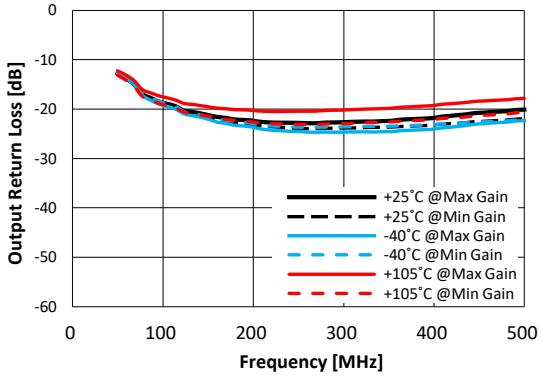
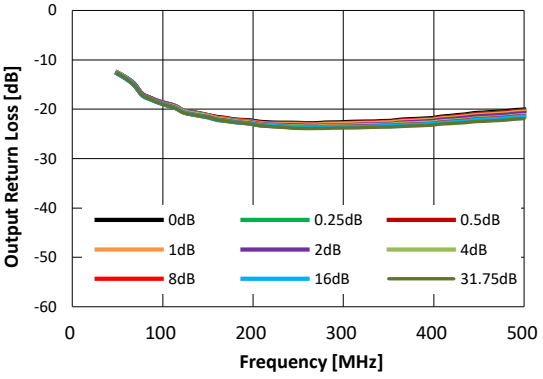


Figure 14. Output Return Loss vs. Frequency
over Major Attenuation States



1.Min Gain was measured in the state is set with attenuation 31.75dB.

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Typical RF Performance Plot - BVA1761 EVK - PCB (Application Circuit:50 ~ 500MHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 11

Figure 15. OIP3 vs. Frequency vs. VDD
Over Temperature (Max Gain State)

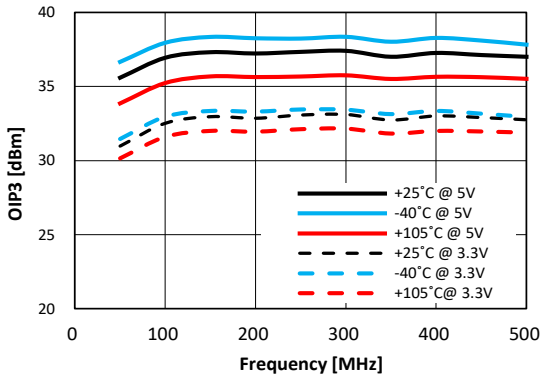


Figure 16. OIP3 vs. Frequency vs VDD
Over Temperature (15.75dB Attenuation State)

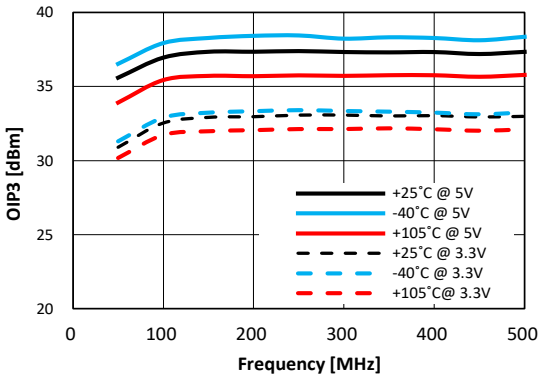


Figure 17. P1dB vs. Frequency vs VDD
Over Temperature (Max Gain State)

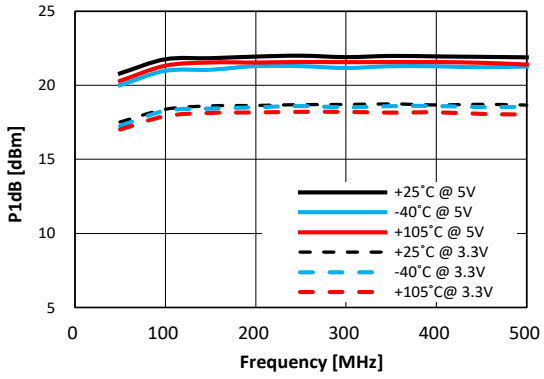


Figure 18. Noise Figure vs. Frequency @ VDD = 5V
Over Temperature (Max Gain State)

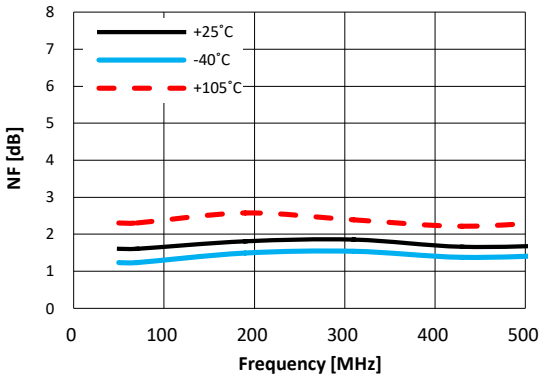
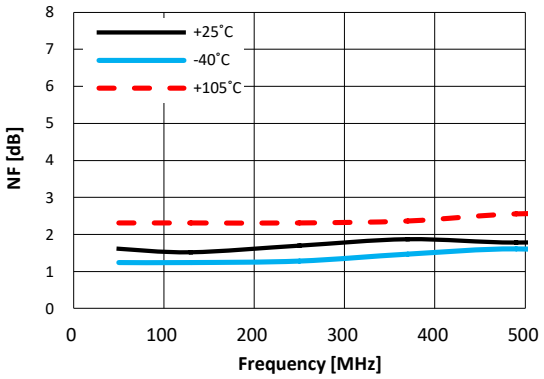


Figure 19. Noise Figure vs. Frequency @ VDD = 3.3V
Over Temperature (Max Gain State)



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Typical RF Performance Plot - BVA1761 EVK - PCB (Application Circuit:50 ~ 500MHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 11

Figure 20. Attenuation Error vs Frequency
over Major Attenuation Steps

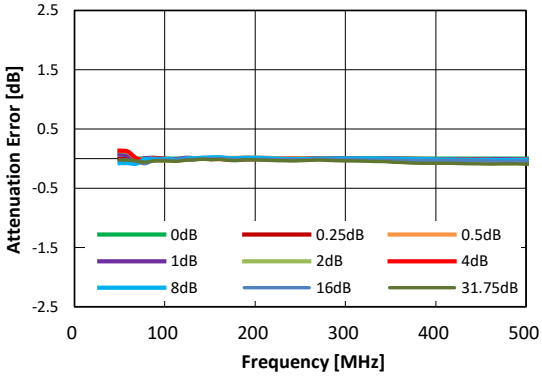


Figure 21. Attenuation Error vs Attenuation Setting
over Major Frequency

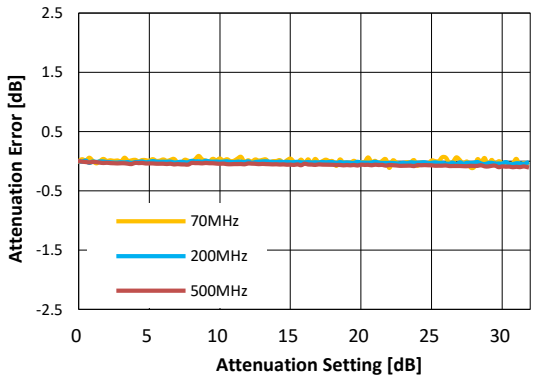


Figure 22. Attenuation Error at 70MHz vs Temperature
Over All Attenuation States

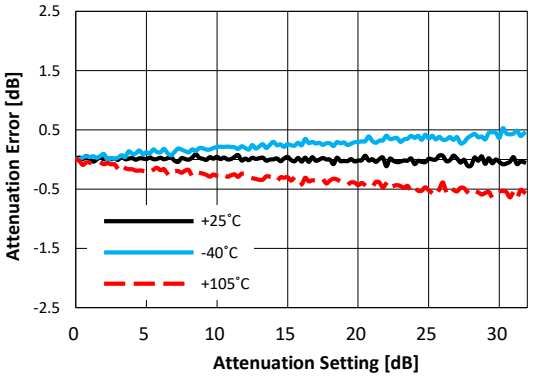


Figure 23. Attenuation Error at 200MHz vs Temperature
Over All Attenuation States

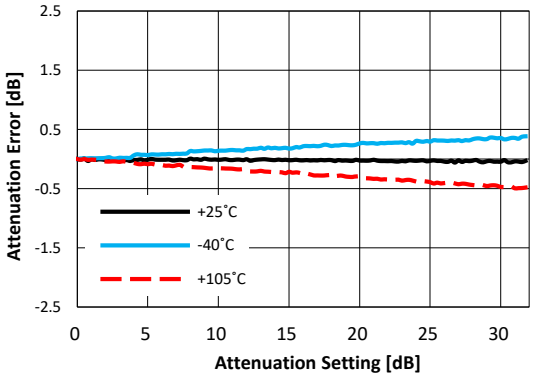
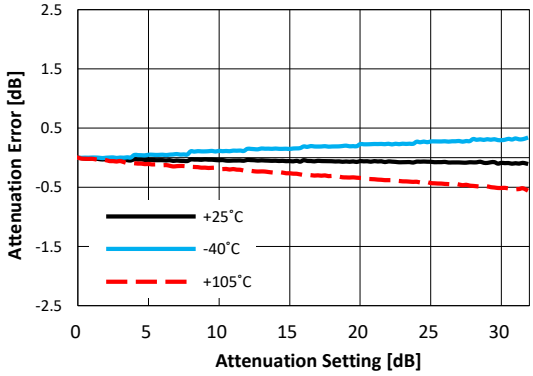


Figure 24. Attenuation Error at 500MHz vs Temperature
Over All Attenuation States

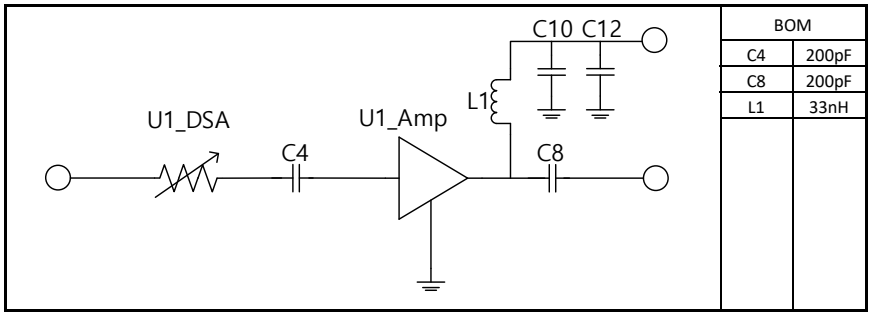


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Typical RF Performance Plot - BVA1761 EVK - PCB (Application Circuit:700 ~ 1000MHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 14

Table 14. 700 ~ 1000MHz RF Application Circuit



BOM	
C4	200pF
C8	200pF
L1	33nH

This value can be changed little by little according to the frequency band and bandwidth.

Table 15. Typical RF Performance @ VDD = 5V

Parameter	Frequency			Unit
	700	800	900	MHz
Gain[1]	20.2	20.1	20.0	dB
S11	-13.6	-14.0	-14.1	dB
S22	-14.4	-15.3	-15.9	dB
OIP3[2]	37.7	37.7	37.5	dBm
P1dB	21.9	21.8	21.8	dBm
Noise Figure	1.9	1.9	2.0	dB

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 _ measured with two tones at an output of 0 dBm per tone separated by 1 MHz.

Table 16. Typical RF Performance @ VDD = 3.3V

Parameter	Frequency			Unit
	700	800	900	MHz
Gain[1]	19.7	19.6	19.6	dB
S11	-12.7	-13.0	-13.1	dB
S22	-14.2	-15.0	-15.4	dB
OIP3[2]	33.1	33.4	33.1	dBm
P1dB	18.6	18.7	18.6	dBm
Noise Figure	1.9	1.9	2.0	dB

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 _ measured with two tones at an output of 0 dBm per tone separated by 1 MHz.

Figure 25. Gain vs. Frequency @ VDD = 5V
over Temperature

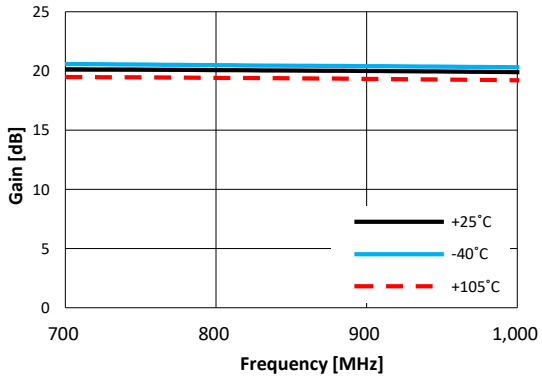
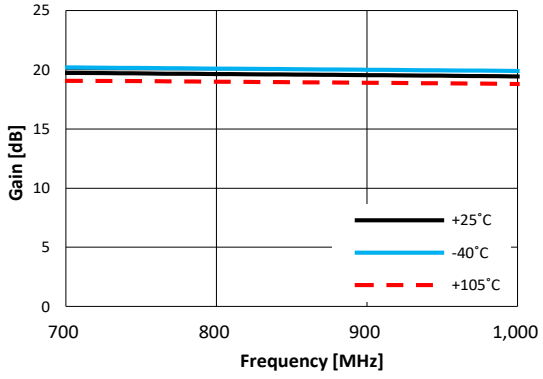


Figure 26. Gain vs. Frequency @ VDD = 3.3V
over Temperature



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Typical RF Performance Plot - BVA1761 EVK - PCB (Application Circuit:700 ~ 1000MHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 14

Figure 27. Gain vs. Frequency
over Major Attenuation States

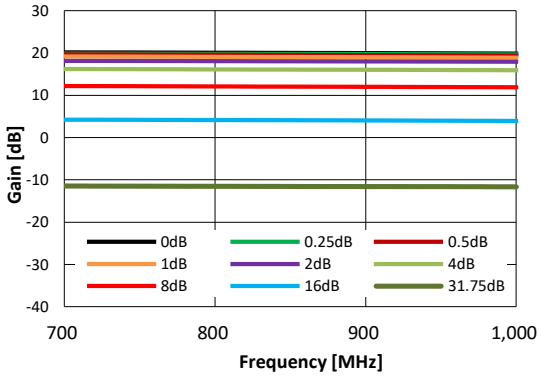


Figure 28. Gain vs. Frequency vs VDD
Max Gain States

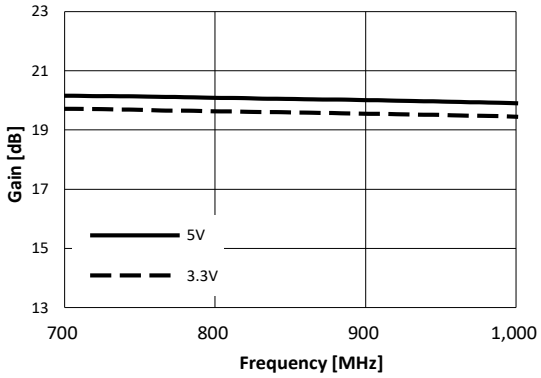


Figure 29. Input Return Loss vs. Frequency
over Temperature (Min[1] / Max Gain State)

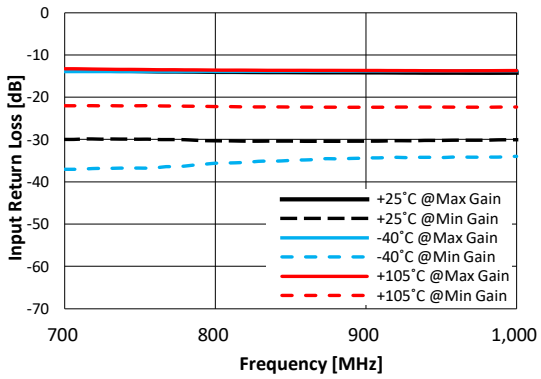
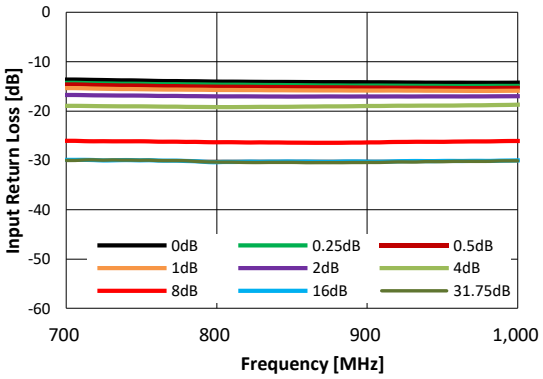


Figure 30. Input Return Loss vs. Frequency
Over Major Attenuation States



1.Min Gain was measured in the state is set with attenuation 31.75dB.

Figure 31. Output Return Loss vs. Frequency
over Temperature (Min[1] / Max Gain State)

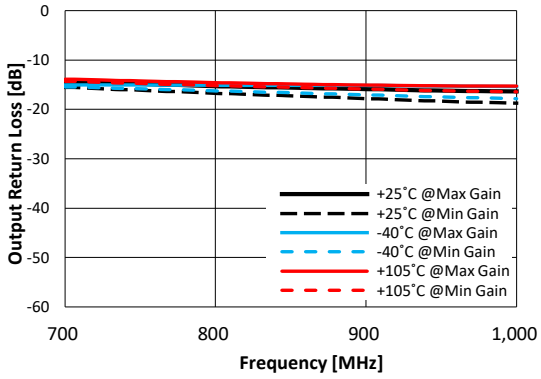
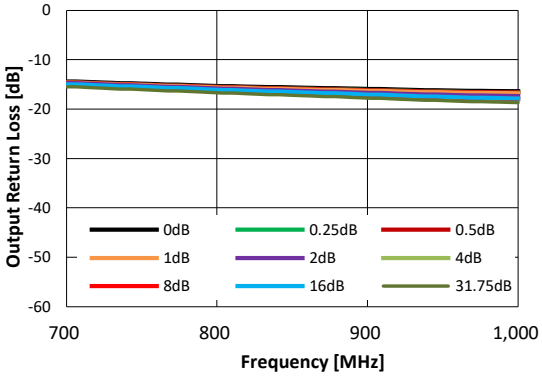


Figure 32. Output Return Loss vs. Frequency
over Major Attenuation States



1.Min Gain was measured in the state is set with attenuation 31.75dB.

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Typical RF Performance Plot - BVA1761 EVK - PCB (Application Circuit:700 ~ 1000MHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 14

Figure 33. OIP3 vs. Frequency vs. VDD
Over Temperature (Max Gain State)

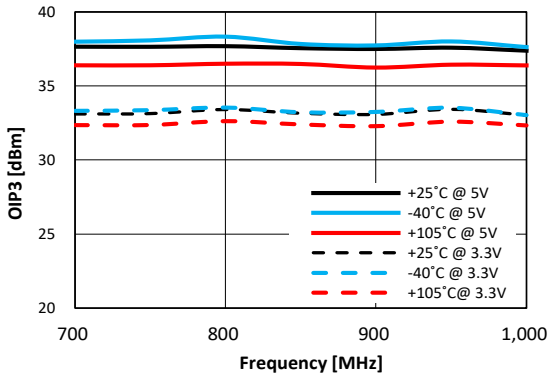


Figure 34. OIP3 vs. Frequency vs. VDD
Over Temperature (15.75dB Attenuation State)

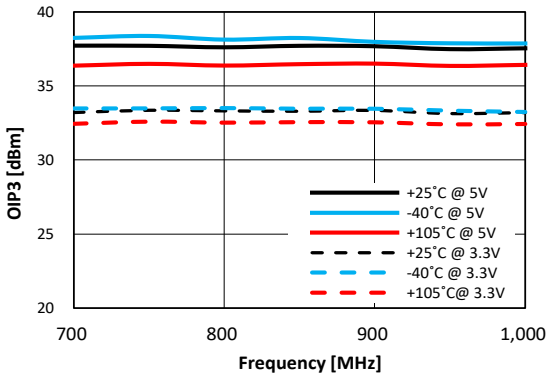


Figure 35. P1dB vs. Frequency vs. VDD
Over Temperature (Max Gain State)

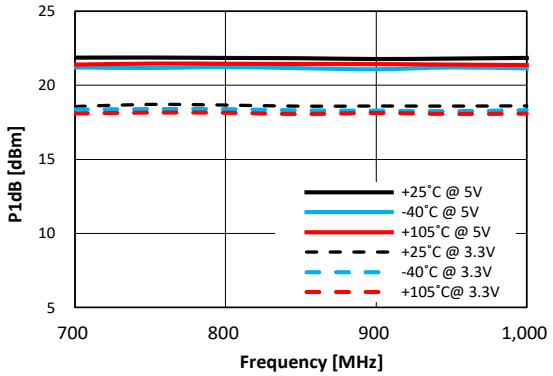


Figure 36. Noise Figure vs. Frequency @ VDD = 5V
Over Temperature (Max Gain State)

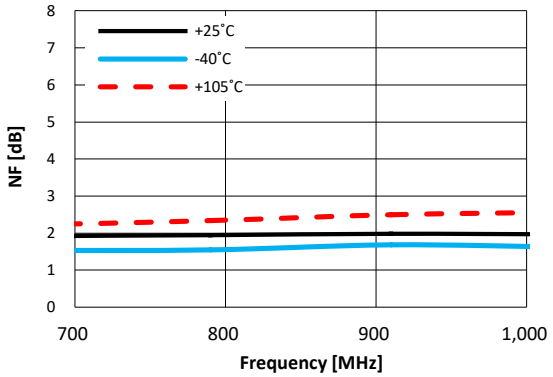
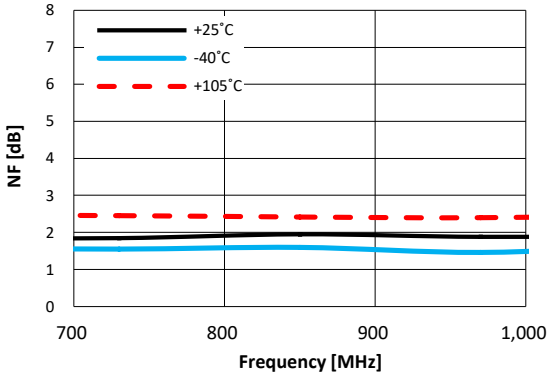


Figure 37. Noise Figure vs. Frequency @ VDD = 3.3V
Over Temperature (Max Gain State)



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Typical RF Performance Plot - BVA1761 EVK - PCB (Application Circuit:700 ~ 1000MHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 14

Figure 38. Attenuation Error vs Frequency
over Major Attenuation Steps

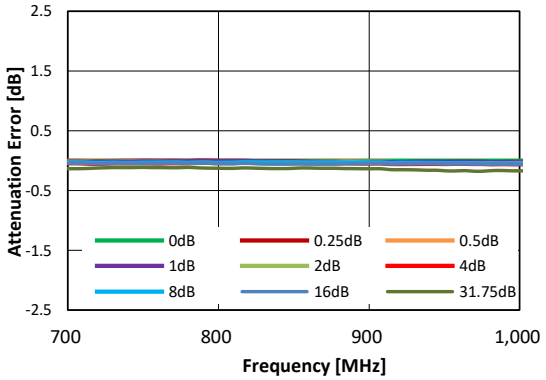


Figure 39. Attenuation Error vs Attenuation Setting
over Major Frequency (Max Gain State)

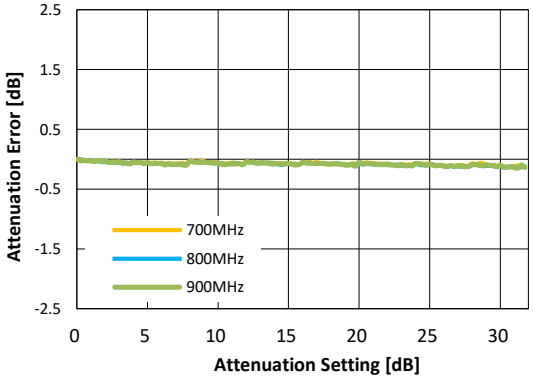


Figure 40. Attenuation Error at 700MHz vs Temperature
Over All Attenuation States

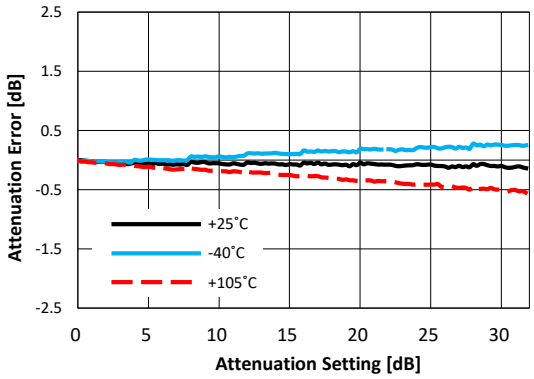


Figure 41. Attenuation Error at 800MHz vs Temperature
Over All Attenuation States

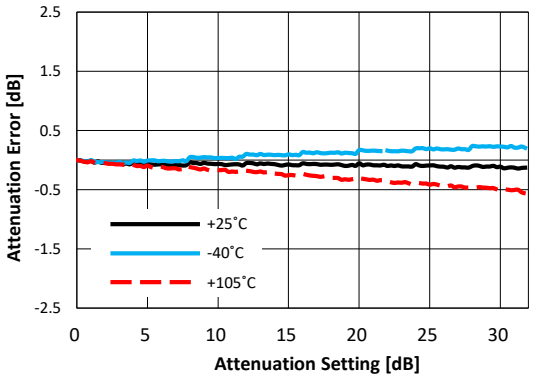
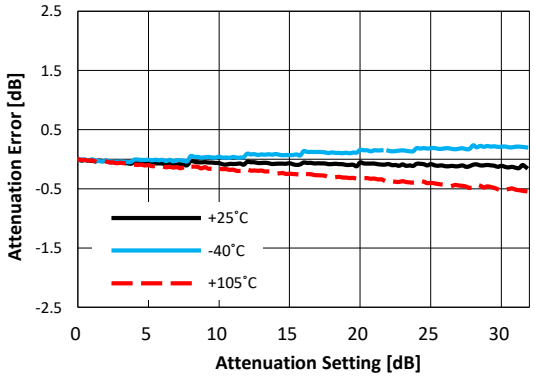


Figure 42. Attenuation Error at 900MHz vs Temperature
Over All Attenuation States

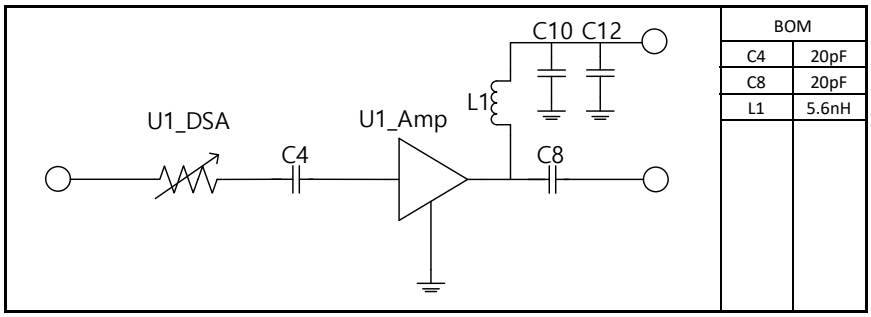


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Typical RF Performance Plot - BVA1761 EVK - PCB (Application Circuit:1.7 ~ 2.7GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 17

Table 17. 1.7 ~ 2.7GHz RF Application Circuit



BOM	
C4	20pF
C8	20pF
L1	5.6nH

This value can be changed little by little according to the frequency band and bandwidth.

Table 18. Typical RF Performance @ VDD = 5V

Parameter	Frequency			Unit
	1800	2140	2650	MHz
Gain[1]	18.7	18.6	18.0	dB
S11	-11.9	-14.6	-17.3	dB
S22	-12.3	-17.8	-13.8	dB
OIP3[2]	36.9	36.8	36.9	dBm
P1dB	20.9	20.6	20.6	dBm
Noise Figure	2.1	2.3	2.3	dB

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 _ measured with two tones at an output of 0 dBm per tone separated by 1MHz.

Table 19. Typical RF Performance @ VDD = 3.3V

Parameter	Frequency			Unit
	1800	2140	2650	MHz
Gain[1]	18.2	18.1	17.5	dB
S11	-11.2	-13.4	-15.7	dB
S22	-12.6	-17.1	-12.5	dB
OIP3[2]	33.3	33.4	33.0	dBm
P1dB	18.0	17.5	17.8	dBm
Noise Figure	2.1	2.3	2.4	dB

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 _ measured with two tones at an output of 0 dBm per tone separated by 1MHz.

Figure 43. Gain vs. Frequency @ VDD = 5V
over Temperature

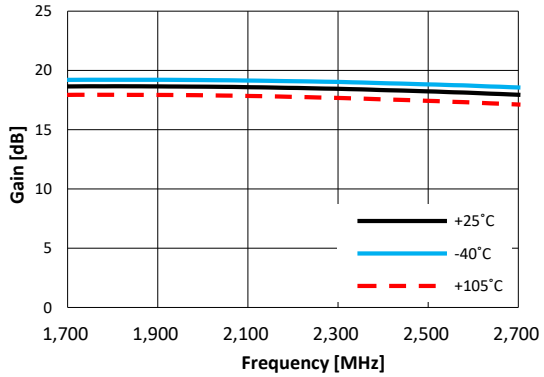
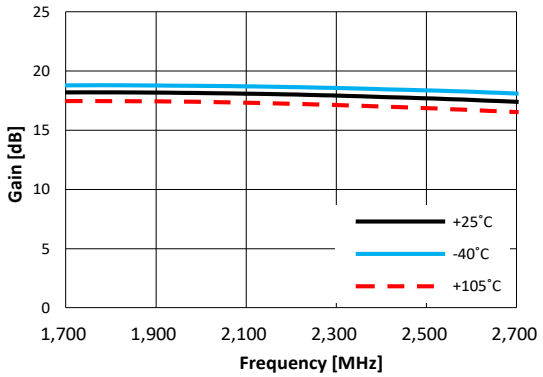


Figure 44. Gain vs. Frequency @ VDD = 3.3V
over Temperature



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Typical RF Performance Plot - BVA1761 EVK - PCB (Application Circuit:1.7 ~ 2.7GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 17

Figure 45. Gain vs. Frequency
over Major Attenuation States

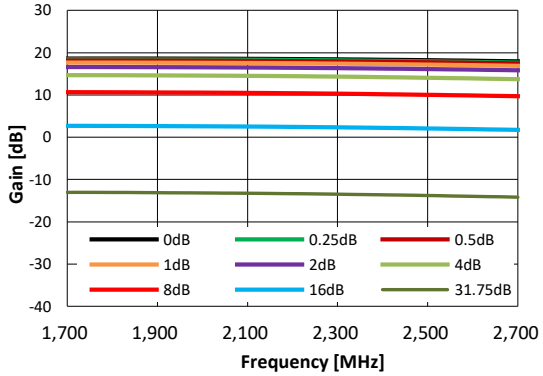


Figure 46. Gain vs. Frequency vs VDD
Max Gain States

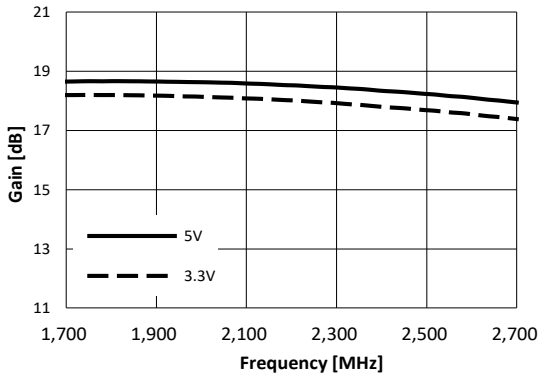


Figure 47. Input Return Loss vs. Frequency
over Temperature (Min[1] / Max Gain State)

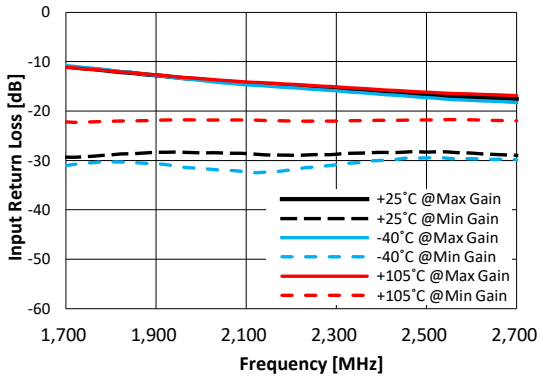
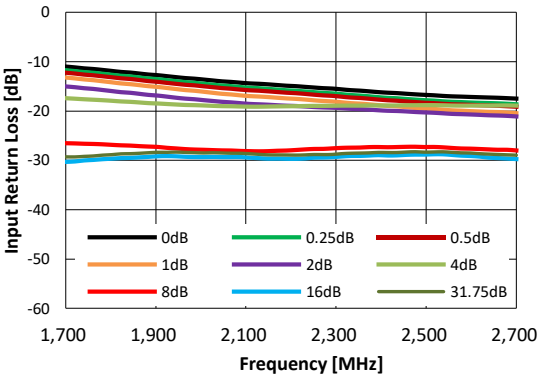


Figure 48. Input Return Loss vs. Frequency
Over Major Attenuation States



1.Min Gain was measured in the state is set with attenuation 31.75dB.

Figure 49. Output Return Loss vs. Frequency
over Temperature (Min[1] / Max Gain State)

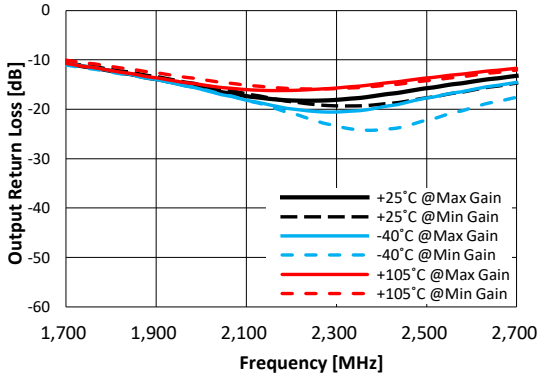
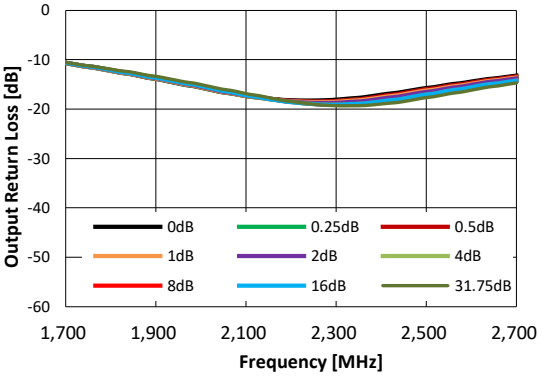


Figure 50. Output Return Loss vs. Frequency
over Major Attenuation States



1.Min Gain was measured in the state is set with attenuation 31.75dB.

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Typical RF Performance Plot - BVA1761 EVK - PCB (Application Circuit:1.7 ~ 2.7GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 17

Figure 51. OIP3 vs. Frequency vs. VDD
Over Temperature (Max Gain State)

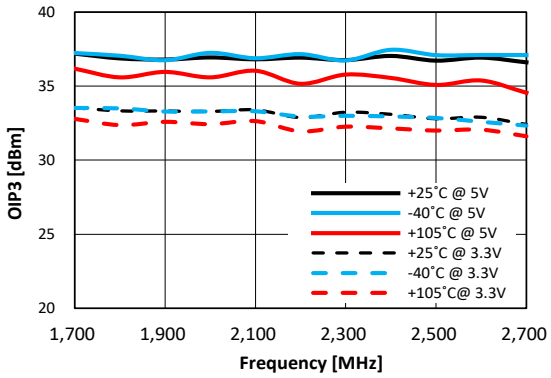


Figure 52. OIP3 vs. Frequency vs. VDD
Over Temperature (15.75dB Attenuation State)

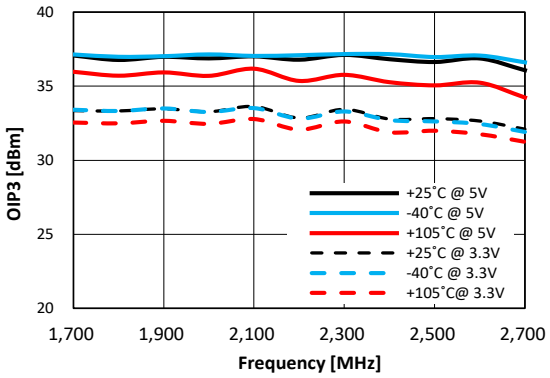


Figure 53. P1dB vs. Frequency vs. VDD
Over Temperature (Max Gain State)

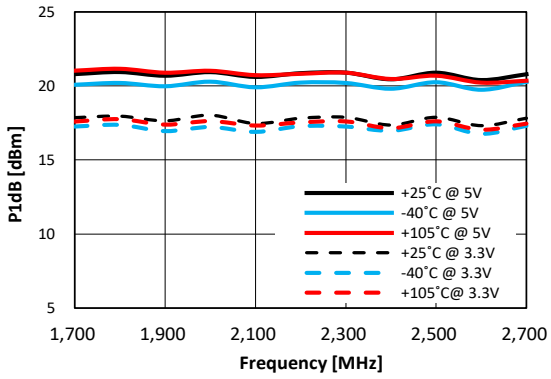


Figure 54. Noise Figure vs. Frequency @ VDD = 5V
Over Temperature (Max Gain State)

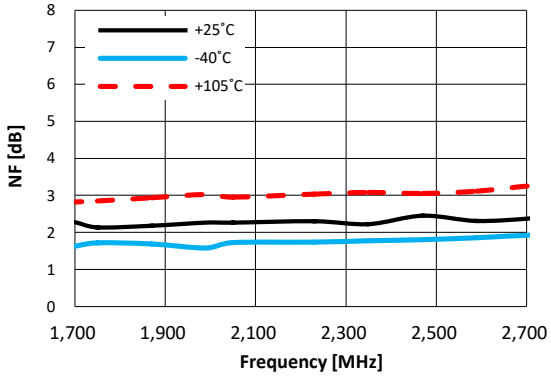
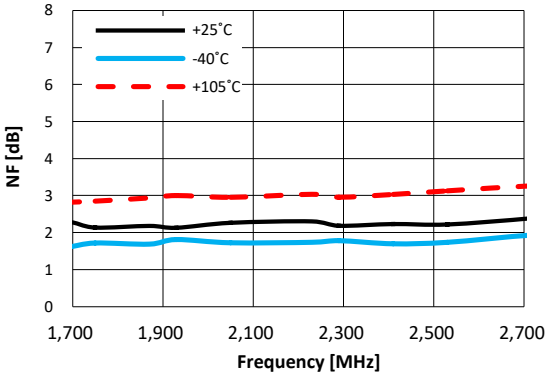


Figure 55. Noise Figure vs. Frequency @ VDD = 3.3V
Over Temperature (Max Gain State)



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Typical RF Performance Plot - BVA1761 EVK - PCB (Application Circuit:1.7~ 2.7GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 17

Figure 56. Attenuation Error vs Frequency
over Major Attenuation Steps

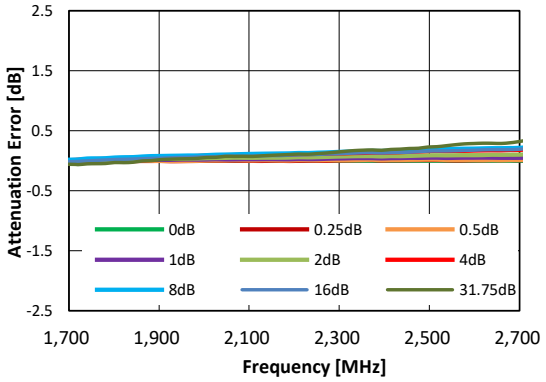


Figure 57. Attenuation Error vs Attenuation Setting
over Major Frequency (Max Gain State)

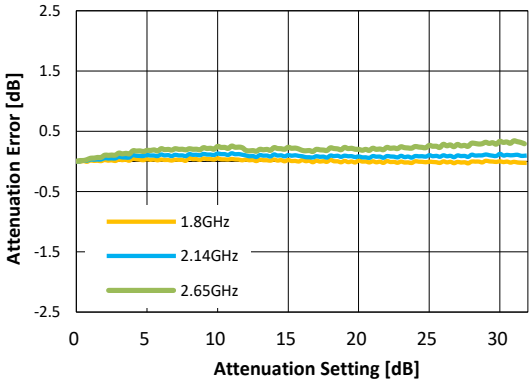


Figure 58. Attenuation Error at 1.8GHz vs Temperature
Over All Attenuation States

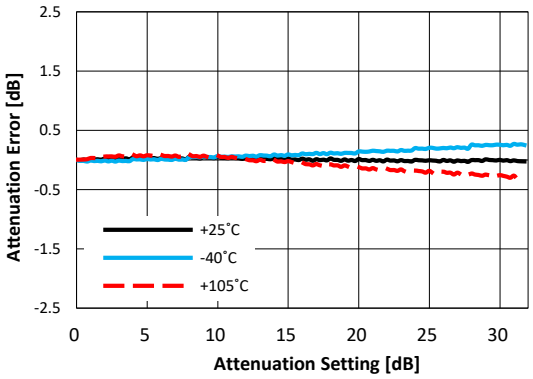


Figure 59. Attenuation Error at 2.14GHz vs Temperature
Over All Attenuation States

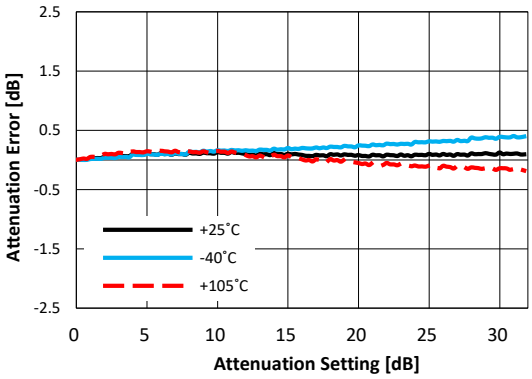
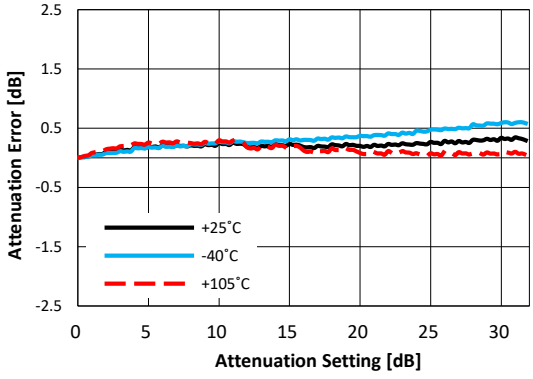


Figure 60. Attenuation Error at 2.65GHz vs Temperature
Over All Attenuation States

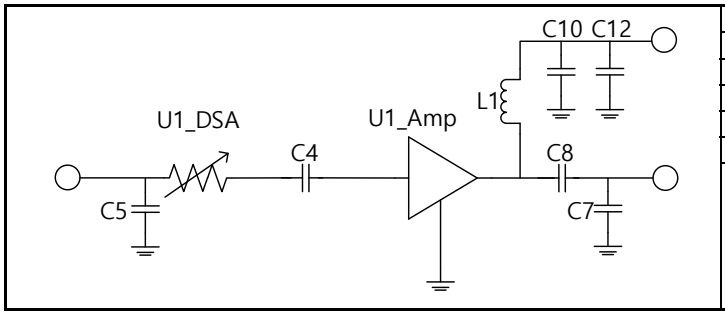


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Typical RF Performance Plot - BVA1761 EVK - PCB (Application Circuit:3.3 ~ 4GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 20

Table 20. 3.3 ~ 4GHz RF Application Circuit



BOM	
C4	18pF
C5	0.2pF
C7	0.75pF
C8	18pF
L1	1.5nH

This value can be changed little by little according to the frequency band and bandwidth.

Table 21. Typical RF Performance @ VDD = 5V

Parameter	Frequency			Unit
	3500	3700	3900	MHz
Gain[1]	17.0	16.8	16.5	dB
S11	-11.0	-10.7	-11.2	dB
S22	-13.3	-16.6	-20.8	dB
OIP3[2]	37.5	36.6	36.9	dBm
P1dB	19.9	20.1	19.9	dBm
Noise Figure	2.8	3.0	3.0	dB

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 _ measured with two tones at an output of 0 dBm per tone separated by 1MHz.

Table 22. Typical RF Performance @ VDD = 3.3V

Parameter	Frequency			Unit
	3500	3700	3900	MHz
Gain[1]	16.5	16.3	16.0	dB
S11	-10.5	-10.2	-10.8	dB
S22	-14.0	-18.8	-25.1	dB
OIP3[2]	33.4	32.7	32.4	dBm
P1dB	16.8	17.0	17.0	dBm
Noise Figure	2.8	3.0	3.0	dB

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 _ measured with two tones at an output of 0 dBm per tone separated by 1MHz.

Figure 61. Gain vs. Frequency @ VDD = 5V
over Temperature

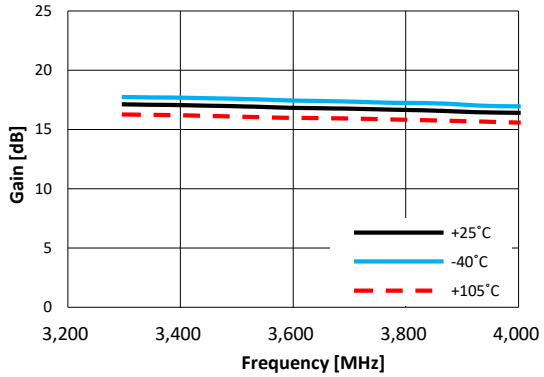
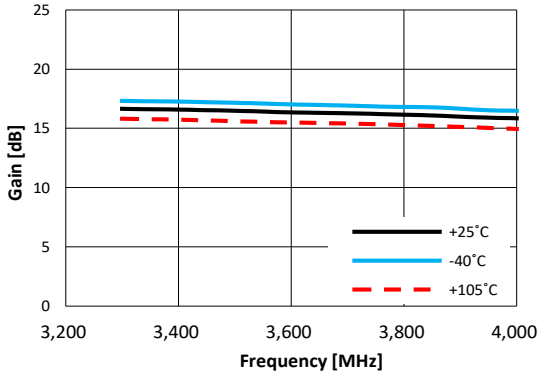


Figure 62. Gain vs. Frequency @ VDD = 3.3V
over Temperature



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Typical RF Performance Plot - BVA1761 EVK - PCB (Application Circuit:3.3 ~ 4GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 20

Figure 63. Gain vs. Frequency
over Major Attenuation States

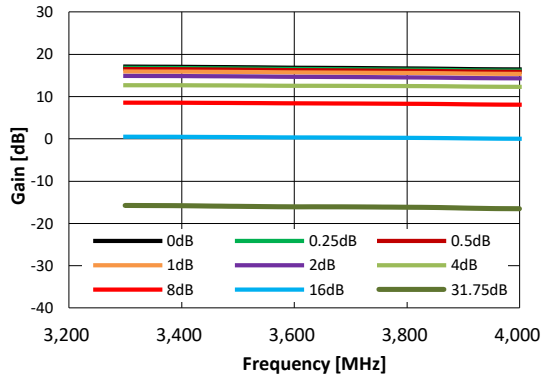


Figure 64. Gain vs. Frequency vs VDD
Max Gain States

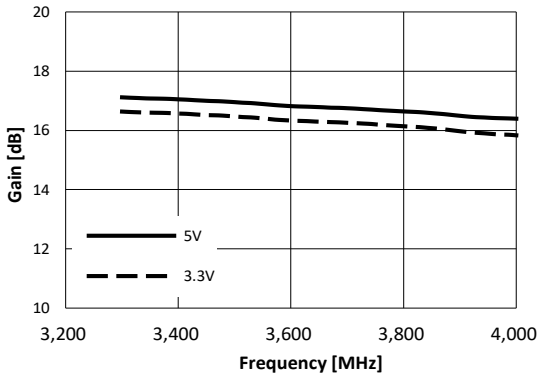


Figure 65. Input Return Loss vs. Frequency
over Temperature (Min[1] / Max Gain State)

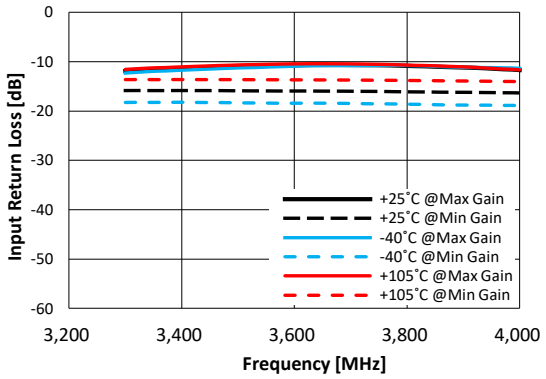
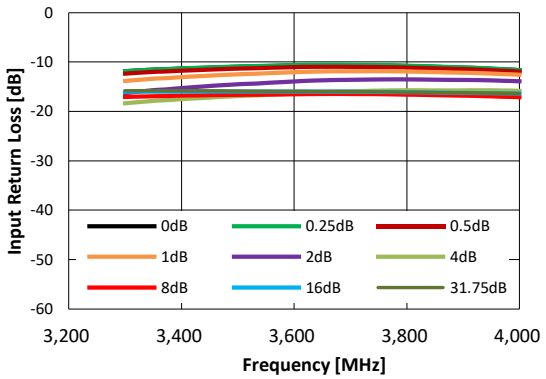


Figure 66. Input Return Loss vs. Frequency
Over Major Attenuation States



1.Min Gain was measured in the state is set with attenuation 31.75dB.

Figure 67. Output Return Loss vs. Frequency
over Temperature (Min[1] / Max Gain State)

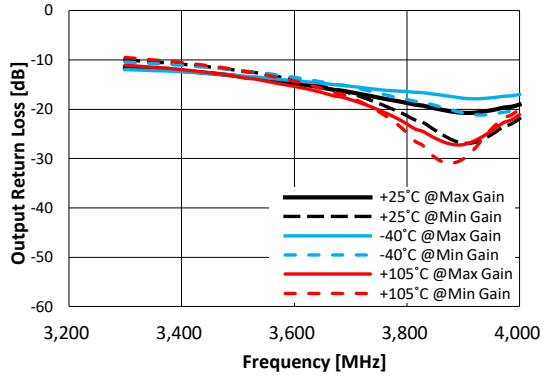
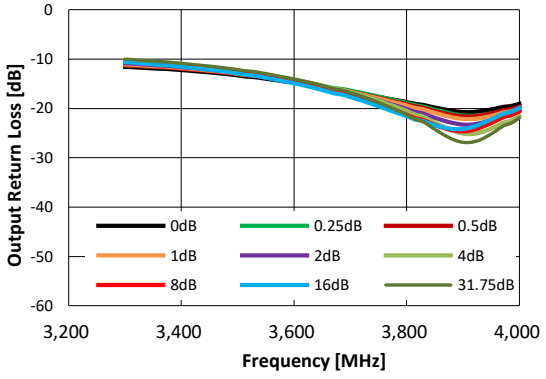


Figure 68. Output Return Loss vs. Frequency
over Major Attenuation States



1.Min Gain was measured in the state is set with attenuation 31.75dB.

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Typical RF Performance Plot - BVA1761 EVK - PCB (Application Circuit:3.3 ~ 4GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 20

Figure 69. OIP3 vs. Frequency vs. VDD
Over Temperature (Max Gain State)

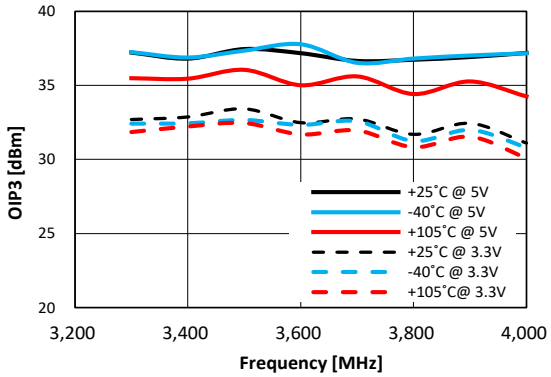


Figure 70. OIP3 vs. Frequency vs. VDD
Over Temperature (15.75dB Attenuation State)

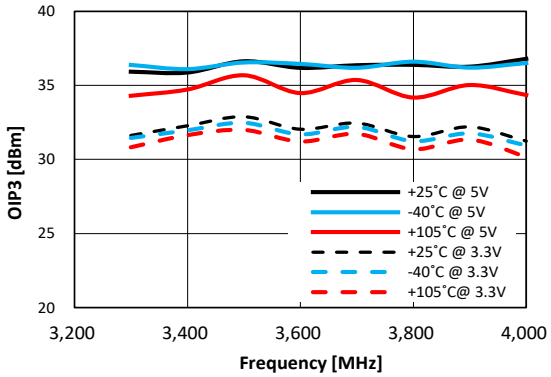


Figure 71. P1dB vs. Frequency vs. VDD
Over Temperature (Max Gain State)

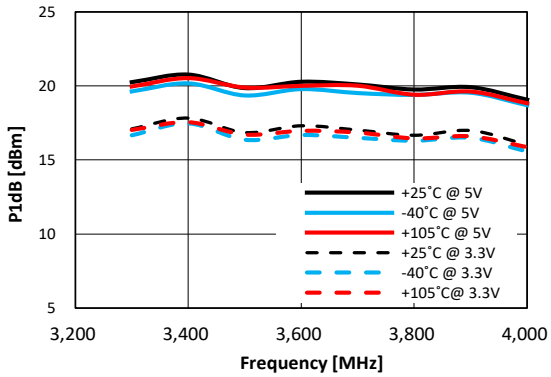


Figure 72. Noise Figure vs. Frequency @ VDD = 5V
Over Temperature (Max Gain State)

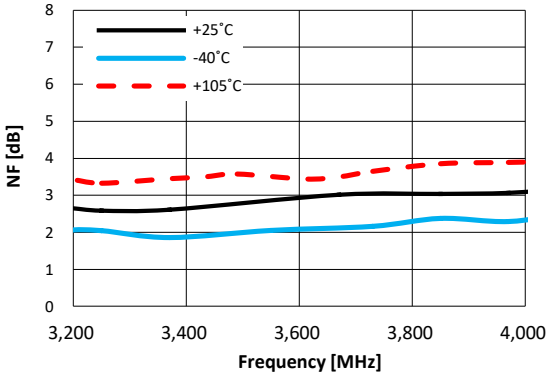
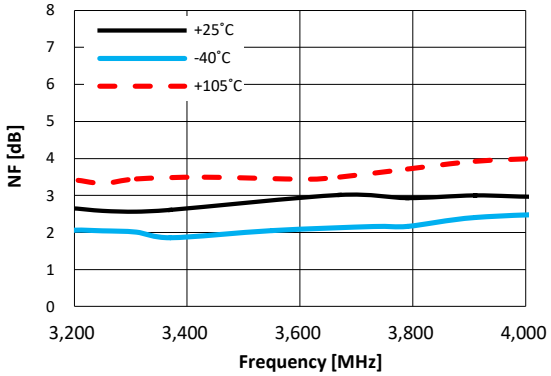


Figure 73. Noise Figure vs. Frequency @ VDD = 3.3V
Over Temperature (Max Gain State)



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Typical RF Performance Plot - BVA1761 EVK - PCB (Application Circuit:3.3~ 4GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 20

Figure 74. Attenuation Error vs Frequency
over Major Attenuation Steps

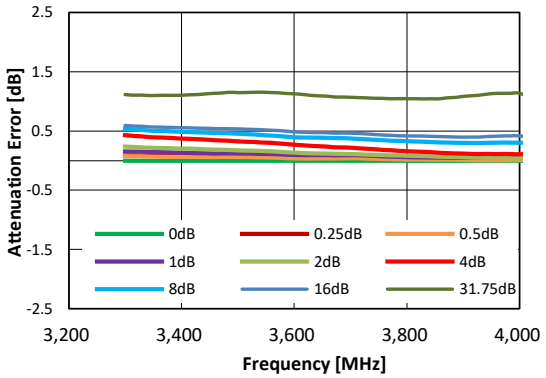


Figure 75. Attenuation Error vs Attenuation Setting
over Major Frequency (Max Gain State)

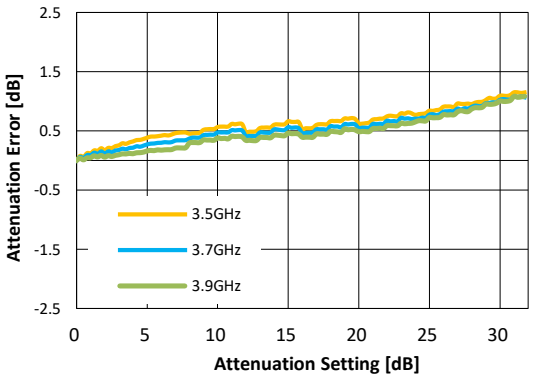


Figure 76. Attenuation Error at 3.5GHz vs Temperature
Over All Attenuation States

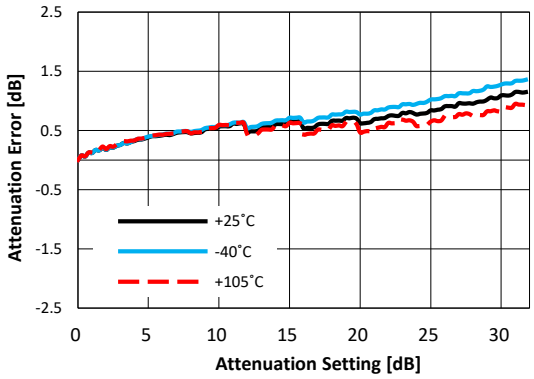


Figure 77. Attenuation Error at 3.7GHz vs Temperature
Over All Attenuation States

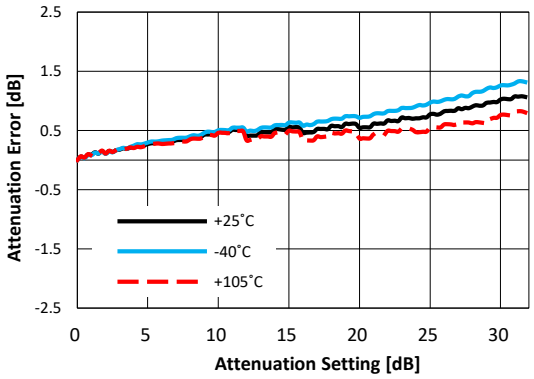
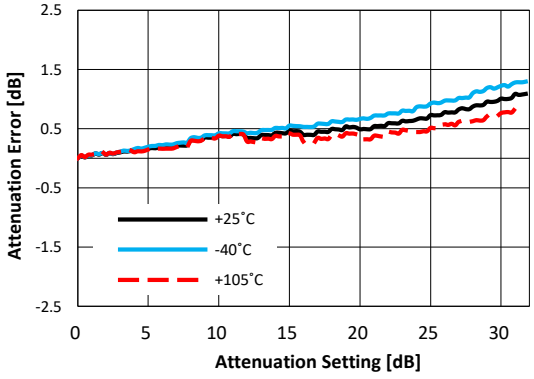


Figure 78. Attenuation Error at 3.9GHz vs Temperature
Over All Attenuation States

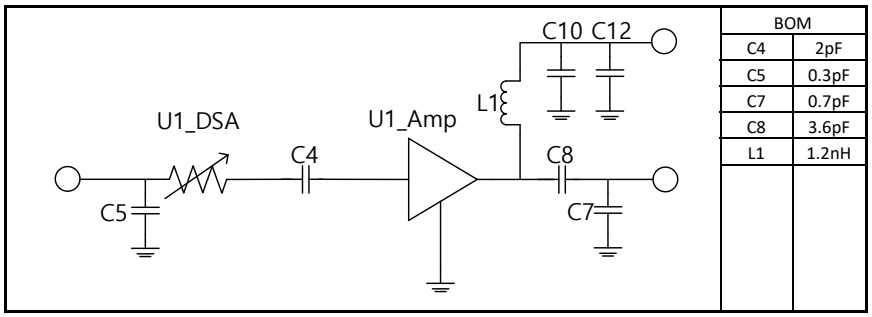


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Typical RF Performance Plot - BVA1761 EVK - PCB (Application Circuit:4.4 ~ 4.9GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 23

Table 23. 4.4 ~ 4.9GHz RF Application Circuit



BOM	
C4	2pF
C5	0.3pF
C7	0.7pF
C8	3.6pF
L1	1.2nH

This value can be changed little by little according to the frequency band and bandwidth.

Table 24. Typical RF Performance @ VDD = 5V

Parameter	Frequency			Unit
	4400	4650	4900	MHz
Gain[1]	16.1	16.0	15.5	dB
S11	-12.1	-12.9	-13.7	dB
S22	-11.7	-14.5	-10.4	dB
OIP3[2]	36.6	36.4	36.4	dBm
P1dB	20.5	19.2	18.8	dBm
Noise Figure	3.1	3.3	3.3	dB

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 _ measured with two tones at an output of 0 dBm per tone separated by 1MHz.

Table 25. Typical RF Performance @ VDD = 3.3V

Parameter	Frequency			Unit
	4400	4650	4900	MHz
Gain[1]	15.5	15.4	14.8	dB
S11	-11.3	-11.9	-12.4	dB
S22	-11.3	-12.9	-8.9	dB
OIP3[2]	34.0	34.1	32.8	dBm
P1dB	17.3	16.6	15.2	dBm
Noise Figure	3.1	3.4	3.4	dB

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 _ measured with two tones at an output of 0 dBm per tone separated by 1MHz.

Figure 79. Gain vs. Frequency @ VDD = 5V
over Temperature

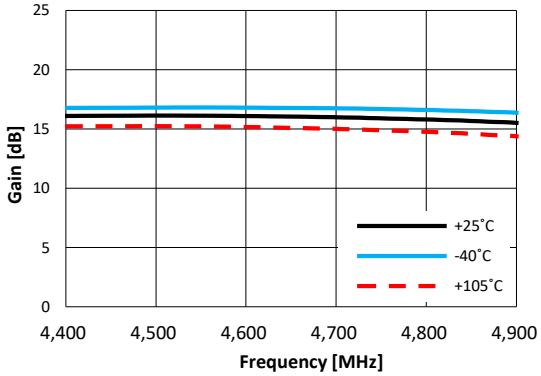
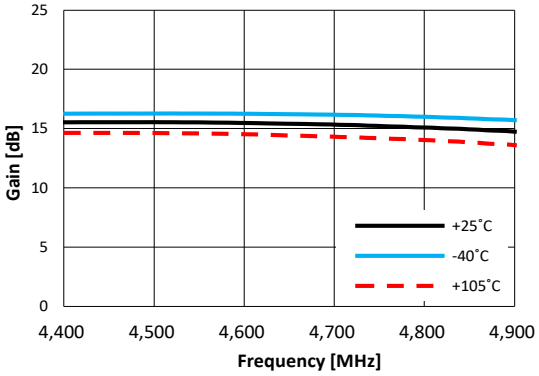


Figure 80. Gain vs. Frequency @ VDD = 3.3V
over Temperature



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Typical RF Performance Plot - BVA1761 EVK - PCB (Application Circuit:4.4 ~ 4.9GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 23

Figure 81. Gain vs. Frequency
over Major Attenuation States

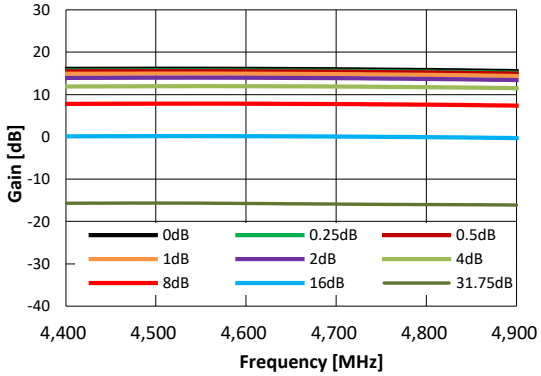


Figure 82. Gain vs. Frequency vs VDD
Max Gain States

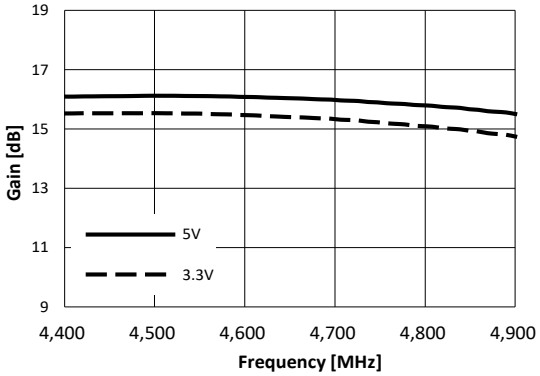


Figure 83. Input Return Loss vs. Frequency
over Temperature (Min[1] / Max Gain State)

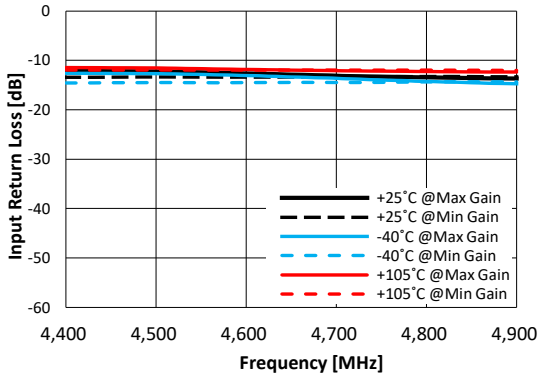
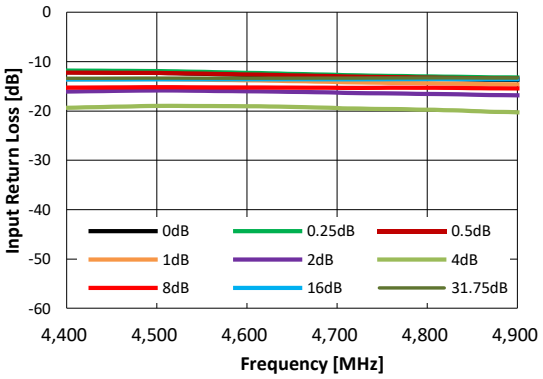


Figure 84. Input Return Loss vs. Frequency
Over Major Attenuation States



1.Min Gain was measured in the state is set with attenuation 31.75dB.

Figure 85. Output Return Loss vs. Frequency
over Temperature (Min[1] / Max Gain State)

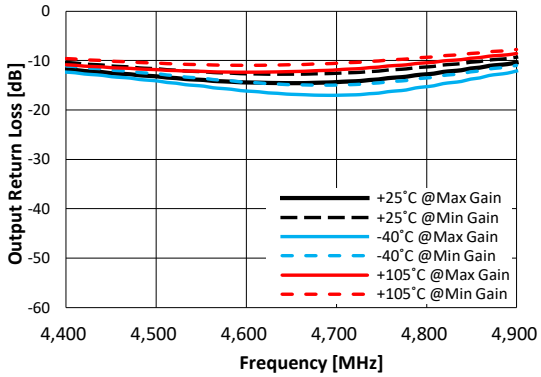
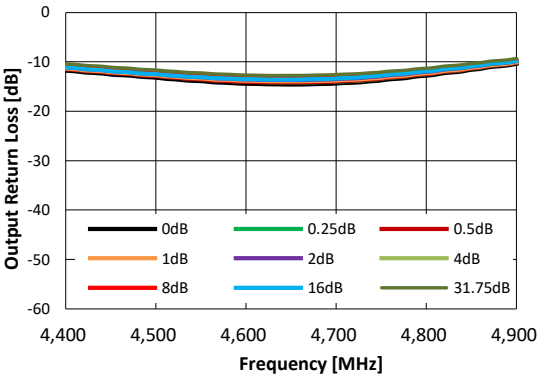


Figure 86. Output Return Loss vs. Frequency
over Major Attenuation States



1.Min Gain was measured in the state is set with attenuation 31.75dB.

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Typical RF Performance Plot - BVA1761 EVK - PCB (Application Circuit:4.4 ~ 4.9GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 23

Figure 87. OIP3 vs. Frequency vs. VDD
Over Temperature (Max Gain State)

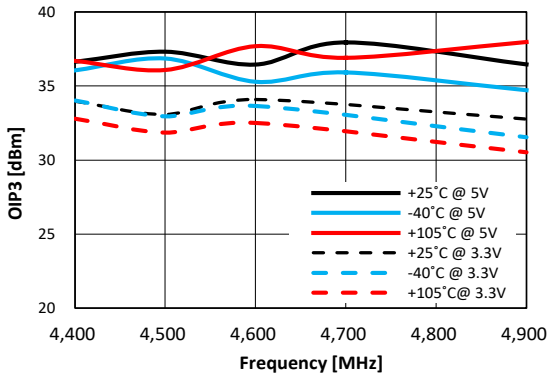


Figure 88. OIP3 vs. Frequency vs. VDD
Over Temperature (15.75dB Attenuation State)

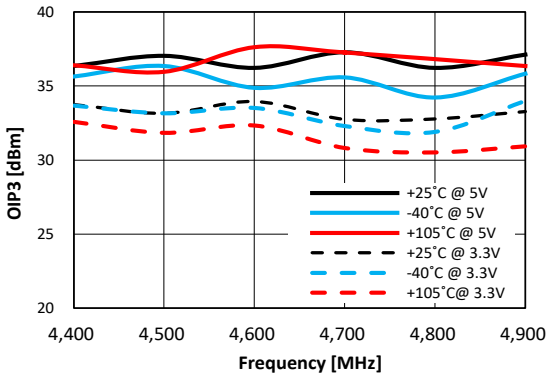


Figure 89. P1dB vs. Frequency vs. VDD
Over Temperature (Max Gain State)

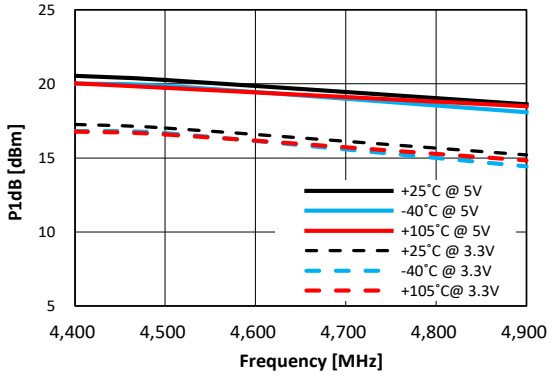


Figure 142. Noise Figure vs. Frequency @ VDD = 5V
Over Temperature (Max Gain State)

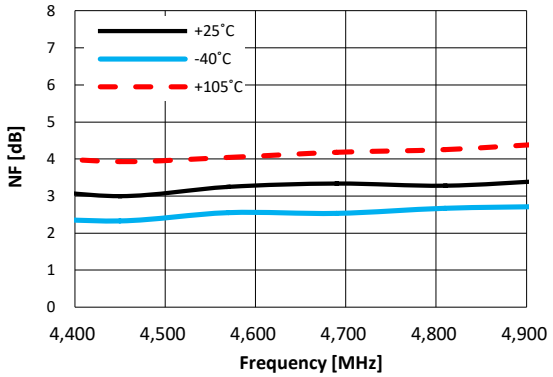
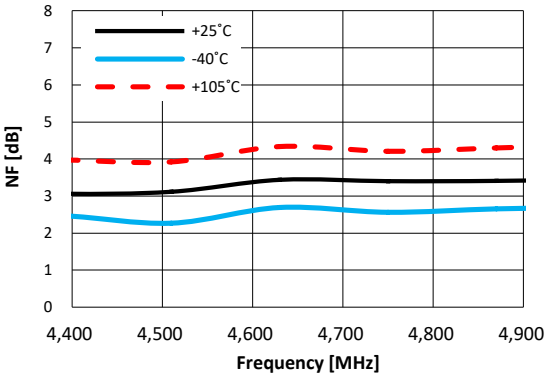


Figure 158. Noise Figure vs. Frequency @ VDD = 3.3V
Over Temperature (Max Gain State)



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Typical RF Performance Plot - BVA1761 EVK - PCB (Application Circuit:4.4~ 4.9GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 23

Figure 90. Attenuation Error vs Frequency
over Major Attenuation Steps

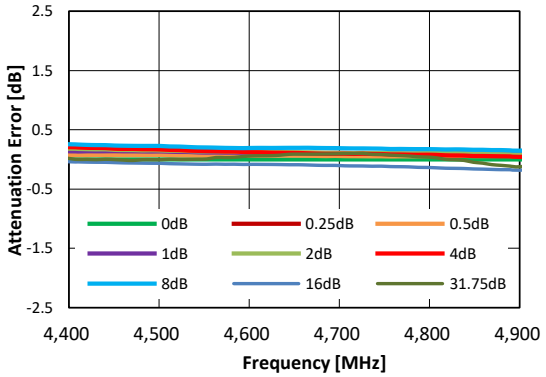


Figure 91. Attenuation Error vs Attenuation Setting
over Major Frequency (Max Gain State)

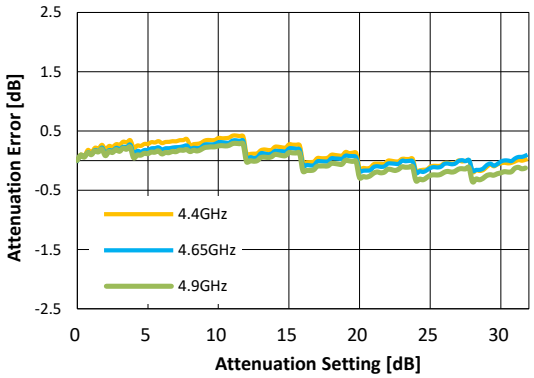


Figure 92. Attenuation Error at 4.4GHz vs Temperature
Over All Attenuation States

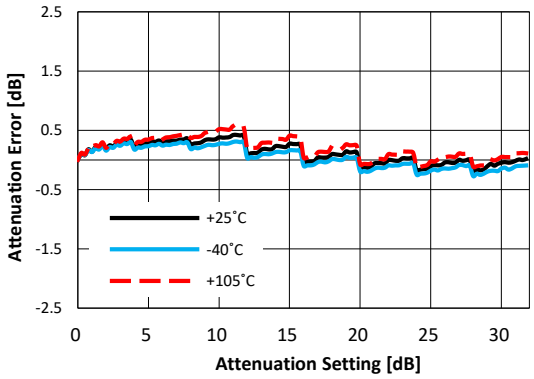


Figure 93. Attenuation Error at 4.65GHz vs Temperature
Over All Attenuation States

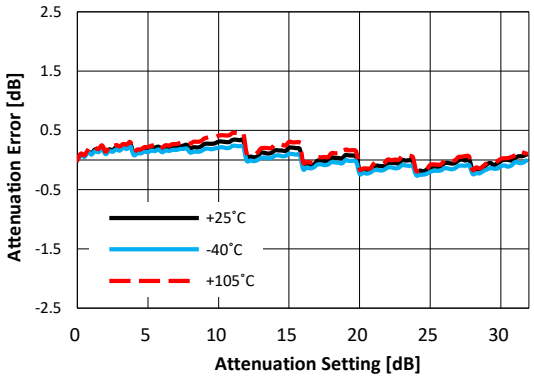
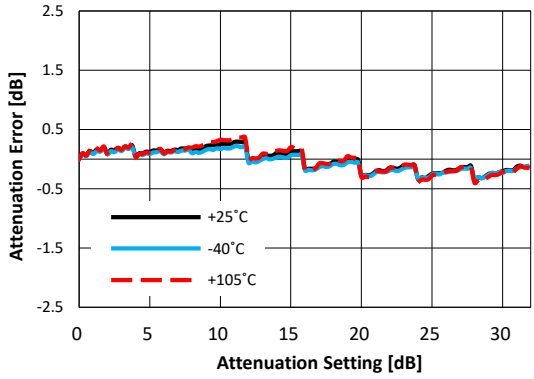


Figure 94. Attenuation Error at 4.9GHz vs Temperature
Over All Attenuation States

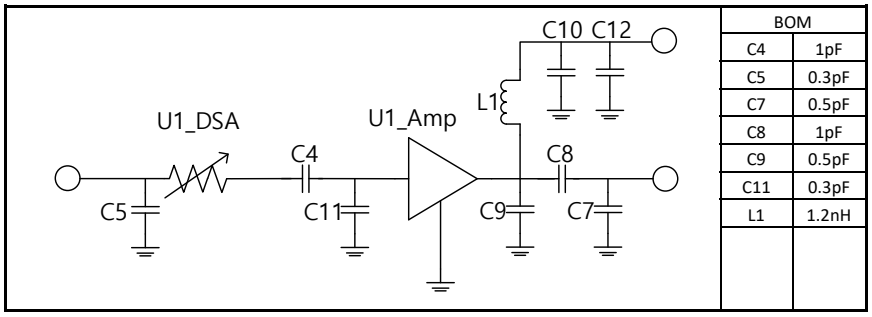


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Typical RF Performance Plot - BVA1761 EVK - PCB (Application Circuit:5.5 ~ 5.8GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 26

Table 26. 5.5 ~ 5.8GHz RF Application Circuit



BOM	
C4	1pF
C5	0.3pF
C7	0.5pF
C8	1pF
C9	0.5pF
C11	0.3pF
L1	1.2nH

This value can be changed little by little according to the frequency band and bandwidth.

Table 27. Typical RF Performance @ VDD = 5V

Parameter	Frequency		Unit
	5500	5800	MHz
Gain[1]	14.9	15.3	dB
S11	-13.1	-16.4	dB
S22	-6.9	-9.9	dB
OIP3[2]	37.0	34.2	dBm
P1dB	20.8	17.4	dBm
Noise Figure	3.6	3.7	dB

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 _ measured with two tones at an output of 0 dBm per tone separated by 1MHz.

Table 28. Typical RF Performance @ VDD = 3.3V

Parameter	Frequency		Unit
	5500	5800	MHz
Gain[1]	14.7	14.8	dB
S11	-12.3	-15.3	dB
S22	-7.3	-7.5	dB
OIP3[2]	33.0	28.7	dBm
P1dB	17.5	14.2	dBm
Noise Figure	3.5	3.8	dB

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 _ measured with two tones at an output of 0 dBm per tone separated by 1MHz.

Figure 95. Gain vs. Frequency @ VDD = 5V
over Temperature

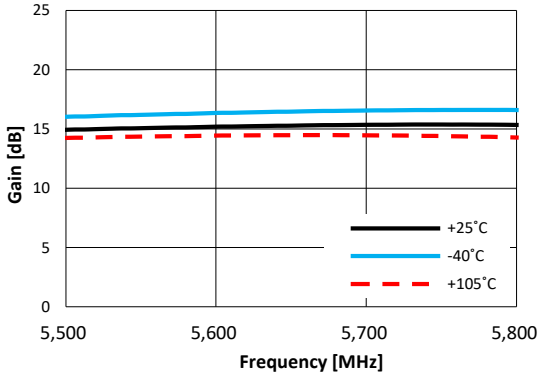
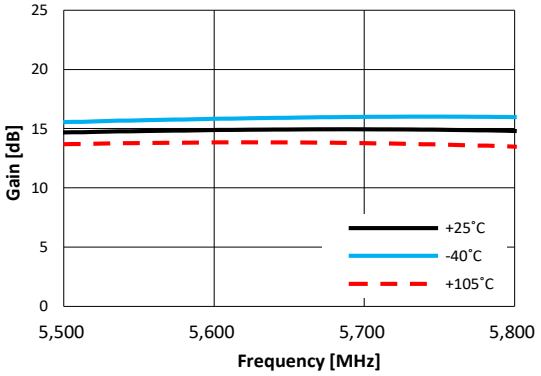


Figure 96. Gain vs. Frequency @ VDD = 3.3V
over Temperature



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Typical RF Performance Plot - BVA1761 EVK - PCB (Application Circuit:5.5 ~ 5.8GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 26

Figure 97. Gain vs. Frequency
over Major Attenuation States

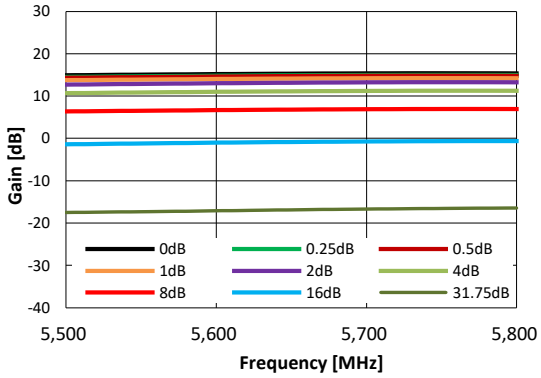


Figure 98. Gain vs. Frequency vs VDD
Max Gain States

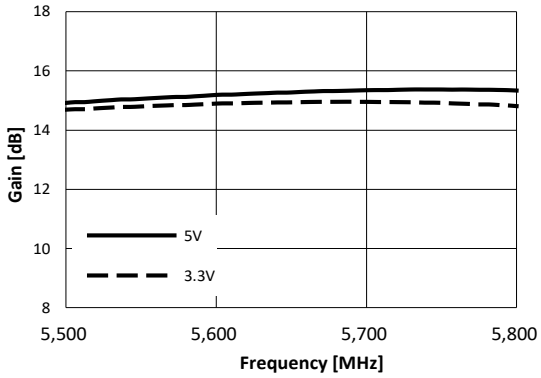


Figure 99. Input Return Loss vs. Frequency
over Temperature (Min[1] / Max Gain State)

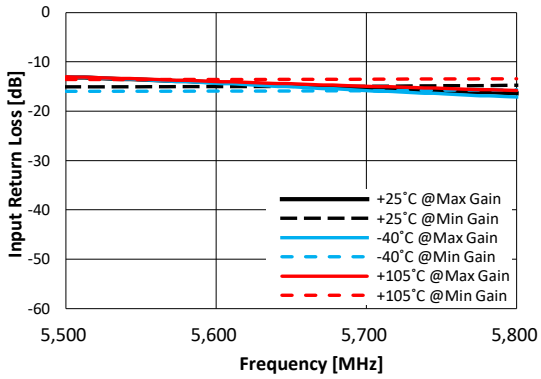
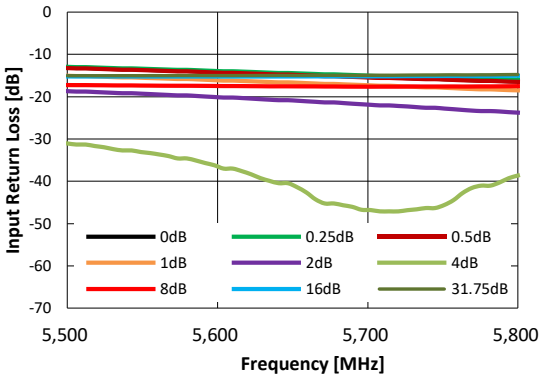


Figure 100. Input Return Loss vs. Frequency
Over Major Attenuation States



1.Min Gain was measured in the state is set with attenuation 31.75dB.

Figure 101. Output Return Loss vs. Frequency
over Temperature (Min[1] / Max Gain State)

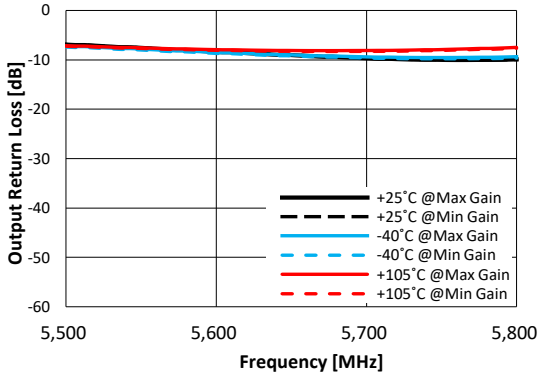
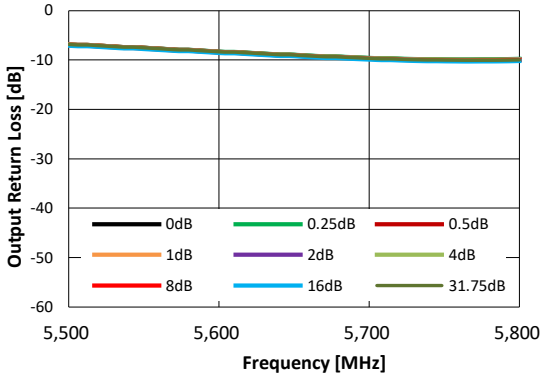


Figure 102. Output Return Loss vs. Frequency
over Major Attenuation States



1.Min Gain was measured in the state is set with attenuation 31.75dB.

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Typical RF Performance Plot - BVA1761 EVK - PCB (Application Circuit:5.5 ~ 5.8GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 26

Figure 103. OIP3 vs. Frequency vs. VDD
Over Temperature (Max Gain State)

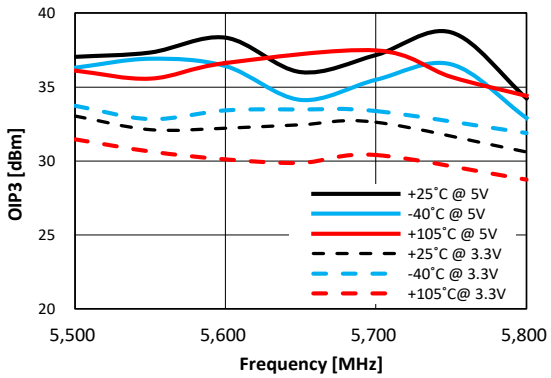


Figure 104. OIP3 vs. Frequency vs. VDD
Over Temperature (15.75dB Attenuation State)

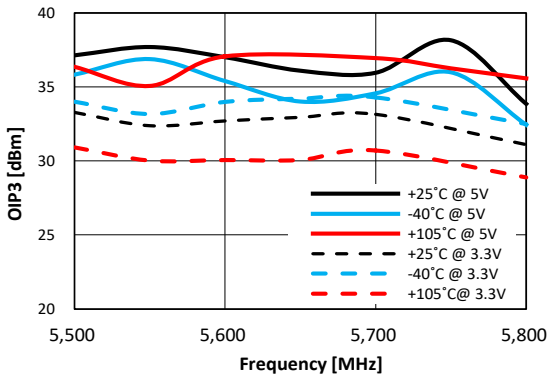


Figure 105. P1dB vs. Frequency vs. VDD
Over Temperature (Max Gain State)

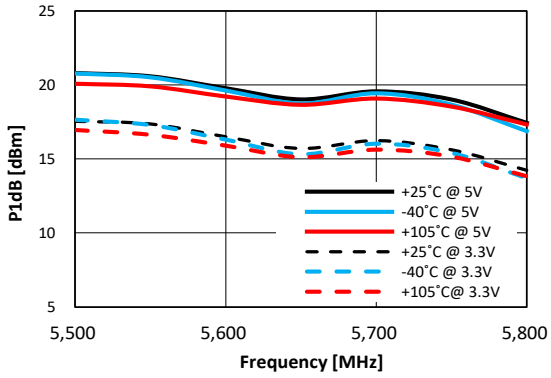


Figure 106. Noise Figure vs. Frequency @ VDD = 5V
Over Temperature (Max Gain State)

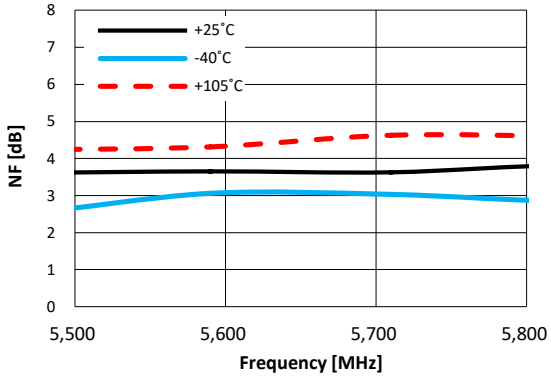
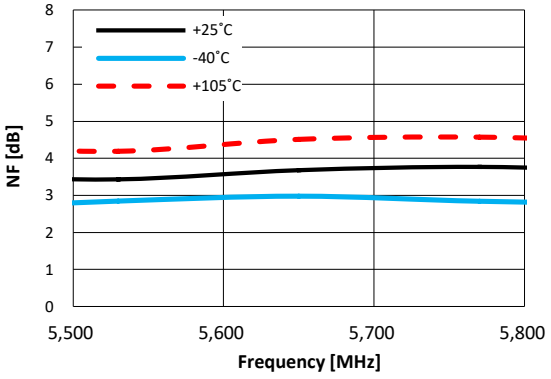


Figure 107. Noise Figure vs. Frequency @ VDD = 3.3V
Over Temperature (Max Gain State)



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Typical RF Performance Plot - BVA1761 EVK - PCB (Application Circuit:5.5 ~ 5.8GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 26

Figure 108. Attenuation Error vs Frequency
over Major Attenuation Steps

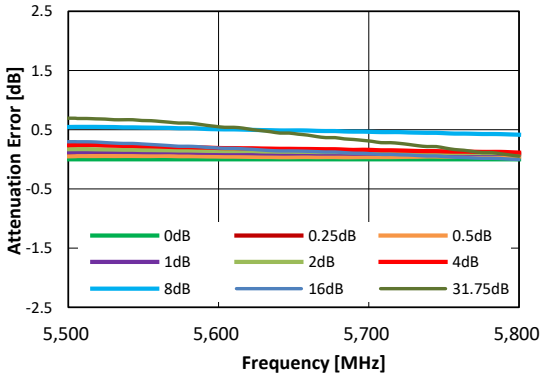


Figure 109. Attenuation Error vs Attenuation Setting
over Major Frequency (Max Gain State)

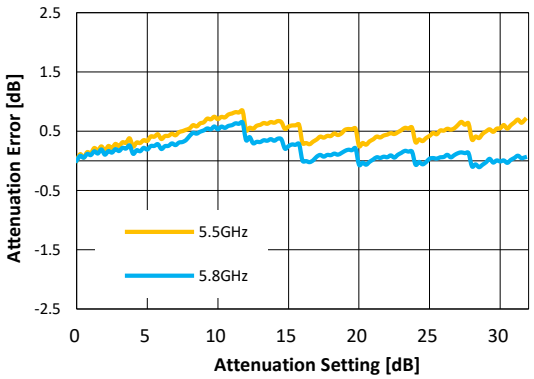


Figure 110. Attenuation Error at 5.5GHz vs Temperature
Over All Attenuation States

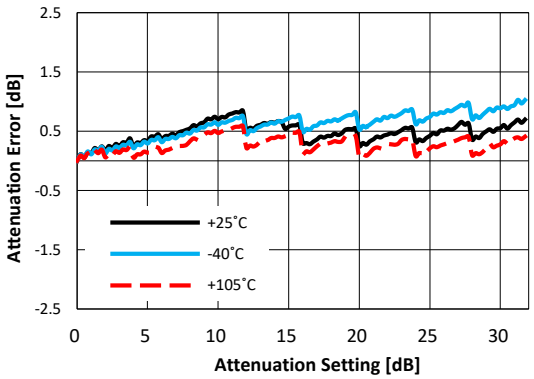
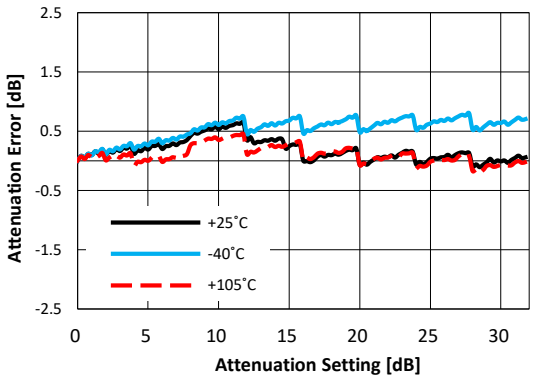


Figure 111. Attenuation Error at 5.8GHz vs Temperature
Over All Attenuation States



1.Min Gain was measured in the state is set with attenuation 31.75dB.

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Figure 112. Evaluation Board Schematic

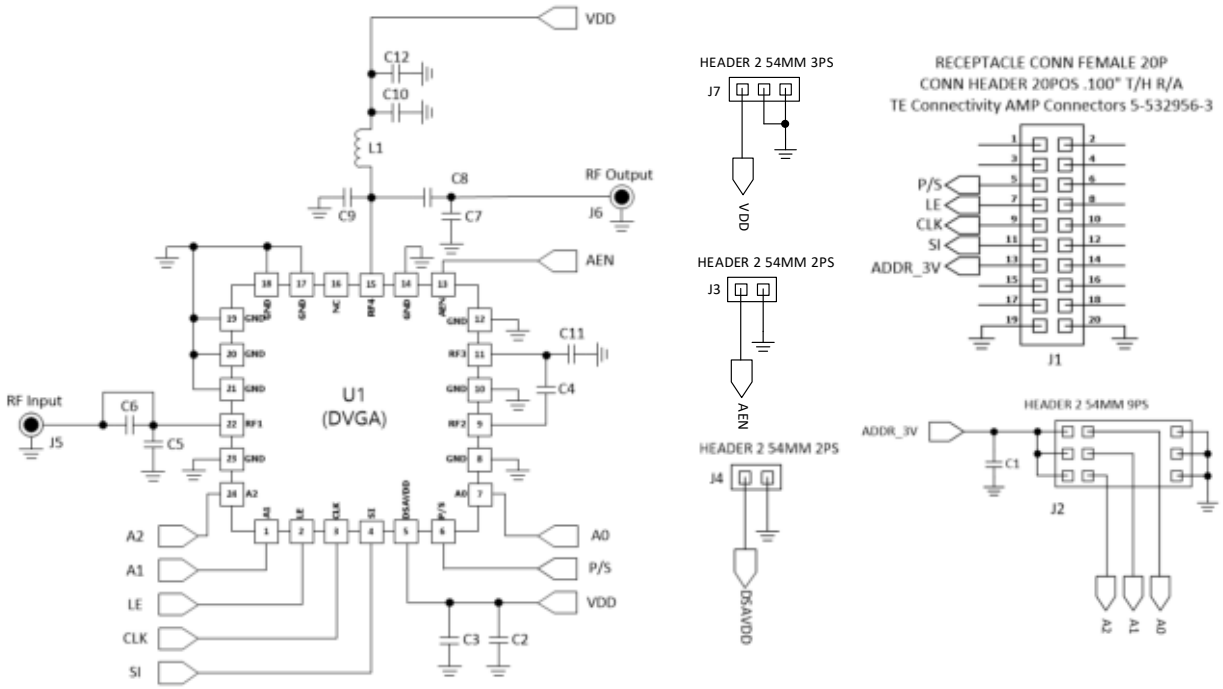


Figure 113. Evaluation Board PCB

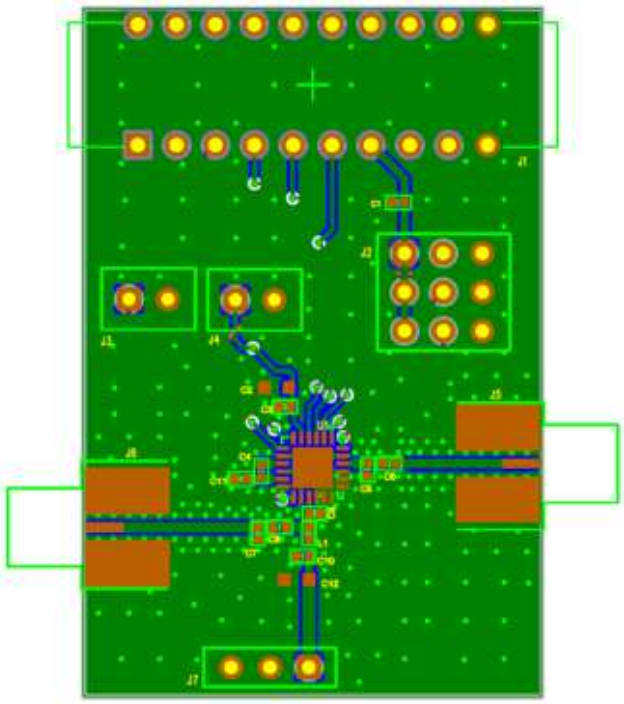


Table 29. Application Circuit

Application Circuit Values Example						
Frequency	50MHz ~ 800MHz	700MHz ~ 1GHz	1.7GHz ~ 2.7GHz	3.3GHz ~ 4GHz	4.4GHz ~ 4.9GHz	5.5GHz ~ 5.8GHz
L1	270nH	33nH	5.6nH	1.5nH	1.2nH	1.2nH
C4	10nF	100pF	20pF	20pF	2pF	1pF
C5	NC	NC	NC	0.2pF	0.3pF	0.3pF
C7	NC	NC	NC	0.75pF	0.7pF	0.5pF
C8	10nF	100pF	20pF	20pF	3.6pF	1pF
C9	NC	NC	NC	NC	NC	0.5pF
C11	NC	NC	NC	NC	NC	0.3pF

Table 30. Bill of Material - Evaluation Board

No.	Ref Des	Qty	Part Number	REMARK
1	L1	2	IND 0402	Refer to Table 29
2	C1	1	CAP 0402 100nF	
3	C4, C8	2	CAP 0402	Refer to Table 29
4	C3, C10	2	CAP 0402 100pF	
5	C2, C12	2	CAP 0603 100nF	
6	C5, C6, C7, C9, C11	5	CAP 0402	Refer to Table 29
7	J1	1	20pin Receptacle connector	2.54mm, female
8	J2	1	3pin x 3 Header array	2.54mm, male
9	J3, J4	2	2pin Header	2.54mm, male
10	J5, J6	2	SMA_END_LAUNCH	RF SMA Connector
11	J3	1	3pin Header	2.54mm, male
12	U1	1	QFN4X4_24L_BVA1761	

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Figure 114. Suggested PCB Land Pattern and PAD Layout

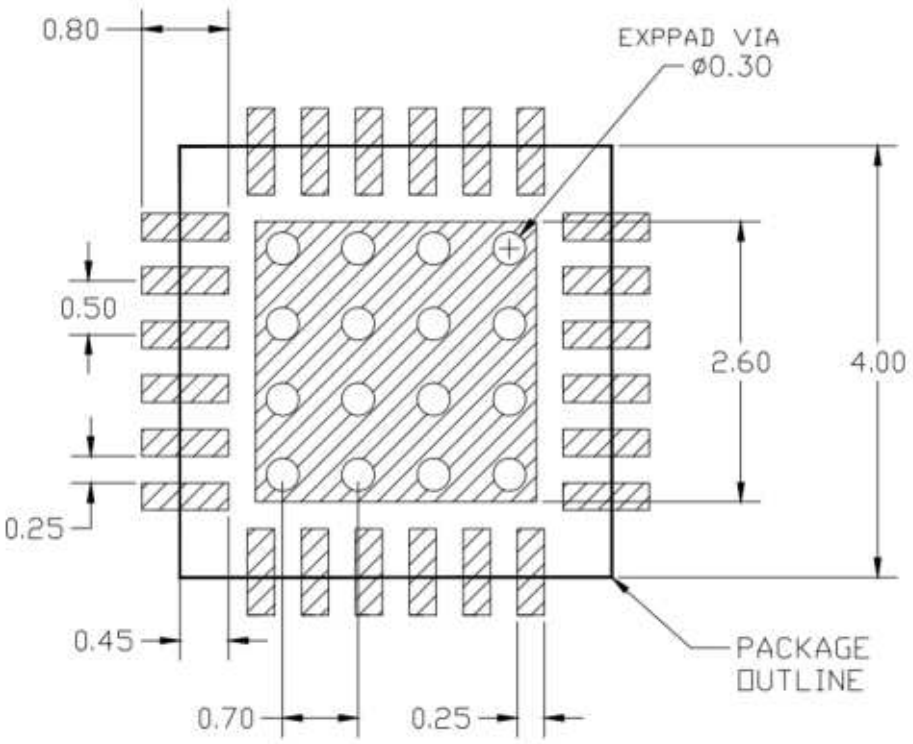
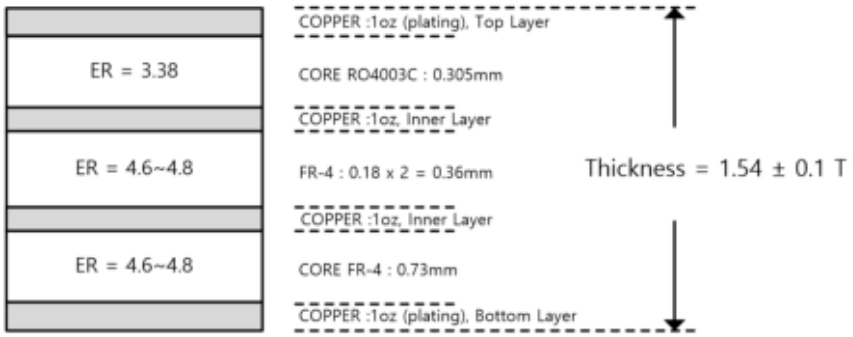
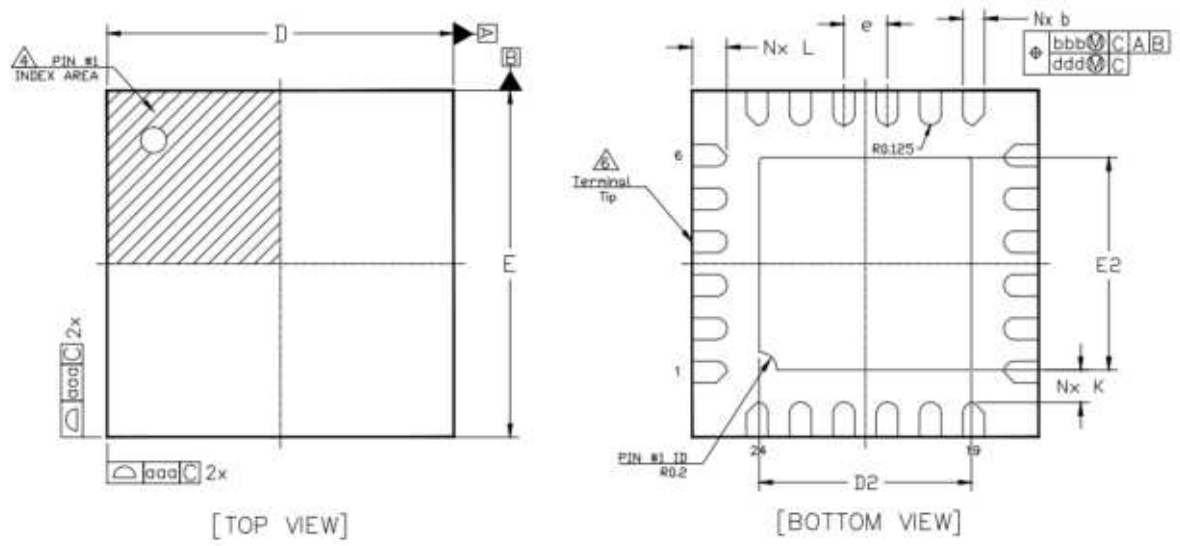


Figure 115. Evaluation Board PCB Layer Information



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Figure 116. Package Outline Dimension



NOTES:

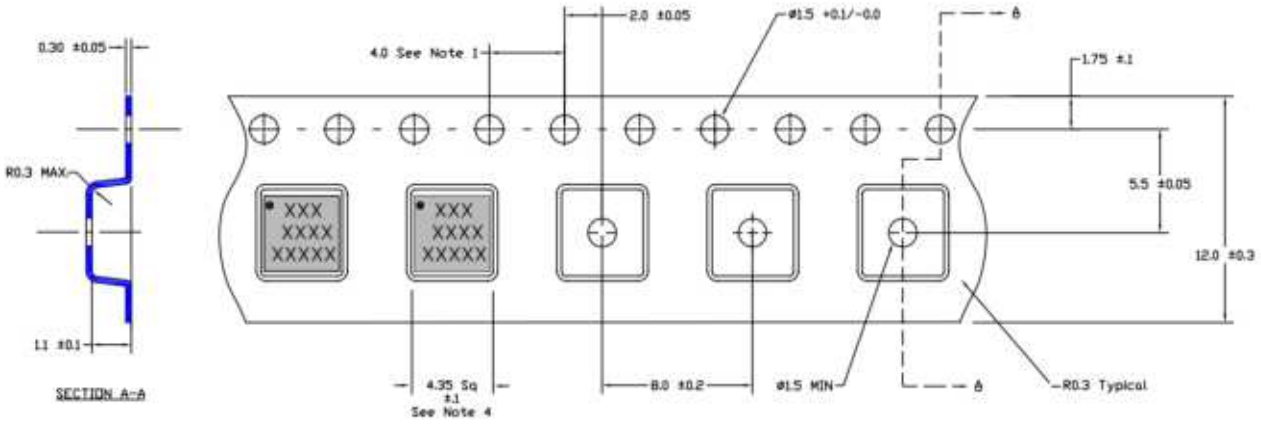
1. Dimensioning and tolerancing conform to ASME Y14.5–2009.
2. All dimensions are in millimeters.
3. N is the total number of terminals.
4. The location of the marked terminal #1 identifier is within the hatched area.
5. ND and NE refer to the number of terminals each D and E side respectively.
6. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.3mm from the terminal tip. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
7. Coplanarity applies to the terminals and all other bottom surface metallization.

Dimension Table (Notes 1,2)

Symbol Thickness	Min	Nominal	Max	Note
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
A3	---	0.20 Ref.	---	
b	0.15	0.25	0.30	6
D		4.00 BSC		
E		4.00 BSC		
e		0.50 BSC		
D2	2.30	2.45	2.55	
E2	2.30	2.45	2.55	
K	0.2	---	---	
L	0.30	0.40	0.50	
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		24		3
ND		6		5
NE		6		5

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Figure 117. Tape & Reel



Packaging information:	
Tape Width	12mm
Reel Size	7”
Device Cavity Pitch	8mm
Devices Per Reel	1K

Figure 118. Package Marking



Marking information:	
BVA1761	Device Name
YY	Year
WW	Work Week
XX	Wafer Run Number

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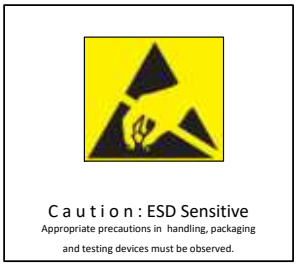
Lead plating finish

100% Tin Matte finish

(All BeRex products undergoes a 1 hour, 150 degree C, Anneal bake to eliminate thin whisker growth concerns.)

MSL / ESD Rating

ESD Rating:	Class 1C
Value:	±1000V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JS-001-2017
MSL Rating:	**Level 1 at +260°C convection reflow**
Standard:	JEDEC Standard J-STD-020



Proper ESD procedures should be followed when handling this device.

RoHS Compliance

This part is compliant with Restrictions on the use of certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2011/65/EU as amended by Directive 2015/863/EU.

This product also is compliant with a concentration of the Substances of Very High Concern (SVHC) candidate list which are contained in a quantity of less than 0.1%(w/w) in each components of a product and/or its packaging placed on the European Community market by the BeRex and Suppliers.

NATO CAGE code:

2	**N**	**9**	**6**	**F**

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