CBTL02GP023

5 Gbps rail-to-rail low insertion loss switch

Rev. 2 — 14 August 2017 Product data sheet

1. General description

The CBTL02GP023 is a one port high performance 5 Gbps rail-to-rail low insertion loss 4x SPST switch chip optimized to interface USB3.0 signals with high voltage (e.g. USB2 signals) off isolation. It supports 5 Gbps USB3.0 signals and large swing USB2 or UART signals in dongle or plug applications. It also can be used as a general purpose 5 Gbps rail-to-rail low insertion loss switch chip in other applications.

The common mode voltage of all the input or output pins have wide common mode range from 0 V to VDD.

CBTL02GP023 is available in 1.5 mm × 2.1 mm × 0.32 mm DHX2QFN14 package with 0.4 mm pitch.

2. Features and benefits

- One port (two differential channels) 5 Gbps rail-to-rail low insertion loss switch
- Differential channels:
  - Low insertion loss: −1.5 dB at 2.5 GHz; −1 dB at 100 MHz
    Low return loss: < −15 dB at 2.5 GHz
  - Low ON-state resistance: 11 Ω (typ)
  - Bandwidth: 7 GHz (typ)
    Low off-state isolation: −16 dB at 2.5 GHz; −40 dB at 100 MHz
    Low DDNEXT crosstalk: < −35 dB at 2.5 GHz and 500 MHz
  - VIC common mode input voltage: 0 to VDD
  - Differential input voltage VID: 1.2 V (Max)
  - Intra-pair skew: 6 ps (typ)
- VDD Power Supply voltage range in the dongle or plug:
  - 2.7 V (min) to 3.5 V (max)
- Low active current consumption: 500 μA (max)
  - Minimum disable current (ENH = LOW): 12 μA (max)
- Back current protection on all I/O pins
- Patent pending high performance analog pass-gate technology
- All channels support rail-to-rail input voltage
- Small DHX2QFN14 1.5mm × 2.1 mm × 0.32 mm package with 0.4 mm pitch
- ESD protection exceeds 2000V HBM per JDS-001-2012 and 750 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Operating temperature range: −20 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
CBTL02GP023	23	DHX2QFN14	Plastic, super thin quad flat package; no leads; 14 terminals; body 1.5 mm x 2.1 mm x 0.32 mm; 0.4 mm pitch	SOT1458-1

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
CBTL02GP023	CBTL02GP023HOZ	DHX2QFN14	REEL 13" Q1/T1 *STANDARD MARK SBB	20000	T_{amb} = −20 °C to +85 °C

4. Block diagram

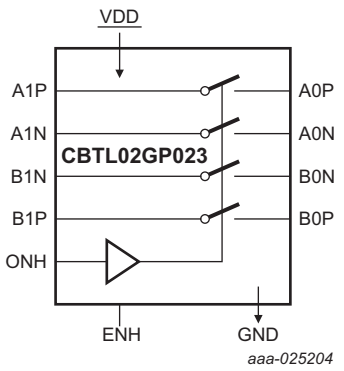


Fig 1. Block diagram

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5. Pinning information

5.1 Pinning

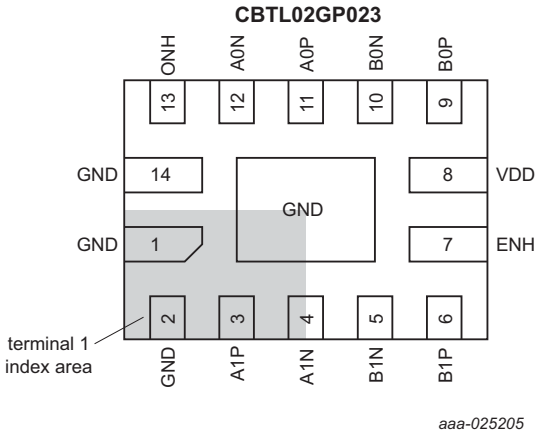


Fig 2. Pin configuration (top view)

Refer to Section 10 “Package outline” for package related information.

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
Data path signals			
A1P	3	differential I/O	USB3.0 differential signals for A port
A1N	4	differential I/O	
A0N	12	differential I/O	USB3.0 differential signals for A port (P and N is crossed for A port)
A0P	11	differential I/O	
B1N	5	differential I/O	USB3.0 differential signals for B port
B1P	6	differential I/O	
B0N	10	differential I/O	USB3.0 differential signals for B port (P and N is a flow through differential path for B port)
B0P	9	differential I/O	
Control signal			
ENH	7	control input	When HIGH, enables switches. When LOW, whole chip is powered down
ONH	13	control input	When HIGH, all switches are turned on. When LOW, all switches are OFF, but the control circuit is still working to improve isolation performance
Power supply			
VDD	8	power	Power supply range between 2.7 V and 3.5 V
Ground connection			
GND	1, 2, 14, center pad	ground	0 V

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6. Functional description

Refer to Figure 1 “Block diagram” of CBTL02GP023.

ENH pin is used to power down the switches. When ENH is low, the switches are in high impedance sleep mode. ONH can also be used to control the switch with better OFF isolation performance.

Table 4. Enable control table

ENH	Switch state	Max current consumption
0	OFF	12 μA
1	ON	500 μA

Table 5. ONH and ENH control table

ONH	ENH	Switch state	Max current	OFF isolation at 2.5 GHz
0	0	OFF	12 μA	−11 dB
0	1	OFF	500 μA	−16 dB
1	0	OFF	12 μA	−11 dB
1	1	ON	500 μA	NA

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7. Limiting values

Table 6. Limiting values [1]

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage		[2]	−0.3	+4.6	V
V_I	input voltage of control pins		[2]	−0.3	+5.5	V
V_{IO}	voltage of I/O pins of switches		[2]	−0.3	+4.6	V
T_{stg}	storage temperature			−65	+150	°C
V_{ESD}	electrostatic discharge voltage	HBM	[3]	-	2000	V
		CDM	[4]	-	750	V

[1] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] All voltage values, except differential voltages, are with respect to network ground terminal.

[3] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

[4] Charged Device Model: ANSI/EOS/ESD-S5.3-1-1999, standard for ESD sensitivity testing, Charged Device Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

8. Recommended operating conditions

Table 7. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD	supply voltage	3.3 V supply option	2.7	-	3.5	V
V_I	input voltage	CMOS inputs	−0.3	-	+5.5	V
		MUX I/O pins	−0.3	-	+3.5	V
T_{amb}	ambient operating temperature	operating in free air	−20	-	+85	°C

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9. Characteristics

9.1 Device general characteristics

Table 8. General characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	supply current	VDD = 3.5 V	-	-	0.5	mA
P_{cons}	power consumption	VDD = 3.5 V	-	-	1.75	mW
P_{sleep}	sleep mode power consumption	ENH = 0	-	-	42	µW
$T_{Startup}$	start-up time	supply voltage valid and ENH goes HIGH to channel specified operating characteristics	-	220	500	µs
T_{switch}	5 Gbps rail-to-rail low insertion loss switching time	ONH goes from LOW to HIGH	-	2	10	µs
		ONH goes from HIGH to LOW	-	200	1000	µs

9.2 Switch channel characteristics

Table 9. Dynamic and static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DDIL	differential insertion loss	Channel is off with ENH = HIGH and ONH = LOW				
		f = 2.5 GHz	-	−16	-	dB
		f = 100 MHz	-	−40	-	dB
		Channel is off with whole chip disabled ENH = LOW and ONH = X (don't care)				
		f = 2.5 GHz	-	−11	-	dB
		f = 100 MHz	-	−30	-	dB
		Channel is on with ONH = HIGH and ENH = HIGH				
		f = 2.5 GHz	-	−1.5	-	dB
		f = 100 MHz	-	−1	-	dB
DDRL	Differential Return Loss	f = 2.5 GHz	-	−15	-	dB

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Table 9. Dynamic and static characteristics *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DDNEXT	High Speed Tx to Rx. Differential near-end crosstalk	A1P/N to B1P/N or A0P/N to B0P/N				
		f=–2.5GHz	-	–20	-	dB
DDFEXT	High Speed Tx to Rx. Differential far-end crosstalk	A1P/N to B0P/N or A0P/N to B1P/N				
			-	–20	-	dB
R_{on}	ON-state resistance	V_{DD} = 2.7 V; V_I = 2.2 V; I_I = 10 mA	-	11	15	Ω
C_{in}	Input capacitance	V_{DD} = 2.8 V; V_I = 1.4 V; at 10 MHz	-	3	-	pF
B_{-3dB}	Bandwidth	V_{IC} = 0 V	-	7	-	GHz
T_{pd}	Propagation delay	From input to output pairs	-	70	-	ps
$T_{sk(diff)}$	Differential skew time	Intra-pair	-	6	-	ps
V_I	Input voltage	for all switch ports	0	-	3.5	V
V_{IC}	Commom-mode input voltage	for all switch ports	0	-	VDD	V
I_{LIH}	High level input leakage current	V_{DD}=MAX; V_I=V_{DD}	-	-	±1	μA
I_{LIL}	Low level input leakage current	V_{DD}=MAX; V_I=GND	-	-	±1	μA

9.3 Control signals characteristics

Table 10. ENH input buffer characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	CMOS inputs	0.7* VDD	-	-	V
V_{IL}	LOW-level input voltage	CMOS inputs	-	-	0.3* VDD	V
I_{LI}	Input leakage current	Measured with input at V_I=VDD and V_I=0V			1	μA

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Table 11. ONH input buffer characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	CMOS input	2.15	-	-	V
V_{IL}	LOW-level input voltage	after glitch filter to debounce noise	-	-	0.5	V
I_{LI}	Input leakage current	Measured with input at V_{IH} = VDD and V_{IL} = 0 V	-	-	0.1	µA
t_{degl}	deglitch time	time from ONH signal going LOW and staying LOW below V_{IL} level	-	200	1000	µs

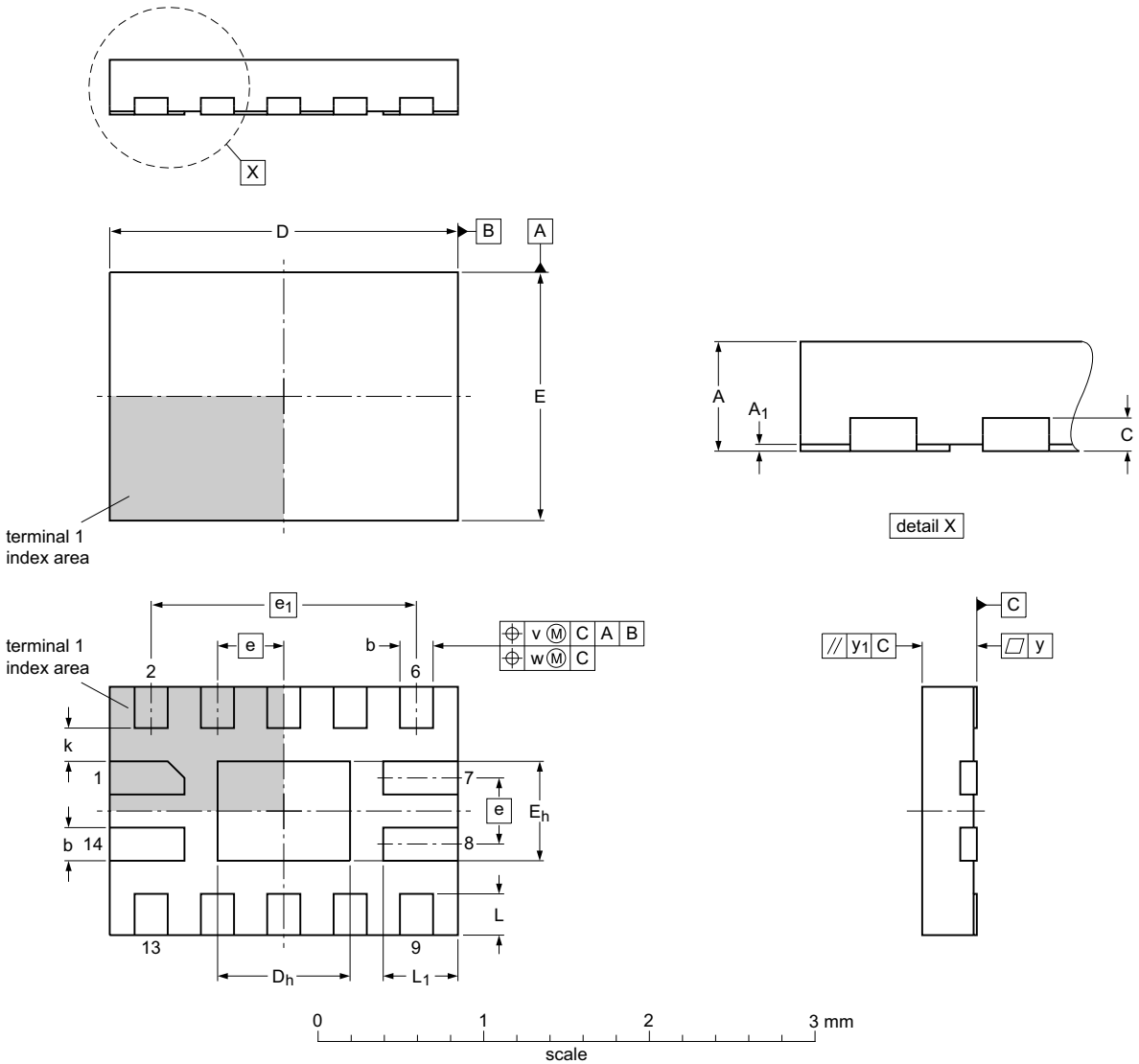
[1] The I_{LI} value is guaranteed by design and bench test

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10. Package outline

DHX2QFN14: plastic dual in-line compatible thermal enchanged super thin quad flat package; no leads; 14 terminals; body 1.5 x 2.1 x 0.32 mm **SOT1458-1**



Dimensions (mm are the original dimensions)

Unit[1]		A[1]	A_1	b	c	D[1]	D_h	E[1]	E_h	e	e_1	k	L	L_1	v	w	y	y_1
	max	0.33	0.05	0.25	0.10	2.15	0.85	1.55	0.65				0.30	0.50				
mm	nom	0.32	0.02	0.20		2.10	0.80	1.50	0.60	0.4	1.60	0.2	0.25	0.45	0.1	0.05	0.05	0.1
	min	0.30	0.00	0.15	0.05	2.05	0.75	1.45	0.55				0.20	0.40				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1458-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1458-1	---	---	---			~~15-09-29~~ 15-11-10

Fig 3. Package outline SOT1458-1 (DHX2QFN14)

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11. Packing information

11.1 DHX2QFN14; Reel pack, SMD, 13"; Q1/T1 standard product orientation; Orderable part number ending ,431 or Z; Ordering code (12NC) ending 431

11.1.1 Packing method

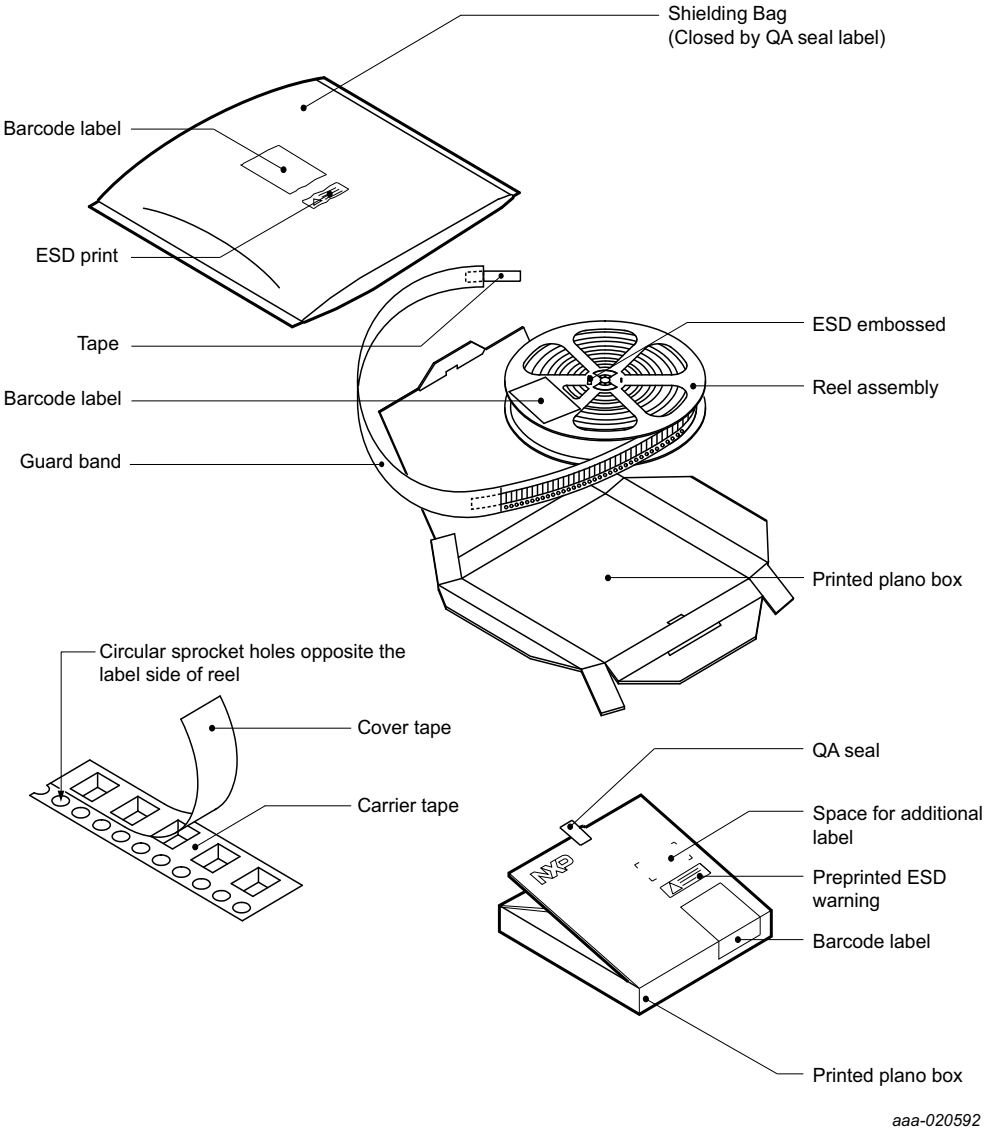


Fig 4. Reel pack for SMD: guard band; ESD shielding bag

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Table 12. Dimensions and quantities

Reel dimensions d × w (mm) [1]	SPQ/PQ (pcs) [2]	Reels per box	Outer box dimensions l × w × h (mm)
330 × 8	20000	1	342 × 338 × 25

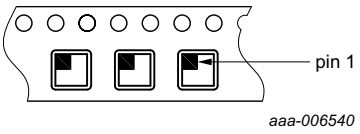
[1] d = reel diameter; w = tape width.

[2] Packing quantity dependent on specific product type.
View ordering and availability details at NXP order portal, or contact your local NXP representative.

11.1.2 Product orientation



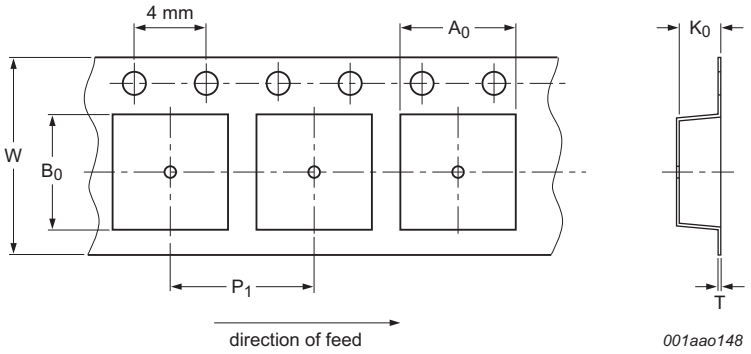
Tape pocket quadrants



Pin 1 is in quadrant Q1/T1

Fig 5. Product orientation in carrier tape

11.1.3 Carrier tape dimensions



Not drawn to scale.

Fig 6. Carrier tape dimensions

Table 13. Carrier tape dimensions
In accordance with IEC 60286-3.

A_0 (mm)	B_0 (mm)	K_0 (mm)	T (mm)	P_1 (mm)	W (mm)
1.80 ± 0.05	2.40 ± 0.05	0.45 ± 0.05	0.25 ± 0.03	4.0 ± 0.10	8.0 ± 0.1

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11.1.4 Reel dimensions

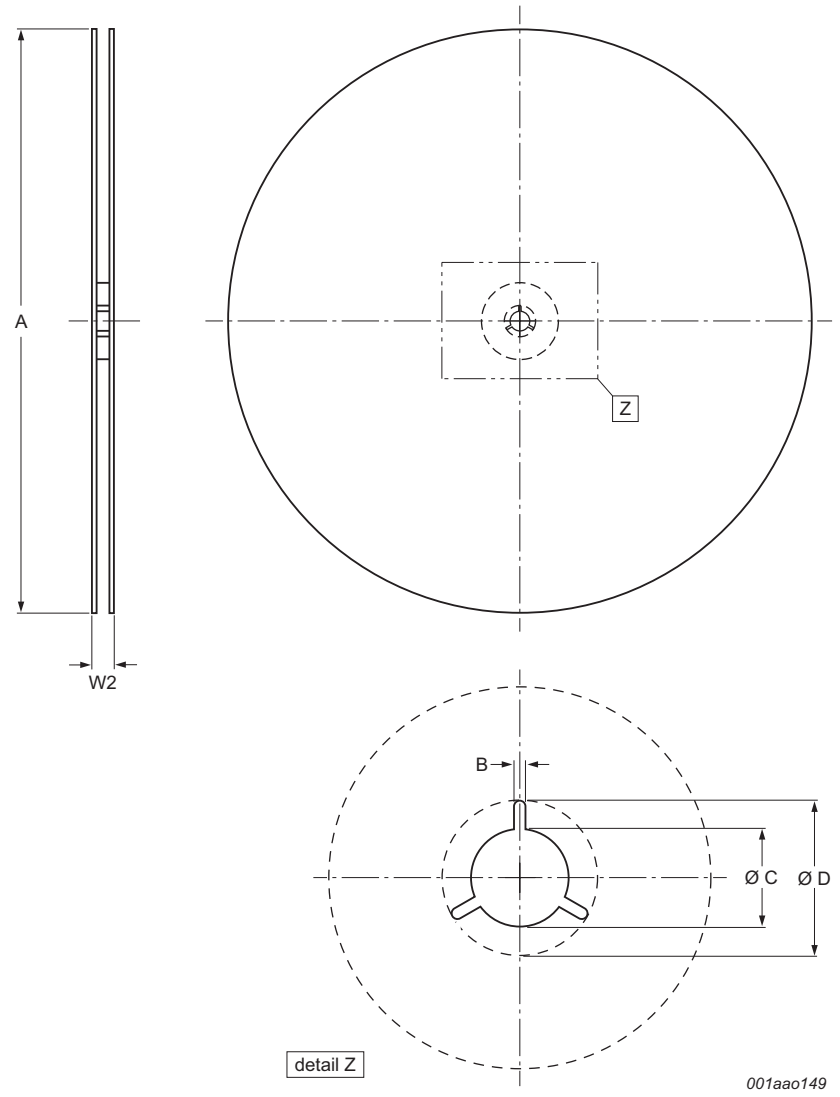


Fig 7. Schematic view of reel

Table 14. Reel dimensions
In accordance with IEC 60286-3.

A [nom] (mm)	W2 [max] (mm)	B [min] (mm)	C [min] (mm)	D [min] (mm)
330	14.4	1.5	12.8	20.2

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11.1.5 Barcode label

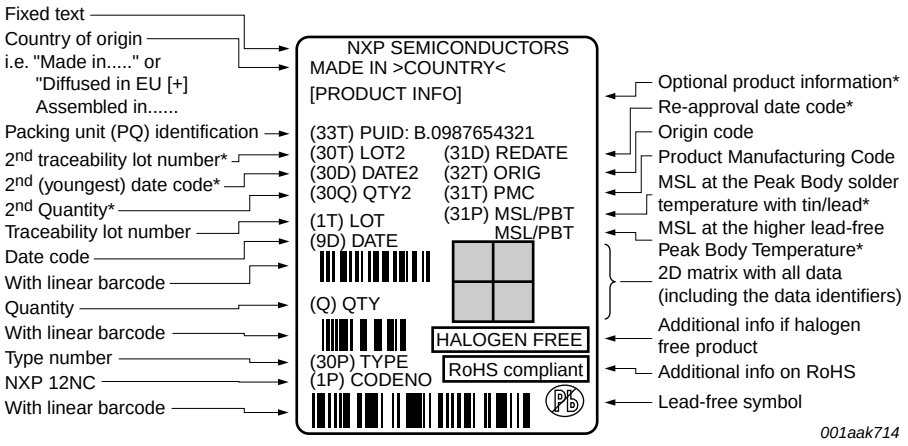


Fig 8. Example of typical box and reel information barcode label

Table 15. Barcode label dimensions

Box barcode label **l × w (mm)**	**Reel barcode label** **l × w (mm)**
100 × 75	100 × 75

12. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

12.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

12.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

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Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

12.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

12.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 9) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 16 and 17

Table 16. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

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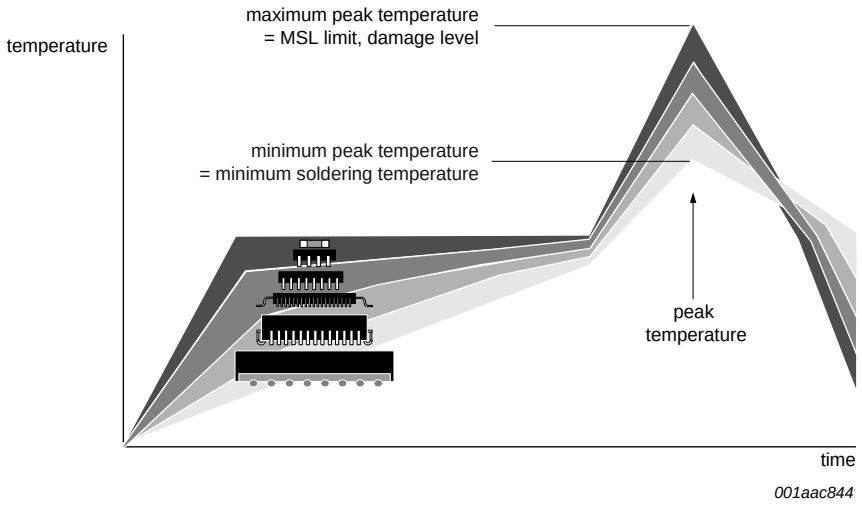
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Table 17. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 9.



MSL: Moisture Sensitivity Level

Fig 9. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

13. Abbreviations

Table 18. Abbreviations

Acronym	Description
CDM	Charged Device Model
Gbps	Gigabits per second
HBM	Human Body Model

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14. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBTL02GP023 v.2	20170814	Product data sheet	-	CBTL02GP023 v.1
Modifications:	Changed description of switch from “ON/OFF switch” to “5 Gbps rail-to-rail low insertion loss switch” throughout			
CBTL02GP023 v.1	20170601	Product data sheet	-	-

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15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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