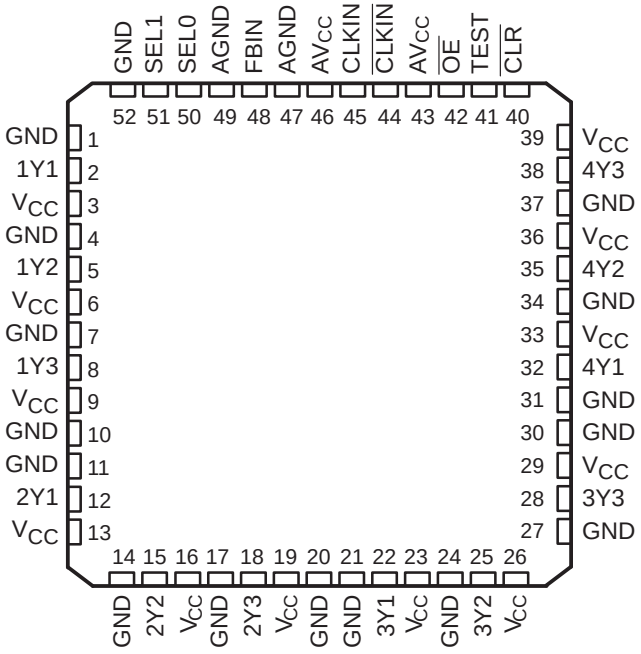
- **Low Output Skew for Clock-Distribution and Clock-Generation Applications**
- **Operates at 3.3-V V_{CC}**
- **Distributes Differential LVPECL Clock Inputs to 12 TTL-Compatible Outputs**
- **Two Select Inputs Configure Up to Nine Outputs to Operate at One-Half or Double the Input Frequency**
- **No External RC Network Required**
- **External Feedback Input (FBIN) Is Used to Synchronize the Outputs With the Clock Inputs**
- **Application for Synchronous DRAMs**
- **Outputs Have Internal 26-Ω Series Resistors to Dampen Transmission-Line Effects**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **Packaged in 52-Pin Quad Flatpack**

PAH PACKAGE
(TOP VIEW)



description

The CDC2582 is a high-performance, low-skew, low-jitter clock driver. It uses a phase-lock loop (PLL) to precisely align the frequency and phase of the clock output signals to the differential LVPECL clock (CLKIN, $\overline{\text{CLKIN}}$) input signals. It is specifically designed to operate at speeds from 50 MHz to 100 MHz or down to 25 MHz on outputs configured as half-frequency outputs. Each output has an internal 26-Ω series resistor that improves the signal integrity at the load. The CDC2582 operates at 3.3-V V_{CC}.

The feedback input (FBIN) synchronizes the frequency of the output clocks with the input clock (CLKIN, $\overline{\text{CLKIN}}$) signals. One of the twelve output clocks must be fed back to FBIN for the PLL to maintain synchronization between the differential CLKIN and $\overline{\text{CLKIN}}$ inputs and the outputs. The output used as feedback is synchronized to the same frequency as the clock (CLKIN and $\overline{\text{CLKIN}}$) inputs.

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description (continued)

The Y outputs can be configured to switch in phase and at the same frequency as differential clock inputs (CLKIN and $\overline{\text{CLKIN}}$). Select (SEL1, SEL0) inputs configure up to nine Y outputs, in banks of three, to operate at one-half or double the differential clock input frequency, depending upon the feedback configuration (see Tables 1 and 2). All output signal duty cycles are adjusted to 50% independent of the duty cycle at the input clocks.

Output-enable ($\overline{\text{OE}}$) is provided for output control. When $\overline{\text{OE}}$ is high, the outputs are in the low state. When $\overline{\text{OE}}$ is low, the outputs are active. $\overline{\text{CLR}}$ is negative-edge triggered and can be used to reset the outputs operating at half frequency. TEST is used for factory testing of the device and can be used to bypass the PLL. TEST should be strapped to GND for normal operation.

Unlike many products containing a PLL, the CDC2582 does not require external RC networks. The loop filter for the PLL is included on chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CDC2582 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required following power up and application of a fixed-frequency, fixed-phase signal at CLKIN and $\overline{\text{CLKIN}}$, as well as following any changes to the PLL reference or feedback signal. Such changes occur upon change of SEL1 and SEL0, enabling the PLL via TEST, and upon enable of all outputs via $\overline{\text{OE}}$.

The CDC2582 is characterized for operation from 0°C to 70°C.

detailed description of output configurations

The voltage-controlled oscillator (VCO) used in the CDC2582 has a frequency range of 100 MHz to 200 MHz, twice the operating frequency range of the CDC2582 outputs. The output of the VCO is divided by 2 and by 4 to provide reference frequencies with a 50% duty cycle of one-half and one-fourth the VCO frequency. SEL0 and SEL1 determine which of the two signals are buffered to each bank of device outputs.

One device output must be externally wired to FBIN to complete the PLL. The VCO operates such that the frequency of this output matches that of the CLKIN/$\overline{\text{CLKIN}}$ signals. In the case that a VCO/2 output is wired to FBIN, the VCO must operate at twice the CLKIN/$\overline{\text{CLKIN}}$ frequency, resulting in device outputs that operate at the same or one-half the CLKIN/$\overline{\text{CLKIN}}$ frequency. If a VCO/4 output is wired to FBIN, the device outputs operate at the same or twice the CLKIN/$\overline{\text{CLKIN}}$ frequency.

output configuration A

Output configuration A is valid when any output configured as a 1× frequency output in Table 1 is fed back to FBIN. The frequency range for the differential clock input is 50 MHz to 100 MHz when using output configuration A. Outputs configured as 1/2× outputs operate at half the input clock frequency, while outputs configured as 1× outputs operate at the same frequency as the differential clock input.

Table 1. Output Configuration A

INPUTS		OUTPUTS	
SEL1	SEL0	1/2× FREQUENCY	1× FREQUENCY
L	L	None	All
L	H	1Yn	2Yn, 3Yn, 4Yn
H	L	1Yn, 2Yn	3Yn, 4Yn
H	H	1Yn, 2Yn, 3Yn	4Yn

NOTE: n = 1, 2, 3

output configuration B

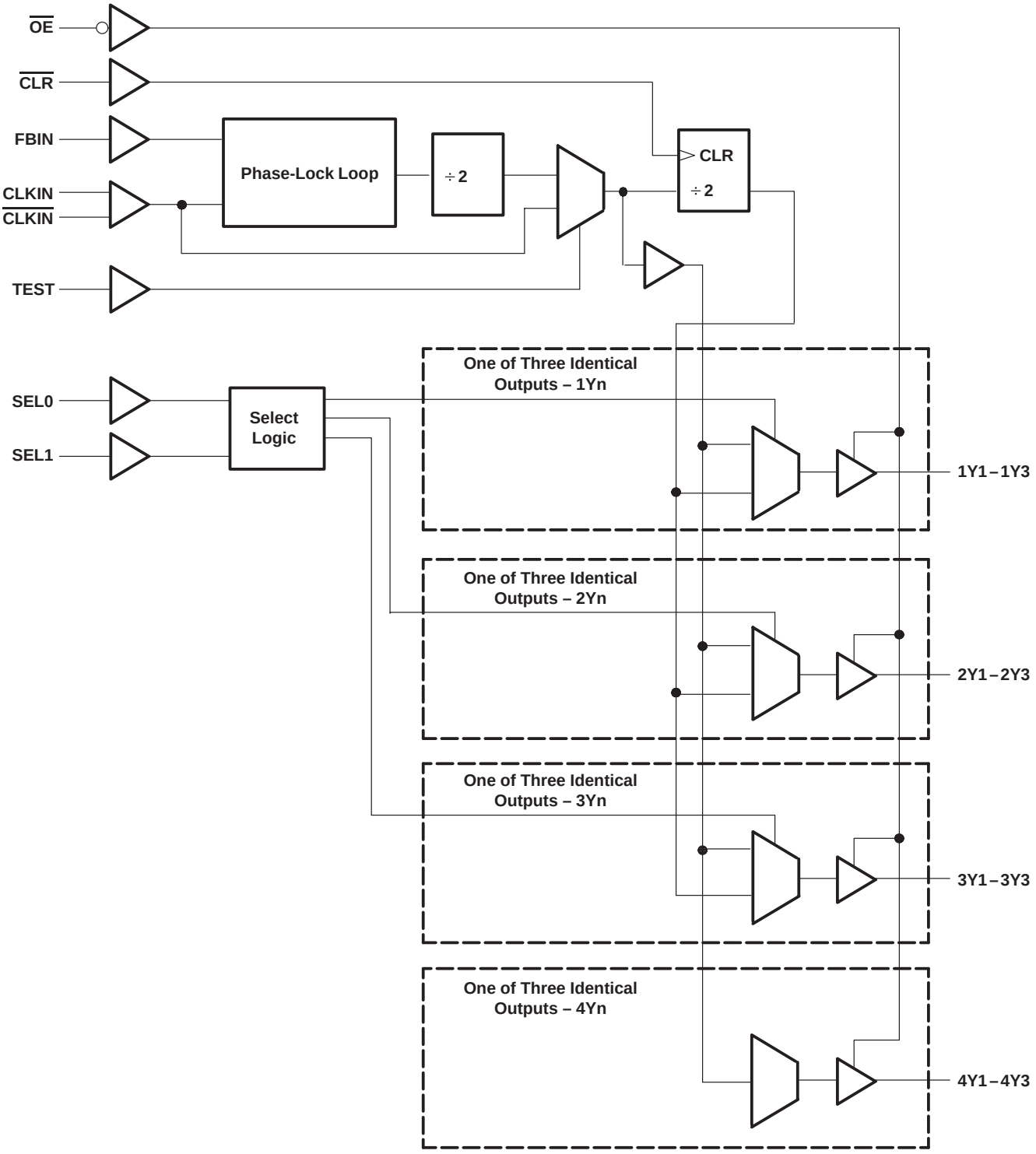
Output configuration B is valid when any output configured as a 1× frequency output in Table 2 is fed back to FBIN. The frequency range for the differential clock inputs is 25 MHz to 50 MHz when using output configuration B. Outputs configured as 1× outputs operate at the input clock frequency, while outputs configured as 2× outputs operate at double the frequency of the differential clock inputs.

Table 2. Output Configuration B

INPUTS		OUTPUTS	
SEL1	SEL0	1× FREQUENCY	2× FREQUENCY
L	L	All	None
L	H	1Yn	2Yn, 3Yn, 4Yn
H	L	1Yn, 2Yn	3Yn, 4Yn
H	H	1Yn, 2Yn, 3Yn	4Yn

NOTE: n = 1, 2, 3

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLKIN $\overline{\text{CLKIN}}$	44, 45	I	Clock input. CLKIN and $\overline{\text{CLKIN}}$ are the differential clock signals to be distributed by the CDC2582 clock-driver circuit. These inputs are used to provide the reference signal to the integrated PLL that generates the clock-output signals. CLKIN and $\overline{\text{CLKIN}}$ must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and valid CLKIN and $\overline{\text{CLKIN}}$ signals are applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
$\overline{\text{CLR}}$	40	I	Clear. $\overline{\text{CLR}}$ is used to reset the VCO/4 reference frequency. $\overline{\text{CLR}}$ is negative-edge triggered and should be strapped to V_{CC} or GND for normal operation.
FBIN	48	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hardwired to one of the twelve clock outputs to provide frequency and phase lock. The internal PLL adjusts the output clocks to obtain zero-phase delay between the FBIN and the differential clock input (CLKIN and $\overline{\text{CLKIN}}$).
$\overline{\text{OE}}$	42	I	Output enable. $\overline{\text{OE}}$ is the output enable for all outputs. When $\overline{\text{OE}}$ is low, all outputs are enabled. When $\overline{\text{OE}}$ is high, all outputs are in the high-impedance state. Since the feedback signal for the PLL is taken directly from an output terminal, placing the outputs in the high-impedance state interrupts the feedback loop; therefore, when a high-to-low transition occurs at $\overline{\text{OE}}$, enabling the output buffers, a stabilization time is required before the PLL obtains phase lock.
SEL1, SEL0	51, 50	I	Output configuration select. SEL0 and SEL1 select the output configuration for each output bank (e.g., 1×, 1/2×, or 2×) (see Tables 1 and 2).
TEST	41	I	TEST is used to bypass the PLL circuitry for factory testing of the device. When TEST is low, all outputs operate using the PLL circuitry. When TEST is high, the outputs are placed in a test mode that bypasses the PLL circuitry. TEST should be strapped to GND for normal operation.
1Y1–1Y3 2Y1–2Y3 3Y1–3Y3	2, 5, 8 12, 15, 18 22, 25, 28	O	These outputs are configured by SEL1 and SEL0 to transmit one-half or one-fourth the frequency of the VCO. The relationship between the input clock frequency and the output frequency is dependent on SEL1 and SEL0 and the frequency of the output being fed back to FBIN. The duty cycle of the Y outputs is nominally 50% independent of the duty cycle of the input clock signals. Each output has an internal series resistor to dampen transmission-line effects and improve the signal integrity at the load.
4Y1–4Y3	32, 35, 38	O	These outputs transmit one-half the frequency of the VCO. The relationship between the input clock frequency and the output frequency is dependent on the frequency of the output being fed back to FBIN. The duty cycle of the Y outputs is nominally 50% independent of the duty cycle of CLKIN. Each output has an internal series resistor to dampen transmission-line effects and improve the signal integrity at the load.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O . . . . . 24 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –20 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) . . . . . 1.2 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	3.6	V
V_{IH}	High-level input voltage	CLKIN, $\overline{\text{CLKIN}}$	V_{CC}–1.025		V
		Other inputs	2		
V_{IL}	Low-level input voltage	CLKIN, $\overline{\text{CLKIN}}$		V_{CC}–1.62	V
		Other inputs		0.8	
V_I	Input voltage		0	5.5	V
I_{OH}	High-level output current			–12	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature		0	70	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C MIN	T_A = 25°C MAX	UNIT
V_{IK}	V_{CC} = 3 V,	I_I = –18 mA			–1.2	V
V_{OH}	V_{CC} = MIN to MAX†,	I_{OH} = –100 µA		V_{CC}–0.2		V
	V_{CC} = 3 V,	I_{OH} = – 12 mA		2		
V_{OL}	V_{CC} = 3 V	I_{OL} = 100 µA			0.2	V
		I_{OL} = 12 mA			0.8	
I_I	V_{CC} = 0 or MAX†,	V_I = 3.6 V			±10	µA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1	
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		5	mA
			Outputs low		5	
C_i	V_I = 3 V or 0				4	pF
C_o	V_O = 3 V or 0				8	pF

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency	VCO is operating at four times the CLKIN/$\overline{\text{CLKIN}}$ frequency	25	50	MHz
		VCO is operating at double the CLKIN/$\overline{\text{CLKIN}}$ frequency	50	100	
	Input clock duty cycle		40%	60%	
	Stabilization time†	After SEL1, SEL0		50	µs
		After $\overline{\text{OE}}\downarrow$		50	
		After power up		50	

† Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLKIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

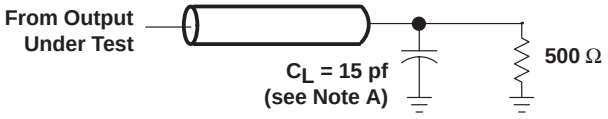
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 15 pF (see Note 4 and Figures 1, 2, and 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
Duty cycle		Y	45%	55%	
f_{max}			100		MHz
$Jitter_{(pk-pk)}$	CLKIN↑	Y↑		200	ps
$t_{phase\ error}$‡	CLKIN↑	Y	–500	500	ps
$t_{sk(o)}$‡		Y		0.5	ns
$t_{sk(pr)}$‡		Y		1	ns
t_r				1.4	ns
t_f				1.4	ns

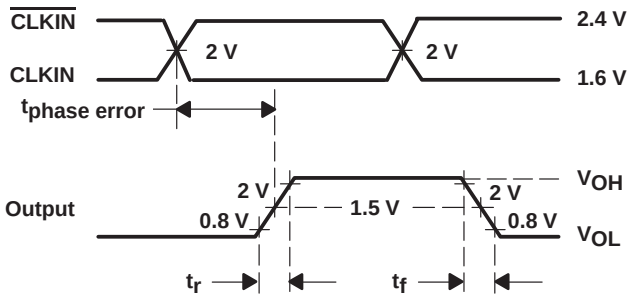
‡ The propagation delay, $t_{phase\ error}$, is dependent on the feedback path from any output to FBIN. The $t_{phase\ error}$, $t_{sk(o)}$, and $t_{sk(pr)}$ specifications are only valid for equal loading of all outputs.

NOTE 4: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS

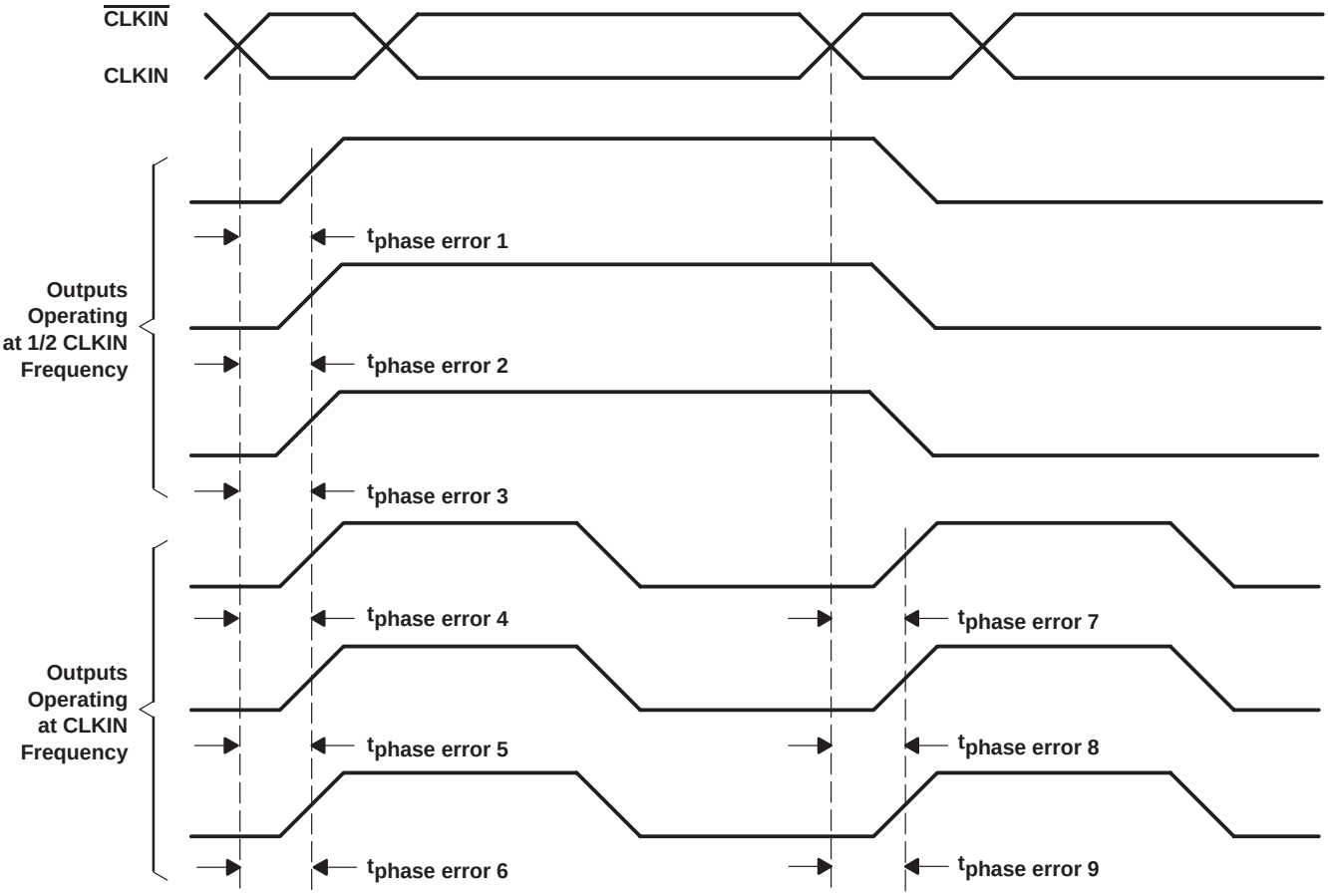


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. The outputs are measured one at a time with one transition per measurement.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

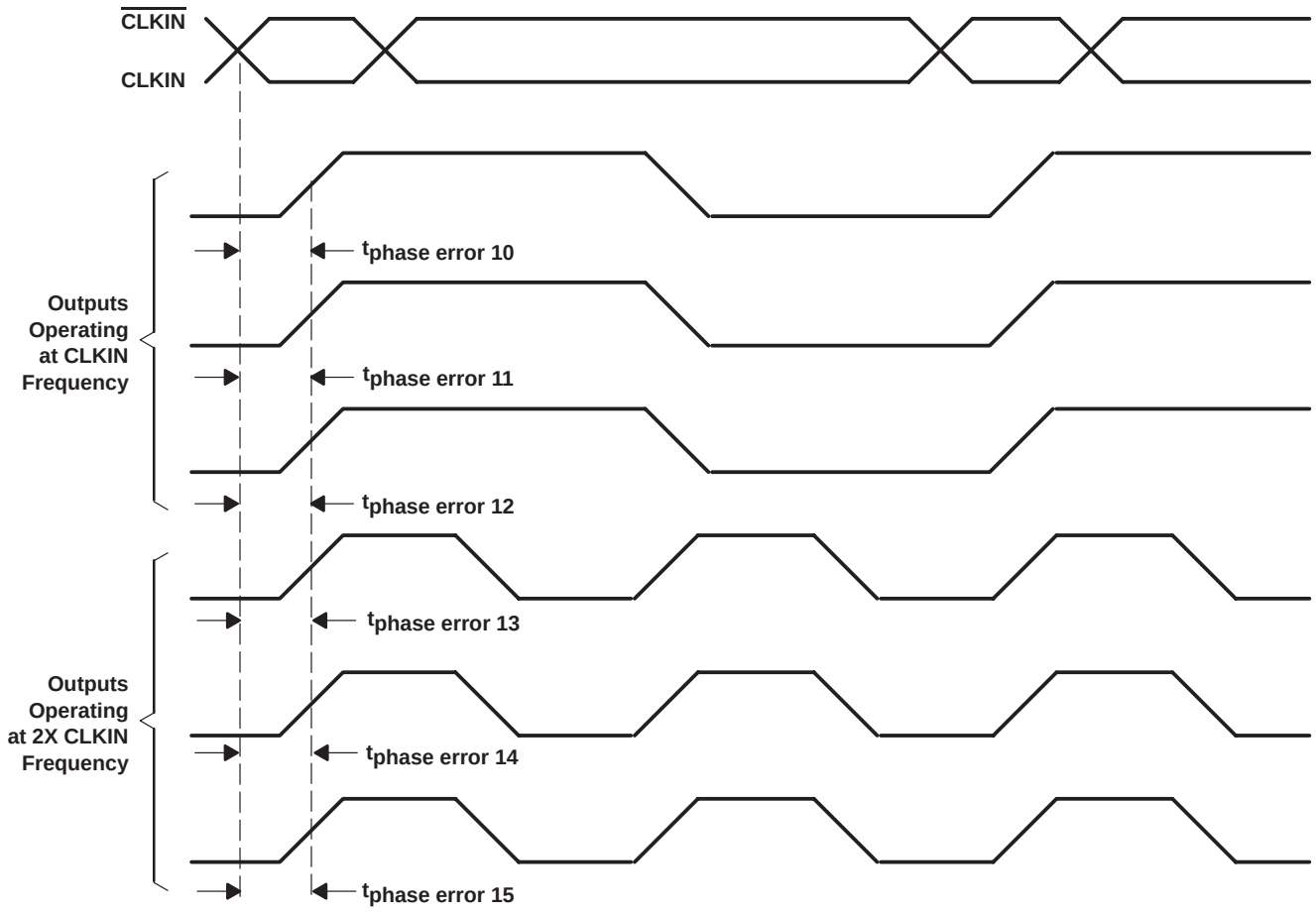


NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 1, 2, . . . 6)
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 7, 8, 9)

B. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
- The difference between the maximum and minimum $t_{phase\ error\ n}$ (n = 1, 2, . . . 6) across multiple devices under identical operating conditions
- The difference between the maximum and minimum $t_{phase\ error\ n}$ (n = 7, 8, 9) across multiple devices under identical operating conditions

Figure 2. Skew Waveforms and Calculations

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
– The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 10, 11, . . . 15)
B. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
– The difference between the maximum and minimum $t_{phase\ error\ n}$ (n = 10, 11, . . . 15) across multiple devices under identical operating conditions

Figure 3. Waveforms for Calculation of $t_{sk(o)}$ and $t_{sk(pr)}$

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