

CDC950

133-MHz DIFFERENTIAL CLOCK SYNTHESIZER/DRIVER FOR PC MOTHERBOARDS/SERVERS

SCAS646B – FEBRUARY 2001 – REVISED OCTOBER 2003

- Generates Clocks for Next Generation Microprocessors
- Uses a 14.318-MHz Crystal Input to Generate Multiple Output Frequencies
- Includes Spread Spectrum Clocking (SSC), 0.6% Downspread for Reduced EMI With Theoretical EMI of 7 dB
- Power Management Control Terminals
- Low Output Skew and Jitter for Clock Distribution
- Operates From a Single 3.3-V Supply
- Generates the Following Clocks:
 - 8 Host (Diff Pairs, 100/133 MHz)
 - 1 CLK33 (3.3 V, 33.3 MHz)
 - 1 REFCLK (3.3 V, 14.318 MHz)
 - 2 3V48 (3.3 V, 180° Shifted Pairs, 48 MHz)
- Packaged in a 48-Pin TSSOP Package

description

The CDC950 is a differential clock synthesizer/driver that generates HCLK/HCLK, CLK33, 3V48, and REFCLK system clock signals to support a computer system with next generation processors and double data rate (DDR) memory subsystems.

All output frequencies are generated from a 14.318-MHz crystal input. A reference clock input can be provided at the XIN input instead of a crystal. Two phase-locked loops (PLLs) are used to generate the host frequencies and the 48-MHz clock frequencies. On-chip loop filters and internal feedback eliminate the need for external components.

The HCLK, CLK33 clock, and 48-MHz clock outputs provide low-skew/low-jitter clock signals for reliable clock operation. All outputs have 3-state capability, which can be selected through control inputs SEL100/133, 3V48/SEL A, and 3V48/SEL B.

The outputs are either differential host clock or 3.3-V single-ended CMOS buffers. With a logic high-level on the PWRDWN terminal, the device operates normally. When a logical low-level input is applied, the device powers down completely with the HOST clock at $2 \times I_{REF}$, HOSTB is undriven, CLK33, 3V48, and REFCLK outputs are in a low-level output state and 3V48B is in a high-level output state.

The host bus can operate at 100 MHz or 133 MHz. Output frequency selection is done with the corresponding setting for SEL100/133 control input. The CLK33 (PCI) frequency is fixed to 33 MHz.

Since the CDC950 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up, as well as following changes to the SEL inputs. With the use of an external reference clock, this signal must be fixed-frequency and fixed-phase prior to stabilization time starts. The CDC950 is characterized for operation from 0°C to 85°C.

DGG PACKAGE
(TOP VIEW)

CLK33	1	48	SEL100/133
V _{DD} 3.3V	2	47	GND
3V48/SEL A	3	46	AV _{DD} 3.3V
3V48/SEL B	4	45	AGND
GND	5	44	PWRDWN
V _{DD} 3.3V	6	43	V _{DD} 3.3V
HCLK(0)	7	42	HCLK(4)
HCLK(0)	8	41	HCLK(4)
GND	9	40	GND
HCLK(1)	10	39	HCLK(5)
HCLK(1)	11	38	HCLK(5)
V _{DD} 3.3V	12	37	V _{DD} 3.3V
HCLK(2)	13	36	HCLK(6)
HCLK(2)	14	35	HCLK(6)
GND	15	34	GND
HCLK(3)	16	33	HCLK(7)
HCLK(3)	17	32	HCLK(7)
V _{DD} 3.3V	18	31	V _{DD} 3.3V
REFCLK	19	30	MultSel0
SPREAD	20	29	MultSel1
GND	21	28	GND
XIN	22	27	AGND
XOUT	23	26	I_REF
V _{DD} 3.3V	24	25	AV _{DD} 3.3V



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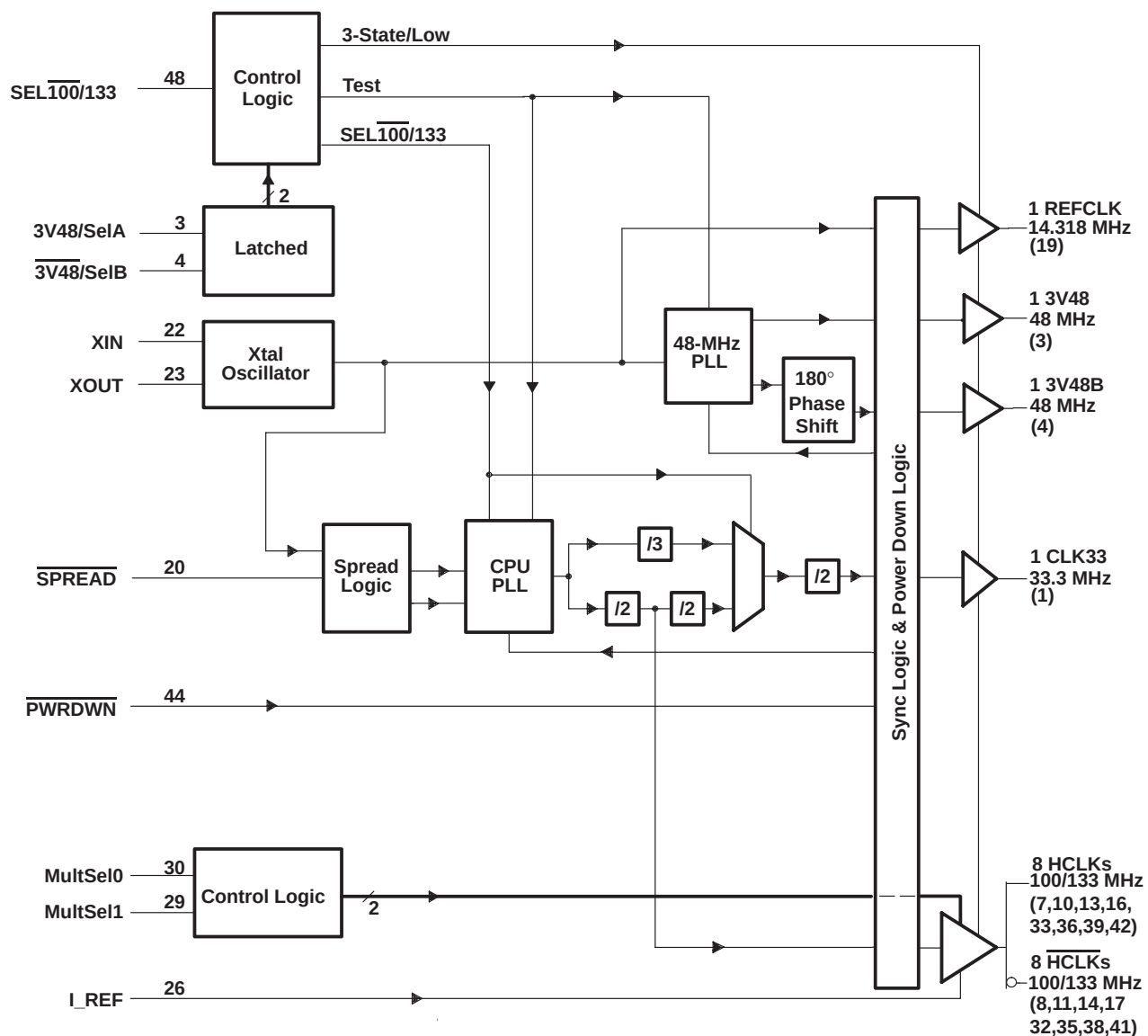
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functional block diagram



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Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
3V48/SelA, 3V48/SelB	3, 4	I/O	48-MHz 180° shifted pair clocks for USB use Logic select pins. Selects the mode of operation, see Table 1 for details.
AGND	27, 45	P	Analog ground
AV _{DD} 3.3V	25, 46	P	Power. Analog power supply
CLK33	1	O	33-MHz reference clock for PCI use, host clock divided by 3 or by 4
GND	5, 9, 15, 21, 28, 34, 40, 47	P	Ground
HCLK	7, 10, 13, 16, 33, 36, 39, 42	O	CPU and host clock outputs [7:0]. These eight differential CPU clock pairs run at 100/133 MHz. The V _{OH} swing amplitude is configured by MultSel0, MultSel1 pins. See Table 5 and Intel's CK00 document for details.
$\overline{\text{HCLK}}$	8, 11, 14, 17, 32, 35, 38, 41	O	CPU and host clock outputs [7:0]. These eight differential CPU clock pairs run at 100/133 MHz. The V _{OH} swing amplitude is configured by MultSel0, MultSel1 pins. See Table 5 and Intel's CK00 document for details.
I _{REF}	26	I	Current reference. This pin establishes the reference current for host clock parts. See Table 5 and Intel's CK00 document for details.
MultSel0	30	I	See Table 5 and Intel's CK00 document for details.
MultSel1	29	I	See Table 5 and Intel's CK00 document for details.
$\overline{\text{PWRDWN}}$	44	I	Power-down input. 3.3-V LVTTL compatible, asynchronous input that requests the device to enter the power-down mode. See Table 2 for details.
REFCLK	19	O	14.138-MHz reference clock output: 3.3 V copy of the 14.318-MHz reference clock.
SEL100/133	48	I	Active low LVTTL level logic select. SEL100/133 is used for enabling 100/133 MHz. Low = 100 MHz, high = 133 MHz
$\overline{\text{SPREAD}}$	20	U	Spread spectrum enable. 3.3-V LVTTL compatible, input that enables the spread spectrum mode when held low. See Table 4 for details.
V _{DD} 3.3V	2, 6, 12, 18, 24, 31, 37, 43	P	Power. Power supply
XIN	22	I	Crystal connection or an external reference frequency input. Connect to either a 14.138-MHz crystal or an external reference signal.
XOUT	23	O	Crystal connection. An output connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.



Function Tables

Table 1. Select Functions

INPUTS			OUTPUTS				FUNCTION
SEL100/133	SelA	SelB	HCLK, $\overline{\text{HCLK}}$	CLK33	3V48, $\overline{3V48}$	REFCLK	
0	0	0	100 MHz	33 MHz	48 MHz	14.318 MHz	Active 100 MHz
0	0	1	100 MHz	33 MHz	L, H	14.318 MHz	100 MHz mode; PLL48 powerdown
0	1	0	105 MHz	35 MHz	48 MHz	14.318 MHz	100 MHz mode 5% overclocking
0	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	All 3-state outputs
1	0	0	133 MHz	33 MHz	48 MHz	14.318 MHz	Active 133 MHz
1	0	1	127 MHz	31.7 MHz	48 MHz	14.318 MHz	133 MHz mode –5% underclocking
1	1	0	133 MHz	33 MHz	48 MHz	14.318 MHz	Test mode
1	1	1	TCLK/2	TCLK/8	TCLK/2	TCLK	Test mode (PLL bypass)

Table 2. Enable Functions

INPUT	OUTPUTS					
$\overline{\text{PWRDWN}}$	HCLK	$\overline{\text{HCLK}}$	CLK33	3V48	$\overline{3V48}$	REFCLK
0	$2 \times I_{\text{REF}}$	Hi-Z	L	L	H	L
1	On	On	On	On	On	On

Table 3. Output Buffer Specifications

BUFFER NAME	V _{DD} RANGE (V)	IMPEDANCE (Ω)	BUFFER TYPE
3V48, REFCLK	3.135 – 3.465	20–60	TYPE 3
CLK33	3.135 – 3.465	12–55	TYPE 5
HCLK/ $\overline{\text{HCLK}}$	3.135 – 3.465		TYPE X1

Table 4. Spread Spectrum Functions

INPUT	OUTPUTS
SPREAD	
0	Spread spectrum clocking active, –0.6% at HCLK/ $\overline{\text{HCLK}}$, CLK33
1	Spread spectrum clocking inactive

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Function Tables (Continued)

Table 5. Host/ $\overline{\text{HOST}}$ Output Buffer Specifications

INPUT		BOARD TARGET TRACE/TERM Z	REFERENCE R, $I_{\text{REF}} = V_{\text{DD}}/(3 R_r)$	OUTPUT CURRENT I_{OH}	V_{OH} at Z
MultSel0	MultSel1				
0	0	60 Ω	$R_r = 475\ 1\%$, $I_{\text{REF}} = 2.32\ \text{mA}$	$5 \times I_{\text{REF}}$	0.71 V at 60 Ω
0	0	50 Ω	$R_r = 475\ 1\%$, $I_{\text{REF}} = 2.32\ \text{mA}$	$5 \times I_{\text{REF}}$	0.59 V at 50 Ω
0	1	60 Ω	$R_r = 475\ 1\%$, $I_{\text{REF}} = 2.32\ \text{mA}$	$6 \times I_{\text{REF}}$	0.85 V at 60 Ω
0	1	50 Ω	$R_r = 475\ 1\%$, $I_{\text{REF}} = 2.32\ \text{mA}$	$6 \times I_{\text{REF}}$	0.71 V at 50 Ω
1	0	60 Ω	$R_r = 475\ 1\%$, $I_{\text{REF}} = 2.32\ \text{mA}$	$4 \times I_{\text{REF}}$	0.56 V at 60 Ω
1	0	50 Ω	$R_r = 475\ 1\%$, $I_{\text{REF}} = 2.32\ \text{mA}$	$4 \times I_{\text{REF}}$	0.47 V at 50 Ω
1	1	60 Ω	$R_r = 475\ 1\%$, $I_{\text{REF}} = 2.32\ \text{mA}$	$7 \times I_{\text{REF}}$	0.99 V at 60 Ω
1	1	50 Ω	$R_r = 475\ 1\%$, $I_{\text{REF}} = 2.32\ \text{mA}$	$7 \times I_{\text{REF}}$	0.82 V at 50 Ω
0	0	30 (dc equivalent)	$R_r = 221\ 1\%$, $I_{\text{REF}} = 5\ \text{mA}$	$5 \times I_{\text{REF}}$	0.75 V at 30 Ω
0	0	25 (dc equivalent)	$R_r = 221\ 1\%$, $I_{\text{REF}} = 5\ \text{mA}$	$5 \times I_{\text{REF}}$	0.62 V at 25 Ω
0	1	30 (dc equivalent)	$R_r = 221\ 1\%$, $I_{\text{REF}} = 5\ \text{mA}$	$6 \times I_{\text{REF}}$	0.90 V at 30 Ω
0	1	25 (dc equivalent)	$R_r = 221\ 1\%$, $I_{\text{REF}} = 5\ \text{mA}$	$6 \times I_{\text{REF}}$	0.75 V at 25 Ω
1	0	30 (dc equivalent)	$R_r = 221\ 1\%$, $I_{\text{REF}} = 5\ \text{mA}$	$4 \times I_{\text{REF}}$	0.60 V at 30 Ω
1	0	25 (dc equivalent)	$R_r = 221\ 1\%$, $I_{\text{REF}} = 5\ \text{mA}$	$4 \times I_{\text{REF}}$	0.5 V at 25 Ω
1	1	30 (dc equivalent)	$R_r = 221\ 1\%$, $I_{\text{REF}} = 5\ \text{mA}$	$7 \times I_{\text{REF}}$	1.05 V at 30 Ω
1	1	25 (dc equivalent)	$R_r = 221\ 1\%$, $I_{\text{REF}} = 5\ \text{mA}$	$7 \times I_{\text{REF}}$	0.84 V at 25 Ω

NOTE: The entries in **boldface** are the primary system configurations of interest. The outputs should be optimized for these configurations.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage range, V_{DD}	–0.5 V to 4.3 V
Input voltage range, V_{I} (see Note 1)	–0.5 V to $V_{\text{DD}} + 0.5\ \text{V}$
Voltage range applied to any output in the high-impedance or power-off state, V_{O} (see Note 1)	–0.5 V to $V_{\text{DD}} + 0.5\ \text{V}$
Current into any output in the low state, I_{O}	$2 \times$ rated I_{OL}
Input clamp current, I_{IK} : ($V_{\text{I}} < 0$)	–50 mA
($V_{\text{I}} > V_{\text{DD}}$)	50 mA
Output clamp current, I_{OK} : ($V_{\text{O}} < 0$)	–50 mA
($V_{\text{O}} > V_{\text{DD}}$)	50 mA
Package thermal impedance, θ_{JA} (see Note 2)	89°C/W
Maximum power dissipation at $T_{\text{A}} = 55^\circ\text{C}$ (in still air) (see Note 3)	1070 mW
Operating free-air temperature range, T_{A}	–0°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for the through-hole packages, which use a trace length of zero.
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.



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DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR [†] ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DGG	1400 mW	11.2 mW/°C	900 mW	730 mW

[†] This is the inverse of the traditional junction-to-case thermal resistance ($R_{\theta JA}$) and uses a board-mounted device at 89°C/W

recommended operating conditions (see Note 4)

		MIN	NOM‡	MAX	UNIT
Supply voltages, V _{DD} , AV _{DD}		3.135	3.3	3.465	V
High-level input voltage, V _{IH}		2			
Low-level input voltage, V _{IL}		0.8			
Input voltage, V _I		−0.3	V _{DD} + 0.3		
High-level output current, I _{OH}	HCLK/ <u>HCLK</u>	−40			mA
	CLK33	−18			
	3V48/SelA and <u>3V48/SelB</u>	−14			
	REFCLK	−14			
Low-level output current, I _{OL}	HCLK/ <u>HCLK</u>	0			
	CLK33	12			
	3V48/SelA and <u>3V48/SelB</u>	9			
	REFCLK	9			
Reference frequency, f _(XIN) [§]	Test mode	14			MHz
Crystal, f _(XTAL) [¶]	Normal mode	13.8	14.318	14.8	
Operating free-air temperature, T _A		0	85		°C

[‡] All nominal values are measured at their respective nominal V_{DD} values.

[§] Reference frequency is a test clock driven on the XIN input during the device test mode or normal mode. In test mode, XIN can be driven externally up to $f_{(XIN)} = 16$ MHz. If XIN is driven externally, XOUT is floating.

[¶] This is a series fundamental crystal with $f_0 = 14.31818$ MHz

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V _{IK}	Input clamp voltage		V _{DD} = 3.135 V,	I _I = –18 mA			–1.2	V
I _{IH}	High-level input current	All inputs except SelA, SelB	V _{DD} = 3.465 V,	V _I = V _{DD}			5	μA
I _{IL}	Low-level input current	All inputs except SelA, SelB	V _{DD} = 3.465 V,	V _I = GND			–5	μA
I _{OZ}	High-impedance-state output current	All outputs including SelA, SelB	V _{DD} = 3.465 V	3V48/SelA, 3V48/SelB = H, SEL100/133 = L, V _O = V _{DD} or GND, PWRDWN = H			±10	μA
I _{DD(Z)}	High-impedance-state supply current [‡]		V _{DD} = 3.465 V	3V48/SelA, 3V48/SelB = H, SEL100/133 = L, PWRDWN = H		19	25	mA
I _{DD(PD)}		SelA, SelB = L		VDD Supply		43	47	mA
A _I DD(PD)	PWRDWN state supply current [‡]	R _(ref) = 475 Ω PWRDWN = L		AVDD Supply		3.4	4.2	mA
I _{DD(D)}	Dynamic supply current [‡]	V _{DD} = 3.465 V, R _{ref} = 475 Ω, I _O = 6 × I _{ref}	PWRDWN = H SSC = ON/OFF C _L = MAX	100 MHz		173	190	mA
				133 MHz		183	200	
A _I DD	Analog power supply current	V _{DD} = 3.465 V	100 MHz and SSC off			19	24	mA
			133 MHz and SSC off			26	33	
			100 MHz and SSC on			26	33	
			133 MHz and SSC on			35	45	
C _I	Input capacitance [§]		V _{DD} = 3.3 V,	V _I = V _{DD} or GND		2	5	pF
C _(XTAL)	Crystal load capacitance [¶]		Effective capacity between C _{IN} and C _{OUT}			13.5	22.5	

[†] All typical values are measured at their respective nominal V_{DD} values.

[‡] C_L = MAX = 5 pF, R_S = 33.2 Ω, R_p = 49.9 Ω at HCLK/HCLK (Type X1)

C_L = MAX = 20 pF, R_L = 500 Ω at 48 MHz, REF (Type 3)

C_L = MAX = 30 pF, R_L = 500 Ω at CLK33 (Type 5)

[§] These parameters are assured by design and lab characterization, not 100% production tested.

[¶] This is the corresponding capacitive load for the XTAL in this oscillator application (Pierce oscillator)

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)**HCLK/HCLK (Type X1)**

PARAMETER	TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
r_O Output resistance			3000			Ω
V_O Output voltage					1.2	V
I_O Output current	$V_{DD} = 3.30\text{ V nom}$	All combinations of Table 5, See Note 5	-7%		7%	mA
	$V_{DD} = 3.30\text{ V, } \pm 5\%$		$I_{(NOM)}$		$I_{(NOM)}$	
C_O Output capacitance	$V_{DD} = 3.30\text{ V nom}$	$V_O = V_{DD}\text{ GND}$		3.5		pF

NOTE 5: $I_{(NOM)}$ is output current (I_{OH}) of table 5.**3V48, 3V48REFCLK (Type 3)**

PARAMETER			TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V _{OH}	High-level output voltage		V _{DD} = min to max, I _{OH} = −1 mA		V _{DD} − 0.1			V
			V _{DD} = 3.135 V, I _{OH} = −14 mA		2.4			
V _{OL}	Low-level output voltage		V _{DD} = min to max, I _{OL} = 1 mA		0.1			
			V _{DD} = 3.135 V, I _{OL} = 9 mA		0.18 0.4			
I _{OH}	High-level output current		V _{DD} = 3.135 V, V _O = 1 V		−29			mA
			V _{DD} = 3.3 V, V _O = 1.65 V		−37			
			V _{DD} = 3.465 V, V _O = 3.135 V		−11 −23			
I _{OL}	Low-level output current		V _{DD} = 3.135 V, V _O = 1.95 V		29			
			V _{DD} = 3.3 V, V _O = 1.65 V		39			
			V _{DD} = 3.465 V, V _O = 0.4 V		16 27			
C _O	Output capacitance		V _{DD} = 3.3 V, V _O = V _{DD} or GND		4.5		7	pF
Z _O	Output impedance	High state	V _O = 0.5 V _{DD} , V _O /I _{OH}		20	40	60	Ω
		Low state	V _O = 0.5 V _{DD} , V _O /I _{OL}		20	40	60	

[†] All typical values are measured at their respective nominal V_{DD} values.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

CLK33 (Type 5)

PARAMETER			TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V _{OH}	High-level output voltage		V _{DD} = min to max, I _{OH} = -1 mA		V _{DD} - 0.1			V
			V _{DD} = 3.135 V, I _{OH} = -18 mA		2.4			
V _{OL}	Low-level output voltage		V _{DD} = min to max, I _{OL} = 1 mA		0.1			
			V _{DD} = 3.135 V, I _{OL} = 12 mA		0.15	0.4		
I _{OH}	High-level output current		V _{DD} = 3.135 V, V _O = 1 V		-33			mA
			V _{DD} = 3.3 V, V _O = 1.65 V		-53			
			V _{DD} = 3.465 V, V _O = 3.135 V		-16	-33		
I _{OL}	Low-level output current		V _{DD} = 3.135 V, V _O = 1.95 V		30			
			V _{DD} = 3.3 V, V _O = 1.65 V		51			
			V _{DD} = 3.465 V, V _O = 0.4 V		21	38		
C _O	Output capacitance		V _{DD} = 3.3 V, V _O = V _{DD} or GND		4.5		7.5	pF
Z _O	Output impedance	High state	V _O = 0.5 V _{DD} , V _O /I _{OH}		12	35	55	Ω
		Low state	V _O = 0.5 V _{DD} , V _O /I _{OL}		12	35	55	

[†] All typical values are measured at their respective nominal V_{DD} values.

switching characteristics, V_{DD} = 3.135 V to 3.465 V, T_A = 0°C to 85°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _(over)	Overshoot [†]			HCLK/HCLK 0.7-V amplitude	V _{OH} + 200			mV
V _(under)	Undershoot [†]				V _{OL} – 200			
V _(over)	Overshoot [†]			Other clocks, C _L = worst case	GND – 0.7			V
V _(under)	Undershoot [†]				V _{DD} + 0.7			
t _{PZL}	Output enable time from low level	SEL100/133	All outputs	SEL100/133 ↑ R _{ref} = 475 Ω	10			ns
t _{PZH}	Output enable time to high level	SEL100/133	All outputs	SEL100/133 ↑ R _{ref} = 475 Ω	10			
t _{PHZ}	Output disable time from high level	SEL100/133	All outputs	SEL100/133 ↓ R _{ref} = 475 Ω	10			
t _{PLZ}	Output disable time from low level	SEL100/133	All outputs	SEL100/133 ↓ R _{ref} = 475 Ω	10			
t _s	Stabilization time [‡]	V _{DD}	All outputs	After power up	0.1			ms
		PWRDWN	All outputs	From PWRDWN ↑	0.25			ms

[†] These parameters are assured by design and lab characterization, not 100% production tested.

[‡] Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at XIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics tables are not applicable. Stabilization time is defined as the time since V_{DD} achieves its nominal operating level (3.3 V) or PWRDWN transition from a low to a high level (2 V) until the output frequency is stable and operating within specification.



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switching characteristics, $V_{DD} = 3.135 \text{ V}$ to 3.465 V , $T_A = 0^\circ\text{C}$ to 85°C (continued)

HCLK/HCLK (Type X1), $C_L = 2 \text{ pF}$, $R_{ref} = 475 \Omega$, $6 \times R_{ref}$

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
HCLK clock period [‡]			f(HCLK) = 100 MHz		10		10.2	ns
			f(HCLK) = 133 MHz		7.5		7.65	
T _{jit(cc)}	Cycle-to-cycle jitter		f(HCLK) = 100 or 133 MHz	SSC off	−80		80	ps
				SSC on	−110		110	
t _{dc}	Duty cycle		f(HCLK) = 100 or 133 MHz, Crossing point		45%		55%	
t _{sk(o)}	HCLK bus skew		f(HCLK) = 100 or 133 MHz, Crossing point			70		ps
t _r	Rise time [†]	0.7-V amplitude	V _O = 0.14 V to 0.56 V		175		700	ps
t _f	Fall time [†]		V _O = 0.14 V to 0.56 V		175		700	
v _(cross)	Cross point voltages [†]	0.7-V amplitude	f(HCLK) = 100 or 133-MHz HCLK and $\overline{\text{HCLK}}$		45% V _{OH}		55% V _{OH}	V

[†] These parameters are assured by design and lab characterization, not 100% production tested.

[‡] The average over any 1- μs period of time is greater than the minimum specified period.

CLK33 (Type 5), $C_L = 30 \text{ pF}$, $R_L = 500 \Omega$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PCI clock period [†]		$f_{(HCLK)} = 100 \text{ or } 133 \text{ MHz}$	30	30.06	30.6	ns
$T_{jit(cc)}$	Cycle-to-cycle jitter	$f_{(HCLK)} = 100 \text{ or } 133 \text{ MHz}$	-150		150	ps
t_{dc}	Duty cycle	$f_{(CLK33)} = 33.3 \text{ MHz}$	45%		55%	
t_r	Rise time	$V_O = 0.4 \text{ V to } 2.4 \text{ V}$	0.5		2	ns
t_f	Fall time	$V_O = 0.4 \text{ V to } 2.4 \text{ V}$	0.5		2	

[†] The average over any 1- μs period of time is greater than the minimum specified period.

3V48 (Type 3), $C_L = 20 \text{ pF}$, $R_L = 500 \Omega$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
3V48 clock period		$f_{(HCLK)} = 100 \text{ or } 133 \text{ MHz}$		20.83		ns
$T_{jit(cc)}$	Cycle-to-cycle jitter	$f_{(HCLK)} = 100 \text{ or } 133 \text{ MHz}$	-300		300	ps
t_{dc}	Duty cycle	$f_{(3V48)} = 48 \text{ MHz}$	45%		55%	
t_r	Rise time	$V_O = 0.4 \text{ V to } 2.4 \text{ V}$	1		4	ns
t_f	Fall time	$V_O = 0.4 \text{ V to } 2.4 \text{ V}$	1		4	

REF (Type 3), $C_L = 20 \text{ pF}$, $R_L = 500 \Omega$

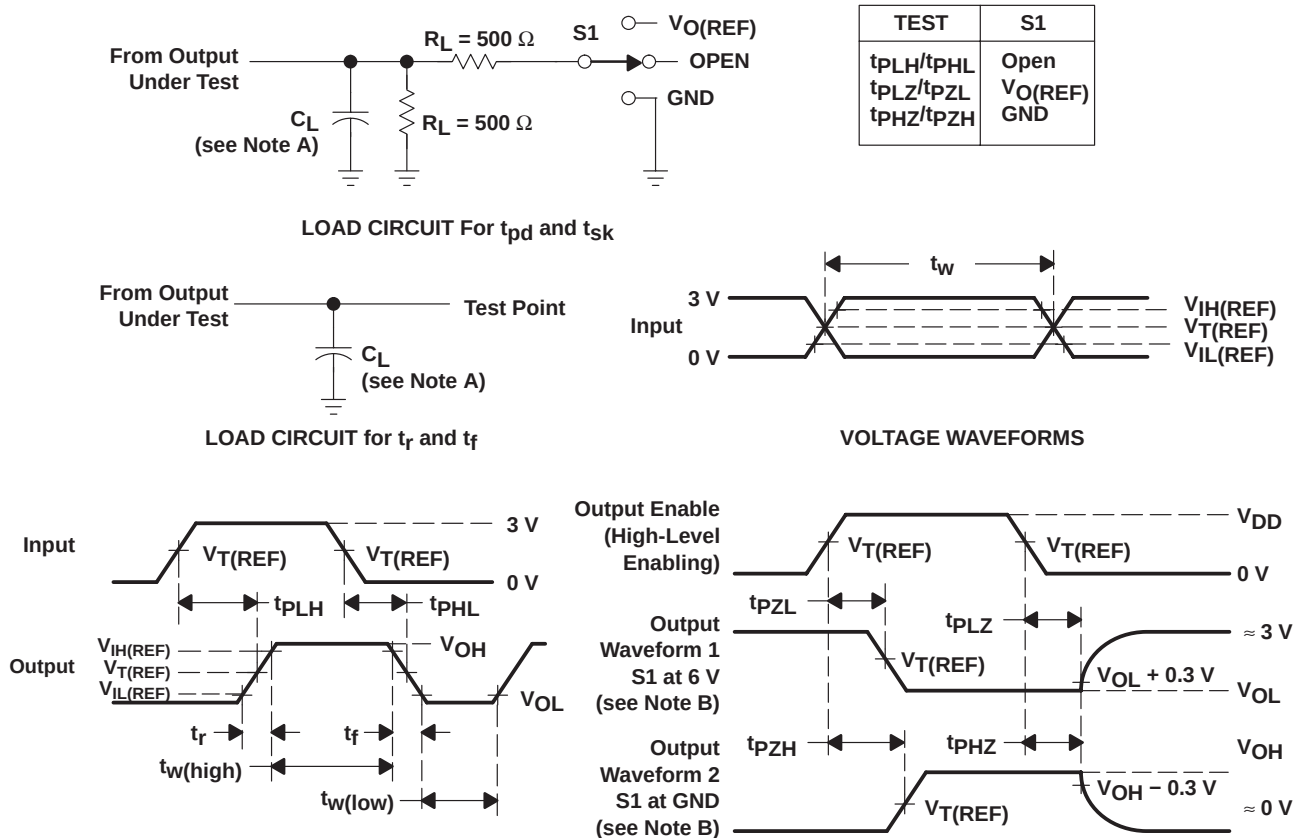
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REF clock period		$f_{(REF)} = 14.318 \text{ MHz}$		69.84		ns
$T_{jit(cc)}$	Cycle-to-cycle jitter	$f_{(HCLK)} = 100 \text{ or } 133 \text{ MHz}$	-0.5		0.5	
t_{dc}	Duty cycle	$f_{(REF)} = 14.318 \text{ MHz}$	45%		55%	
t_r	Rise time	$V_O = 0.4 \text{ V to } 2.4 \text{ V}$	1		4	ns
t_f	Fall time	$V_O = 0.4 \text{ V to } 2.4 \text{ V}$	1		4	

CDC950

133-MHz DIFFERENTIAL CLOCK SYNTHESIZER/DRIVER FOR PC MOTHERBOARDS/SERVERS

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PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance. $C_L = 2$ pF (HCLK, $\overline{\text{HCLK}}$), $C_L = 20$ pF (48 MHz, REF), $C_L = 30$ pF (CLK33).
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 14.318 MHz, $Z_O = 50$ Ω , $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

PARAMETER	3.3-V INTERFACE	UNIT
$V_{IH(REF)}$ High-level reference voltage	2.4	V
$V_{IL(REF)}$ Low-level reference voltage	0.4	
$V_{T(REF)}$ Input threshold reference voltage	1.5	
$V_{O(REF)}$ Off-state reference voltage	6	

Figure 1. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

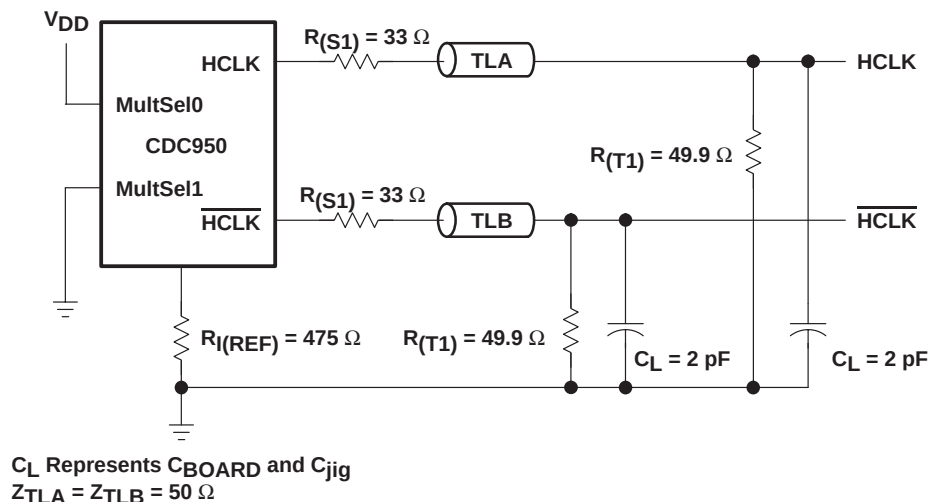


Figure 2. Load Circuit for HCLK Bus

spread spectrum clock (SSC) implementation for CDC950

Simultaneously switching at a fixed frequency generates a significant power peak at the selected frequency, which in turn causes EMI disturbance to the environment. The purpose of the internal frequency modulation of the CPU-PLL allows energy to be distributed to many different frequencies which reduces the power peak.

A typical characteristic for a single frequency spectrum and a frequency modulated spectrum is shown in Figure 3.

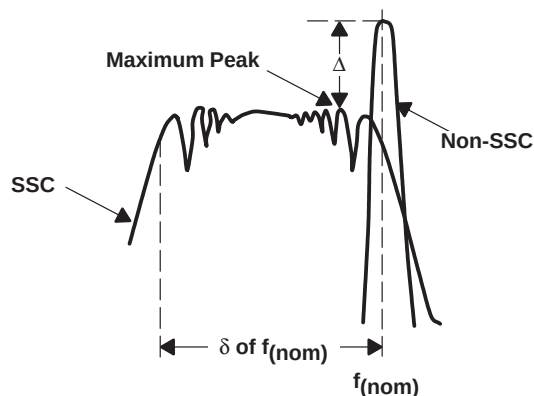


Figure 3. Frequency Power Spectrum With and Without the Use of SSC

The modulated spectrum has its distribution (left side) associated with the single-frequency spectrum which indicates a down-spread modulation.

The peak reduction depends on the modulation scheme and modulation profile. System performance and timing requirements are the limiting factors for actual design implementations. The implementation was driven to keep the average clock frequency close to its upper specification limit. The modulation amount was set to approximately -0.6% .

To allow a downstream PLL to follow the frequency modulated signal, the bandwidth of the modulation signal is limited in order to minimize SSC induced tracking skew jitter. The modulation frequency is approximately 31 kHz.

CDC950

133-MHz DIFFERENTIAL CLOCK SYNTHESIZER/DRIVER FOR PC MOTHERBOARDS/SERVERS

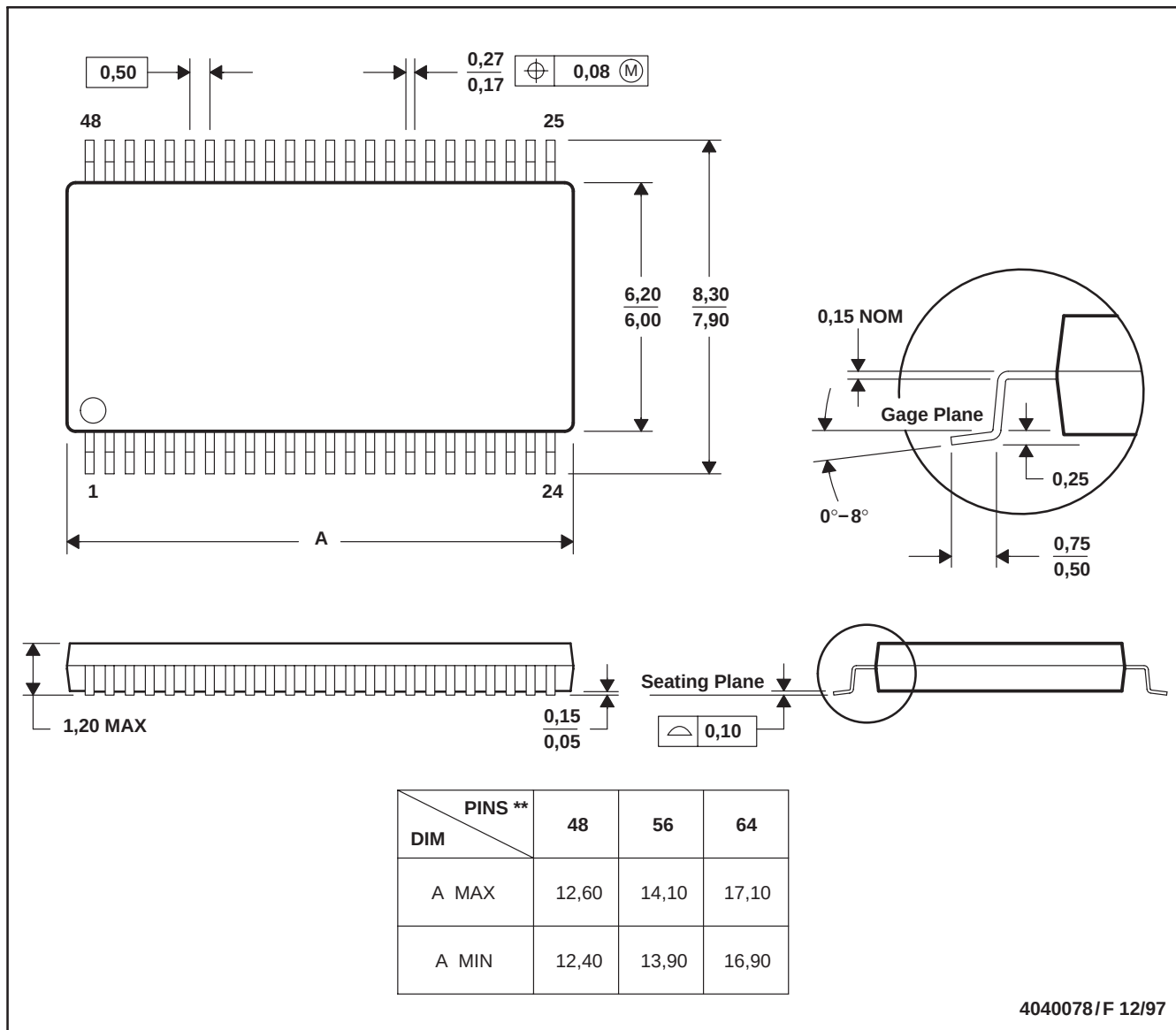
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MECHANICAL DATA

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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