SILICON LABS

128/64 SEGMENT LCD DRIVER

LCD Driver
- Controls up to 128 segments (48-pin packages) or 64 segments (32-pin package)
- Supports static, 2-mux, 3-mux, and 4-mux displays
- On-chip bias generation with internal charge pump
- Low power blink capability

GPIO Expander
- Expands GPIO count by up to 36 pins (48-pin packages) or 20 pins (32-pin package)
- GPIO pins may be configured to push-pull or open-drain outputs with two drive levels. GPIO may also be used as digital inputs (CP2400/1/2/3 pullups included)
- Port Match Capability can wake up host controller using interrupt pin
- 5 V Tolerant I/O

Real Time Clock, SmaRTClock
- Precision time keeping with 32.768 kHz watch crystal; self-oscillate mode requires no external crystal; accepts external 32 kHz CMOS clock
- 36-hour programmable counter with wake up alarm
- Can wake up the host controller using interrupt pin
- Low power (<1.5 µA)

256 Bytes RAM
- General purpose RAM expands the memory available to host controller.

16-bit Timers
- Two general purpose 16-bit timers

Clock Sources
- 20 MHz Internal oscillator
- Can be clocked from an external CMOS clock

Digital Bus Interface
- 4-wire SPI Interface operates up to 2.5 Mbps with synchronous external clock or up to 1 Mbps with internal clock (CP2400/2 only).
- 2-wire SMBus/I^2C Interface operates up to 400 kHz with internal clock (CP2401/3 only).
- Dedicated $\overline{RST}$ and $\overline{INT}$ pins.
- Optional $\overline{CLK}$ pin can be used as a CMOS clock input.
- Optional $\overline{PWR}$ pin (SMBus/I^2C devices only) places the device in a low power mode. SPI devices use the NSS pin to place the device in a low power mode.

Low Power
- 1.8–3.6 V operation with integrated LDO
- Ultra Low Power Mode w/ LCD (<3 µA typical)
- Shutdown current (0.05 µA typical)

Example Applications
- Handheld Equipment
- Utility Meters
- Thermostat Display
- Home Security Systems

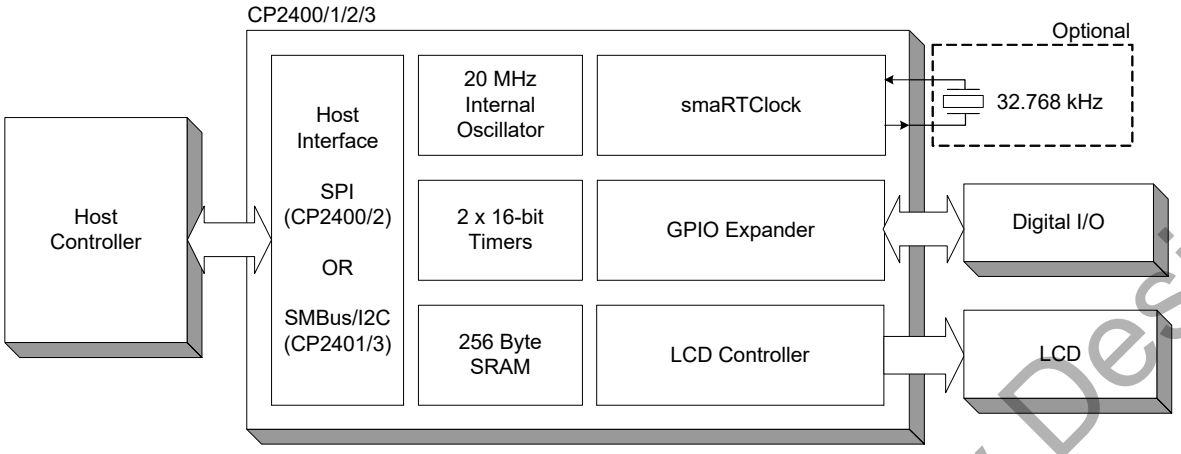
Packages
- Pb-free 48-pin QFP (9x9 mm footprint) [-Q]
- Pb-free 48-pin QFN (7x7 mm footprint) [-M]
- Pb-free 32-pin QFN (5x5 mm footprint)

Ordering Part Numbers
- CP2400-GM (SPI Interface) - End of Life (EOL)
- CP2400-GQ (SPI Interface)
- CP2401-GM (SMBus/I^2C Interface)
- CP2401-GQ (SMBus/I^2C Interface) - EOL
- CP2402-GM (SPI Interface) - EOL
- CP2403-GM (SMBus/I^2C Interface) - EOL

Temperature Range: –40 to +85 °C

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1. System Overview

CP2400/1/2/3 devices are fixed function LCD drivers that can also be used for expanding GPIO, timekeeping, and increasing available system RAM by up to 256 bytes. The device is controlled using direct and indirect internal registers accessible through the 4-wire SPI or 2-wire SMBus interface. All digital pins on the device are 5 V tolerant.

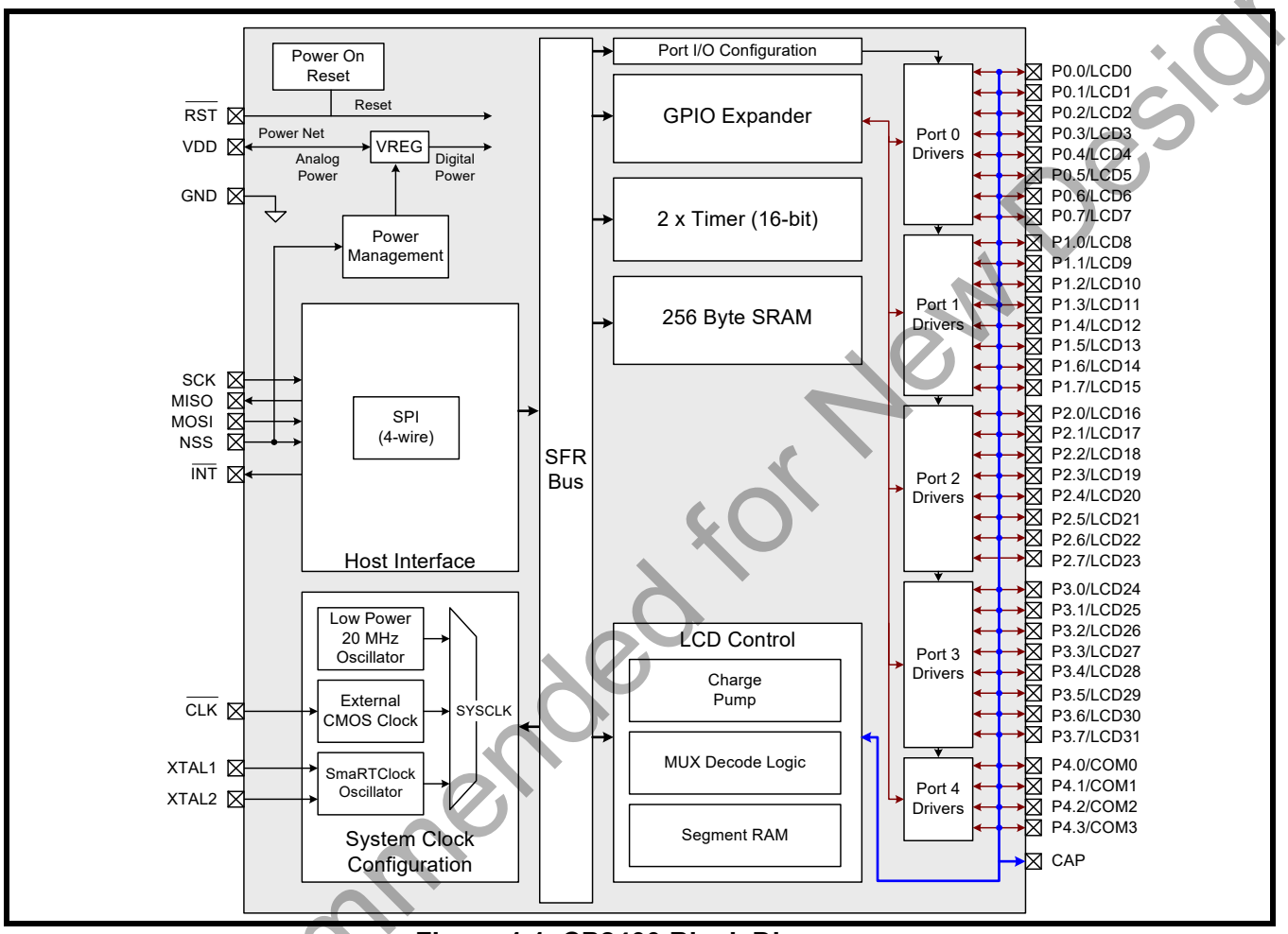


Figure 1.1. CP2400 Block Diagram

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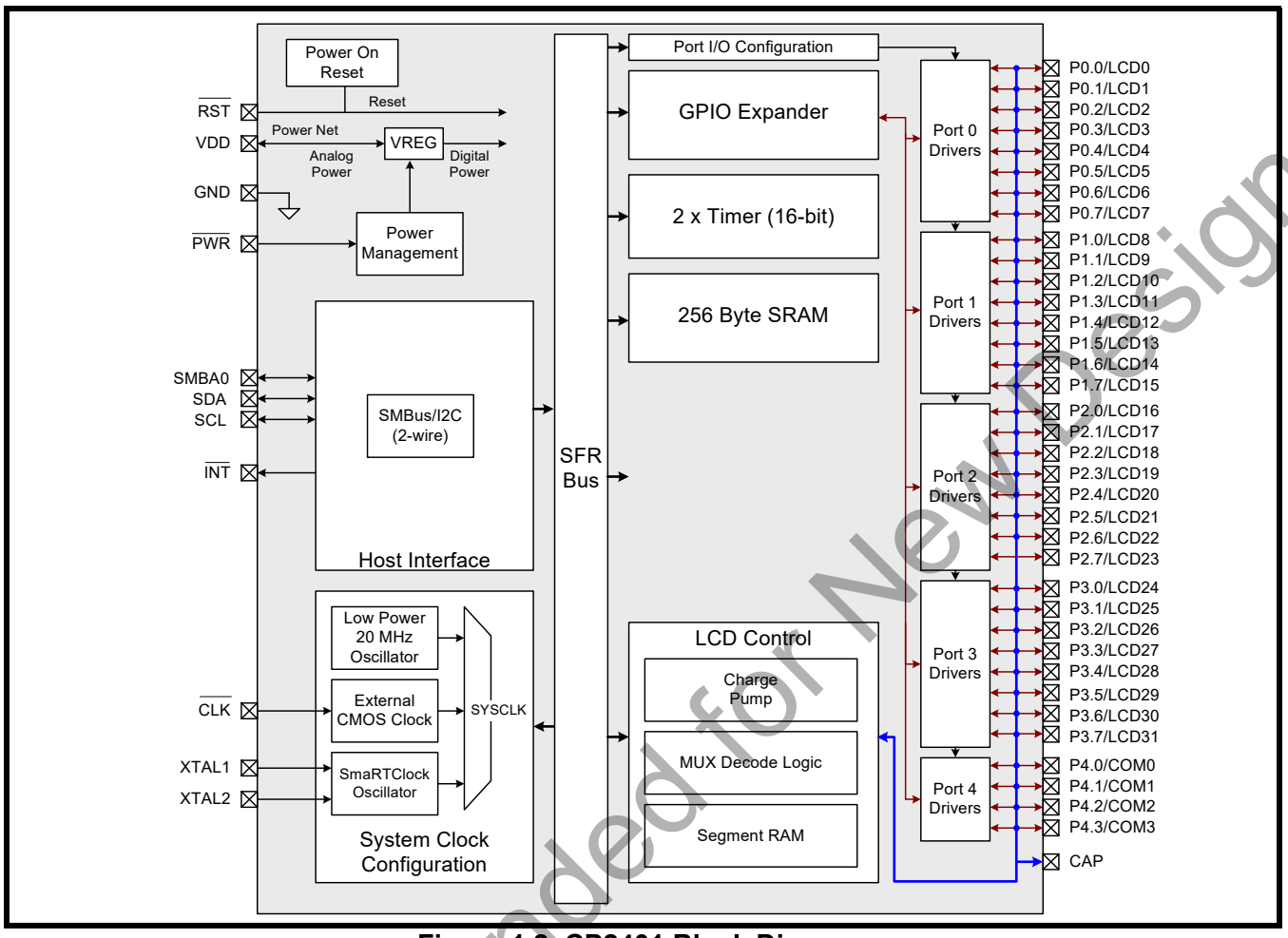


Figure 1.2. CP2401 Block Diagram

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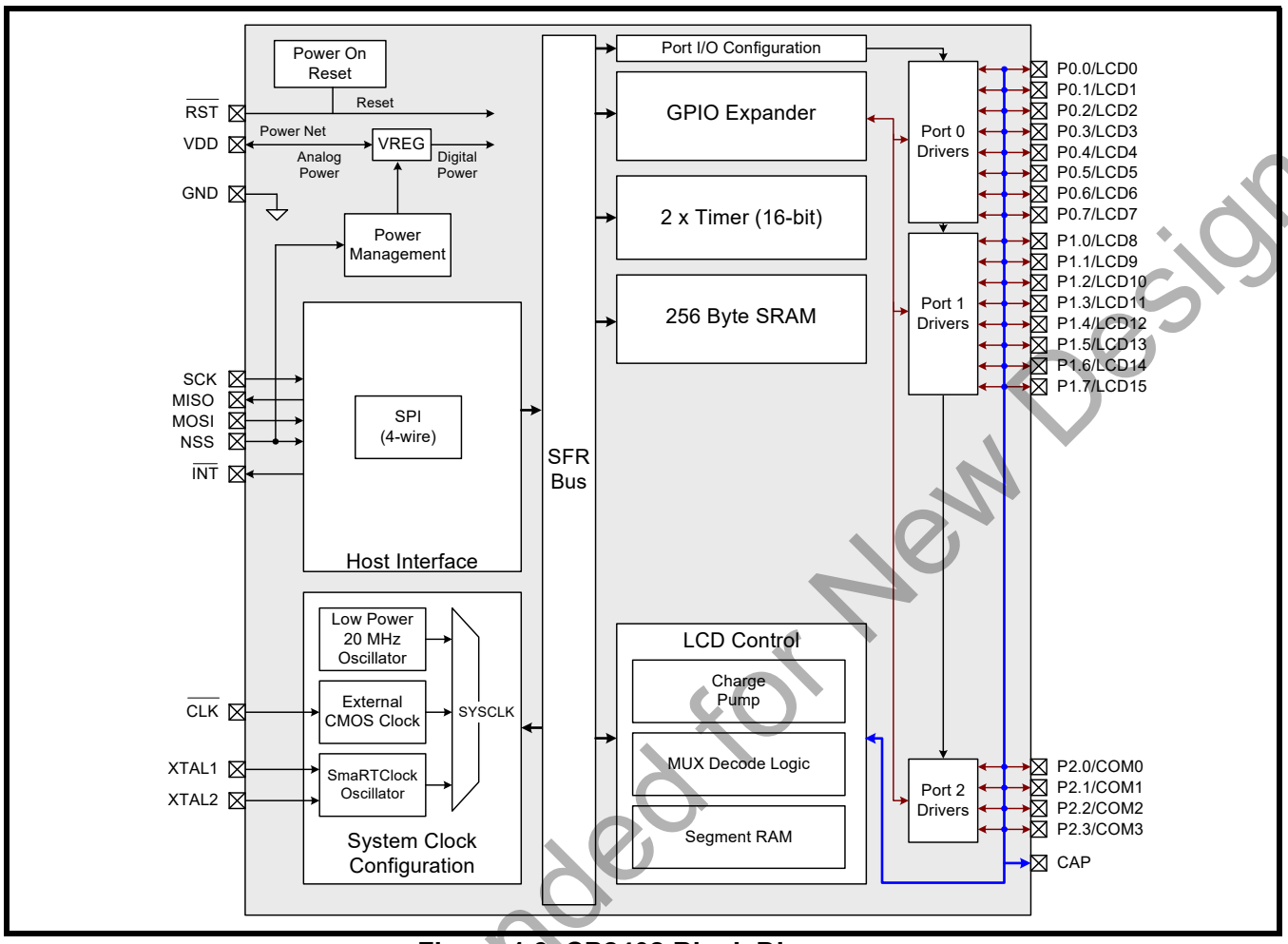


Figure 1.3. CP2402 Block Diagram

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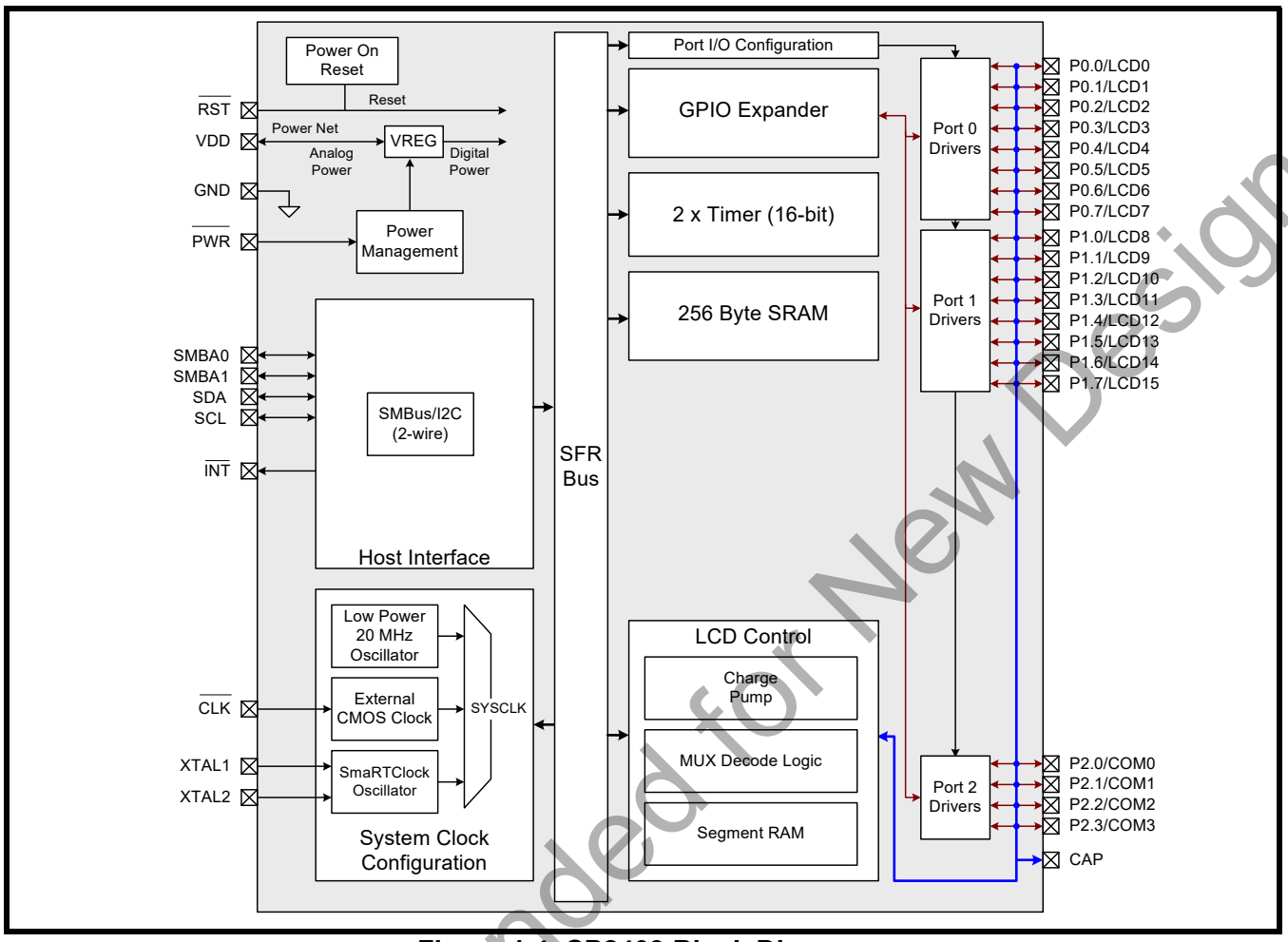


Figure 1.4. CP2403 Block Diagram

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1.1. Typical Connection Diagram

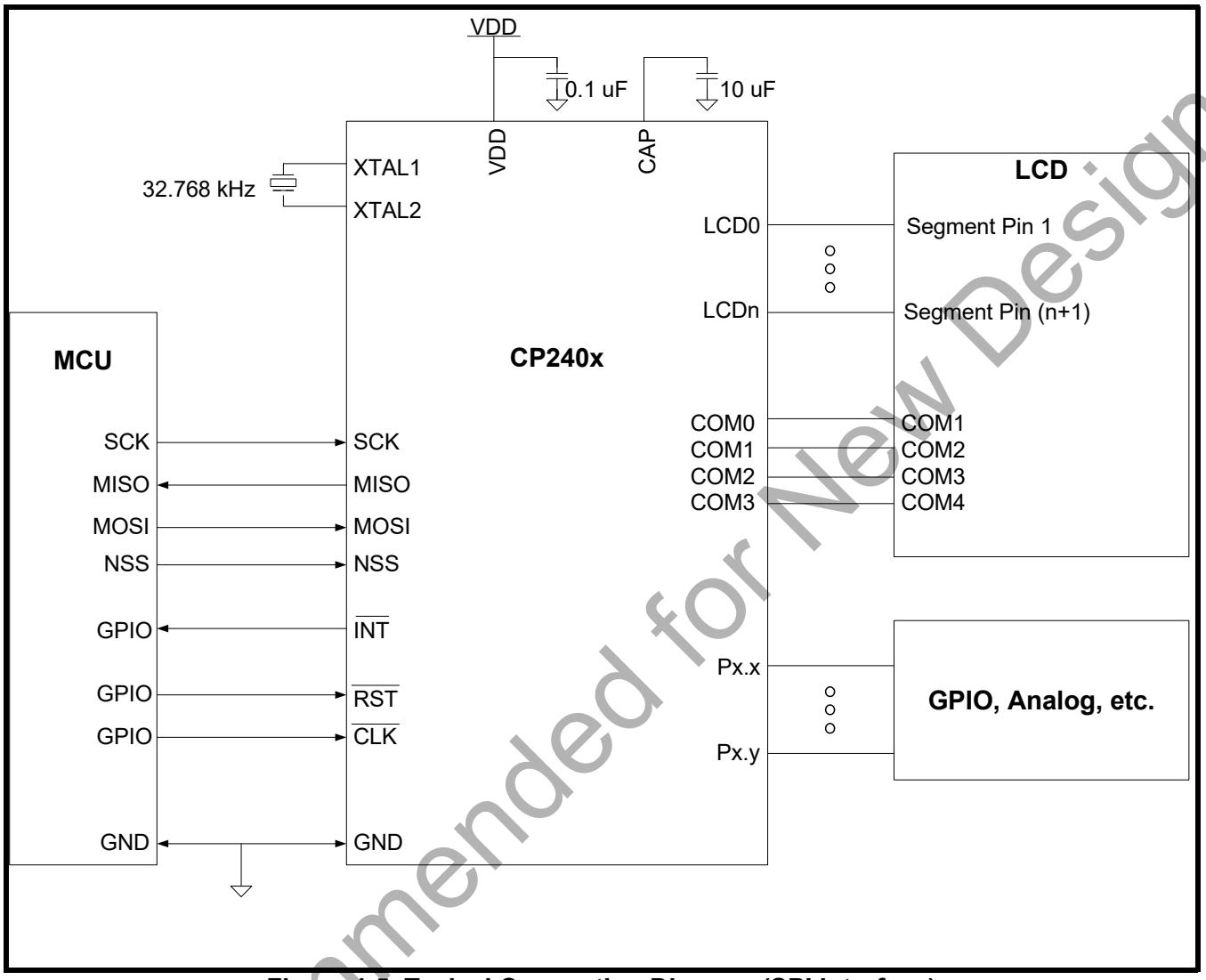


Figure 1.5. Typical Connection Diagram (SPI Interface)

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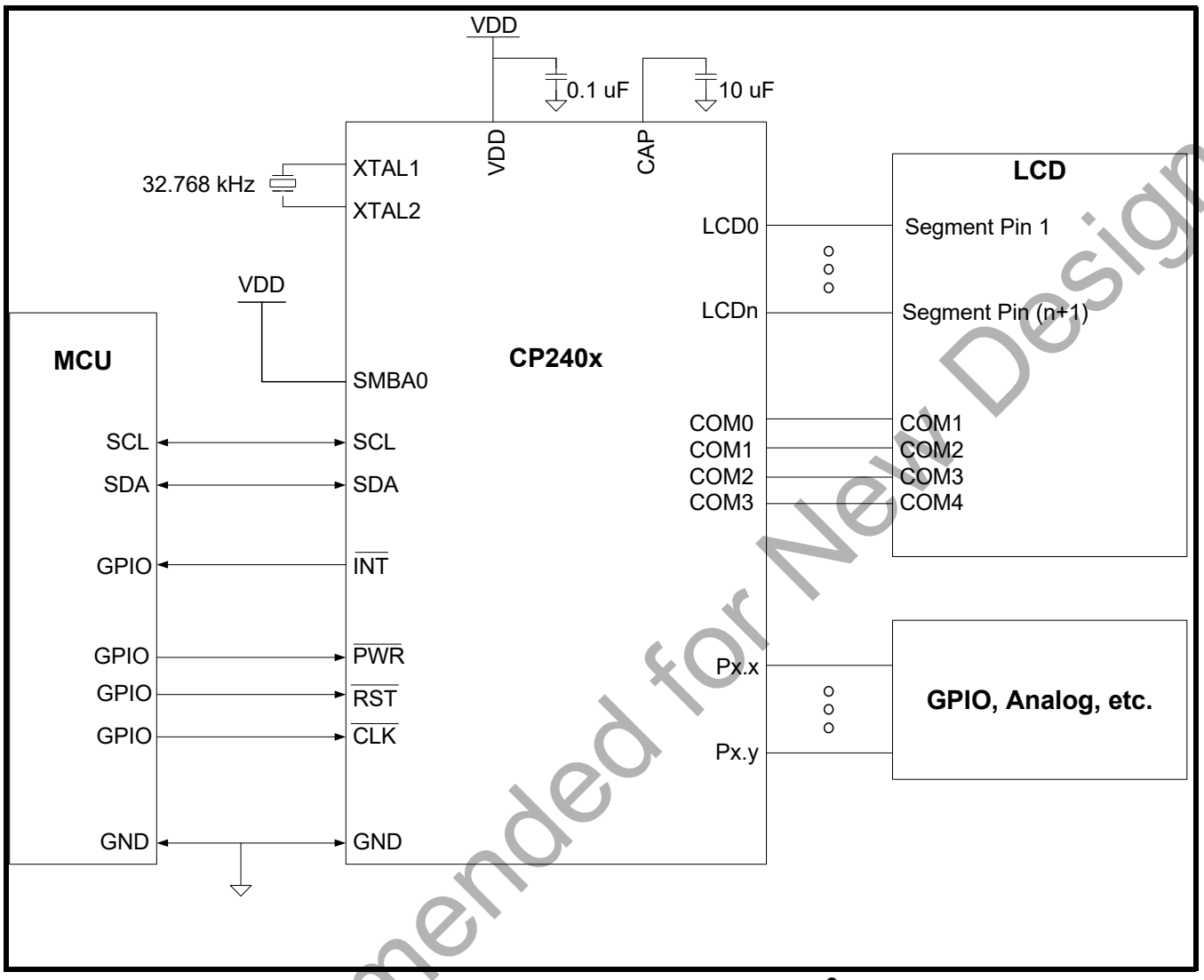


Figure 1.6. Typical Connection Diagram (SMBus/I^{2}C Interface)

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2. Absolute Maximum Ratings

Table 2.1. Absolute Maximum Ratings

Parameter	Conditions	Min	Typ	Max	Units
Ambient temperature under bias		–55	—	125	°C
Storage Temperature		–65	—	150	°C
Voltage on any I/O Pin or $\overline{RST}$ with respect to GND	V_{DD} > 2.2 V V_{DD} < 2.2 V	–0.3	—	5.8 V_{DD} + 3.6	V
Voltage on V_{DD} with respect to GND		–0.3	—	4.2	V
Maximum Total current through V_{DD} and GND		—	—	500	mA
Maximum output current sunk by $\overline{RST}$ or any I/O pin		—	—	100	mA

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the devices at or exceeding the conditions in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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3. Electrical Characteristics

Table 3.1. Global Electrical Characteristics

V_{DD} = 1.8 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage		1.8	3.3	3.6	V
SYSCLK		0	—	25	MHz
T_{SYSH} (SYSCLK High Time)		18	—	—	ns
T_{SYSL} (SYSCLK Low Time)		18	—	—	ns
Specified Operating Temperature Range		–40	—	+85	°C
Normal Mode Supply Current (V_{DD} = 3.0 V, 25 °C unless otherwise specified)					
20 MHz Internal Oscillator divided by 1, SYSCLK = 20 MHz, SPI data rate = 1 Mbps*	V_{DD} = 3.6 V V_{DD} = 3.0 V V_{DD} = 1.8 V	— — —	740 700 630	790 — —	µA
Accessing RAM at 1 Mbps		—	740	—	µA
SYSCLK = 10 MHz, SPI data rate* = 500 kbps		—	380	—	µA
SYSCLK = 5 MHz, SPI data rate* = 250 kbps		—	230	—	µA
SYSCLK = 2.5 MHz, SPI data rate* = 125 kbps		—	150	—	µA
RAM Preservation Mode Supply Current (V_{DD} = 3.0 V, 25 °C unless otherwise specified)					
32.768 kHz SmaRTClock Selected as the System Clock, Internal Oscillator Disabled		—	20	—	µA
Ultra Low Power LCD Mode Supply Current (V_{DD} = 3.0 V, 25 °C unless otherwise specified)					
LCD Enabled with Charge Pump Enabled, 60 Hz Refresh Rate, No Load SmaRTClock with 32.768 kHz crystal	4-Mux mode 3-Mux mode 2-Mux mode static mode	— — — —	2.3 2.3 2.2 2.1	— — — —	µA
LCD Enabled with Charge Pump Enabled, 60 Hz Refresh Rate, No Load SmaRTClock in Self-Oscillate Mode (AGC Enabled, LOADCAP = 0x0F)	4-Mux mode 3-Mux mode 2-Mux mode static mode	— — — —	1.7 1.7 1.7 1.5	— — — —	µA
Ultra Low Power SmaRTClock Mode Supply Current (V_{DD} = 3.0 V, 25 °C unless otherwise specified)					
External Crystal (RTC Timer Enabled)	Fosc = 32.768 kHz	—	2.5	—	µA
CMOS Clock Input on XTAL1 and XTAL2 Pins (RTC Timer Enabled)	Fosc = 32.768 kHz	—	2.3	—	µA
Self-Oscillate Mode (AGC enabled, LOADCAP = 0x0F) (RTC Timer Enabled)	Fosc = 14 kHz	—	2.0	—	µA
Shutdown Mode (V_{DD} = 3.0 V, 25 °C unless otherwise specified)					
Shutdown (no clocks active, regulator disabled)	V_{DD} = 3.6 V V_{DD} = 3.0 V V_{DD} = 1.8 V	— — —	0.030 0.020 0.015	— — —	µA
***Note:** Indicates maximum allowed SPI data rate in this mode. Power measurement taken with no SPI traffic.					

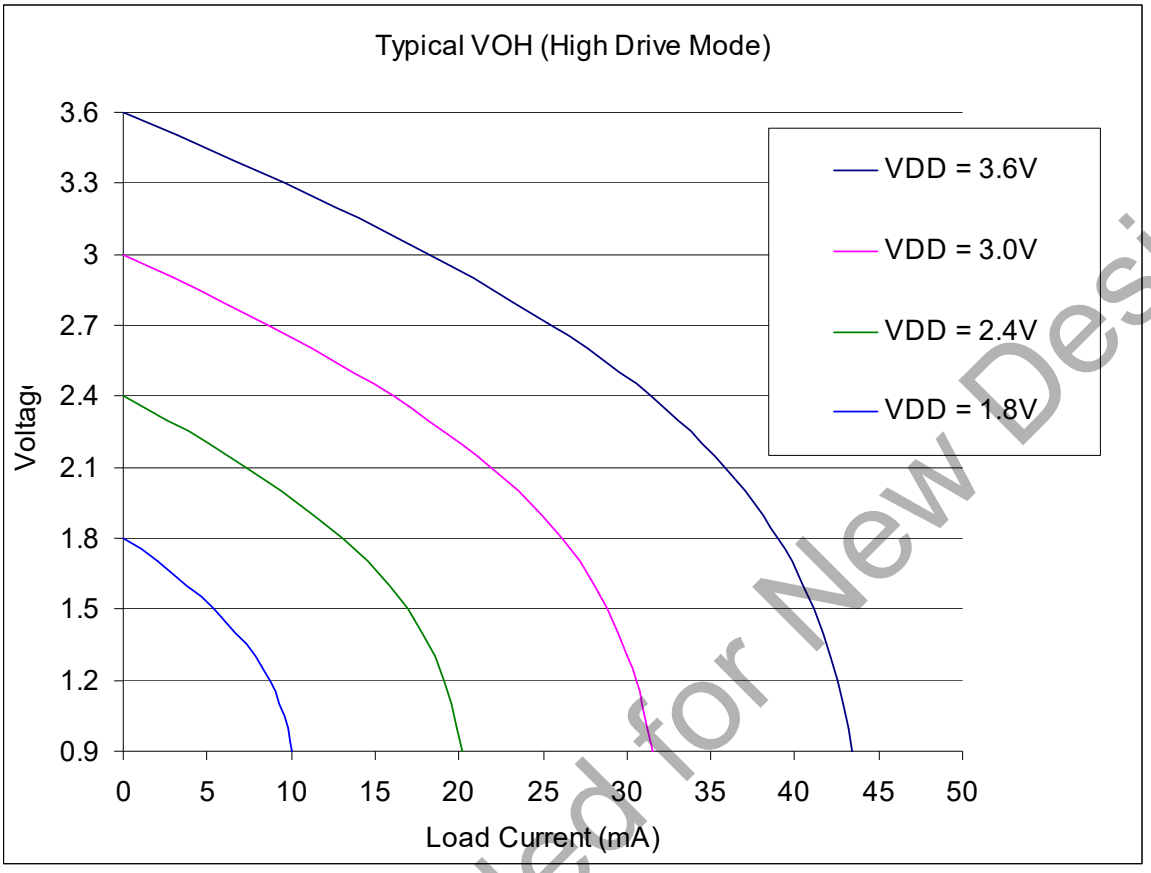
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Table 3.2. Port I/O DC Electrical Characteristics

V_{DD} = 1.8 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameters	Conditions	Min	Typ	Max	Units
Output High Voltage	High Drive Strength, PnDRV.n = 1				
	I_{OH} = –3 mA, Port I/O push-pull	V_{DD} – 0.7	—	—	
	I_{OH} = –10 µA, Port I/O push-pull	V_{DD} – 0.1	—	—	
	I_{OH} = –10 mA, Port I/O push-pull	—	See Chart	—	V
	Low Drive Strength, PnDRV.n = 0				
	I_{OH} = –1 mA, Port I/O push-pull	V_{DD} – 0.7	—	—	
	I_{OH} = –10 µA, Port I/O push-pull	V_{DD} – 0.1	—	—	
	I_{OH} = –3 mA, Port I/O push-pull	—	See Chart	—	
Output Low Voltage	High Drive Strength, PnDRV.n = 1				
	I_{OL} = 8.5 mA	—	—	0.6	
	I_{OL} = 10 µA	—	—	0.1	
	I_{OL} = 15 mA	—	See Chart	—	V
	Low Drive Strength, PnDRV.n = 0				
	I_{OL} = 1.4 mA	—	—	0.6	
	I_{OL} = 10 µA	—	—	0.1	
	I_{OL} = 4 mA	—	See Chart	—	
Input High Voltage	V_{DD} = 2.0 to 3.6 V	V_{DD} – 0.6	—	—	V
	V_{DD} = 1.8 to 2.0 V	0.7 x V_{DD}	—	—	V
Input Low Voltage	V_{DD} = 2.0 to 3.6 V	—	—	0.6	V
	V_{DD} = 1.8 to 2.0 V	—	—	0.3 x V_{DD}	V
Input Leakage Current	Weak Pullup On, V_{IN} = 0 V, V_{DD} = 1.8 V	—	4	—	µA
	Weak Pullup On, Vin = 0 V, V_{DD} = 3.6 V	—	20	30	

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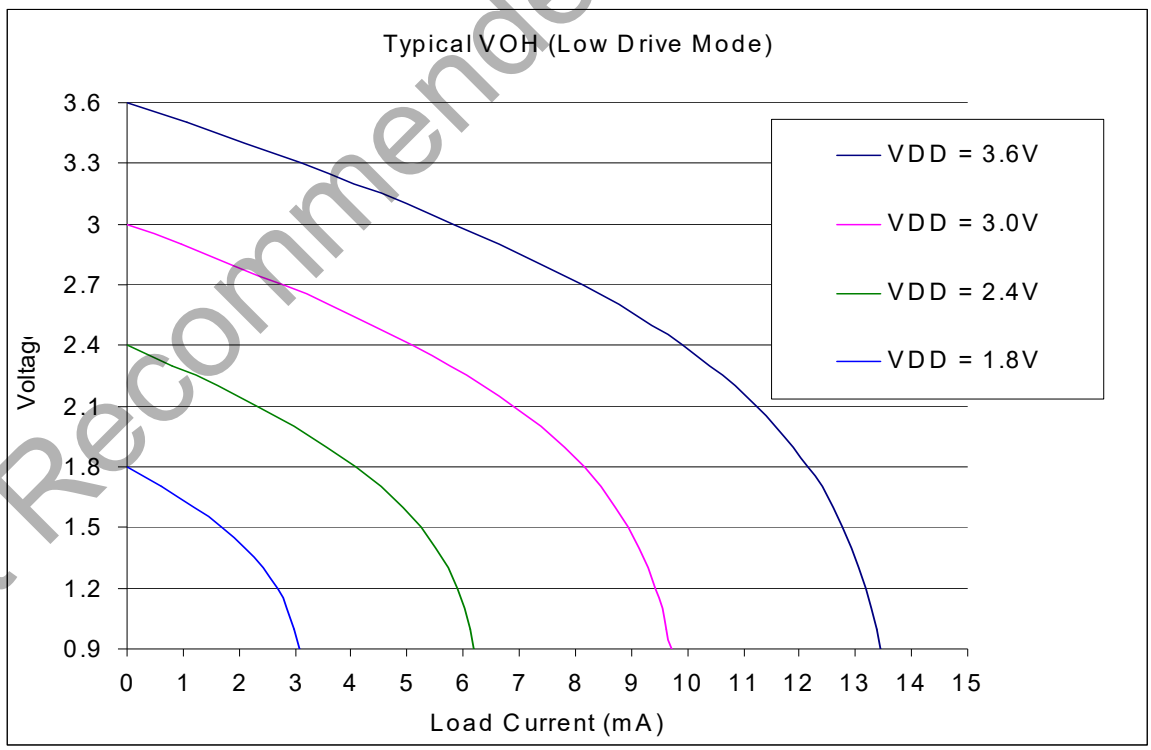
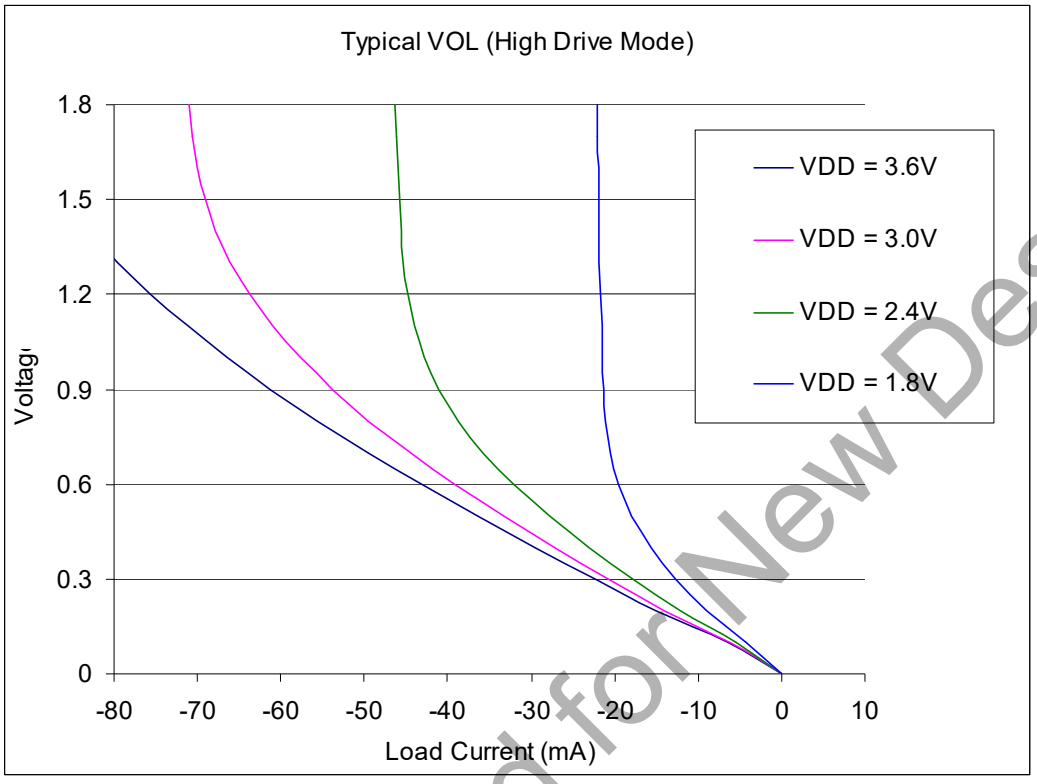


Figure 3.1. Typical VOH

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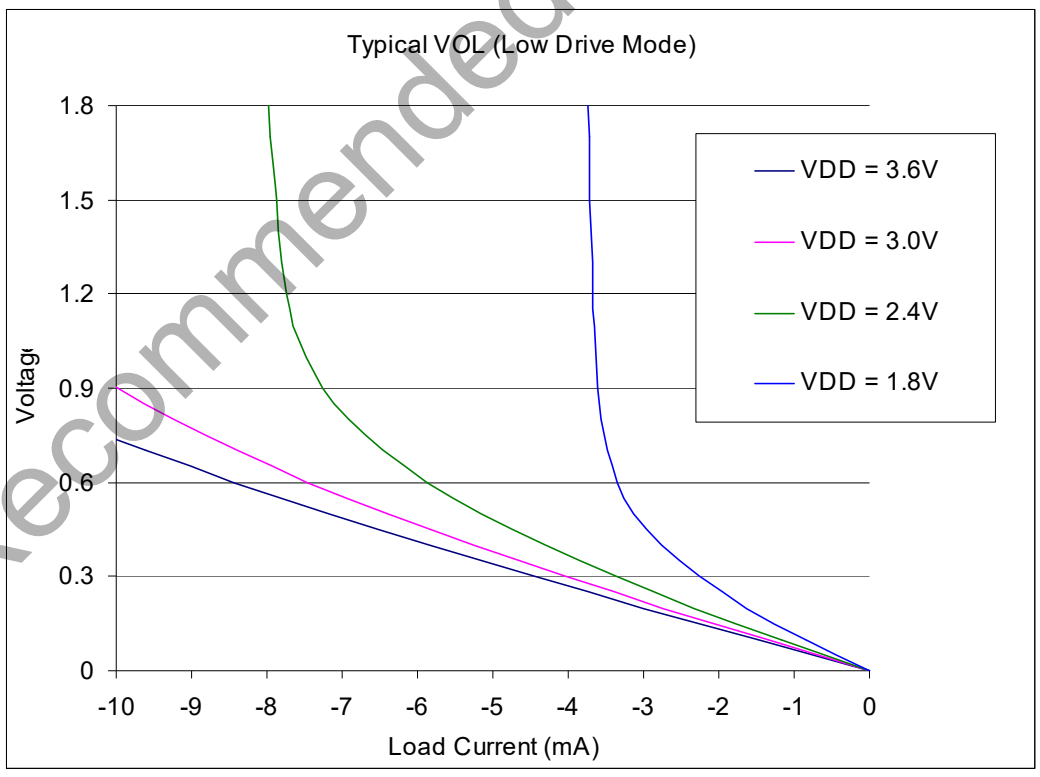


Figure 3.2. Typical VOL

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Table 3.3. Reset Electrical Characteristics

V_{DD} = 1.8 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameters	Conditions	Min	Typ	Max	UNITS
$\overline{RST}$ Input High Voltage		0.7 x V_{DD}	—	—	V
$\overline{RST}$ Input Low Voltage		—	—	0.3 x V_{DD}	V
$\overline{RST}$ Input Pullup Current	$\overline{RST}$ = 0 V, V_{DD} = 1.8 V $\overline{RST}$ = 0 V, V_{DD} = 3.6 V	— —	4 20	— 30	µA
V_{DD} Ramp Time for Power On[1]	V_{DD} Ramp from 0–1.8 V	—	—	1	ms
Power on Reset Delay ($T_{PORDelay}$) from Start of Ramp until the Reset Complete Interrupt	V_{DD} = 1.8 V V_{DD} = 3.0 V V_{DD} = 3.6 V	— — —	1200 660 575	— 900 —	µs
Required $\overline{RST}$ Low Time to guarantee a System Reset (T_{RST})	See Note 2	15	—	—	µs
Startup Delay from Reset De-asserted until the Reset Complete Interrupt ($T_{STARTUP}$)	Pin Reset	—	90	100	µs

Notes:
1. There is no restriction on VDD ramp time if the $\overline{RST}$ pin is toggled at the end of the ramp.
2. If the $\overline{RST}$ pin is held low for a shorter time period, a device reset may occur.

Table 3.4. Power Management Electrical Specifications

V_{DD} = 1.8 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
RAM Preservation Mode Wake-Up Time	From the falling edge of $\overline{CLK}$ until host interface ready		10		ns
ULP Mode Wake-Up Time (from the falling edge of NSS/PWR to the reset complete interrupt)	Port Match or SmaRTClock Wakeup NSS/PWR Pin Wakeup	3 7	— —	4 8	RTC Cycles

Table 3.5. Internal Oscillator Electrical Characteristics

V_{DD} = 1.8 to 3.6 V; T_A = –40 to +85 °C unless otherwise specified; Using factory-calibrated settings.

Parameter	Conditions	Min	Typ	Max	Units
Oscillator Frequency	–40 to +85 °C, V_{DD} = 1.8–3.6 V	15	20	25	MHz
Oscillator Supply Current (from V_{DD})	25 °C	—	50	—	µA

Table 3.6. LCD Electrical Characteristics

V_{DD} = 1.8 to 3.6 V; T_A = –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Charge Pump Output Voltage Error		—	±30	—	mV

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4. Pinout and Package Definitions

Table 4.1. CP2400/1/2/3 Pin Definitions

Name	Pin Numbers				Type	Description
	48-pin		32-pin			
	SPI	I^2C	SPI	I^2C		
XTAL1	1	1	1	1	A In	Crystal Input. This pin is the return for the external oscillator driver. This pin can be overdriven by an external CMOS clock.
XTAL2	2	2	2	2	A Out	Crystal Output. This pin is the excitation driver for a quartz crystal.
V_{DD}	3	3	3	3	Power In	1.8–3.6 V Power Supply Voltage Input.
GND	4	4	4	4		Ground
CAP	48	48	32	32	Power Out	LCD Power Supply Voltage Output. This pin requires a 10 µF decoupling capacitor.
$\overline{CLK}$	47	47	31	31	D In	CMOS clock input. This pin should not be left floating.
$\overline{RST}$	46	46	30	30	D In	Device Reset. An external source can initiate a system reset by driving this pin low for at least 15 µs. This pin has an internal weak pullup.
$\overline{INT}$	45	45	29	29	D Out	Interrupt Service Request. This pin provides notification to the host. This pin is a push-pull output.
NSS	44	—	28	—	D In	Slave select signal for SPI interface. This pin should not be left floating.
MOSI	43	—	27	—	D In	Master Out/Slave In data signal for SPI interface. This pin should not be left floating.
MISO	42	—	26	—	D Out	Master In/Slave Out data signal for SPI interface
SCK	41	—	25	—	D In	Clock signal for SPI interface. This pin should not be left floating.
$\overline{PWR}$	—	44	—	28	D In	Allows SMBus device to enter the Ultra Low Power mode. This pin should not be left floating.
SCL	—	43	—	27	D I/O	Clock signal for SMBus interface. This pin should not be left floating.
SDA	—	42	—	26	D I/O	Data signal for SMBus interface. This pin should not be left floating.
SMBA0	—	41	—	25	D In	Bit 0, SMBus Slave Address. This pin should not be left floating.
P0.0 LCD0	40	40	24	24	D I/O A Out	Bit 0, Port 0
P0.1 LCD1	39	39	23	23	D I/O A Out	Bit 1, Port 0

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Table 4.1. CP2400/1/2/3 Pin Definitions (Continued)

Name	Pin Numbers				Type	Description
	48-pin		32-pin			
	SPI	I^2C	SPI	I^2C		
P0.2 LCD2	38	38	22	22	D I/O A Out	Bit 2, Port 0
P0.3 LCD3	37	37	21	21	D I/O A Out	Bit 3, Port 0
P0.4 LCD4	36	36	20	20	D I/O A Out	Bit 4, Port 0
P0.5 LCD5	35	35	19	19	D I/O A Out	Bit 5, Port 0
P0.6 LCD6	34	34	18	18	D I/O A Out	Bit 6, Port 0
P0.7 LCD7	33	33	17	17	D I/O A Out	Bit 7, Port 0
P1.0 LCD8	32	32	16	16	D I/O A Out	Bit 0, Port 1
P1.1 LCD9	31	31	15	15	D I/O A Out	Bit 1, Port 1
P1.2 LCD10	30	30	14	14	D I/O A Out	Bit 2, Port 1
P1.3 LCD11	29	29	13	13	D I/O A Out	Bit 3, Port 1
P1.4 LCD12	28	28	12	12	D I/O A Out	Bit 4, Port 1
P1.5 LCD13	27	27	11	11	D I/O A Out	Bit 5, Port 1
P1.6 LCD14	26	26	10	10	D I/O A Out	Bit 6, Port 1
P1.7 LCD15	25	25	9	9	D I/O A Out	Bit 7, Port 1
P2.0 LCD16	24	24	—	—	D I/O A Out	Bit 0, Port 2
P2.1 LCD17	23	23	—	—	D I/O A Out	Bit 1, Port 2

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Table 4.1. CP2400/1/2/3 Pin Definitions (Continued)

Name	Pin Numbers				Type	Description
	48-pin		32-pin			
	SPI	I^2C	SPI	I^2C		
P2.2 LCD18	22	22	—	—	D I/O A Out	Bit 2, Port 2
P2.3 LCD19	21	21	—	—	D I/O A Out	Bit 3, Port 2
P2.0 COM0	—	—	8	8	D I/O A Out	Bit 0, Port 2
P2.1 COM1	—	—	7	7	D I/O A Out	Bit 1, Port 2
P2.2 COM2	—	—	6	6	D I/O A Out	Bit 2, Port 2
P2.3 COM3	—	—	5	5	D I/O A Out	Bit 3, Port 2
P2.4 LCD20	20	20	—	—	D I/O A Out	Bit 4, Port 2
P2.5 LCD21	19	19	—	—	D I/O A Out	Bit 5, Port 2
P2.6 LCD22	18	18	—	—	D I/O A Out	Bit 6, Port 2
P2.7 LCD23	17	17	—	—	D I/O A Out	Bit 7, Port 2
P3.0 LCD24	16	16	—	—	D I/O A Out	Bit 0, Port 3
P3.1 LCD25	15	15	—	—	D I/O A Out	Bit 1, Port 3
P3.2 LCD26	14	14	—	—	D I/O A Out	Bit 2, Port 3
P3.3 LCD27	13	13	—	—	D I/O A Out	Bit 3, Port 3
P3.4 LCD28	12	12	—	—	D I/O A Out	Bit 4, Port 3
P3.5 LCD29	11	11	—	—	D I/O A Out	Bit 5, Port 3

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Table 4.1. CP2400/1/2/3 Pin Definitions (Continued)

Name	Pin Numbers				Type	Description
	48-pin		32-pin			
	SPI	I^2C	SPI	I^2C		
P3.6 LCD30	10	10	—	—	D I/O A Out	Bit 6, Port 3
P3.7 LCD31	9	9	—	—	D I/O A Out	Bit 7, Port 3
P4.0 COM0	8	8	—	—	D I/O A Out	Bit 0, Port 4
P4.1 COM1	7	7	—	—	D I/O A Out	Bit 1, Port 4
P4.2 COM2	6	6	—	—	D I/O A Out	Bit 2, Port 4
P4.3 COM3	5	5	—	—	D I/O A Out	Bit 3, Port 4

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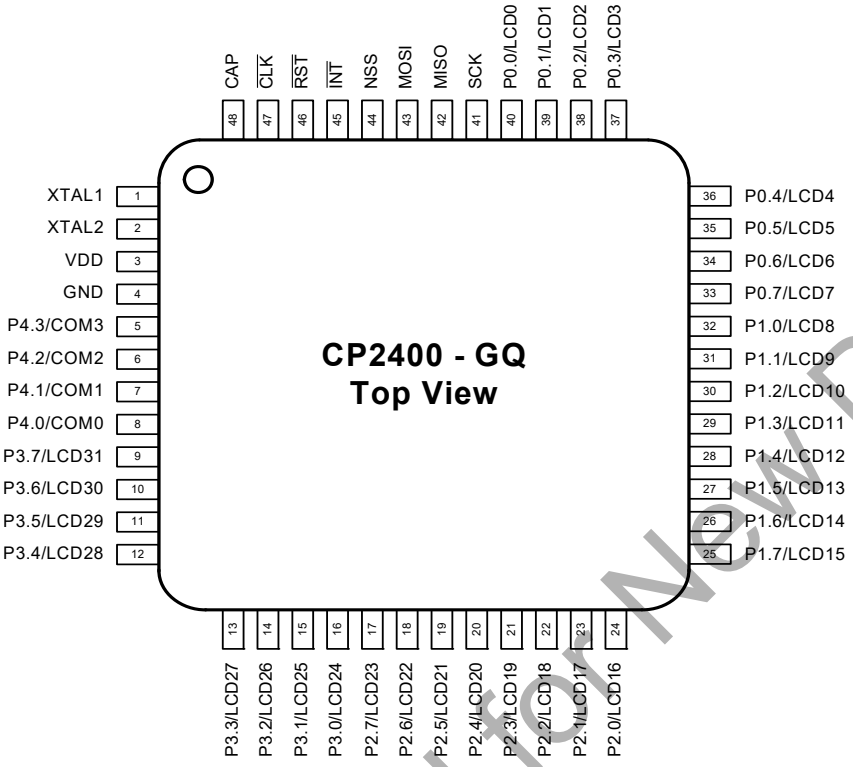


Figure 4.1. CP2400-GQ Pinout (SPI Interface)

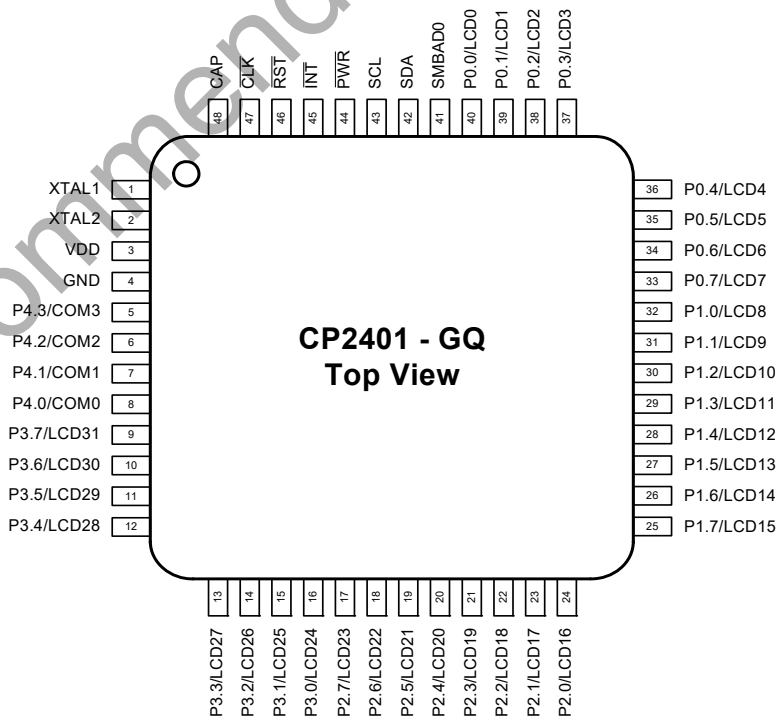


Figure 4.2. CP2401-GQ Pinout (SMBus/I^{2}C Interface)

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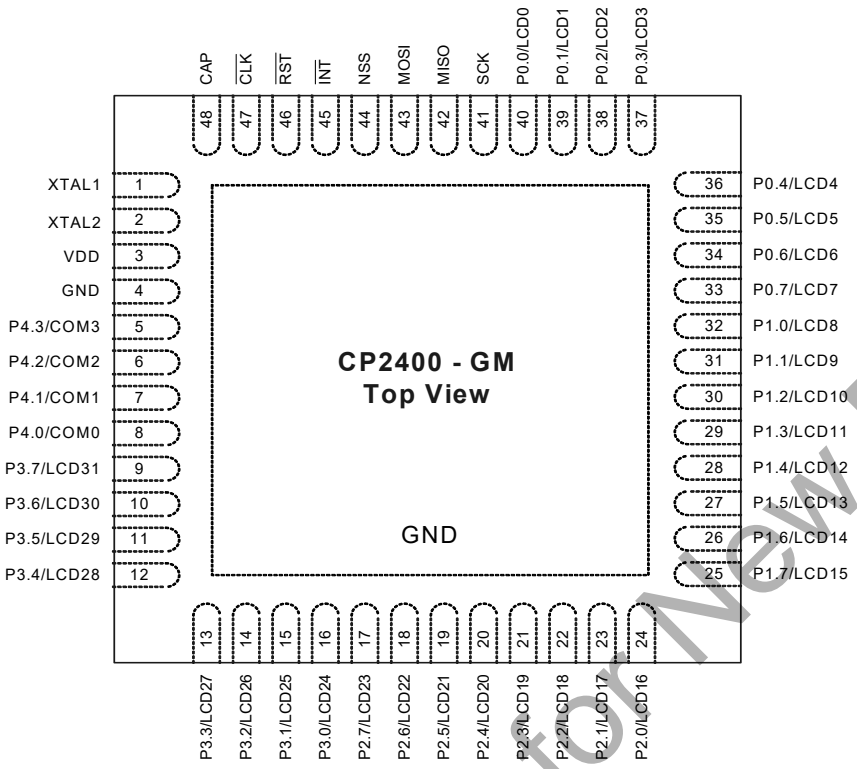


Figure 4.3. CP2400-GM Pinout (SPI Interface)

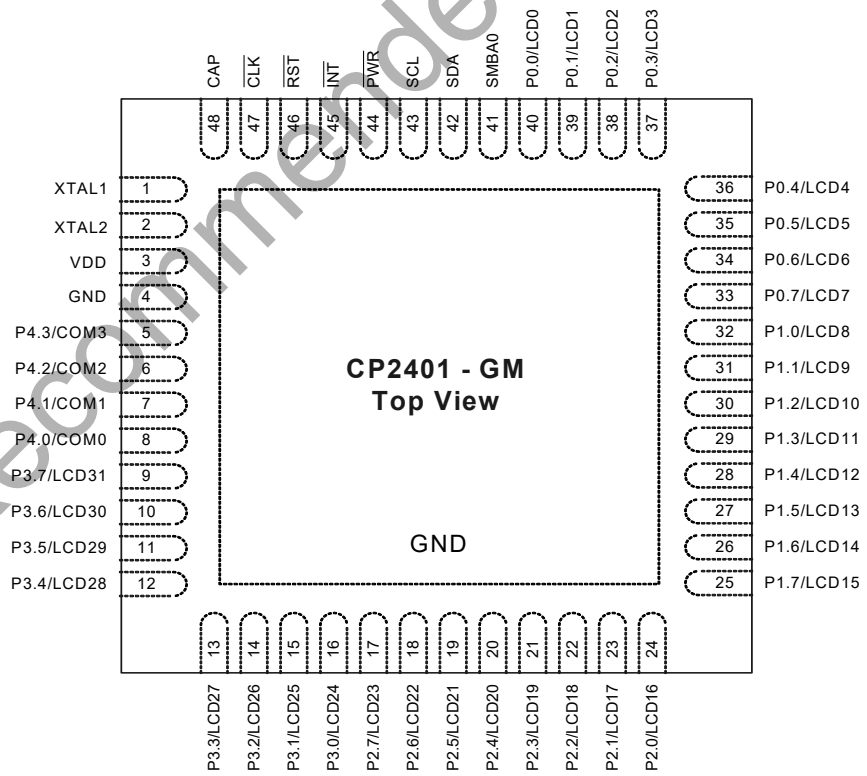


Figure 4.4. CP2401-GM Pinout (SMBus/I^{2}C Interface)

Not Recommended for New Designs

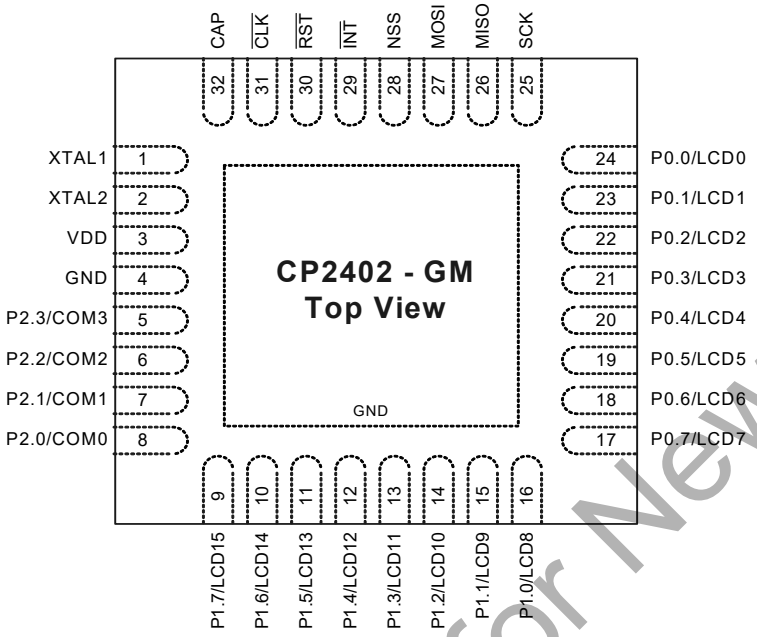


Figure 4.5. CP2402-GM Pinout (SPI Interface)

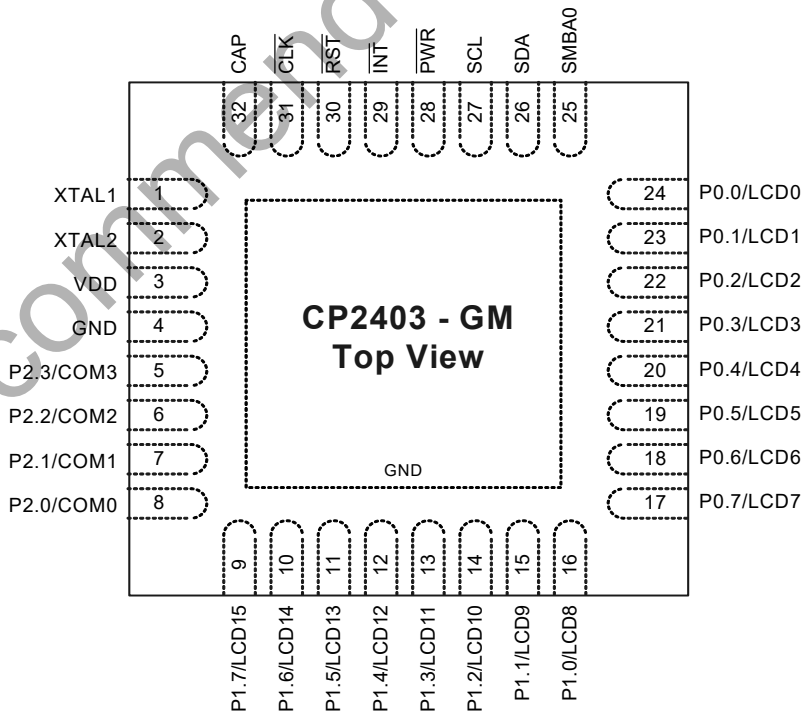
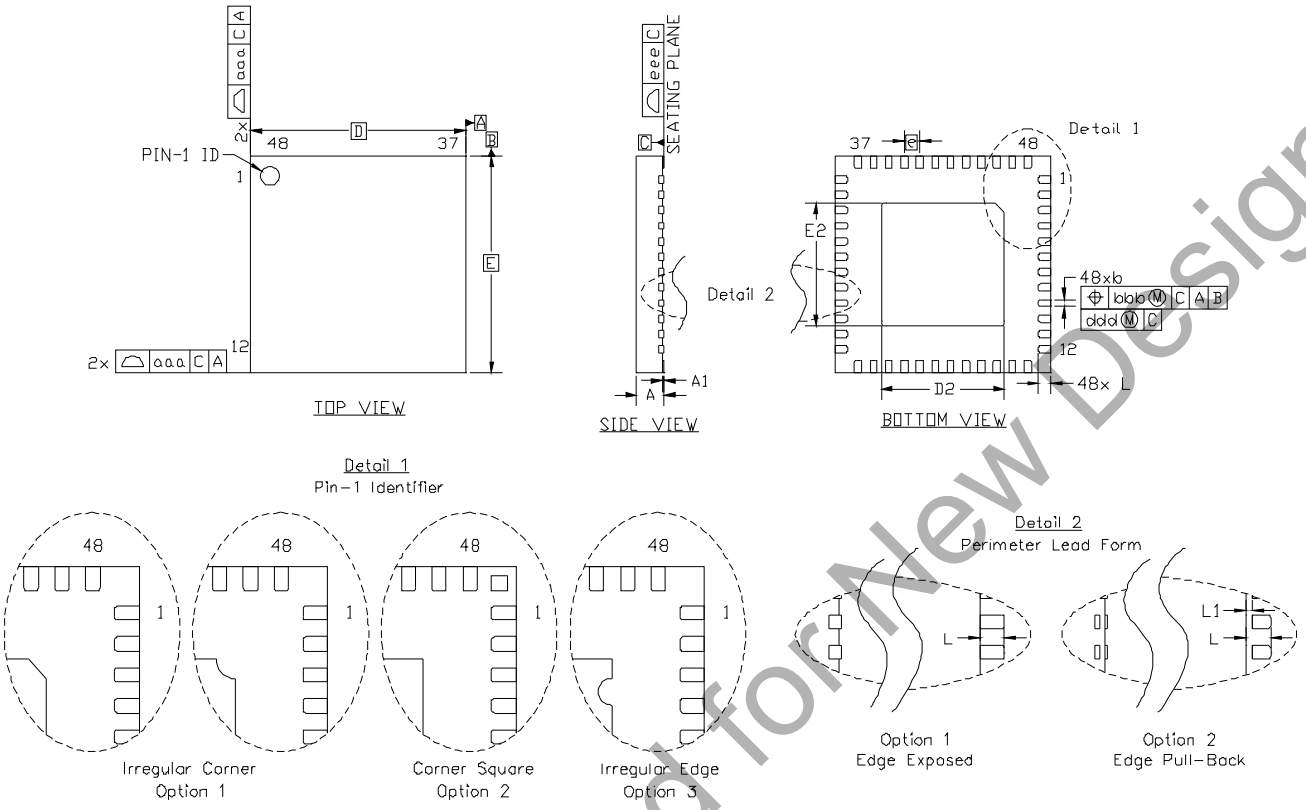


Figure 4.6. CP2403-GM Pinout (SMBus Interface)

Not Recommended for New Designs



Dimension	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	- -	0.05
b	0.18	0.23	0.30
D		7.00 BSC.	
D2	3.90	4.00	4.10
e		0.50 BSC.	
E		7.00 BSC.	
E2	3.90	4.00	4.10
L	0.30	0.40	0.50
L1	0.00	- -	0.10
aaa	--	--	0.10
bbb	--	--	0.10
ddd	--	--	0.05
eee	--	--	0.08

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VKKD-4 except for features D2 and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Figure 4.7. QFN-48 Package Drawing

Not Recommended for New Designs

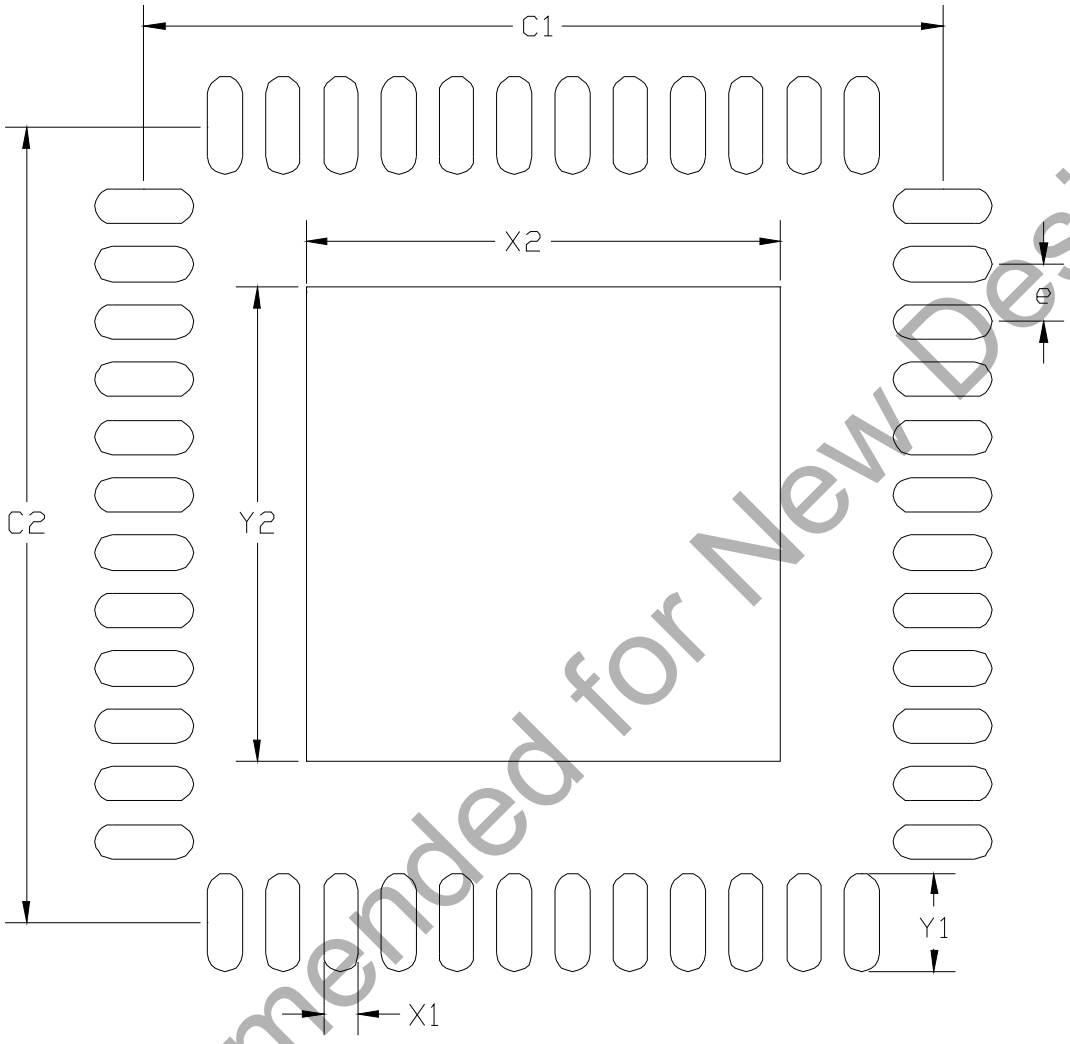


Figure 4.8. QFN-48 Landing Diagram

Not Recommended for New Designs

Table 4.2. PCB Land Pattern

Dimension	MIN	MAX
C1	6.80	6.90
C2	6.80	6.90
e	0.50 BSC	
X1	0.20	0.30
X2	4.00	4.10
Y1	0.75	0.85
Y2	4.00	4.10

Notes:

General

3. All dimensions shown are in millimeters (mm) unless otherwise noted.
4. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
5. This Land Pattern Design is based on IPC-SM-782 guidelines.
6. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 3 x 3 array of 1.20 mm square openings on 1.40 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Not Recommended for New Designs

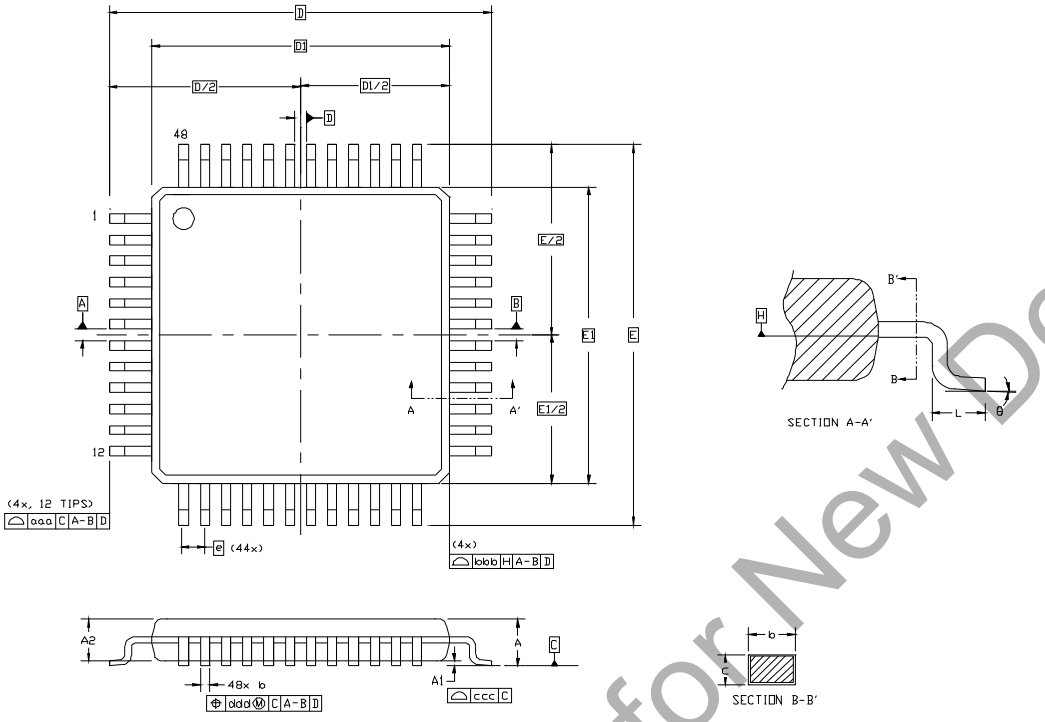


Figure 4.9. TQFP-48 Package Diagram

Table 4.3. TQFP-48 Package Dimensions

Dimension	Min	Nom	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
aaa	0.20		
bbb	0.20		
ccc	0.08		
ddd	0.08		
θ	0°	3.5°	7°

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026, variation ABC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

Not Recommended for New Designs

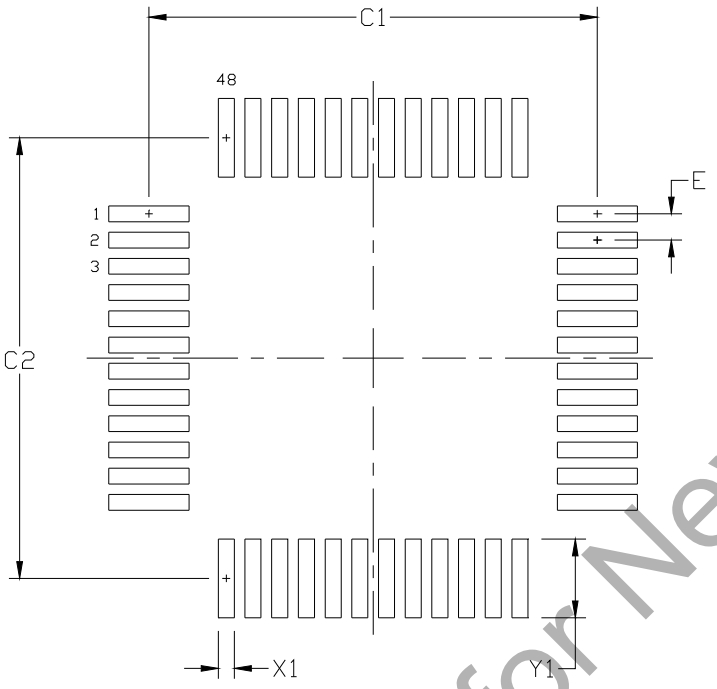


Figure 4.10. TQFP-48 Recommended PCB Land Pattern

Table 4.4. TQFP-48 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	8.30	8.40
C2	8.30	8.40
E	0.50 BSC	
X1	0.20	0.30
Y1	1.40	1.50

Notes:

General:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design:

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design:

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all pads.

Card Assembly:

7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Not Recommended for New Designs

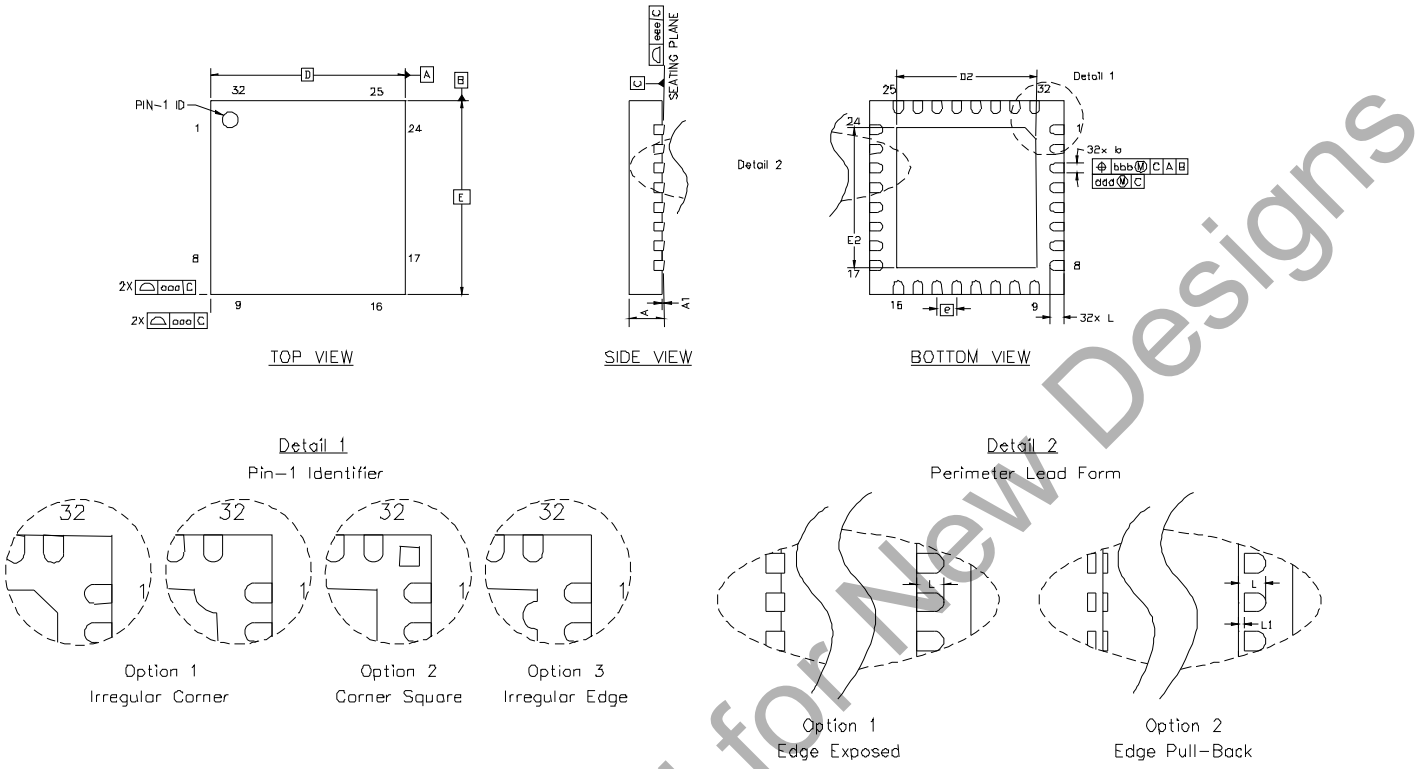


Figure 4.11. QFN-32 Package Drawing

Table 4.5. QFN-32 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.9	1.00
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		5.00 BSC	
D2	3.20	3.30	3.40
e		0.50 BSC	
E		5.00 BSC	

Dimension	Min	Typ	Max
E2	3.20	3.30	3.40
L	0.30	0.40	0.50
L1	0.00	—	0.15
aaa	—	—	0.15
bbb	—	—	0.10
ddd	—	—	0.05
eee	—	—	0.08

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, variation VHHD except for custom features D2, E2, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Not Recommended for New Designs

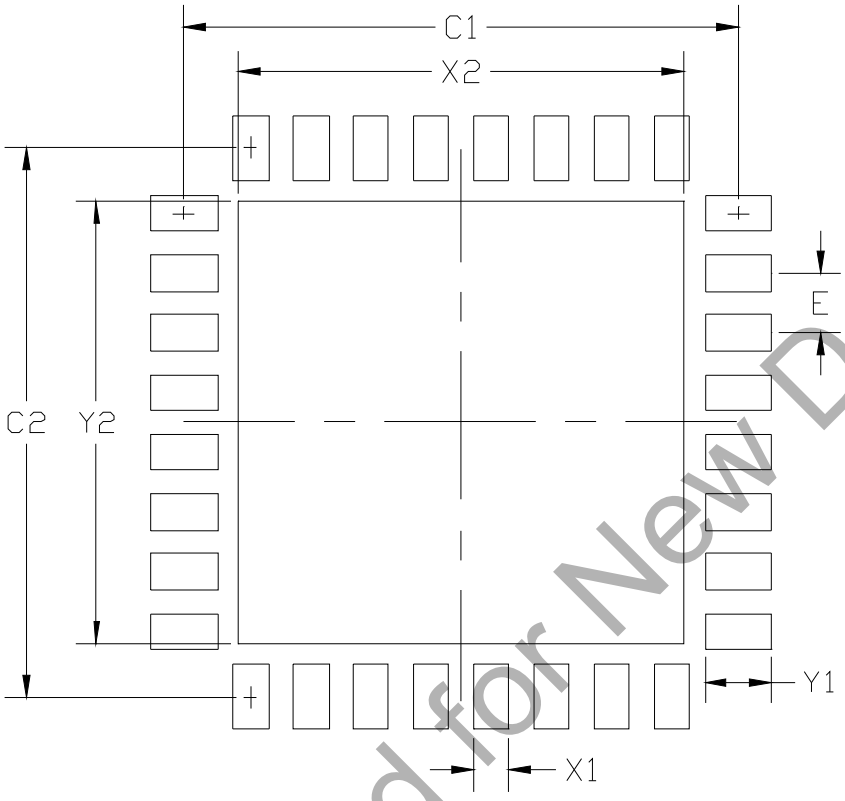


Figure 4.12. Typical QFN-32 Landing Diagram

Not Recommended for New Designs

Table 4.6. PCB Land Pattern

Dimension	MIN	MAX
C1	4.80	4.90
C2	4.80	4.90
E	0.50 BSC	
X1	0.20	0.30
X2	3.20	3.40
Y1	0.75	0.85
Y2	3.20	3.40

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 3 x 3 array of 1.0 mm square openings on 1.25 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Not Recommended for New Designs

5. Clocking Options

CP2400/1/2/3 devices include a 20 MHz internal oscillator that is selected as the system clock source upon reset. Additional clocking options include an external CMOS clock input, the internal oscillator divided by 2, 4, or 8, and the SmaRTClock real time clock oscillator. The system clock source is selected using the CLKSEL register. The system clock selection may always be overridden by an external CMOS clock if the CLKOVR bit (MSCN.2) is set.

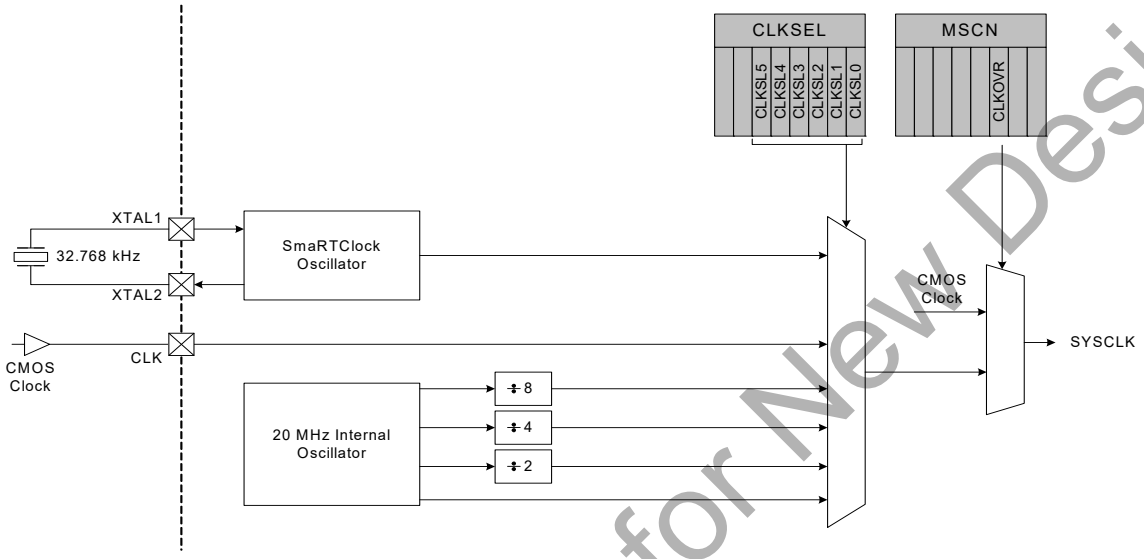


Figure 5.1. Clocking Options

SFR Definition 5.1. CLKSL: Clock Select

Bit	7	6	5	4	3	2	1	0
Name						CLKSL		
Type	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0	0	0

Internal Register Address = 0x32

Bit	Name	Function
7:3	Unused	Read = 00000. Write = Don't Care.
2:0	CLKSL	**System Clock Select**. Selects the oscillator to be used as system clock source. 000: Internal oscillator divided by 1. 001: Internal oscillator divided by 2. 010: Internal oscillator divided by 4. 011: Internal oscillator divided by 8. 100: CMOS clock (CLK pin). 101: SmaRTClock oscillator. All other values reserved.

Not Recommended for New Designs

SFR Definition 5.2. IOSCCN: Internal Oscillator Control

Bit	7	6	5	4	3	2	1	0
Name					Reserved	INTCTL	OSCEN	EXTCTL
Type	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	1	1	0

Internal Register Address = 0x33

Bit	Name	Function
7:4	Unused	Read = 00000. Write = Don't Care.
3	Reserved	Read = 0. Write = Must Write 0b.
2	INTCTL	**Oscillator Internal Control Enable.** When set to 1, forces the oscillator to remain enabled. Setting this bit to 0 will gate the clock output, but will not disable the oscillator.
1	OSCEN	**Internal Oscillator Enable.** When set to 0, disables power to the internal oscillator. When set to 1, allows the internal oscillator to be powered (under the control of INTCTL and EXTCTL).
0	EXTCTL	**Oscillator External Control Enable.** When set to 1 and INTCTL is cleared to 0, a rising edge on $\overline{CLK}$ will cause the internal oscillator to be disabled. The internal oscillator is re-enabled by the next falling edge on $\overline{CLK}$.

Note: To control the internal oscillator enable from an external pin (EXTCTL = 1, INTCTL = 0), first write both bits to logic 1, then clear the INTCTL bit. See **Section "9.2. RAM Preservation Mode" on page 50** for information on how to place the device in RAM Preservation Mode. When running from an external clock, the internal oscillator may be disabled by writing 0x00 to IOSCCN.

SFR Definition 5.3. REVID: Revision Identification

Bit	7	6	5	4	3	2	1	0
Name	REVID[7:0]							
Type	R/W							
Reset	Varies	Varies	Varies	Varies	Varies	Varies	Varies	Varies

Internal Register Address = 0x34

Bit	Name	Function
7:0	REVID[7:0]	**Revision ID.** Indicates the device revision. For example 0x01 indicates Revision C.

Not Recommended for New Designs

6. Internal Registers and Memory

The CP2400/1/2/3 is controlled by internal registers and provides the system with up to 256 bytes of additional RAM. The internal registers and memory are controlled through an indirect interface accessible through a 4-wire SPI interface (CP2400/2) or 2-wire SMBus/I^2C interface (CP2401/3). A memory map of the internal registers and RAM is shown in Figure 6.1. The internal registers are listed in “6.3. Internal Registers” on page 37.

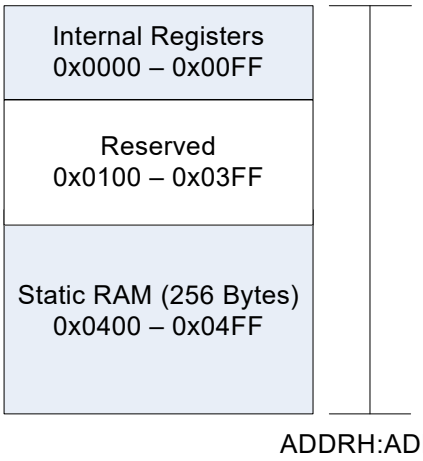


Figure 6.1. Internal Register and RAM Memory Map

Not Recommended for New Designs

6.1. Accessing Internal Registers and RAM over the SPI Interface

The SPI interface supports 6 commands which provide access to all internal registers and RAM. The six commands are listed in Table 6.1. Detailed information on the SPI interface including bus timing can be found in Section "**14. Serial Peripheral Interface (SPI)**" on page **101**.

Table 6.1. SPI Command Set

Command	OPCODE	Description
REGPOLL	0x01	Reads data from a single register. Used for polling a status bit.
REGREAD	0x02	Reads one or more bytes from registers with sequential addresses.
REGSET	0x03	Writes one or more bytes to a single register. Used for generating a waveform on a GPIO pin or updating the SmaRTClock registers.
REGWRITE	0x04	Writes one or more bytes to registers with sequential addresses.
RAMREAD	0x06	Reads one or more bytes from sequential RAM locations.
RAMWRITE	0x08	Writes one or more bytes to sequential RAM locations.

Figure 6.2 shows a typical SPI transfer used to access internal registers or RAM. The first three bytes of the transfer are interpreted as COMMAND, ADDRH, and ADDRL. On a read, the fourth byte is a wait state in which the SPI shift register contents are ignored; starting with the fifth byte, data transfer begins. On a write, the fourth byte is the first data byte. The direction of data transfer depends on the specified command. The SPI transaction ends when NSS is de-asserted.

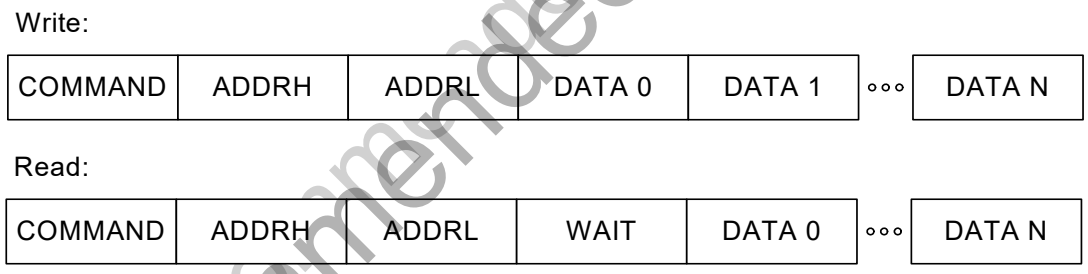


Figure 6.2. SPI Transfer

Note: Using the RAMREAD command to read an address outside the 0x400–0x4FF range will result in a data value of 0xDE.

Not Recommended for New Designs

6.2. Accessing Internal Registers and RAM over the SMBus Interface

The SMBus interface supports 6 commands which provide access to all internal registers and RAM. The six commands are listed in Table 6.2. Detailed information on the SMBus interface including bus timing can be found in Section "15. SMBus Interface" on page 104.

Table 6.2. SMBus Command Set

Command	OPCODE	Description
REGPOLL	0x01	Reads data from a single register. Used for polling a status bit.
REGREAD	0x02	Reads one or more bytes from registers with sequential addresses.
REGSET	0x03	Writes one or more bytes to a single register. Used for generating a waveform on a GPIO pin or updating the SmaRTClock registers.
REGWRITE	0x04	Writes one or more bytes to registers with sequential addresses.
RAMREAD	0x06	Reads one or more bytes from sequential RAM locations.
RAMWRITE	0x08	Writes one or more bytes to sequential RAM locations.

Figure 6.3 shows typical SMBus read and write transfers used to access internal registers or RAM. The first three bytes of a write transfer are interpreted as COMMAND, ADDRH, and ADDRL. For the REGPOLL, REGREAD, and RAMREAD commands, a repeated start is required to begin data transfer. The host controller may also choose to end the transfer with a STOP and then start a new read transfer using the same setup information. For the WRITE and RAMWRITE command, an SMBus write transfer is required. Starting with the fourth byte following the slave address, all bytes written are interpreted as data. The SMBus transfer ends when the host sends a STOP.

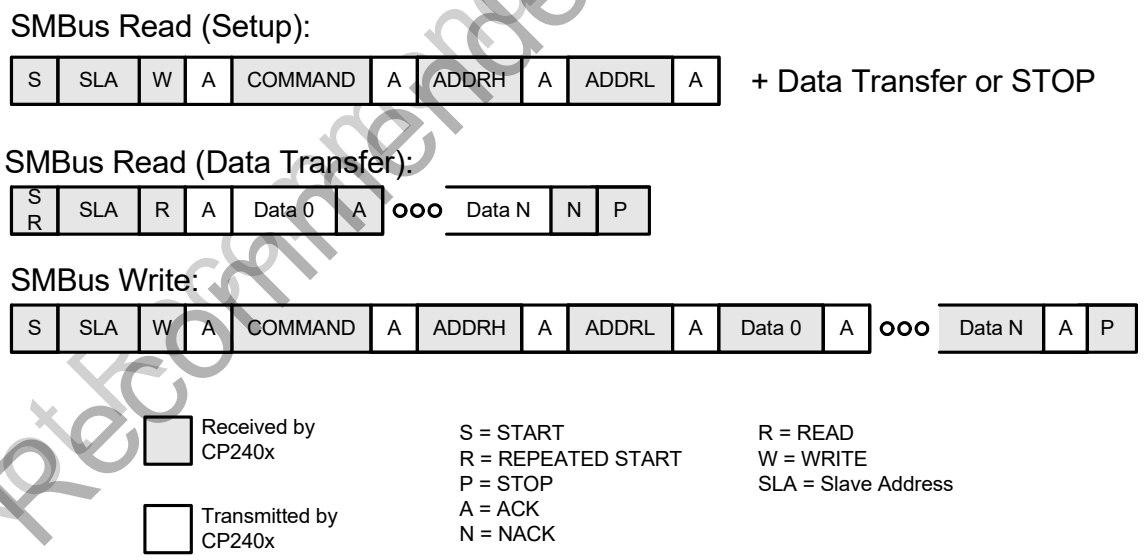


Figure 6.3. SMBus Transfers

Note: Using the RAMREAD command to read an address outside the 0x400–0x4FF range will result in a data value of 0xDE.

Not Recommended for New Designs

6.3. Internal Registers

The CP2400/1/2/3 internal registers are grouped into categories based on function. The memory map is organized to minimize register access time, by sequentially locating registers that can be read or written with a single block read or write. Table 6.3 shows the register memory map for all registers available on the device.

Table 6.3. Internal Register Memory Map

Register	Address	Description	Preserved	Page No.
SmaRTClock Registers				
RTCKEY	0x0A	RTC0 Indirect Address	N	72
RTCADR	0x0B	RTC0 Indirect Data	N	73
RTCDAT	0x0C	RTC0 Lock and Key	N	73
Interrupt Mask and Clocking Registers				
INT0EN	0x30	Interrupt Enable Register 0	N	43
INT1EN	0x31	Interrupt Enable Register 1	N	46
CLKSL	0x32	Clock Select	N	32
IOSCCN	0x33	Internal Oscillator Control	N	33
REVID	0x34	Revision Identifier	Y	33
Interrupt Status Registers				
INT0RD	0x40	Interrupt Status Register 0 (read-only)	N	42
INT1RD	0x41	Interrupt Status Register 1 (read-only)	N	45
ULPST	0x42	Ultra Low Power Status	Y	55
INT0	0x43	Interrupt Status Register 0 (self-clearing)	N	41
INT1	0x44	Interrupt Status Register 1 (self-clearing)	N	44
Timer 0 and Timer 1 Registers				
TMR0RLL	0x50	Timer 0 Reload Register Low Byte	N	94
TMR0RLH	0x51	Timer 0 Reload Register High Byte	N	94
TMR0L	0x52	Timer 0 Low Byte	N	95
TMR0H	0x53	Timer 0 High Byte	N	95
TMR0CN	0x54	Timer 0 Control	N	93
TMR1RLL	0x55	Timer 1 Reload Register Low Byte	N	99
TMR1RLH	0x56	Timer 1 Reload Register High Byte	N	99
TMR1L	0x57	Timer 1 Low Byte	N	100
TMR1H	0x58	Timer 1 High Byte	N	100
TMR1CN	0x59	Timer 1 Control	N	98
SMBus Registers				
SMBCF	0x68	SMBus Configuration	N	107
ULP/LCD0 Data Registers				
LCD0BLINK	0x80	LCD0 Segment Blink	Y	91
ULPMEM00	0x81	ULP Memory Byte 0	Y	57
ULPMEM01	0x82	ULP Memory Byte 1	Y	57
ULPMEM02	0x83	ULP Memory Byte 2	Y	57

Not Recommended for New Designs

Table 6.3. Internal Register Memory Map (Continued)

Register	Address	Description	Preserved	Page No.
ULPMEM03	0x84	ULP Memory Byte 3	Y	57
ULPMEM04	0x85	ULP Memory Byte 4	Y	57
ULPMEM05	0x86	ULP Memory Byte 5	Y	57
ULPMEM06	0x87	ULP Memory Byte 6	Y	57
ULPMEM07	0x88	ULP Memory Byte 7	Y	57
ULPMEM08	0x89	ULP Memory Byte 8	Y	57
ULPMEM09	0x8A	ULP Memory Byte 9	Y	57
ULPMEM10	0x8B	ULP Memory Byte 10	Y	57
ULPMEM11	0x8C	ULP Memory Byte 11	Y	57
ULPMEM12	0x8D	ULP Memory Byte 12	Y	57
ULPMEM13	0x8E	ULP Memory Byte 13	Y	57
ULPMEM14	0x8F	ULP Memory Byte 14	Y	57
ULPMEM15	0x90	ULP Memory Byte 15	Y	57
LCD Control Registers				
LCD0CN	0x95	LCD0 Control	Y	84
CONTRAST	0x96	LCD0 Contrast Adjustment	Y	85
LCD0CF	0x97	LCD0 Configuration	Y	86
LCD0DIVL	0x98	LCD0 Clock Divider High Byte	Y	87
LCD0DIVH	0x99	LCD0 Clock Divider Low Byte	Y	87
LCD0TOGR	0x9A	LCD0 Toggle Rate	Y	88
LCD0PWR	0x9B	LCD0 Power Mode	Y	89
Ultra Low Power Control Registers				
MSCN	0xA0	Master Control	Y	58
MSCF	0xA1	Master Configuration	Y	59
ULPCN	0xA2	Ultra Low Power Control	Y	54
Port I/O Configuration Registers				
P0OUT	0xB0	Port 0 Output Data Latch	N	66
P1OUT	0xB1	Port 1 Output Data Latch	N	66
P2OUT	0xB2	Port 2 Output Data Latch	N	66
P3OUT	0xB3	Port 3 Output Data Latch	N	66
P4OUT	0xB4	Port 4 Output Data Latch	N	66
P0MDI	0xB5	Port 0 Input Mode	N	67
P1MDI	0xB6	Port 1 Input Mode	N	67
P2MDI	0xB7	Port 2 Input Mode	N	67
P3MDI	0xB8	Port 3 Input Mode	N	67
P4MDI	0xB9	Port 4 Input Mode	N	67
P0MDO	0xBA	Port 0 Output Mode	N	67
P1MDO	0xBB	Port 1 Output Mode	N	67
P2MDO	0xBC	Port 2 Output Mode	N	67
P3MDO	0xBD	Port 3 Output Mode	N	67

Not Recommended for New Designs

Table 6.3. Internal Register Memory Map (Continued)

Register	Address	Description	Preserved	Page No.
P4MDO	0xBE	Port 4 Output Mode	N	67
P0DRIVE	0xBF	Port 0 Drive Strength	N	68
P1DRIVE	0xC0	Port 1 Drive Strength	N	68
P2DRIVE	0xC1	Port 2 Drive Strength	N	68
P3DRIVE	0xC2	Port 3 Drive Strength	N	68
P4DRIVE	0xC3	Port 4 Drive Strength	N	68
P0MATCH	0xC4	Port 0 Match	N	64
P1MATCH	0xC5	Port 1 Match	N	64
P2MATCH	0xC6	Port 2 Match	N	64
P3MATCH	0xC7	Port 3 Match	N	64
P4MATCH	0xC8	Port 4 Match	N	64
P0MSK	0xC9	Port 0 Mask	N	64
P1MSK	0xCA	Port 1 Mask	N	64
P2MSK	0xCB	Port 2 Mask	N	64
P3MSK	0xCC	Port 3 Mask	N	64
P4MSK	0xCD	Port 4 Mask	N	64
Port I/O Input and Status Registers				
PMATCHST	0xD0	Port Match Status	N	63
P0IN	0xD1	Port 0 Input	N	66
P1IN	0xD2	Port 1 Input	N	66
P2IN	0xD3	Port 2 Input	N	66
P3IN	0xD4	Port 3 Input	N	66
P4IN	0xD5	Port 4 Input	N	66

Not Recommended for New Designs

7. Interrupt Sources

The CP2400/1/2/3 can alert the host processor when any of the interrupt source events listed in Table 7.1 triggers an interrupt. The CP2400/1/2/3 alerts the host of pending interrupt events by setting the appropriate flags in the interrupt status registers and driving the $\overline{INT}$ pin low. The $\overline{INT}$ pin will remain asserted until all interrupt flags for enabled interrupts have been cleared by the host. Interrupt flags are cleared by reading the self-clearing interrupt status registers, INT0 and INT1. Interrupts can be disabled by clearing the corresponding bits in INT0EN and INT1EN.

Note: When SmaRTClock interrupts are enabled, they are also captured in the ULPST register. If the bits in ULPST are set, then the SmaRTClock interrupt flags in the INT0 register will not clear. To clear SmaRTClock interrupt events, first clear the ULPST register then clear INT0.

If the host processor does not utilize the $\overline{INT}$ pin, it can periodically read the interrupt status registers to determine if any interrupt-generating events have occurred. The INT0RD and INT1RD read-only registers provide a method of checking for interrupts without clearing the interrupt status registers.

Table 7.1. Interrupt Source Events

Event	Description	Pending Flag	Enable Flag
SmaRTClock Alarm	A SmaRTClock Alarm has occurred.	INT0.4	INT0EN.4
SmaRTClock Oscillator Failure	The SmaRTClock Oscillator has experienced a failure.	INT0.3	INT0EN.3
Port Match	A Port Match event has occurred.	INT0.0	INT0EN.0
Reset Complete	The device is now initialized and ready to communicate over the host interface.	INT1.4	INT1EN.4
Timer 1 Overflow	Timer 1 has overflowed from 0xFFFF to 0x0000 or a SmaRTClock capture event has occurred.	INT1.3	INT1EN.3
Timer 0 Overflow	Timer 0 has overflowed from 0xFFFF to 0x0000.	INT1.2	INT1EN.2

Not Recommended for New Designs

SFR Definition 7.1. INT0: Interrupt Status Register 0 (Self-Clearing)

Bit	7	6	5	4	3	2	1	0
Name			Reserved	ALRM	RTCFAIL			PMINT
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Address = 0x43

Bit	Name	Function
7:6	Unused	Read = 00b.
5	Reserved	Read = 0.
4	ALRM	**SmaRTClock Alarm Interrupt Flag.** 0: No SmaRTClock Alarm pending since ALRM was last cleared. 1: SmaRTClock Alarm pending.
3	RTCFAIL	**SmaRTClock Oscillator Fail Interrupt Flag.** 0: No SmaRTClock oscillator failure events detected since RTCFAIL was last cleared. 1: SmaRTClock oscillator failure detected.
2:1	Unused	Read = 00b.
0	PMINT	**Port Match Interrupt Flag.** 0: No Port Match events detected since PMINT was last cleared. 1: Port Match event pending.

Not Recommended for New Designs

SFR Definition 7.2. INT0RD: Interrupt Status Register 0 (Read-Only)

Bit	7	6	5	4	3	2	1	0
Name			Reserved	ALRMR	RTCFAILR			PMINTR
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Address = 0x40

Bit	Name	Function
7:6	Unused	Read = 00b.
5	Reserved	Read = 0.
4	ALRMR	**SmaRTClock Alarm Interrupt Flag.** 0: No SmaRTClock Alarm pending since ALRM was last cleared. 1: SmaRTClock Alarm pending.
3	RTCFAILR	**SmaRTClock Oscillator Fail Interrupt Flag.** 0: No SmaRTClock oscillator failure events detected since RTCFAIL was last cleared. 1: SmaRTClock oscillator failure detected.
2:1	Unused	Read = 00b.
0	PMINTR	**Port Match Interrupt Flag.** 0: No Port Match events detected since PMINT was last cleared. 1: Port Match event pending.

Not Recommended for New Designs

SFR Definition 7.3. INT0EN: Interrupt Enable Register 0

Bit	7	6	5	4	3	2	1	0
Name			Reserved	EALRM	ERTCFAIL			EPMINT
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	0	1	1	1

Address = 0x30

Bit	Name	Function
7:6	Unused	Read = 11b. Write = don't care.
5	Reserved	Read = varies. Write = must write 0b.
4	EALRM	**Enable SmaRTClock Alarm Interrupt.** This bit sets the masking of the SmaRTClock Alarm interrupt. 0: Disable SmaRTClock Alarm interrupts. 1: Enable interrupt requests generated by SmaRTClock Alarm Events.
3	ERTCFAIL	**Enable SmaRTClock Fail Interrupt.** This bit sets the masking of the SmaRTClock Oscillator Fail interrupt. 0: Disable SmaRTClock Oscillator Fail interrupt. 1: Enable interrupt requests generated by SmaRTClock Oscillator Failure.
2:1	Unused	Read = 11b. Write = don't care.
0	EPMINT	**Enable Port Match Interrupt.** This bit sets the masking of Port Match Interrupt. 0: Disable Port Match Interrupt. 1: Enable interrupt requests generated by Port Match events.

Not Recommended for New Designs

SFR Definition 7.4. INT1: Interrupt Status Register 1 (Self-Clearing)

Bit	7	6	5	4	3	2	1	0
Name				RSTC	T1F	T0F		
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	1	0	0

Address = 0x44

Bit	Name	Function
7:5	Unused	Read = 000b.
4	RSTC	**Reset Complete Interrupt Flag.** 0: Device has not yet finished initialization. 1: Device is ready for communication over the host interface.
3	T1F	**Timer 1 Overflow Interrupt Flag.** 0: Timer 1 has not overflowed and no capture events have occurred since T1F was last cleared. 1: Timer 1 has overflowed or a capture event has occurred since T1F was last cleared.
2	T0F	**Timer 0 Overflow Interrupt Flag.** 0: Timer 0has not overflowed since T0F was last cleared. 1: Timer 0 has overflowed since T0F was last cleared.
1:0	Unused	Read = 00b.

Not Recommended for New Designs

SFR Definition 7.5. INT1RD: Interrupt Status Register 1 (Read-Only)

Bit	7	6	5	4	3	2	1	0
Name				RSTCR	T1FR	T0FR		
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	1	0	1	0	0

Address = 0x41

Bit	Name	Function
7:5	Unused	Read = 000b.
4	RSTCR	**Reset Complete Interrupt Flag.** 0: Device has not yet finished initialization. 1: Device is ready for communication over the host interface.
3	T1FR	**Timer 1 Overflow Interrupt Flag.** 0: Timer 1 has not overflowed and no capture events have occurred since T1F was last cleared. 1: Timer 1 has overflowed or a capture event has occurred since T1F was last cleared.
2	T0FR	**Timer 0 Overflow Interrupt Flag.** 0: Timer 0has not overflowed since T0F was last cleared. 1: Timer 0 has overflowed since T0F was last cleared.
1:0	Unused	Read = 00b.

Not Recommended for New Designs

SFR Definition 7.6. INT1EN: Interrupt Enable Register 1

Bit	7	6	5	4	3	2	1	0
Name				ERSTC	ET1F	ET0F		
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Address = 0x31

Bit	Name	Function
7:5	Unused	Read = 111. Write = don't care.
4	ERSTC	**Enable Reset Complete Interrupt.** 0: Disable Reset Complete interrupt. 1: Enable interrupt requests generated when device is ready for communication over the host interface.
3	ET1F	**Enable Timer 1 Overflow Interrupt.** 0: Disable Timer 1 Overflow Interrupt. 1: Enable interrupt requests generated by Timer 1.
2	ET0F	**Enable Timer 0 Overflow Interrupt.** 0: Disable Timer 0 Overflow Interrupt. 1: Enable interrupt requests generated by Timer 0.
1:0	Unused	Read = 11. Write = don't care.

Not Recommended for New Designs

8. Reset Sources

Reset circuitry allows the CP2400/1/2/3 to be easily placed in a predefined default condition. Upon entry to this reset state, the following events occur:

- All direct and indirect registers are initialized to their defined reset values.
- Port I/O pins are forced into a high impedance state with a weak pull-up to V_{DD}.
- The $\overline{INT}$ pin is forced to a logic high state.
- The internal oscillator is stopped.
- All interrupts (except SmaRTClock Oscillator Fail) are enabled.

The CP2400/1/2/3 has two reset sources that place the device in the reset state. The method of entry to the reset state determines the amount of time spent in reset. Each of the following reset sources is described in the following sections:

- Power-On
- External $\overline{RST}$ Pin

Upon exit from the reset state, the device automatically starts the internal oscillator then asserts the interrupt pin. The device is fully functional after the interrupt pin is asserted.

8.1. Reset Initialization

After every CP2400/1/2/3 reset, the following initialization procedure is recommended to ensure proper device operation:

1. Wait for the Reset Complete Interrupt (interrupt pin assertion).
2. Disable interrupts (using INT0EN and INT1EN on page 43 and page 46) for events that will not be monitored or handled by the host processor. By default, all interrupts except for SmaRTClock Oscillator Fail are enabled after every reset.
3. Configure the device for the intended mode of operation.

Not Recommended for New Designs

8.2. Power-On Reset

During power-up, the CP2400/1/2/3 is held in the reset state until V_{DD} settles above VRST. A delay ($T_{PORDelay}$) occurs between the time V_{DD} reaches VRST and the time the device is released from reset. Refer to Table 3.3 for the Electrical Characteristics of the power-on reset circuit.

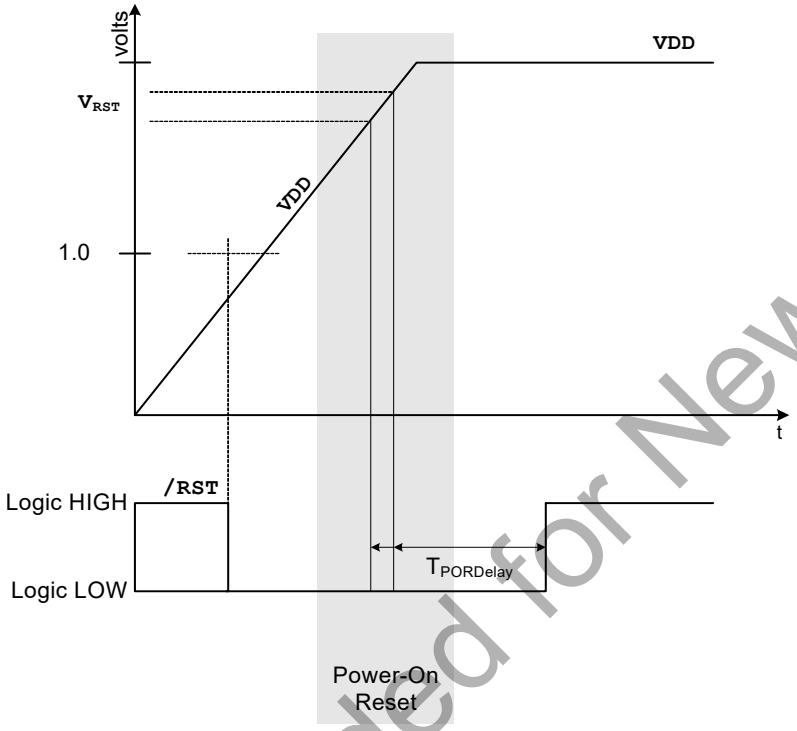


Figure 8.1. Reset Timing

8.3. External Pin Reset

The $\overline{RST}$ pin provides a means for external circuitry to force the CP2400/1/2/3 into a reset state. Asserting $\overline{RST}$ for at least T_{RST} will cause the CP2400/1/2/3 to enter the reset state. It is recommended to drive $\overline{RST}$ with a push-pull driver or add an external pull-up resistor to avoid erroneous noise-induced resets. The CP2400/1/2/3 will exit the reset state and generate a Reset Complete Interrupt approximately one $T_{STARTUP}$ delay after a logic high is detected on $\overline{RST}$. Refer to Table 3.3 on page 16 for the Electrical Characteristics.

Not Recommended for New Designs

9. Power Modes

The CP2400/1/2/3 has four power modes that can be used to minimize overall system power consumption. The power modes vary in device functionality and wake-up methods. Each of the following power modes is explained in the following sections:

- Normal Mode (Device Fully Functional)
- RAM Preservation Mode (Internal Oscillator Disabled)
- Ultra Low Power LCD Mode (Regulator Disabled)
- Ultra Low Power SmaRTClock Mode (Regulator Disabled, LCD Disabled)
- Shut Down Mode (All functionality Disabled)

The power modes above are achieved by disabling specific primary functions of the CP2400/1/2/3. Figure 9.1 shows how power is distributed throughout the CP2400/1/2/3. Additional secondary functions may also be disabled to save power. These are described in **Section "9.8. Disabling Secondary Device Functions" on page 58**.

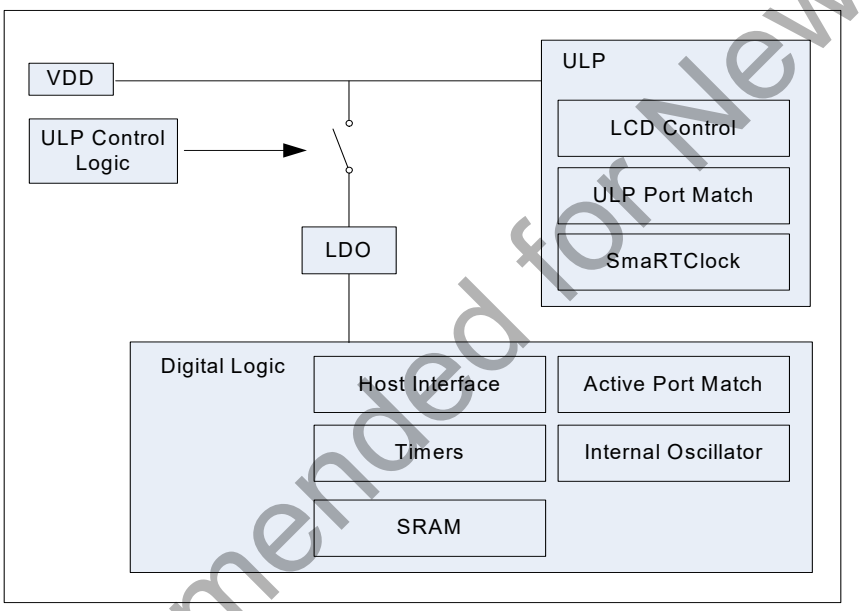


Figure 9.1. Power and Clock Distribution Control

Not Recommended for New Designs

9.1. Normal Mode

Normal mode should be used whenever the host controller is communicating with the CP2400/1/2/3. In this mode, the device is fully functional and the host interface is capable of operating at full speed. Typical normal mode power consumption is listed in Table 3.1 on page 12.

9.2. RAM Preservation Mode

In RAM Preservation Mode, the internal oscillator is disabled and the SmaRTClock oscillator provides the system clock. RAM Preservation Mode should be used when the CP2400/1/2/3 needs to be active for a prolonged period of time in which communication with the host microcontroller is not required. Examples of this include preserving the contents of RAM or using the fully featured Active port match capabilities. LCD and SmaRTClock functionality remains fully functional in RAM Preservation Mode. Interrupt latency does increase in this mode.

From Normal Mode, the device can be placed in RAM Preservation Mode using the following procedure:

1. Drive the $\overline{\text{CLK}}$ pin LOW.
2. Write 0x07 to the IOSCCN register to synchronize the oscillator control logic.
3. Write 0x03 to the IOSCCN register to switch oscillator control to the CLK pin.
4. Write 0x05 to the CLKSL register to select SmaRTClock oscillator as the system clock.
5. Drive the $\overline{\text{CLK}}$ pin HIGH.

From RAM Preservation Mode, the device can be returned to Normal Mode using the following procedure:

1. Drive the $\overline{\text{CLK}}$ pin LOW. This will force the system clock to Internal Oscillator divided by 1.
2. Write 0x06 to the IOSCCN register to force the internal oscillator to remain enabled.

See Table 3.4 for RAM Preservation Mode wake-up time. When using the SPI Interface, the $\overline{\text{CLK}}$ pin may be tied to NSS in order to wake the device from RAM Preservation Mode on NSS falling. The CLKOVR bit (MSCN.2) must be set to logic 0 and the SmaRTClock must be enabled and running in order to place the device in RAM Preservation Mode.

Not Recommended for New Designs

9.3. Ultra Low Power LCD Mode

In Ultra Low Power LCD Mode, the on-chip LDO is placed in a low power state and power is gated off from all digital logic residing outside the ULP block. The ULP block allows the device to refresh an LCD, maintain a real time clock, detect SmaRTClock Alarm, SmaRTClock Oscillator Fail, and ULP Port Match events. The Port Match functionality in ULP Mode differs from the functionality of Port Match when the device is in Normal or RAM Preservation Mode. See **Section "9.7. Port Match Functionality in the Ultra Low Power Modes" on page 56** for more details.
All Port I/O with the exception of P3.3-P4.3 must be configured to Analog mode prior to entering ULP Mode.

From Normal Mode, the device can be placed in ULP LCD Mode using the following procedure:

1. Set INT0EN:INT1EN to 0x1900. This enables the SmaRTClock Fail, SmaRTClock Alarm, and Port Match interrupts and disables all others.
2. Configure the bandgap into one of its low power modes by writing 0xC0 or 0x80 to MSCF. Choosing the loose bandgap regulation (MSCF = 0x80) will result in the lowest supply current at the expense of increased ripple in the LCD output voltage.
3. Drive the $\overline{\text{PWR}}$ or NSS pin LOW.
4. Set the LCDEN (ULPCN.3) to logic 1. If Port Match functionality is desired, also set the ULPEN (ULPCN.1) bit to logic 1.
5. Drive the $\overline{\text{PWR}}$ or NSS pin HIGH.

The device will not enter ULP mode if there are pending wake-up events, and the $\overline{\text{INT}}$ pin will remain asserted. To ensure that the device has successfully entered the low power mode, the host processor should verify that there are no pending wake-up events prior to placing the device in a ULP mode and that the $\overline{\text{INT}}$ pin remains de-asserted for 100 µs after placing the device in ULP mode. If the $\overline{\text{INT}}$ pin is found to be asserted, then the host controller should treat the situation as if the device has entered ULP and has been awoken by a wake-up event. The state of RAM and unpreserved registers should not be relied upon since the host controller will not be able to determine if the regulator has been disabled and re-enabled, or never disabled. The Port Match, SmaRTClock Alarm, and SmaRTClock Oscillator Fail interrupts should always be enabled any time the device is placed in a ULP mode.

Once the device enters ULP LCD Mode, it will remain in this low power mode until a SmaRTClock Alarm, SmaRTClock Oscillator Fail, or ULP Port Match wake-up event occurs. Once the device wakes up, it will generate a reset complete interrupt and assert the $\overline{\text{INT}}$ pin. The host controller may also wake up the device at any time.

To resume Normal Mode operation, the host controller should use the following procedure:

1. Drive the $\overline{\text{PWR}}$ or NSS pin LOW.
2. Wait for the $\overline{\text{INT}}$ pin to be asserted. See Table 3.4 for ULP Mode wake up time.
3. Re-initialize all registers which are not preserved during ULP mode. See Table 6.3 for a list of registers that preserve their state in ULP mode.

Note: The Port I/O state and configuration settings are preserved as long as the device is in the low power mode. Upon wake-up, all Port I/O state and configuration settings will reset, making all Port I/O digital inputs with weak pullups enabled. They will remain in this state until the host controller re-initializes the Port I/O state and configuration registers.

In the ULP LCD Mode, the SmaRTClock oscillator may be disabled if a low frequency CMOS clock (~32 kHz) is present at $\overline{\text{CLK}}$ pin. Set the RTCBYP bit (MSCN.7) to logic 1 in order to override the SmaRTClock with the CMOS clock available at the $\overline{\text{CLK}}$ pin. The SmaRTClock should be disabled by writing 0x00 to the indirect RTC0CN register instead of setting the RTCDIS bit (ULPCN.4) while entering ULP LCD Mode. When the SmaRTClock is disabled, SmaRTClock alarm and SmaRTClock oscillator fail detection functionality is no longer available.

Not Recommended for New Designs

9.4. Ultra Low Power SmaRTClock Mode

In Ultra Low Power SmaRTClock Mode, the on-chip LDO is placed in a low power state and power is gated off from all digital logic residing outside the ULP block. LCD functionality is disabled. The ULP block allows the device to maintain a real time clock and detect SmaRTClock Alarm, SmaRTClock Oscillator Fail, and ULP Port Match events. The Port Match functionality in ULP Mode differs from the functionality of Port Match when the device is in normal or RAM Preservation Mode. See **Section "9.7. Port Match Functionality in the Ultra Low Power Modes" on page 56** for more details.

From normal mode, the device can be placed in ULP SmaRTClock Mode using the following procedure:

1. Set INT0EN:INT1EN to 0x1900. This enables the SmaRTClock Fail, SmaRTClock Alarm, and Port Match interrupts and disables all others.
2. Place the bandgap into its lowest power mode by writing 0x80 to MSCF.
3. Drive the $\overline{\text{PWR}}$ or NSS pin LOW.
4. Set the ULPEN (ULPCN.1) bit to logic 1. If port match functionality is not desired, ensure that all the ULP Port Mask bits are set to logic 0 by writing 1 to ULPRST (ULPCN.1).
5. Drive the $\overline{\text{PWR}}$ or NSS pin HIGH.

The device will not enter any ULP mode if there are pending wake-up events, and the $\overline{\text{INT}}$ pin will remain asserted. To ensure that the device has successfully entered the low power mode, the host processor should verify that there are no pending wake-up events prior to placing the device in a ULP mode and that the $\overline{\text{INT}}$ pin remains de-asserted for 100 us after placing the device in ULP mode. If the $\overline{\text{INT}}$ pin is found to be asserted, then the host controller should treat the situation as if the device has entered ULP and has been awoken by a wake-up event. The state of RAM and unpreserved registers should not be relied upon since the host controller will not be able to determine if the regulator has been disabled and re-enabled, or never disabled. The Port Match, SmaRTClock Alarm, and SmaRTClock Oscillator Fail interrupts should always be enabled any time the device is placed in a ULP mode.

Once the device enters ULP SmaRTClock Mode, it will remain in this low power mode until a SmaRTClock Alarm, SmaRTClock Oscillator Fail, or ULP Port Match wake-up event occurs. Once the device wakes up, it will generate a reset complete interrupt and assert the $\overline{\text{INT}}$ pin. The host controller may also wake up the device at any time.

To resume normal mode operation, the host controller should use the following procedure:

1. Drive the $\overline{\text{PWR}}$ or NSS pin LOW.
2. Wait for the $\overline{\text{INT}}$ pin to be asserted. See Table 3.4 for ULP Mode wake up time.
3. Re-initialize all registers which are not preserved during ULP mode. See Table 6.3 for a list of registers that preserve their state in ULP mode.

Note: The Port I/O state and configuration settings are preserved as long as the device is in the low power mode. Upon wake-up, all Port I/O state and configuration settings will reset, making all Port I/O digital inputs with weak pullups enabled. They will remain in this state until the host controller re-initializes the Port I/O state and configuration registers.

In the ULP SmaRTClock Mode, the SmaRTClock oscillator may be disabled if a low frequency CMOS clock (~32 kHz) is present at $\overline{\text{CLK}}$ pin. Set the RTCBYP bit (MSCN.7) to logic 1 in order to override the SmaRTClock with the CMOS clock available at the $\overline{\text{CLK}}$ pin. The SmaRTClock should be disabled by writing 0x00 to the indirect RTC0CN register instead of setting the RTCDIS bit (ULPCN.4). When the SmaRTClock is disabled, SmaRTClock alarm and SmaRTClock oscillator fail detection functionality is no longer available.

Not Recommended for New Designs

9.5. Shutdown Mode

Shutdown mode is the lowest power mode for the CP2400/1/2/3. All device functionality is disabled in this mode and a reset is required to wake up the device. This mode is typically used when the device is not needed for prolonged periods of time.

From Normal Mode, the device can be placed in shutdown mode using the following procedure:

1. Set INT0EN:INT1EN to 0x1900. This enables the SmaRTClock Fail, SmaRTClock Alarm, and Port Match interrupts and disables all others.
2. Ensure that all ULP Port Mask bits are set to logic 0 by writing 1 to ULPRST (ULPCN.1).
3. Configure the bandgap for Shutdown Mode by writing 0x80 to MSCF.
4. Drive the $\overline{\text{PWR}}$ or NSS pin LOW.
5. Set the $\overline{\text{RTCDIS}}$ (ULPCN.4) and the ULPEN (ULPCN.1) bit to logic 1.
6. Drive the $\overline{\text{PWR}}$ or NSS pin HIGH.

The device will not enter Shutdown if there are pending wake-up events, and the $\overline{\text{INT}}$ pin will remain asserted. To ensure that the device has successfully entered the low power mode, the host processor should verify that there are no pending wake-up events prior to placing the device in Shutdown Mode and that the $\overline{\text{INT}}$ pin remains de-asserted for 100 µs after placing the device in Shutdown Mode. If the $\overline{\text{INT}}$ pin is found to be asserted after the device has been placed in Shutdown, the device should be reset and placed in shutdown again. It is essential that all ULP Port Mask bits be set to logic 0 before the device is placed in Shutdown in order to prevent the possibility of a partial wake-up due to a Port Match event. The Port Match, SmaRTClock Alarm, and SmaRTClock Oscillator Fail interrupts should always be enabled any time the device is placed in Shutdown mode.

Note: The Port I/O state and configuration settings are preserved as long as the device is in Shutdown. Upon reset, all Port I/O state and configuration settings will reset, making all Port I/O digital inputs with weak pull-ups enabled. They will remain in this state until the host controller re-initializes the Port I/O state and configuration registers.

Not Recommended for New Designs

SFR Definition 9.1. ULPCN: Ultra Low Power Control Register

Bit	7	6	5	4	3	2	1	0
Name				RTCDIS	LCDEN	Reserved	ULPEN	ULPPMPOL
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Address = 0xA2

Bit	Name	Function
7:5	Unused	Read = 000b. Write = Don't Care.
4	RTCDIS	**Ultra Low Power Mode SmaRTClock Disable.** When set to 1, the SmaRTClock oscillator will be disabled two SmaRTClock cycles after entry into ULP Mode. This allows the device to enter its Shutdown Mode. Any write operation that sets this bit to 1b must also set ULPEN to 1b.
3	LCDEN	**Ultra Low Power LCD Enable.** When set to 1, LCD Functionality is enabled in ULP mode. Rising edge transitions on NSS and $\overline{PWR}$ disable the internal LDO and place the device into the ultra low power mode. A falling edge transition on NSS or $\overline{PWR}$ will re-enable the regulator and return the device to normal power mode. This bit is self-clearing upon wake-up from the ultra low power mode.
2	Reserved	Read = 0b. Must write 0b.
1	ULPEN	**Ultra Low Power Port Match Enable.** When set to 1, Port Match Functionality is enabled in ULP mode. Rising edge transitions on NSS and $\overline{PWR}$ disable the internal LDO and place the device into the ultra low power mode. A falling edge transition on NSS or $\overline{PWR}$ will re-enable the regulator and return the device to normal power mode. This bit is self-clearing upon wake-up from the ultra low power mode.
0	ULPPMPOL	**Ultra Low Power Port Match Polarity.** 0: ULP Port Match wake-up occurs on rising edge transitions (level sensitive). 1: ULP Port Match wake-up occurs on falling edge transitions (level sensitive).

Note: The state of ULPPMPOL should not be changed in the same write which enables the ULP modes. Rather, the state of ULPPMPOL should be set first, then the ULP mode should be enabled.

Not Recommended for New Designs

9.6. Determining the ULP Mode Wake-Up Source

After waking from ULP Mode, the ULPST register may be used to determine the cause of wake up. The three possible wake up sources are SmaRTClock Alarm, SmaRTClock Oscillator Failure, and ULP Port Match. If none of the bits in ULPST are set, then the wake up was due to the NSS or $\overline{PWR}$ pin falling edge.

This register may be cleared by writing a 1 to the CLEAR (MSCN.6) bit in the master control register.

SFR Definition 9.2. ULPST: Ultra Low Power Status Register

Bit	7	6	5	4	3	2	1	0
Name						RTCFAIL	RTCALRM	ULPPM
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	varies

Address = 0x42

Bit	Name	Function
7:3	Unused	Read = 00000b. Write = Don't Care.
2	RTCFAIL	**SmaRTClock Oscillator Fail Wake Up Indicator.** 0: Source of last wake up was not a SmaRTClock Oscillator Fail. 1: Source of last wake up was a SmaRTClock Oscillator Fail.
1	RTCALRM	**SmaRTClock Alarm Wake Up Indicator.** 0: Source of last wake up was not a SmaRTClock Alarm. 1: Source of last wake up was a SmaRTClock Alarm.
0	ULPPM	**Ultra Low Power Port Match Wake Up Indicator.** 0: Source of last wake up was not a ULP Port Match. 1: Source of last wake up was a ULP Port Match.

Not Recommended for New Designs

9.7. Port Match Functionality in the Ultra Low Power Modes

The ultra low power LCD and SmaRTClock modes support port match wake-up. ULP SmaRTClock mode supports port match on all P0, P1, P2, and P3 pins. ULP LCD mode supports port match on P3.3, P3.4, P3.5, P3.6, and P3.7. ULP Port Match events can be generated on rising or falling edges; however, all events are configured to the same polarity using the ULPPMPOL bit (ULPCN.0). ULP Port Match is level sensitive and a new Port Match event will be generated every clock cycle as long as the I/O state matches the polarity set by the ULPPMPOL bit.

Note: In ULP LCD Mode, when using a 4-mux LCD, port match may only be used to detect rising edges.

Each Port I/O that participates in ULP Port Match is individually maskable to allow or disallow the generation of Port Match events. The most significant bit in each 4-bit nibble of ULP Memory controls the masking of a single Port I/O. For example, the masking of P3.4 and P3.5 are controlled by bit 3 and bit 7 of ULPMEM14, respectively. Table 9.1 and Table 9.2 show the ULP Mask bit locations for all I/O capable of port match when the device is in ULP SmaRTClock and ULP LCD mode, respectively. A mask setting of 0 will prevent the generation of Port Match events from the specified I/O and a mask setting of 1 will allow generation of Port Match events from the specified I/O. Port I/O to be used for ULP Port Match must be configured as digital pins. Setting the ULPRST (ULPCN.1) to logic 1 will reset all Port Mask bits to 0.

ULP Port Match is enabled upon entry into ULP mode when the ULPEN bit (ULPCN.1) is set to logic 1 and disabled upon wake-up from ULP mode. The ULPST register may be used to determine when a ULP Port Match event has occurred. When enabled, the Port Match interrupt will occur when an Active Mode Port Match or ULP Port Match event occurs.

Table 9.1. ULP SmaRTClock Port Match Mask Bit Locations

ULP Memory	Bit 7 Masks	Bit 3 Masks
ULPMEM00	P0.1	P0.0
ULPMEM01	P0.3	P0.2
ULPMEM02	P0.5	P0.4
ULPMEM03	P0.7	P0.6
ULPMEM04	P1.1	P1.0
ULPMEM05	P1.3	P1.2
ULPMEM06	P1.5	P1.4
ULPMEM07	P1.7	P1.6
ULPMEM08	P2.1	P2.0
ULPMEM09	P2.3	P2.2
ULPMEM10	P2.5	P2.4
ULPMEM11	P2.7	P2.6
ULPMEM12	P3.1	P3.0
ULPMEM13	P3.3	P3.2
ULPMEM14	P3.5	P3.4
ULPMEM15	P3.7	P3.6

Table 9.2. ULP LCD Port Match Mask Bit Locations

ULP Memory	Bit 7 Masks	Bit 3 Masks
ULPMEM13	P3.3	N/A
ULPMEM14	P3.5	P3.4
ULPMEM15	P3.7	P3.6

Not Recommended for New Designs

SFR Definition 9.3. ULPMEMn: ULP Memory

Bit	7	6	5	4	3	2	1	0
Name	ULPMEMn							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Addresses: ULPMEM00 = 0x81, ULPMEM01 = 0x82, ULPMEM02 = 0x83, ULPMEM03 = 0x84, ULPMEM04 = 0x85, ULPMEM05 = 0x86, ULPMEM06 = 0x87, ULPMEM07 = 0x88, ULPMEM08 = 0x89, ULPMEM09 = 0x8A, ULPMEM10 = 0x8B, ULPMEM11 = 0x8C, ULPMEM12 = 0x8D, ULPMEM13 = 0x8E, ULPMEM14 = 0x8F, ULPMEM15 = 0x90.

Bit	Name	Function
7:0	ULPMEMn	**ULP Memory.** Each nibble controls one I/O pin. See “12.5. Mapping ULP Memory to LCD Pins” on page 90 for information on how ULP Memory is used with the LCD function. See **Section “9.7. Port Match Functionality in the Ultra Low Power Modes” on page 56** for information on how ULP Memory is used with the ULP Port Match function.

Not Recommended for New Designs

9.8. Disabling Secondary Device Functions

The MSCN and MSCF registers provide additional ways of saving power by disabling unnecessary functionality.

SFR Definition 9.4. MSCN: Master Control Register

Bit	7	6	5	4	3	2	1	0
Name	RTCBYP	CLEAR	ADRINV	RTCOD	SRAMD	CLKOVR	ULPRST	LCDEN
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Address = 0xA0

Bit	Name	Function
7	RTCBYP	**SmaRTClock Oscillator Bypass.** When set to 1, the SmaRTClock oscillator clock is bypassed and the $\overline{CLK}$ pin is used to drive the low frequency clock used for ULP operations.
6	CLEAR	**ULP Status Clear.** Writing 1 to this register clears all bits in the ULP status register (ULPST).
5	ADRINV	**SRAM Address Invert.** When set to 1, the least significant byte of the SRAM target address is inverted. This allows the SRAM to be accessed in reverse sequential order using a single block read or write. For example, a block read from addresses 0x0400 to 0x04FF will return data from RAM locations 0x04FF to 0x0400.
4	RTCOD	**SmaRTClock Oscillator Output Disable.** When set to 1, the SmaRTClock oscillator output is gated off, and does not drive the low frequency clock used for ULP operations.
3	SRAMD	**SRAM Disable.** 0: The SRAM is enabled. 1: The SRAM is disabled.
2	CLKOVR	**System Clock Override.** 0: The CLKSL register determines the system clock. 1: The system clock is the CMOS clock input through the $\overline{CLK}$ pin.
1	ULPRST	**ULP Memory Reset.** Writing 1 to this bit clears all values in the ULP Memory to 0x00. This bit can be used to quickly set all ULP Port Mask bits to logic 0.
0	LCDEN	**LCD Enable.** 0: LCD Functionality is disabled. 1: LCD Functionality is enabled.

Not Recommended for New Designs

SFR Definition 9.5. MSCF: Master Configuration Register

Bit	7	6	5	4	3	2	1	0
Name	BGMD[1:0]		Reserved	Reserved	Reserved	Reserved	Reserved	CPBYP
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Address = 0xA1

Bit	Name	Function
7:6	BGMD[1:0]	**Band Gap Power Mode.** 00: Band Gap is in Normal Power Mode. 01: Reserved. 10: Band Gap is configured for low power with loose voltage regulation (required setting for Shutdown Mode). 11: Band Gap is configured for low power with tight voltage regulation.
5:1	Reserved	Read = Varies. Must write 00000b.
0	CPBYP	**Charge Pump Bypass.** When set to 1, the charge pump is bypassed and disabled. VDD is used as the VLCD supply voltage.

Note: When the band gap is configured for low power mode with loose voltage regulation, the LCD0CF register should be adjusted so that charge pump cycles occur at least once every 2 ms.

Not Recommended for New Designs

10. Port Input/Output

CP2400/1/2/3 devices have 36 (48-pin packages) or 20 (32-pin packages) multi-function I/O pins. Port pins are organized as byte-wide ports and may be used for general purpose I/O, generating a Port Match interrupt, or for an analog function (e.g., LCD).

Note: The port match functionality described in this chapter only applies when the device is awake (Normal and Idle Power Modes). Refer to the Power Modes chapter for information on port match wake-up from ULP or shutdown mode.

All Port I/Os are 5 V tolerant when used as digital inputs or open-drain outputs. For Port I/Os configured as digital push-pull outputs, current is sourced from the V_{DD} supply. See Section 10.1 for more information on Port I/O operating modes and the electrical specifications chapter for detailed electrical specifications. Figure shows a block diagram of the Port I/O for the 48-pin packaged devices. The 32-pin packaged devices are functionally the same, however, they have less I/O. Refer to the System Overview for a detailed block diagram of 32-pin devices.

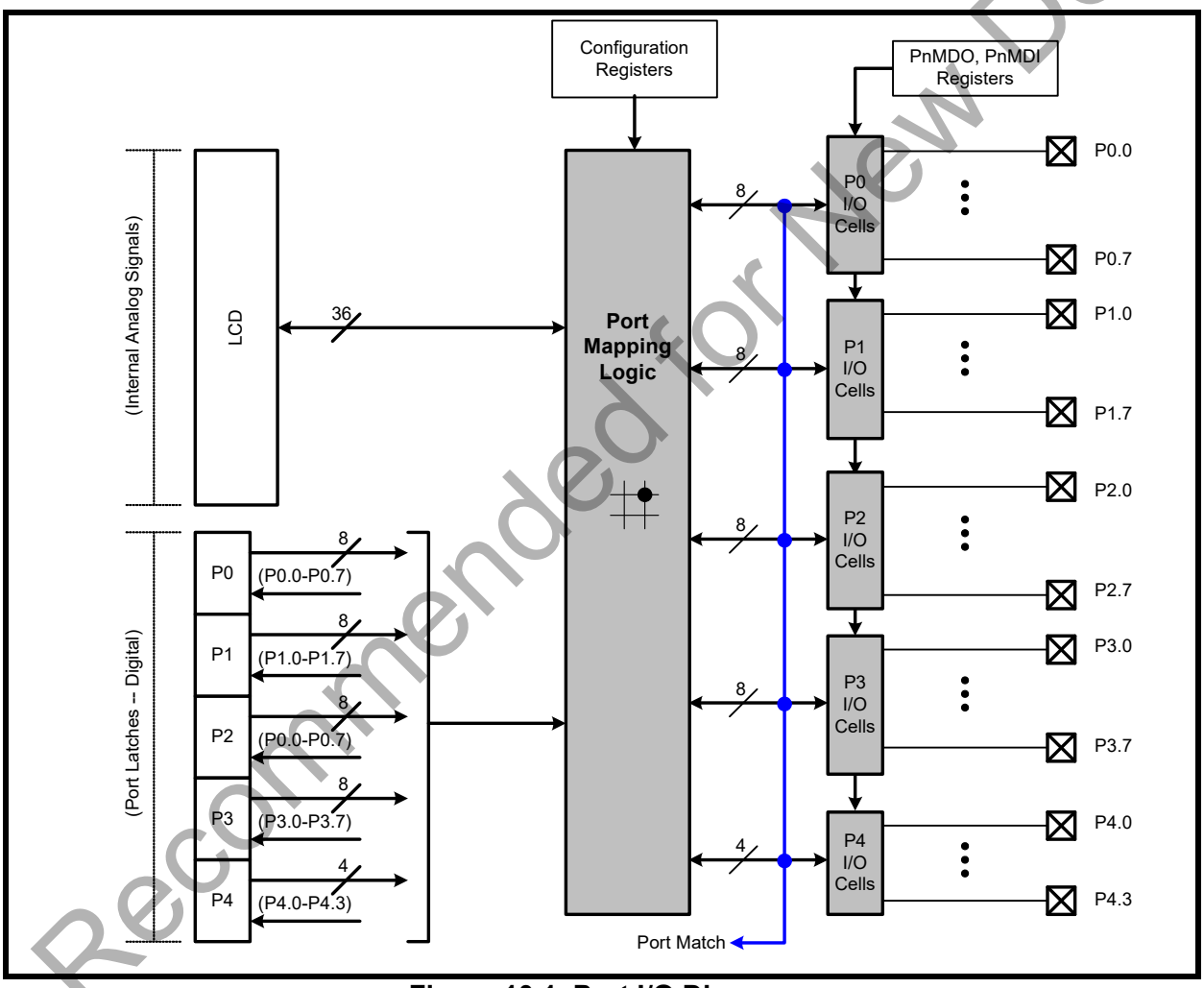


Figure 10.1. Port I/O Diagram

Not Recommended for New Designs

10.1. Port I/O Modes of Operation

All port pins use the Port I/O cell shown in Figure 10.2. Each Port I/O cell can be configured by software for analog I/O or digital I/O using the PnMDI registers. On reset or wake-up from ULP mode, all Port I/O cells default to a digital high impedance state with weak pull-ups enabled.

10.1.1. Port Pins Configured for Analog I/O

Any pins to be used for LCD should be configured for analog I/O (PnMDI.n = 0). When a pin is configured for analog I/O, its weak pullup and digital output driver and receiver are disabled. Port pins configured for analog I/O will always read back a value of 0 regardless of the actual voltage on the pin.

10.1.2. Port Pins Configured For Digital I/O

Any pins to be used for GPIO or Port Match should be configured as digital I/O (PnMDI.n = 1). For digital I/O pins, one of two output modes (push-pull or open-drain) must be selected using the PnMDO registers.

Push-pull outputs (PnMDO.n = 1) always drive the Port pad to the V_{DD} or GND supply rails based on the output logic value of the Port pin. Open-drain outputs have the high side driver disabled; therefore, they only drive the Port pad to GND when the output logic value is 0 and become high impedance inputs (both high and low drivers turned off) when the output logic value is 1.

When a digital I/O cell is placed in the high impedance state, a weak pull-up transistor pulls the Port pad to the VDD supply voltage to ensure the digital input is at a defined logic state. Weak pullups are disabled when the I/O cell is driven to GND to minimize power consumption. The user must ensure that digital I/O are always internally or externally pulled or driven to a valid logic state. An analog signal applied to a digital I/O pin will result in increased power consumption.

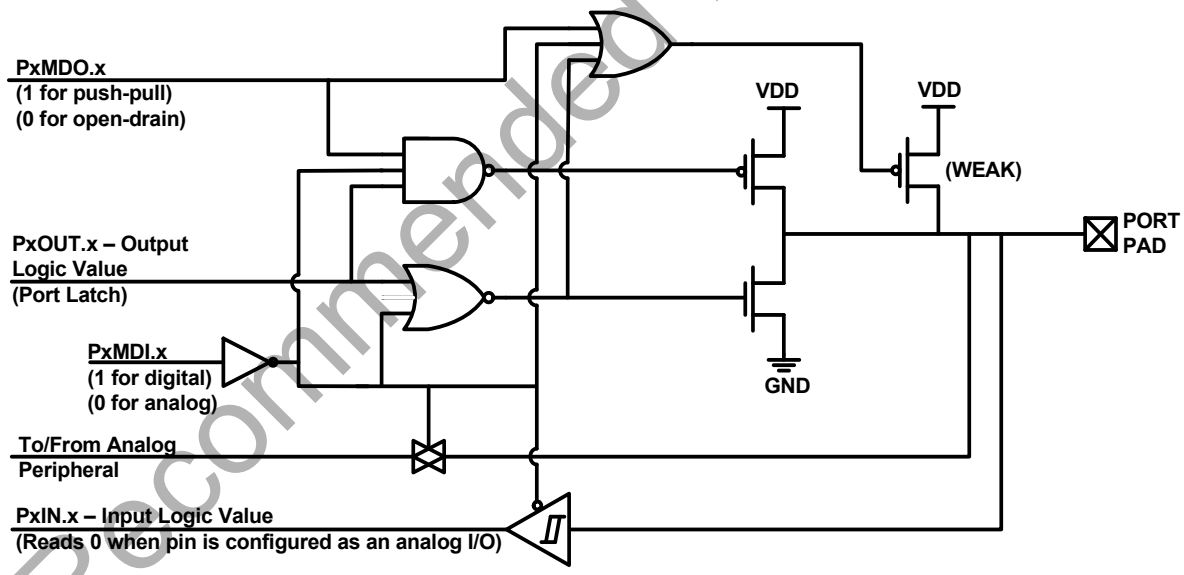


Figure 10.2. Port I/O Cell Block Diagram

Not Recommended for New Designs

10.1.3. Interfacing Port I/O to 5 V and 3.3 V Logic

All Port I/Os configured for digital, open-drain operation are capable of interfacing to digital logic operating at a supply voltage higher than 4.5 V and less than 5.25 V. When the supply voltage is in the range of 1.8 to 2.2 V, the I/O may also interface to digital logic operating between 3.0 to 3.6 V. An external pull-up resistor to the higher supply voltage is typically required for most systems.

Important Notes:

- When interfacing to a signal that is between 4.5 and 5.25 V, the maximum clock frequency that may be input on a GPIO pin is 12.5 MHz. The exception to this rule is when routing an external CMOS clock to P0.3, in which case a signal up to 25 MHz is valid as long as the rise time (10% to 90%) is shorter than 1.8 ns.
- When the supply voltage is less than 2.8 V and interfacing to a signal that is between 3.0 and 3.6 V, the maximum clock frequency that may be input on a GPIO pin is 3.125 MHz. The exception to this rule is when routing an external CMOS clock to P0.3, in which case a signal up to 25 MHz is valid as long as the rise time (10% to 90%) is shorter than 1.2 ns.
- In a multi-voltage interface, the external pull-up resistor should be sized to allow a current of at least 150 µA to flow into the Port pin when the supply voltage is between (VDD_MCU/DC+ plus 0.4 V) and (VDD_MCU/DC+ plus 1.0 V). Once the Port pad voltage increases beyond this range, the current flowing into the Port pin is minimal.
- These guidelines only apply to multi-voltage interfaces. Port I/Os may always interface to digital logic operating at the same supply voltage.

10.1.4. Increasing Port I/O Drive Strength

Port I/O digital output drivers support a high and low drive strength; the default is low drive strength. The drive strength of a Port I/O can be configured using the PnDRIVE registers. See **Table 3.2 on page 13** for the difference in output drive strength between the two modes.

10.2. Assigning Port I/O Pins to Analog and Digital Functions

Port I/O pins are multi-function and may be used for multiple purposes. The following process can be used to assign GPIO pins to their appropriate function.

1. Determine the pins to be used for the LCD function. These pins need to be configured for Analog I/O.
2. Any remaining unused pins may be used for GPIO or Port Match. These pins need to be configured for Digital I/O. Note: ULP Port Match is only available on a limited number of pins. See **Section "9.7. Port Match Functionality in the Ultra Low Power Modes" on page 56** for more details. All Port I/O with the exception of P3.3–P4.3 must be configured to Analog mode prior to entering ULP Mode.

Not Recommended for New Designs

10.3. Active Mode Port Match

Port match functionality allows system events to be triggered by a logic value change on a GPIO pin. A software controlled value stored in the PnMATCH registers specifies the expected or normal logic values of the associated Port. A Port mismatch event occurs if the logic levels of the Port's input pins no longer match the software controlled value. This allows software to be notified if a certain change or pattern occurs on an input pin.

The PnMSK registers can be used to individually select which pins should be compared against the PnMATCH registers. A Port mismatch event is generated if (PnIN & PnMSK) does not equal (PnMATCH & PnMSK) for all Ports.

A Port mismatch event may be used to generate an interrupt. **See "7. Interrupt Sources" on page 40** for more details on handling an interrupt.

SFR Definition 10.1. PMATCHST: Port Match Status Register

Bit	7	6	5	4	3	2	1	0
Name				P4M	P3M	P2M	P1M	P0M
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Address = 0xD0

Bit	Name	Function
7:5	Unused	Read = 000b. Write = Don't Care.
4	P4M	**Port 4 Match.** 0: No port mismatch events have been detected on P4. 1: A port mismatch event is present on P4.
3	P3M	**Port 3 Match.** 0: No port mismatch events have been detected on P3. 1: A port mismatch event is present on P3.
2	P2M	**Port 2 Match.** 0: No port mismatch events have been detected on P2. 1: A port mismatch event is present on P2.
1	P1M	**Port 1 Match.** 0: No port mismatch events have been detected on P1. 1: A port mismatch event is present on P1.
0	P0M	**Port 0 Match.** 0: No port mismatch events have been detected on P0. 1: A port mismatch event is present on P0.

Not Recommended for New Designs

SFR Definition 10.2. PnMSK: Port n Mask Register

Bit	7	6	5	4	3	2	1	0
Name	PnMSK[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

Address: P0MSK = 0xC9; P1MSK = 0xCA; P2MSK = 0xCB; P3MSK = 0xCC; P4MSK = 0xCD

Bit	Name	Function
7:0	PnMSK[7:0]	**Port n Mask Value.** Selects the Pn pins to be compared with the corresponding bits in PnMATCH. 0: Pn.x pin pad logic value is ignored and cannot cause a Port Mismatch event. 1: Pn.x pin pad logic value is compared to PnMATCH.x.

SFR Definition 10.3. PnMATCH: Port n Match Register

Bit	7	6	5	4	3	2	1	0
Name	PnMATCH[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

Address: P0MATCH = 0xC4; P1MATCH = 0xC5; P2MATCH = 0xC6; P3MATCH = 0xC7; P4MATCH = 0xC8

Bit	Name	Function
7:0	PnMATCH[7:0]	**Port n Match Value.** Match comparison value used on Port n for bits whose PnMSK is set to 1. 0: Pn.x pin logic value is compared with logic LOW. 1: Pn.x pin logic value is compared with logic HIGH.

Not Recommended for New Designs

10.4. Registers for Accessing and Configuring Port I/O

All Port I/O are accessed and configured through registers. When writing to a Port, the value written to the PnOUT register is latched to maintain the output data value at each pin. When reading, the logic levels of the Port's input pins are returned in the PnIN. If the PnOUT register is read, the value returned will be the value of the output latch, not the logic level of the port pad. The PnIN register is read only.

The Port input mode of the I/O pins is defined using the Port Input Mode registers (PnMDI). Each Port cell can be configured for analog or digital I/O. The output driver characteristics of the digital I/O pins are defined using the Port Output Mode registers (PnMDO). Each Port Output driver can be configured as either open drain or push-pull. To configure a pin as a digital input, configure it as an open drain output and write 1 to its port latch.

The drive strength of the output drivers are controlled by the Port Drive Strength (PnDRIVE) registers. The default is low drive strength. See **Table 3.2 on page 13** for the difference in output drive strength between the two modes.

Not Recommended for New Designs

SFR Definition 10.4. PnOUT: Port n Output Latch

Bit	7	6	5	4	3	2	1	0
Name	PnOUT[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

Address: P0OUT = 0xB0; P1OUT = 0xB1; P2OUT = 0xB2; P3OUT = 0xB3; P4OUT = 0xB4

Bit	Name	Function
7:0	PnOUT[7:0]	**Port n Output Latch.** Sets or reads the Port latch logic value. 0: Pn.x output latch is logic LOW. 1: Pn.x output latch is logic HIGH.

SFR Definition 10.5. PnIN: Port n Input

Bit	7	6	5	4	3	2	1	0
Name	PnIN[7:0]							
Type	R							
Reset	1	1	1	1	1	1	1	1

Address: P0IN = 0xD1; P1IN = 0xD2; P2IN = 0xD3; P3IN = 0xD4; P4IN = 0xD5

Bit	Name	Function
7:0	PnIN[7:0]	**Port n Input.** Reads the Port pin logic state in Port cells configured for digital I/O. 0: Pn.x Port pin is logic LOW. 1: Pn.x Port pin is logic HIGH.

Not Recommended for New Designs

SFR Definition 10.6. PnMDI: Port n Input Mode

Bit	7	6	5	4	3	2	1	0
Name	P0MDI[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

Address: P0MDI = 0xB5; P1MDI = 0xB6; P2MDI = 0xB7; P3MDI = 0xB8; P4MDI = 0xB9

Bit	Name	Function
7:0	PnMDI[7:0]	**Pn Analog Configuration Bits.** Port pins configured for analog mode have their weak pullup, digital driver, and digital receiver disabled. 0: Corresponding Pn.x pin is configured for analog I/O. 1: Corresponding Pn.x pin is configured for digital I/O.

SFR Definition 10.7. PnMDO: Port n Output Mode

Bit	7	6	5	4	3	2	1	0
Name	PnMDO[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

Address: P0MDO = 0xBA; P1MDO = 0xBB; P2MDO = 0xBC; P3MDO = 0xBD; P4MDO = 0xBE

Bit	Name	Function
7:0	PnMDO[7:0]	**Pn Output Configuration Bits.** 0: Corresponding Pn.x Output is open-drain. 1: Corresponding Pn.x Output is push-pull.

Not Recommended for New Designs

SFR Definition 10.8. PnDRIVE: Port n Drive Strength

Bit	7	6	5	4	3	2	1	0
Name	PnDRIVE[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

Address: P0DRIVE = 0xBF; P1DRIVE = 0xC0; P2DRIVE = 0xC1; P3DRIVE = 0xC2; P4DRIVE = 0xC3

Bit	Name	Function
7:0	PnDRIVE[7:0]	**Pn Drive Strength Configuration Bits.** Configures digital I/O Port cells to high or low output drive strength. 0: Corresponding Pn.x has low output drive strength. 1: Corresponding Pn.x has high output drive strength.

Not Recommended for New Designs

11. SmaRTClock (Real Time Clock)

CP2400/1/2/3 devices include an ultra low power 32-bit SmaRTClock Peripheral (Real Time Clock) with alarm. The SmaRTClock has a dedicated 32 kHz oscillator that can be configured for use with or without a crystal. No external resistor or loading capacitors are required. The on-chip loading capacitors are programmable to 16 discrete levels allowing compatibility with a wide range of crystals.

The SmaRTClock allows a maximum of 36 hour 32-bit independent time-keeping when used with a 32.768 kHz Watch Crystal. The SmaRTClock provides an Alarm and Missing SmaRTClock events, which could be used to wake up from the ultra low power mode.

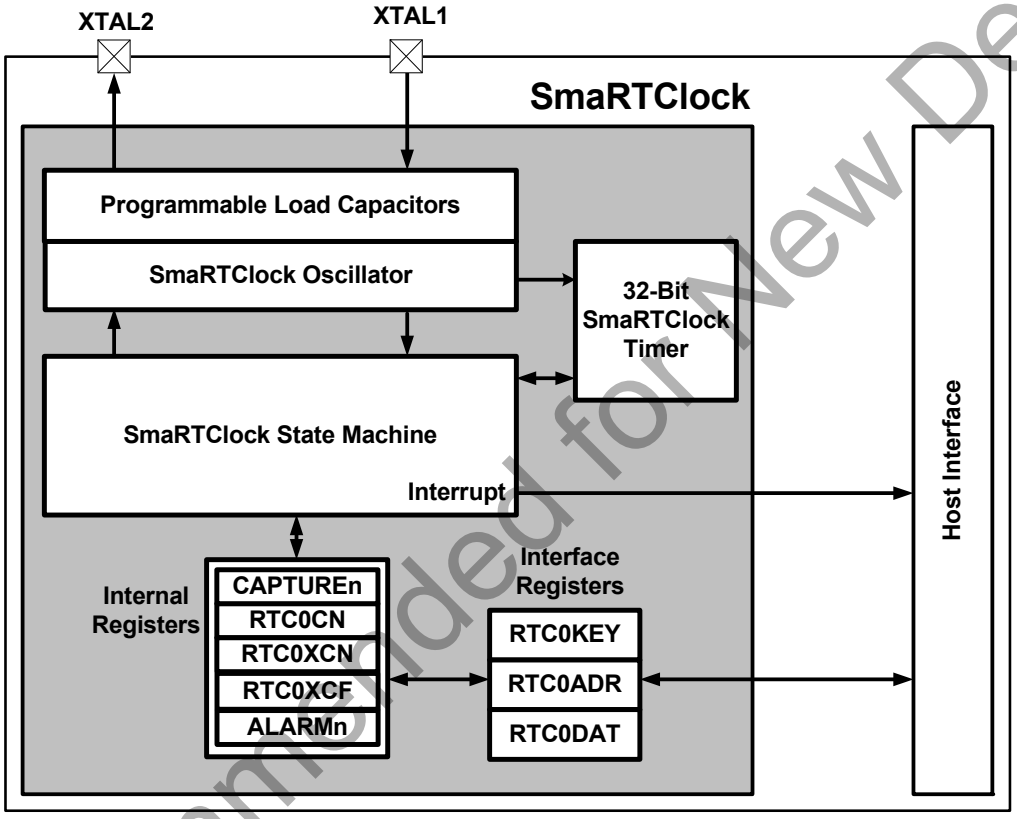


Figure 11.1. SmaRTClock Block Diagram

Not Recommended for New Designs

11.1. SmaRTClock Interface

The SmaRTClock Interface consists of three registers: RTCKEY, RTCADR, and RTCDAT. These interface registers are located on the CP2400/1/2/3 register map and provide access to the SmaRTClock internal registers listed in Table 11.1. The SmaRTClock internal registers can only be accessed indirectly through the SmaRTClock Interface.

Table 11.1. SmaRTClock Internal Registers

SmaRTClock Address	SmaRTClock Register	Register Name	Description
0x00–0x03	CAPTUREn	SmaRTClock Capture Registers	Four Registers used for setting the 32-bit SmaRTClock timer or reading its current value.
0x04	RTC0CN	SmaRTClock Control Register	Controls the operation of the SmaRTClock State Machine.
0x05	RTC0XCN	SmaRTClock Oscillator Control Register	Controls the operation of the SmaRTClock Oscillator.
0x06	RTC0XCF	SmaRTClock Oscillator Configuration Register	Controls the value of the progammable oscillator load capacitance and enables/ disables AutoStep.
0x08–0x0B	ALARMn	SmaRTClock Alarm Registers	Four registers used for setting or reading the 32-bit SmaRTClock alarm value.

11.1.1. SmaRTClock Lock and Key Functions

The SmaRTClock Interface is protected with a lock and key function. The SmaRTClock Lock and Key Register (RTCKEY) must be written with the correct key codes, in sequence, before writes and reads to RTCADR and RTCDAT may be performed. The key codes are: 0xA5, 0xF1. There are no timing restrictions, but the key codes must be written in order. If the key codes are written out of order, the wrong codes are written, or an indirect register read or write is attempted while the interface is locked, the SmaRTClock interface will be disabled, and the RTCADR and RTCDAT registers will become inaccessible until the next system reset. Once the SmaRTClock interface is unlocked, software may perform any number of accesses to the SmaRTClock registers until the interface is re-locked or the device is reset. Any write to RTCKEY while the SmaRTClock interface is unlocked will re-lock the interface.

Reading the RTCKEY register at any time will provide the SmaRTClock Interface status and will not interfere with the sequence that is being written. The RTCKEY register description in SFR Definition 11.1 lists the definition of each status code.

Not Recommended for New Designs

11.1.2. Using RTCADR and RTCDAT to Access SmaRTClock Internal Registers

The SmaRTClock internal registers can be read and written using RTCADR and RTCDAT. The RTCADR register selects the SmaRTClock internal register that will be targeted by subsequent reads or writes.

A SmaRTClock Write operation is initiated by writing to the RTCDAT register. Below is an example of writing to a SmaRTClock internal register.

1. Write 0x05 to RTCADR. This selects the internal RTC0CN register at SmaRTClock Address 0x05.
2. Write 0x00 to RTCDAT. This operation writes 0x00 to the internal RTC0CN register.

A SmaRTClock Read operation is initiated by setting the SmaRTClock Interface Busy bit. This transfers the contents of the internal register selected by RTCADR to RTCDAT. The transferred data will remain in RTCDAT until the next read or write operation. Below is an example of reading a SmaRTClock internal register.

1. Write 0x05 to RTCADR. This selects the internal RTC0CN register at SmaRTClock Address 0x05.
2. Write 1 to BUSY. This initiates the transfer of data from RTC0CN to RTCDAT. Note: Step 1 and Step 2 may be combined into a single write.
3. Read data from RTCDAT. This data is a copy of the RTC0CN register.

11.1.3. SmaRTClock Interface Autoread Feature

When Autoread is enabled, each read from RTCDAT initiates the next indirect read operation on the SmaRTClock internal register selected by RTCADR. Software should set the BUSY bit once at the beginning of each series of consecutive reads. Software must check if the SmaRTClock Interface is busy prior to reading RTCDAT. Autoread is enabled by setting AUTORD (RTCADR.6) to logic 1.

11.1.4. RTCADR Autoincrement Feature

For ease of reading and writing the 32-bit CAPTURE and ALARM values, RTCADR automatically increments after each read or write to a CAPTUREn or ALARMn register. This speeds up the process of setting an alarm or reading the current SmaRTClock timer value by allowing all 4 CAPTURE or ALARM registers to be read or written in a single block write. Autoincrement is always enabled.

Notes: Autoincrement should only be used with block reads/writes. When using single-byte reads/writes, RTCADR must be written before each data read or write.

When using SMBus to perform a block read/write, the RTCADR register must be written using the REGSET command.

Not Recommended for New Designs

SFR Definition 11.1. RTCKEY: SmaRTClock Lock and Key

Bit	7	6	5	4	3	2	1	0
Name	RTC0ST[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

Address = 0x0A

Bit	Name	Function
7:0	RTC0ST	**SmaRTClock Interface Lock/Key and Status.** Locks/unlocks the SmaRTClock interface when written. Provides lock status when read. **Read:** **0x00:** SmaRTClock Interface is locked. **0x01:** SmaRTClock Interface is locked. First key code (0xA5) has been written, waiting for second key code. **0x02:** SmaRTClock Interface is unlocked. First and second key codes (0xA5, 0xF1) have been written. **0x03:** SmaRTClock Interface is disabled until the next system reset. **Write:** When RTC0ST = 0x00 (locked), writing 0xA5 followed by 0xF1 unlocks the SmaRT-Clock Interface. When RTC0ST = 0x01 (waiting for second key code), writing any value other than the second key code (0xF1) will change RTC0STATE to 0x03 and disable the SmaRTClock Interface until the next system reset. When RTC0ST = 0x02 (unlocked), any write to RTCKEY will lock the SmaRTClock Interface. When RTC0ST = 0x03 (disabled), writes to RTCKEY have no effect.

Not Recommended for New Designs

SFR Definition 11.2. RTCADR: SmaRTClock Address

Bit	7	6	5	4	3	2	1	0
Name	BUSY	AUTORD		SHORT	ADDR[3:0]			
Type	R/W	R/W	R	R/W	R/W			
Reset	0	0	0	0	varies	varies	varies	varies

Address = 0x0B

Bit	Name	Function
7	BUSY	**SmaRTClock Interface Busy Indicator.** Indicates SmaRTClock interface status. Writing 1 to this bit initiates an indirect read.
6	AUTORD	**SmaRTClock Interface Autoread Enable.** Enables/disables Autoread. 0: Autoread Disabled. 1: Autoread Enabled.
5	Unused	Read = 0b; Write = Don't Care.
4	SHORT	**Short Strobe Enable.** Enables/disables the Short Strobe Feature. It is recommended to always enable the short strobe feature to minimize the read/write time. 0: Short Strobe disabled. 1: Short Strobe enabled.
3:0	ADDR[3:0]	**SmaRTClock Indirect Register Address.** Sets the currently selected SmaRTClock register. See Table 11.1 for a listing of all SmaRTClock indirect registers.

Note: The ADDR bits increment after each indirect read/write operation that targets a CAPTUREn or ALARMn internal SmaRTClock register. Autoincrement should only be used with block reads/writes.

SFR Definition 11.3. RTCDAT: SmaRTClock Data

Bit	7	6	5	4	3	2	1	0
Name	RTCDAT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

Address = 0x0C

Bit	Name	Function
7:0	RTCDAT	**SmaRTClock Data Bits.** Holds data transferred to/from the internal SmaRTClock register selected by RTCADR.

Not Recommended for New Designs

11.2. SmaRTClock Clocking Sources

The SmaRTClock peripheral is clocked from its own timebase, independent of the system clock. The SmaRTClock timebase is derived from the SmaRTClock oscillator circuit, which has two modes of operation: crystal mode, and self-oscillate mode. The oscillation frequency is 32.768 kHz in crystal mode and can be programmed in the range of sub 20 kHz to above 40 kHz in self-oscillate mode. In crystal mode, XTAL1 and XTAL2 may be overdriven by an external CMOS clock.

11.2.1. Using the SmaRTClock Oscillator with a Crystal or External CMOS Clock

When using crystal mode, a 32.768 kHz crystal should be connected between XTAL3 and XTAL4. No other external components are required. The following steps show how to start the SmaRTClock crystal oscillator in software:

1. Set SmaRTClock to Crystal Mode (XMODE = 1).
2. *Optional.* Enable/Disable Automatic Gain Control (AGCEN) and Bias Doubling (BIASX2). See Section 11.2.4 for recommendations on using these oscillator features.
3. Set the desired loading capacitance (RTC0XCF).
4. Enable power to the SmaRTClock oscillator circuit (RTC0EN = 1).
5. Wait 2 ms.
6. Poll the SmaRTClock Clock Valid Bit (CLKVLD) until the crystal oscillator stabilizes.
7. Poll the SmaRTClock Load Capacitance Ready Bit (LOADRDY) until the load capacitance reaches its programmed value.
8. Enable the SmaRTClock missing clock detector.
9. Wait 2 ms.
10. Clear the PMU0CF wake-up source flags.

In crystal mode, the SmaRTClock oscillator may be driven by an external CMOS clock. The CMOS clock should be applied to both XTAL1 and XTAL2. The input low voltage (VIL) and input high voltage (VIH) for these pins when used with an external CMOS clock are 0.1 and 0.8 V, respectively. The SmaRTClock oscillator should be configured to its lowest bias setting with AGC disabled. The CLKVLD bit is indeterminate when using a CMOS clock, however, the OSCFAIL bit may be checked 2 ms after SmaRTClock oscillator is powered on to ensure that there is a valid clock.

11.2.2. Using the SmaRTClock Oscillator in Self-Oscillate Mode

The following steps show how to configure SmaRTClock for use in self-oscillate mode:

1. Set SmaRTClock to Self-Oscillate Mode (XMODE = 0).
2. Set the desired oscillation frequency:
   For oscillation at about 20 kHz, set BIASX2 = 0.
   For oscillation at about 40 kHz, set BIASX2 = 1.
3. The oscillator starts oscillating instantaneously.
4. Fine tune the oscillation frequency by adjusting the load capacitance (RTC0XCF).

Not Recommended for New Designs

11.2.3. Programmable Load Capacitance

The programmable load capacitance has 16 values to support crystal oscillators with a wide range of recommended load capacitance. If Automatic Load Capacitance Stepping is enabled, the crystal load capacitors start at the smallest setting to allow a fast startup time, then slowly increase the capacitance until the final programmed value is reached. The final programmed loading capacitor value is specified using the LOADCAP bits in the RTC0XCF register. The LOADCAP setting specifies the amount of on-chip load capacitance and does not include any stray PCB capacitance. Once the final programmed loading capacitor value is reached, the LOADRDY flag will be set by hardware to logic 1.

When using the SmaRTClock oscillator in self-oscillate mode, the programmable load capacitance can be used to fine tune the oscillation frequency. In most cases, increasing the load capacitor value will result in a decrease in oscillation frequency.

.Table 11.2 shows the crystal load capacitance for various settings of LOADCAP.

Table 11.2. SmaRTClock Load Capacitance Settings

LOADCAP	Crystal Load Capacitance	Equivalent Capacitance seen on XTAL1 and XTAL2
0000	4.0 pF	8.0 pF
0001	4.5 pF	9.0 pF
0010	5.0 pF	10.0 pF
0011	5.5 pF	11.0 pF
0100	6.0 pF	12.0 pF
0101	6.5 pF	13.0 pF
0110	7.0 pF	14.0 pF
0111	7.5 pF	15.0 pF
1000	8.0 pF	16.0 pF
1001	8.5 pF	17.0 pF
1010	9.0 pF	18.0 pF
1011	9.5 pF	19.0 pF
1100	10.5 pF	21.0 pF
1101	11.5 pF	23.0 pF
1110	12.5 pF	25.0 pF
1111	13.5 pF	27.0 pF

Not Recommended for New Designs

11.2.4. Automatic Gain Control and SmaRTClock Bias Doubling

Automatic Gain Control allows the SmaRTClock oscillator to trim the oscillation amplitude of a crystal in order to achieve the lowest possible power consumption. Automatic Gain Control automatically detects when the oscillation amplitude has reached a point where it safe to reduce the drive current, therefore, it may be enabled during crystal startup. It is recommended to enable Automatic Gain Control in any system which uses the SmaRTClock oscillator in crystal mode.

Turning off Automatic Gain Control will allow the crystal drive strength after oscillation is started to remain at the same level used for starting the crystal. This will result in increased power consumption, however the crystal will have higher immunity against external factors.

Note: Automatic Gain Control may be turned on in self-oscillate mode to reduce the oscillation frequency and the supply current.

The SmaRTClock Bias Doubling feature allows the self-oscillation frequency to be increased (almost doubled) and allows a higher crystal drive strength in crystal mode. High crystal drive strength is recommended when using a crystal with a high ESR and high loading capacitance. Table 11.3 shows a summary of the oscillator operating modes and allowed operating conditions. SmaRTClock Bias Doubling is enabled by setting BIASX2 (RTC0XCN.5) to 1.

Table 11.3. SmaRTClock Bias Settings and Allowed Operating Conditions

Mode	Setting	Power Consumption	Allowed Operating Condition
Crystal	Bias Double Off, AGC On	Lowest	ESR < 40 kΩ, any load ESR < 50 kΩ, Cload < 10 pF ESR < 80 kΩ, Cload < 8 pF
	Bias Double Off, AGC Off	Low	ESR < 80 kΩ, Cload < 10 pF
	Bias Double On, AGC On	High	ESR < 50 kΩ, any load ESR < 80 kΩ, Cload < 10 pF
	Bias Double On, AGC Off	Highest	This mode is only recommended for debugging purposes due to its increased power consumption.
Self-Oscillate	Bias Double Off	Low	20 kHz
	Bias Double On	High	40 kHz

Not Recommended for New Designs

11.2.5. Missing SmaRTClock Detector

The missing SmaRTClock detector is a one-shot circuit enabled by setting MCLKEN (RTC0CN.6) to 1. When the SmaRTClock Missing Clock Detector is enabled, OSCFAIL (RTC0CN.5) is set by hardware if SmaRTClock oscillator remains high or low for more than 100 µs.

A SmaRTClock Missing Clock detector timeout can trigger an interrupt and wake the device from a low power mode. See Section "7. Interrupt Sources" on page 40 and Section "9. Power Modes" on page 49, and for more information.

Note: The SmaRTClock Missing Clock Detector should be disabled when making changes to the oscillator settings in RTC0XCN.

11.2.6. SmaRTClock Oscillator Crystal Valid Detector

The SmaRTClock oscillator crystal valid detector is an oscillation amplitude detector circuit used during crystal startup to determine when oscillation has started and is nearly stable. The output of this detector can be read from the CLKVLD bit (RTX0XCN.4).

Notes: The CLKVLD bit has a blanking interval of 2 ms. During the first 2 ms after turning on the crystal oscillator, the output of CLKVLD is not valid.

This SmaRTClock crystal valid detector (CLKVLD) is not intended for detecting an oscillator failure. The missing SmaRTClock detector (CLKFAIL) should be used for this purpose.

11.3. SmaRTClock Timer and Alarm Function

The SmaRTClock timer is a 32-bit counter that, when running (RTC0TR = 1), is incremented every SmaRTClock oscillator cycle. The timer has an alarm function that can be set to generate an interrupt and wake the device from a low power mode. See Section "7. Interrupt Sources" on page 40 and Section "9. Power Modes" on page 49 more information.

The SmaRTClock timer includes an Auto Reset feature, which automatically resets the timer to zero one SmaRTClock cycle after an alarm occurs. When using Auto Reset, the Alarm match value should always be set to 1 count less than the desired match value. Auto Reset can be enabled by writing a 1 to ALRM (RTC0CN.2).

11.3.1. Setting and Reading the SmaRTClock Timer Value

The 32-bit SmaRTClock timer can be set or read using the six CAPTUREn internal registers. Note that the timer does not need to be stopped before reading or setting its value. The following steps can be used to set the timer value:

1. Write the desired 32-bit set value to the CAPTUREn registers.
2. Write 1 to RTC0SET. This will transfer the contents of the CAPTUREn registers to the SmaRTClock timer.
3. Operation is complete when RTC0SET is cleared to 0 by hardware.

The following steps can be used to read the current timer value:

1. Write 1 to RTC0CAP. This will transfer the contents of the timer to the CAPTUREn registers.
2. Poll RTC0CAP until it is cleared to 0 by hardware.
3. A snapshot of the timer value can be read from the CAPTUREn registers

11.3.2. Setting a SmaRTClock Alarm

The SmaRTClock alarm function compares the 32-bit value of SmaRTClock Timer to the value of the ALARMn registers. An alarm event is triggered if the SmaRTClock timer is **equal to** the ALARMn registers. If Auto Reset is enabled, the 32-bit timer will be cleared to zero one SmaRTClock cycle after the alarm event.

The SmaRTClock alarm event can be configured to generate a wake-up from a low power mode, or generate an interrupt. See Section "7. Interrupt Sources" on page 40, Section "9. Power Modes" on page 49, and for more information.

The following steps can be used to set up a SmaRTClock Alarm:

Not Recommended for New Designs

1. Disable SmaRTClock Alarm Events (RTC0AEN = 0).
2. Set the ALARMn registers to the desired value.
3. Enable SmaRTClock Alarm Events (RTC0AEN = 1).

Notes: The ALRM bit, which is used as the SmaRTClock Alarm Event flag, is cleared by disabling SmaRTClock Alarm Events (RTC0AEN = 0).

Disabling (RTC0AEN = 0) then re-enabling Alarm Events (RTC0AEN = 1) after a SmaRTClock Alarm without modifying ALARMn registers will automatically schedule the next alarm after 2^32 SmaRTClock cycles (approximately 36 hours using a 32.768 kHz crystal).

The SmaRTClock Alarm Event flag will remain asserted for a maximum of one SmaRTClock cycle. The Alarm Event however will be captured by the interrupt logic and will post a non-transient interrupt.

11.3.3. Software Considerations for using the SmaRTClock Timer and Alarm

The SmaRTClock timer and alarm have two operating modes to suit varying applications. The two modes are described below:

Mode 1:
The first mode uses the SmaRTClock timer as a perpetual timebase which is never reset to zero. Every 36 hours, the timer is allowed to overflow without being stopped or disrupted. The alarm interval is software managed and is added to the ALRMn registers by software after each alarm. This allows the alarm match value to always stay ahead of the timer by one software managed interval. If software uses 32-bit unsigned addition to increment the alarm match value, then it does not need to handle overflows since both the timer and the alarm match value will overflow in the same manner.

This mode is ideal for applications which have a long alarm interval (e.g., 24 or 36 hours) and/or have a need for a perpetual timebase. An example of an application that needs a perpetual timebase is one whose wake-up interval is constantly changing. For these applications, software can keep track of the number of timer overflows in a 16-bit variable, extending the 32-bit (36 hour) timer to a 48-bit (272 year) perpetual timebase.

Mode 2:
The second mode uses the SmaRTClock timer as a general purpose up counter which is auto reset to zero by hardware after each alarm. The alarm interval is managed by hardware and stored in the ALRMn registers. Software only needs to set the alarm interval once during device initialization. After each alarm, software should keep a count of the number of alarms that have occurred in order to keep track of time.

This mode is ideal for applications that require minimal software intervention and/or have a fixed alarm interval. This mode is the most power efficient since it requires less CPU time per alarm.

Not Recommended for New Designs

Internal Register Definition 11.4. RTC0CN: SmaRTClock Control

Bit	7	6	5	4	3	2	1	0
Name	RTC0EN	MCLKEN	OSCFAIL	RTC0TR	RTC0AEN	ALRM	RTC0SET	RTC0CAP
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	Varies	0	0	0	0	0

SmaRTClock Address = 0x04

Bit	Name	Function		
7	RTC0EN	**SmaRTClock Enable.** Enables/disables the SmaRTClock oscillator and associated bias currents. 0: SmaRTClock oscillator disabled. 1: SmaRTClock oscillator enabled.		
6	MCLKEN	**Missing SmaRTClock Detector Enable.** Enables/disables the missing SmaRTClock detector. 0: Missing SmaRTClock detector disabled. 1: Missing SmaRTClock detector enabled.		
5	OSCFAIL	**SmaRTClock Oscillator Fail Event Flag.** Set by hardware when a missing SmaRTClock detector timeout occurs. Must be cleared by software. The value of this bit is not defined when the SmaRTClock oscillator is disabled.		
4	RTC0TR	**SmaRTClock Timer Run Control.** Controls if the SmaRTClock timer is running or stopped (holds current value). 0: SmaRTClock timer is stopped. 1: SmaRTClock timer is running.		
3	RTC0AEN	**SmaRTClock Alarm Enable.** Enables/disables the SmaRTClock alarm function. Also clears the ALRM flag. 0: SmaRTClock alarm disabled. 1: SmaRTClock alarm enabled.		
2	ALRM	**SmaRTClock Alarm Event Flag and Auto Reset Enable** Reads return the state of the alarm event flag. Writes enable/disable the Auto Reset function.	Read: 0: SmaRTClock alarm event flag is de-asserted. 1: SmaRTClock alarm event flag is asserted.	Write: 0: Disable Auto Reset. 1: Enable Auto Reset.
1	RTC0SET	**SmaRTClock Timer Set.** Writing 1 initiates a SmaRTClock timer set operation. This bit is cleared to 0 by hardware to indicate that the timer set operation is complete.		
0	RTC0CAP	**SmaRTClock Timer Capture.** Writing 1 initiates a SmaRTClock timer capture operation. This bit is cleared to 0 by hardware to indicate that the timer capture operation is complete.		

Note: The ALRM flag will remain asserted for a maximum of one SmaRTClock cycle.

Not Recommended for New Designs

Internal Register Definition 11.5. RTC0XCN: SmaRTClock Oscillator Control

Bit	7	6	5	4	3	2	1	0
Name	AGCEN	XMODE	BIASX2	CLKVLD				
Type	R/W	R/W	R/W	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

SmaRTClock Address = 0x05

Bit	Name	Function
7	AGCEN	**SmaRTClock Oscillator Automatic Gain Control (AGC) Enable.** 0: AGC disabled. 1: AGC enabled.
6	XMODE	**SmaRTClock Oscillator Mode.** Selects Crystal or Self Oscillate Mode. 0: Self-Oscillate Mode selected. 1: Crystal Mode selected.
5	BIASX2	**SmaRTClock Oscillator Bias Double Enable.** Enables/disables the Bias Double feature. 0: Bias Double disabled. 1: Bias Double enabled.
4	CLKVLD	**SmaRTClock Oscillator Crystal Valid Indicator.** Indicates if oscillation amplitude is sufficient for maintaining oscillation. 0: Oscillation has not started or oscillation amplitude is too low to maintain oscillation. 1: Sufficient oscillation amplitude detected.
3:0	Unused	Read = 0000b; Write = Don't Care.

Not Recommended for New Designs

Internal Register Definition 11.6. RTC0XCF: SmaRTClock Oscillator Configuration

Bit	7	6	5	4	3	2	1	0
Name	AUTOSTP	LOADRDY			LOADCAP			
Type	R/W	R	R	R	R/W			
Reset	0	0	0	0	0	0	0	0

SmaRTClock Address = 0x06

Bit	Name	Function
7	AUTOSTP	**Automatic Load Capacitance Stepping Enable.** Enables/disables automatic load capacitance stepping. 0: Load capacitance stepping disabled. 1: Load capacitance stepping enabled.
6	LOADRDY	**Load Capacitance Ready Indicator.** Set by hardware when the load capacitance matches the programmed value. 0: Load capacitance is currently stepping. 1: Load capacitance has reached it programmed value.
5:4	Unused	Read = 00b; Write = Don't Care.
3:0	LOADCAP	**Load Capacitance Programmed Value.** Holds the user's desired value of the load capacitance. See Table 11.2 on page 75.

Not Recommended for New Designs

Internal Register Definition 11.7. CAPTUREn: SmaRTClock Timer Capture

Bit	7	6	5	4	3	2	1	0
Name	CAPTURE[31:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SmaRTClock AddressCAPTURE0 = 0x00; CAPTURE1 = 0x01; CAPTURE2 =0x02; CAPTURE3: 0x03.

Bit	Name	Function
7:0	CAPTURE[31:0]	**SmaRTClock Timer Capture.** These 4 registers (CAPTURE3–CAPTURE0) are used to read or set the 32-bit SmaRTClock timer. Data is transferred to or from the SmaRTClock timer when the RTC0SET or RTC0CAP bits are set.
Note: The least significant bit of the timer capture value is in CAPTURE0.0.		

Internal Register Definition 11.8. ALARMn: SmaRTClock Alarm Programmed Value

Bit	7	6	5	4	3	2	1	0
Name	ALARM[31:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SmaRTClock AddressALARM0 = 0x08; ALARM1 = 0x09; ALARM2 = 0x0A; ALARM3 = 0x0B

Bit	Name	Function
7:0	ALARM[31:0]	**SmaRTClock Alarm Programmed Value.** These 4 registers (ALARM3–ALARM0) are used to set an alarm event for the SmaRTClock timer. The SmaRTClock alarm should be disabled (RTC0AEN=0) when updating these registers.
Note: The least significant bit of the alarm programmed value is in ALARM0.0.		

Not Recommended for New Designs

12. LCD Segment Driver

CP2400/1/2/3 devices contain an LCD segment driver and on-chip bias generation that supports static, 2-mux, 3-mux and 4-mux LCDs with 1/2 or 1/3 bias. The on-chip charge pump with programmable output voltage allows software contrast control which is independent of the VDD supply voltage. LCD timing is derived from the SmaRTClock oscillator to allow precise control over the refresh rate. A low frequency clock present on the CLK pin may also be used as the LCD clock source.

The CP2400/1/2/3 contains on-chip ULP memory to store the enabled/disabled state of individual LCD segments. All LCD waveforms are generated on-chip and software only needs to access the ULP memory to change the information displayed on the LCD. An LCD blinking function is also supported. A block diagram of the LCD segment driver is shown in Figure 12.1.

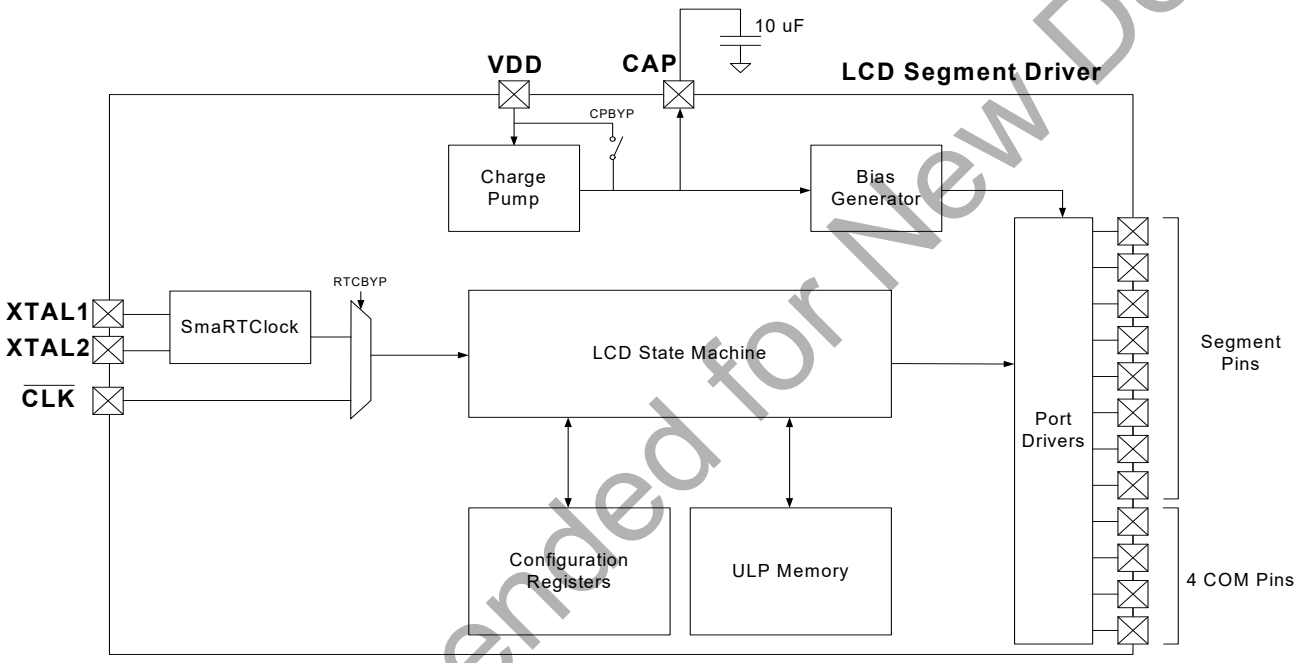


Figure 12.1. LCD Segment Driver Block Diagram

12.1. Initializing the LCD Segment Driver

The following procedure is recommended for using the LCD Segment Driver:

1. Configure the LCD size, mux mode, and bias using the LCD0CN register.
2. Configure the Port I/O pins to be used for LCD as Analog I/O.
3. Set the LCD contrast using the CONTRAST register.
4. Write the reserved value of 0x9F to LCD0CF.
5. Set the LCD refresh rate using the LCD0DIVH:LCD0DIVL registers.
6. Set the LCD toggle rate using the LCD0TOGR register.
7. Set the LCD power mode using the LCD0PWR register.
8. Write a pattern to the ULP memory.
9. Enable the LCD using the master control (MSCN) register.

Not Recommended for New Designs

12.2. LCD Configuration

The LCD segment driver supports multiple mux options: static, 2-mux, 3-mux, and 4-mux mode. It also supports 1/2 and 1/3 bias options. The desired mux mode and bias is configured through the LCD0CN register.

SFR Definition 12.1. LCD0CN: LCD0 Control Register

Bit	7	6	5	4	3	2	1	0
Name				BLANK	SIZE	MUXMD		BIAS
Type	R/W	R/W	R/W	R/W	R/W	R/W		R/W
Reset	0	0	0	0	0	0	0	0

Address = 0x95

Bit	Name	Function
7:5	Unused	Read = 000. Write = Don't Care.
4	BLANK	**Blank All Segments.** Blanks all LCD segments using a single bit. 0: All LCD segments are controlled by the LCD memory. 1: All LCD segments are blank (turned off).
3	SIZE	**LCD Size Select.** Selects whether 16 or 32 segment pins will be used for the LCD function. 0: P0 and P1 are used as LCD segment pins. 1: P0, P1, P2, and P3 are used as LCD segment pins.
2:1	MUXMD[1:0]	**LCD Bias Power Mode.** Selects the mux mode. 00: Static mode selected. 01: 2-mux mode selected. 10: 3-mux mode selected. 11: 4-mux mode selected.
0	BIAS	**Bias Select.** Selects between 1/2 Bias and 1/3 Bias. 0: LCD0 is configured for 1/3 Bias. 1: LCD0 is configured for 1/2 Bias.

Not Recommended for New Designs

12.3. LCD Bias Generation and Contrast Adjustment

The LCD Bias voltages are generated using the on-chip charge pump with programmable output voltage. The programmable output voltage allows software contrast control in 60 mV steps from 2.6 to 3.44 V. The LCD contrast is controlled by the CONTRAST register.

Note: An external 4.7 µF decoupling capacitor is required (10 µF recommended) on the CAP pin to create a charge reservoir at the output of the charge pump.

Intermediate voltages used for 1/2 and 3/4 bias configurations are generated on-chip using a novel approach that allows driving extra large LCD segments while maintaining ultra low power consumption. This eliminates the need for off-chip biasing when driving a large LCD. The LCD drive capability can be set using the LCD0PWR register. The highest power setting should be used for extra large LCDs (which require charging the largest capacitance) and the lowest power setting should be used with small LCDs (smaller than 1 inch).

SFR Definition 12.2. CONTRAST: Contrast Adjustment

Bit	7	6	5	4	3	2	1	0
Name					CNTRST			
Type	R/W	R/W	R/W	R/W	R/W			
Reset	0	0	0	0	0	0	0	0

Address = 0x96

Bit	Name	Function
7:4	Unused	Read = 0000. Write = Don't Care.
3:0	CNTRST	**Contrast Adjustment.** Selects the on-chip charge pump output voltage. 0000: 2.60 V 0001: 2.60 V 0010: 2.66 V 0011: 2.72 V 0100: 2.78 V 0101: 2.84 V 0110: 2.90 V 0111: 2.96 V 1000: 3.02 V 1001: 3.08 V 1010: 3.14 V 1011: 3.20 V 1100: 3.26 V 1101: 3.32 V 1110: 3.38 V 1111: 3.44 V

Not Recommended for New Designs

SFR Definition 12.3. LCD0CF: LCD Configuration

Bit	7	6	5	4	3	2	1	0
Name	Reserved		CPCYC[5:0]					
Type	R/W		R/W					
Reset	1	0	0	1	1	1	1	1

Address = 0x97

Bit	Name	Function
7:4	Reserved	Read = 10b. Must Write 10b.
5:0	CPCYC[5:0]	**Charge Pump Cycle Period.** The number of SmaRTClock oscillator periods between charge pump cycles is CPCYC[5:0]+1. The time between charge pump cycles should not exceed 2 ms.

Not Recommended for New Designs

12.4. LCD Timing Generation

All LCD timing is derived from the SmaRTClock oscillator divided by 2. The LCD0DIVH:LCD0DIVL registers store the prescaler for generating the LCD refresh rate. The LCD mux mode must be taken into account when determining the prescaler value. See the LCD0DIVH/LCD0DIVL register descriptions for more details. For maximum power savings, choose a slow LCD refresh rate. For the least flicker, choose a fast LCD refresh rate.

SFR Definition 12.4. LCD0DIVH: LCD Refresh Rate Prescaler High Byte

Bit	7	6	5	4	3	2	1	0
Name							LCD0DIV[9:8]	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

Address = 0x98

Bit	Name	Function
7:2	Unused	Read = 000000. Write = Don't Care.
1:0	LCD0DIV[9:8]	**LCD Refresh Rate Prescaler**. Sets the LCD refresh rate according to the following equation: $\text{LCD Refresh Rate} = \frac{\text{SmaRTClock Oscillator Frequency}}{4 \times \text{mux_mode} \times (\text{LCD0DIV} + 1)}$

SFR Definition 12.5. LCD0DIVL: LCD Refresh Rate Prescaler Low Byte

Bit	7	6	5	4	3	2	1	0
Name	LCD0DIV[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

Address = 0x99

Bit	Name	Function
7:0	LCD0DIV[7:0]	**LCD Refresh Rate Prescaler**. Sets the LCD refresh rate according to the following equation: $\text{LCD Refresh Rate} = \frac{\text{SmaRTClock Oscillator Frequency}}{4 \times \text{mux_mode} \times (\text{LCD0DIV} + 1)}$

Not Recommended for New Designs

SFR Definition 12.6. LCD0TOGR: LCD Toggle Rate

Bit	7	6	5	4	3	2	1	0
Name					TOGR[3:0]			
Type	R/W	R/W	R/W	R/W	R/W			
Reset	0	0	0	0	0	0	0	0

Address = 0x9A

Bit	Name	Function
7:4	Unused	Read = 0000. Write = Don't Care.
3:0	TOGR[3:0]	**LCD Toggle Rate Divider**. Sets the LCD Toggle Rate according to the following equation: $\text{LCD Toggle Rate} = \frac{\text{Refresh Rate} \times \text{mux_mode} \times 2}{\text{Toggle Rate Divider}}$ 0000: Reserved. 0001: Reserved. 0010: Toggle Rate Divider is set to divide by 2. 0011: Toggle Rate Divider is set to divide by 4. 0100: Toggle Rate Divider is set to divide by 8. 0101: Toggle Rate Divider is set to divide by 16. 0110: Toggle Rate Divider is set to divide by 32. 0111: Toggle Rate Divider is set to divide by 64. 1000: Toggle Rate Divider is set to divide by 128. 1001: Toggle Rate Divider is set to divide by 256. 1010: Toggle Rate Divider is set to divide by 512. 1011: Toggle Rate Divider is set to divide by 1024. 1100: Toggle Rate Divider is set to divide by 2048. 1101: Toggle Rate Divider is set to divide by 4096. All other values reserved.

Not Recommended for New Designs

SFR Definition 12.7. LCD0PWR: LCD0 Power Register

Bit	7	6	5	4	3	2	1	0
Name				CPCLK[1:0]				
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Address = 0x9B

Bit	Name	Function
7:5	Reserved	Read = 000b. Must Write 000b.
4:3	CPCLK[1:0]	**Charge Pump Clock Select.** 00: 1 MHz charge pump clock (normal operation). 01: 2 MHz charge pump clock. 10: 0.5 MHz charge pump clock. 11: 0.67 MHz charge pump clock.
2:0	Reserved	Read = 000b. Must Write 000b.

Not Recommended for New Designs

12.5. Mapping ULP Memory to LCD Pins

The ULP memory is organized in 16 bytes (32 half-bytes or nibbles), each nibble controlling 1 LCD output pin. Each LCD output pin can control 1 to 4 LCD segments depending on the selected mux mode. The least significant bit of each nibble controls the segment connected to the backplane signal COM0 and the most significant bit of each nibble controls the segment connected to the backplane signal COM3. In static mode, only COM0 is used and the three remaining bits in each nibble are ignored. In 4-mux mode, each bit controls an LCD segment. Bits with a value of 1 turn on the associated segment and bits with a value of 0 turn off the associated segment.

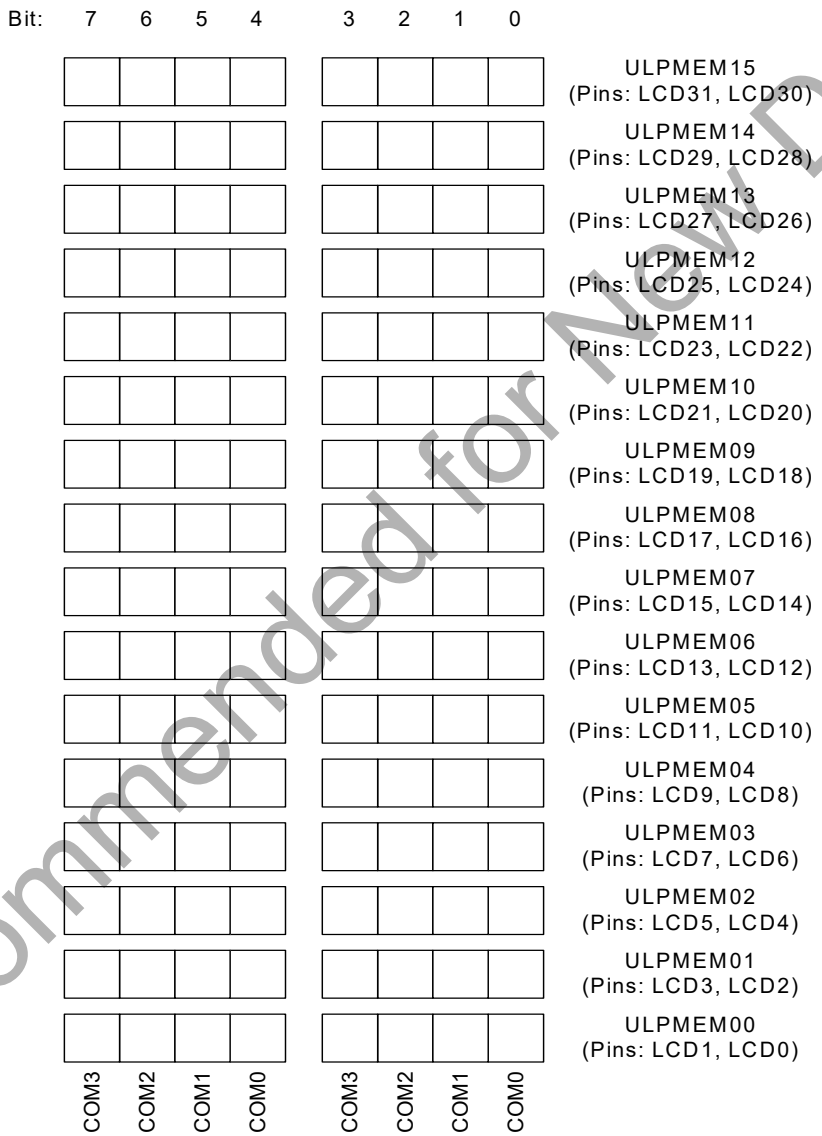


Figure 12.2. ULP Memory Map

Not Recommended for New Designs

12.6. Blinking LCD Segments

The LCD driver supports blinking LCD applications such as clock applications where the “colon” separator toggles on and off once per second. If the LCD is only displaying the hours and minutes, then the device only needs to wake up once per minute to update the display. The once per second blinking is automatically handled by the CP2400/1/2/3.

The LCD0BLINK register can be used to enable blinking on any LCD segment connected to the LCD0 or LCD1 segment pin. In static mode, a maximum of 2 segments can blink. In 4-mux mode, a maximum of 8 segments can blink. The LCD0BLINK mask register targets the same LCD segments as the ULPMEM00 register. If an LCD0BLINK bit corresponding to an LCD segment is set to 1, then that segment will toggle at the frequency set by the LCD0TOGR register without any software intervention.

SFR Definition 12.8. LCD0BLINK: LCD0 Blink Mask

Bit	7	6	5	4	3	2	1	0
Name	LCD0BLINK[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Address = 0x80

Bit	Name	Function
7:0	LCD0BLINK[7:0]	**LCD0 Blink Mask.** Each bit maps to a specific LCD segment connected to the LCD0 and LCD1 segment pins. A value of 1 indicates that the segment is blinking. A value of 0 indicates that the segment is not blinking. This bit to segment mapping is the same as the ULPMEM00 register.

Not Recommended for New Designs

13. Timers

CP2400/1/2/3 devices include two 16-bit auto-reload timers. These timers can be used to measure time intervals and generate periodic interrupt requests. Both timers can be clocked from the system clock source divided by 12. Timer 1 has an additional SmaRTClock divided by 8 input and capture mode that can be used to measure the SmaRTClock oscillation frequency with respect to the system clock. When SMBus SCL low timeout is enabled, Timer 0 becomes unavailable for general purpose use. Timer 0 is enabled on reset.

13.1. Timer 0

Timer 0 is a 16-bit timer formed by two 8-bit SFRs: TMR0L (low byte) and TMR0H (high byte). Timer 0 operates in 16-bit auto-reload mode and is clocked by the system clock divided by 12. As the 16-bit timer register increments and overflows from 0xFFFF to 0x0000, the 16-bit value in the Timer 0 reload registers (TMR0RLH and TMR0RLL) is loaded into the Timer 0 register as shown in Figure 13.1, and the Timer 0 Overflow Flag (INT1.2) is set. If Timer 0 interrupts are enabled (if INT1EN.2 is set), an interrupt will be generated on each Timer 0 overflow. Additionally, if Timer 0 interrupts are enabled and the TF0LEN bit is set (TMR0CN.5), an interrupt will be generated each time the lower 8 bits (TMR0L) overflow from 0xFF to 0x00.

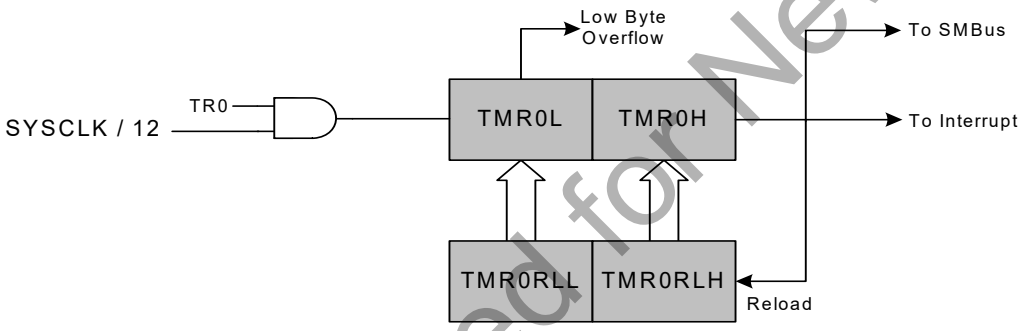


Figure 13.1. Timer 0 Block Diagram

Not Recommended for New Designs

SFR Definition 13.1. TMR0CN: Timer 0 Control

Bit	7	6	5	4	3	2	1	0
Name			TF0LEN			TR0		
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	1	0	0

SFR Address = 0x54

Bit	Name	Function
7:6	Unused	Read = 00b. Write = Don't Care.
5	TF0LEN	**Timer 0 Low Byte Interrupt Enable.** When set to 1, this bit enables Timer 0 Low Byte interrupts. If Timer 0 interrupts are enabled, an interrupt will be generated when the low byte of Timer 0 overflows.
4:3	Unused	Read = 00b. Write = Don't Care.
2	TR0	**Timer 0 Run Control.** Timer 0 is enabled by setting this bit to 1.
1:0	Unused	Read = 00b. Write = Don't Care.

Not Recommended for New Designs

SFR Definition 13.2. TMR0RLL: Timer 0 Reload Register Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR0RLL[7:0]							
Type	R/W							
Reset	1	0	0	0	1	1	0	1

SFR Address = 0x50

Bit	Name	Function
7:0	TMR0RLL[7:0]	**Timer 0 Reload Register Low Byte.** TMR0RLL holds the low byte of the reload value for Timer 0.

SFR Definition 13.3. TMR0RLH: Timer 0 Reload Register High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR0RLH[7:0]							
Type	R/W							
Reset	0	0	1	1	0	1	0	0

SFR Address = 0x51

Bit	Name	Function
7:0	TMR0RLH[7:0]	**Timer 0 Reload Register High Byte.** TMR0RLH holds the high byte of the reload value for Timer 0.

Not Recommended for New Designs

SFR Definition 13.4. TMR0L: Timer 0 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR0L[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x52

Bit	Name	Function
7:0	TMR0L[7:0]	**Timer 0 Low Byte.** Contains the low byte of the 16-bit Timer 0.

SFR Definition 13.5. TMR0H Timer 0 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR0H[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x53

Bit	Name	Function
7:0	TMR0H[7:0]	**Timer 0 High Byte.** Contains the high byte of the 16-bit Timer 0.

Not Recommended for New Designs

13.2. Timer 1

Timer 1 is a 16-bit timer formed by two 8-bit SFRs: TMR1L (low byte) and TMR1H (high byte). Timer 1 operates in 16-bit auto-reload mode and is clocked by the system clock divided by 12 or SmaRTClock divided by 8. As the 16-bit timer register increments and overflows from 0xFFFF to 0x0000, the 16-bit value in the Timer 1 reload registers (TMR1RLH and TMR1RLL) is loaded into the Timer 1 register as shown in Figure 13.1, and the Timer 1 Overflow Flag (INT1.3) is set. If Timer 1 interrupts are enabled (if IN1EN.3 is set), an interrupt will be generated on each Timer 1 overflow. Additionally, if Timer 1 interrupts are enabled and the TF0LEN bit is set (TMR0CN.5), an interrupt will be generated each time the lower 8 bits (TMR0L) overflow from 0xFF to 0x00.

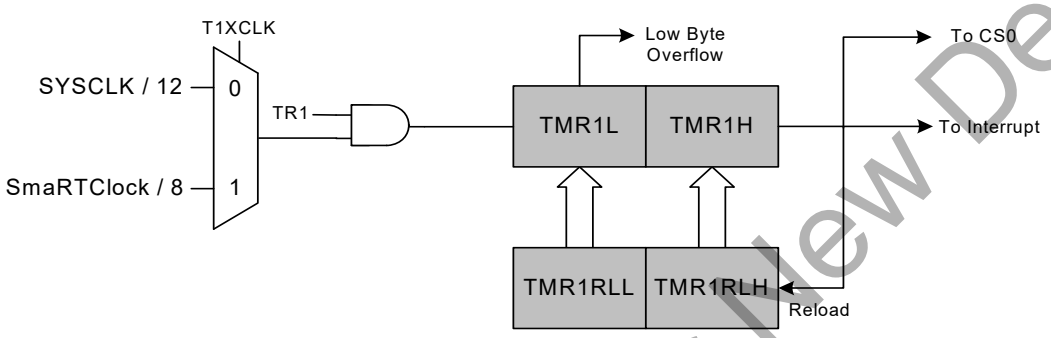


Figure 13.2. Timer 1 Block Diagram

Not Recommended for New Designs

13.2.1. Timer 1 SmaRTClock Oscillator Capture Mode

The Capture Mode in Timer 1 allows the SmaRTClock oscillator period to be measured against the system clock d by 12. Setting TF1CEN to 1 enables the SmaRTClock Oscillator Capture Mode for Timer 1.

When Capture Mode is enabled, a capture event will be generated every 8 SmaRTClock oscillator cycles. When the capture event occurs, the contents of Timer 1 (TMR1H:TMR1L) are loaded into the Timer 1 reload registers (TMR3RLH:TMR3RLL) and the T1F interrupt flag is set (triggering an interrupt if Timer 1 interrupts are enabled). By recording the difference between two successive timer capture values, the SmaRTClock period can be determined with respect to the system clock divided by 12. The system clock divided by 12 should be much faster than the SmaRTClock to achieve an accurate reading.

For example, if T1XCLK = 0b, and TF1CEN = 1b, Timer 1 will increment every 12 system clock cycles and capture every 8 SmaRTClock cycles. If the system clock is 24.5 MHz and the SmaRTClock is 32.768 kHz, the difference between two successive captures should be approximately 498 counts. Knowing the system clock frequency, the SmaRTClock frequency can be estimated as:

(SYSCLK x 8 / 12) / Counts = (24500000 Hz x 8 / 12) / 498 = 16333333 / 498 = 32797 Hz.

This mode allows software to determine the SmaRTClock oscillator frequency when the SmaRTClock oscillator is being used in self-oscillate mode without a crystal.

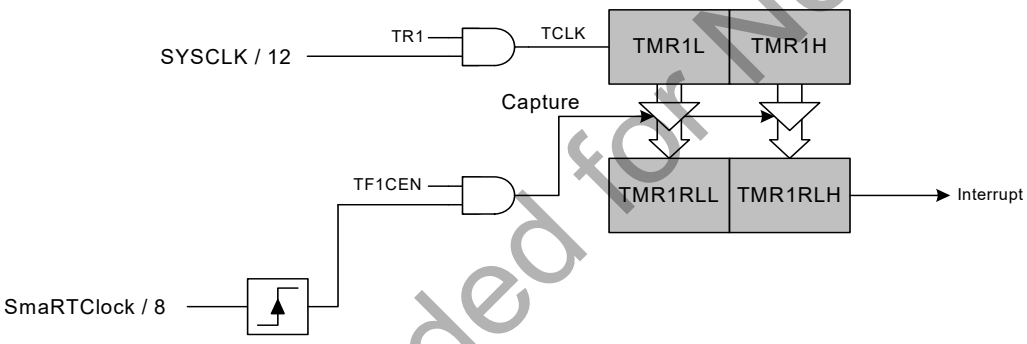


Figure 13.3. Timer 1 Capture Mode Block Diagram

Not Recommended for New Designs

SFR Definition 13.6. TMR1CN: Timer 1 Control

Bit	7	6	5	4	3	2	1	0
Name			TF1LEN	TF1CEN		TR1		
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x59

Bit	Name	Function
7:6	Unused	Read = 00b. Write = Don't Care.
5	TF1LEN	**Timer 1 Low Byte Interrupt Enable.** When set to 1, this bit enables Timer 1 Low Byte interrupts. If Timer 1 interrupts are enabled, an interrupt will be generated when the low byte of Timer 1 overflows.
4	TF1CEN	**Timer 1 SmaRTClock Oscillator Capture Enable.** When set to 1, this bit enables the Timer 1 SmaRTClock Oscillator capture mode.
3	Unused	Read = 00b. Write = Don't Care.
2	TR1	**Timer 1 Run Control.** Timer 1 is enabled by setting this bit to 1.
1	Unused	Read = 0b. Write = Don't Care.
0	T1XCLK	**Timer 1 External Clock Select.** 0: Timer 1 is clocked from the system clock divided by 12. 1: Timer 1 is clocked from the SmaRTClock oscillator divided by 8.

Not Recommended for New Designs

SFR Definition 13.7. TMR1RLL: Timer 1 Reload Register Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR1RLL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x55

Bit	Name	Function
7:0	TMR1RLL[7:0]	**Timer 1 Reload Register Low Byte.** TMR1RLL holds the low byte of the reload value for Timer 1.

SFR Definition 13.8. TMR1RLH: Timer 1 Reload Register High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR1RLH[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x56

Bit	Name	Function
7:0	TMR1RLH[7:0]	**Timer 1 Reload Register High Byte.** TMR1RLH holds the high byte of the reload value for Timer 1.

Not Recommended for New Designs

SFR Definition 13.9. TMR1L: Timer 1 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR1L[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x57

Bit	Name	Function
7:0	TMR1L[7:0]	**Timer 1 Low Byte.** Contains the low byte of the 16-bit Timer 1.

SFR Definition 13.10. TMR1H Timer 1 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR1H[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x58

Bit	Name	Function
7:0	TMR1H[7:0]	**Timer 1 High Byte.** Contains the high byte of the 16-bit Timer 1.

Not Recommended for New Designs

14. Serial Peripheral Interface (SPI)

CP2400/2 devices have a 4-wire Serial Peripheral Interface which provides access to the internal registers and memory. A typical connection to a SPI master is shown in Figure 14.1.

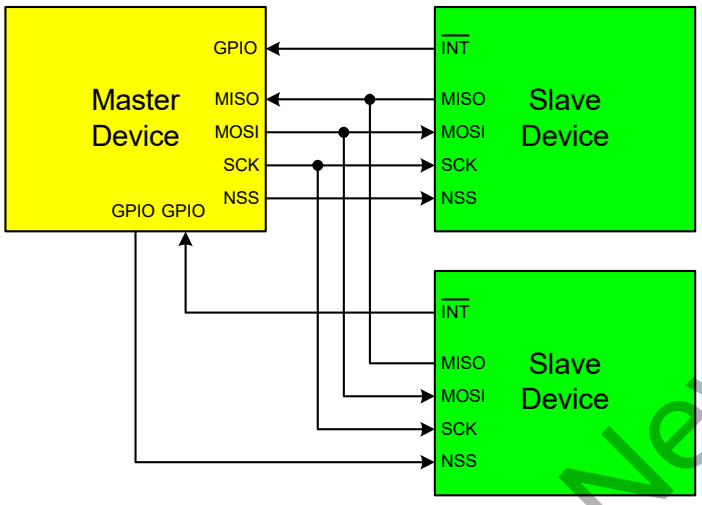


Figure 14.1. SPI Connection Diagram

14.1. Signal Descriptions

The four signals used by the SPI (MOSI, MISO, SCK, NSS) are described below.

14.1.1. Master Out, Slave In (MOSI)

The master-out, slave-in (MOSI) signal is an output from a master device and an input to slave devices. It is used to serially transfer data from the master to the slave. This signal is always in input for CP2402/1 devices. Data is transferred most-significant bit first.

14.1.2. Master In, Slave Out (MISO)

The master-in, slave-out (MISO) signal is an output from a slave device and an input to the master device. It is used to serially transfer data from the slave to the master. This signal is always an output for CP2402/1 devices. Data is transferred most-significant bit first. The MISO pin is placed in a high-impedance state when the slave select (NSS) signal is de-asserted.

14.1.3. Serial Clock (SCK)

The serial clock (SCK) signal is an output from the master device and an input to slave devices. It is used to synchronize the transfer of data between the master and slave on the MOSI and MISO lines. This signal is always an input for CP2402/1 devices. The SCK signal is ignored when the slave select (NSS) signal is de-asserted.

14.1.4. Slave Select (NSS)

The active-low slave-select (NSS) signal allows support for multiple slave devices on a single bus. It is also used by the CP2402/1 to detect the start and end of a SPI transfer.

Not Recommended for New Designs

14.2. Serial Clock Timing

The clock to data relationship is shown in Figure 14.2. If the SPI master is a C8051 microcontroller, its SPI peripheral must be configured for Mode 0 communication (CKPOL = 0, CKPHA = 0).

The maximum data transfer rate (bits/sec) for full-duplex operation is 1/10 the system clock frequency, provided that the master issues SCK, NSS, and the serial input data synchronously with the system clock. If the master issues SCK, NSS, and the serial input data asynchronously, the maximum data transfer rate (bits/sec) must be less than 1/10 the system clock frequency. In the special case where the master only wants to transmit data to the device and does not need to receive data back (i.e. half-duplex operation), the slave can receive data at a maximum data transfer rate (bits/sec) of 1/4 the system clock frequency. This is provided that the master issues SCK, NSS, and the serial input data synchronously with the system clock.

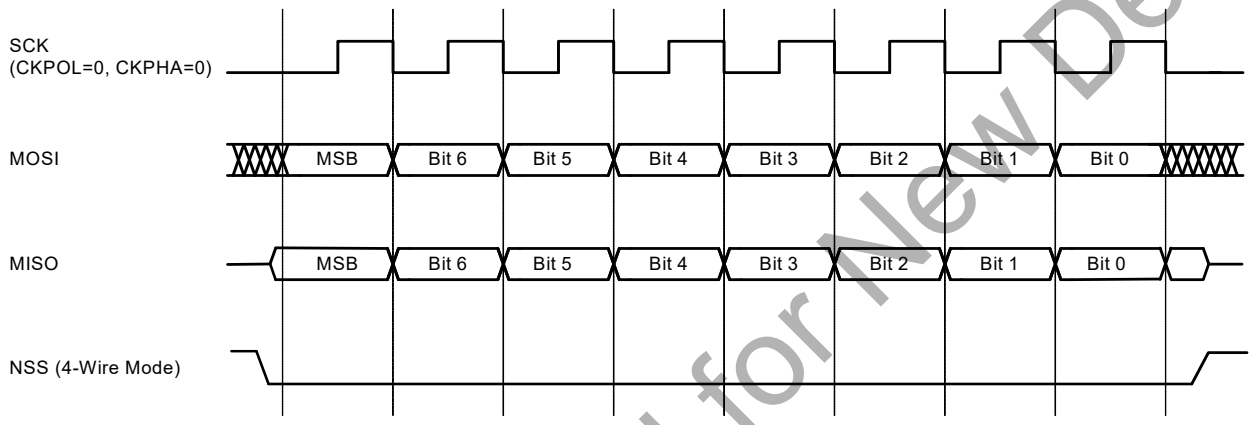


Figure 14.2. Data/Clock Timing

Not Recommended for New Designs

Table 14.1. SPI Slave Timing Parameters

Parameter	Description	Min	Max	Units
T_{SE}	NSS Falling to First SCK Edge	2 x T_{SYSCLK}	—	ns
T_{SD}	Last SCK Edge to NSS Rising	2 x T_{SYSCLK}	—	ns
T_{SEZ}	NSS Falling to MISO Valid	—	4 x T_{SYSCLK}	ns
T_{SDZ}	NSS Rising to MISO High-Z	—	4 x T_{SYSCLK}	ns
T_{CKH}	SCK High Time	5 x T_{SYSCLK}	—	ns
T_{CKL}	SCK Low Time	5 x T_{SYSCLK}	—	ns
T_{SIS}	MOSI Valid to SCK Sample Edge	2 x T_{SYSCLK}	—	ns
T_{SIH}	SCK Sample Edge to MOSI Change	2 x T_{SYSCLK}	—	ns
T_{SOH}	SCK Shift Edge to MISO Change	—	4 x T_{SYSCLK}	ns
T_{SLH}	Last SCK Edge to MISO Change (CKPHA = 1 ONLY)	6 x T_{SYSCLK}	8 x T_{SYSCLK}	ns

Note: T_{SYSCLK} is equal to one period of the device system clock (SYSCLK).

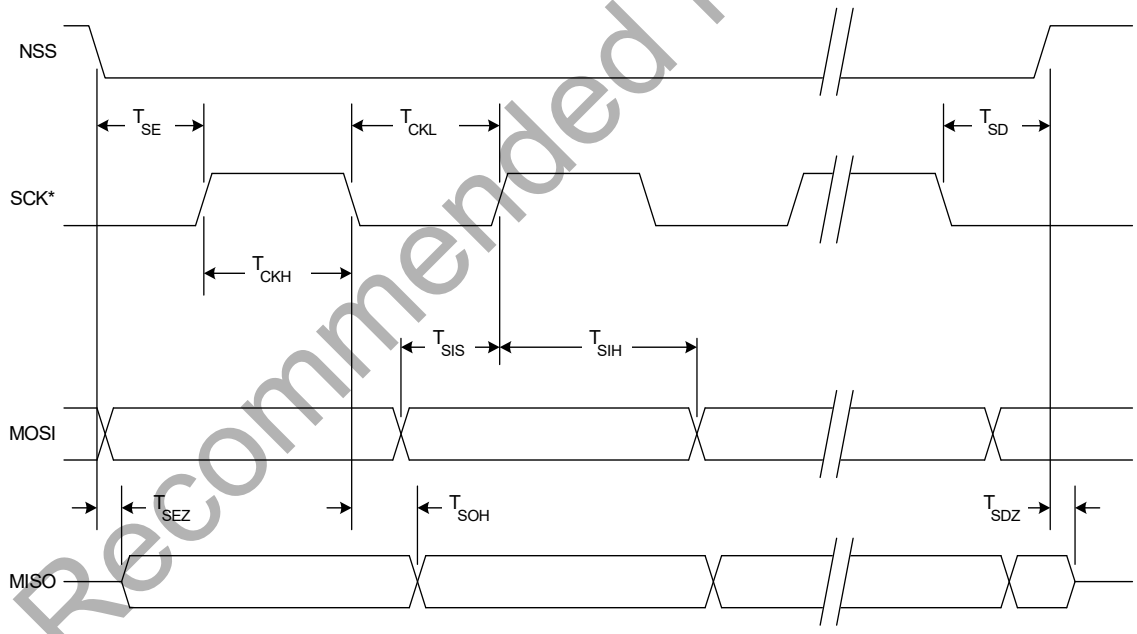


Figure 14.3. SPI Slave Timing

Not Recommended for New Designs

15. SMBus Interface

The SMBus I/O interface is a two-wire, bi-directional serial bus that can be used to access the internal registers and memory on CP2401/3 devices. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I2C serial bus. Reads and writes to the interface by the system controller are byte oriented with the SMBus interface autonomously controlling the serial transfer of the data. Data can be transferred at up to 1/20th of the system clock (this can be faster than allowed by the SMBus specification, depending on the system clock used). A method of extending the clock-low duration is available to accommodate devices with different speed capabilities on the same bus.

15.1. Supporting Documents

It is assumed the reader is familiar with or has access to the following supporting documents:

1. The I^2C-Bus and How to Use It (including specifications), Philips Semiconductor.
2. The I^2C-Bus Specification—Version 2.0, Philips Semiconductor.
3. System Management Bus Specification—Version 1.1, SBS Implementers Forum.

15.2. SMBus Configuration

Figure 15.1 shows a typical SMBus configuration. The SMBus specification allows any recessive voltage between 3.0 V and 5.0 V; different devices on the bus may operate at different voltage levels. The bi-directional SCL (serial clock) and SDA (serial data) lines must be connected to a positive power supply voltage through a pullup resistor or similar circuit. Every device connected to the bus must have an open-drain or open-collector output for both the SCL and SDA lines, so that both are pulled high (recessive state) when the bus is free. The maximum number of devices on the bus is limited only by the requirement that the rise and fall times on the bus not exceed 300 ns and 1000 ns, respectively.

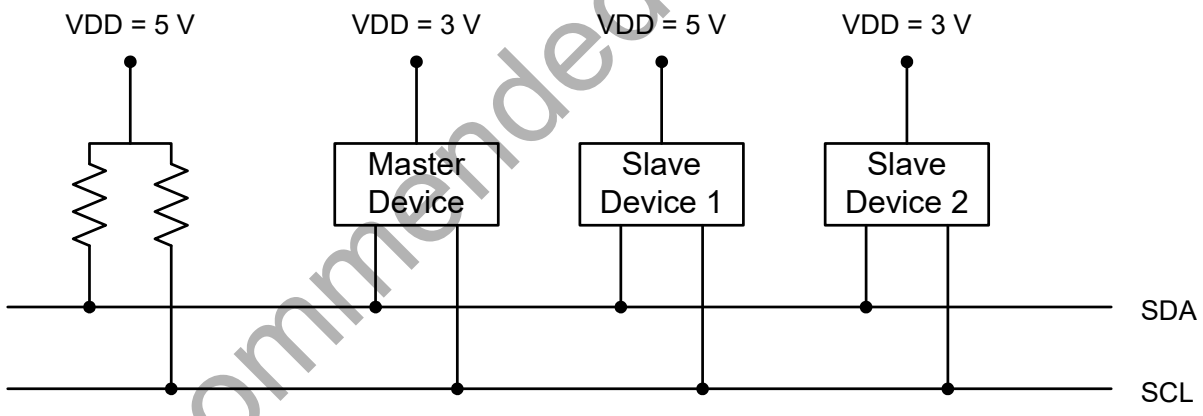


Figure 15.1. Typical SMBus Configuration

Not Recommended for New Designs

15.3. SMBus Operation

Two types of data transfers are possible: data transfers from a master transmitter to an addressed slave receiver (WRITE), and data transfers from an addressed slave transmitter to a master receiver (READ). The master device initiates both types of data transfers and provides the serial clock pulses on SCL. The SMBus interface on CP2401/3 devices only supports slave receiver and slave transmitter modes.

A typical SMBus transaction consists of a START condition followed by an address byte (Bits7–1: 7-bit slave address; Bit0: R/W direction bit), one or more bytes of data, and a STOP condition. Bytes that are received (by a master or slave) are acknowledged (ACK) with a low SDA during a high SCL (see Figure 15.2). If the receiving device does not ACK, the transmitting device will read a NACK (not acknowledge), which is a high SDA during a high SCL.

The direction bit (R/W) occupies the least-significant bit position of the address byte. The direction bit is set to logic 1 to indicate a "READ" operation and cleared to logic 0 to indicate a "WRITE" operation.

All transactions are initiated by a master, with one or more addressed slave devices as the target. The master generates the START condition and then transmits the slave address and direction bit. If the transaction is a WRITE operation from the master to the slave, the master transmits the data a byte at a time waiting for an ACK from the slave at the end of each byte. For READ operations, the slave transmits the data waiting for an ACK from the master at the end of each byte. At the end of the data transfer, the master generates a STOP condition to terminate the transaction and free the bus. Figure 15.2 illustrates a typical SMBus transaction.

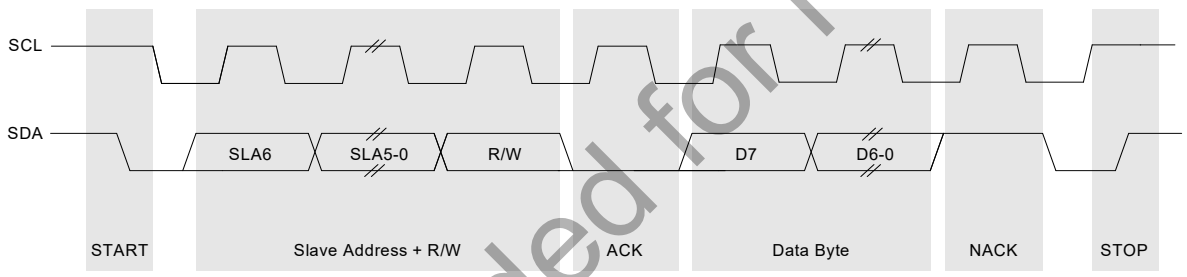


Figure 15.2. SMBus Transaction

15.3.1. Transmitter Vs. Receiver

On the SMBus communications interface, a device is the “transmitter” when it is sending an address or data byte to another device on the bus. A device is a “receiver” when an address or data byte is being sent to it from another device on the bus. The transmitter controls the SDA line during the address or data byte. After each byte of address or data information is sent by the transmitter, the receiver sends an ACK or NACK bit during the ACK phase of the transfer, during which time the receiver controls the SDA line.

15.3.2. Clock Low Extension

SMBus provides a clock synchronization mechanism, similar to I^2C, which allows devices with different speed capabilities to coexist on the bus. A clock-low extension is used during a transfer in order to allow slower slave devices to communicate with faster masters. The slave may temporarily hold the SCL line LOW to extend the clock low period, effectively decreasing the serial clock frequency.

Not Recommended for New Designs

15.3.3. SCL Low Timeout

If the SCL line is held low by a slave device on the bus, no further communication is possible. Furthermore, the master cannot force the SCL line high to correct the error condition. To solve this problem, the SMBus protocol specifies that devices participating in a transfer must detect any clock cycle held low longer than 25 ms as a “timeout” condition. Devices that have detected the timeout condition must reset the communication no later than 10 ms after detecting the timeout condition.

When SMBus is used for communication with the host microcontroller, Timer 0 is used to detect SCL low timeouts. Timer 0 is forced to reload when SCL is high, and allowed to count when SCL is low. With Timer 0 enabled and configured to overflow after 25 ms, the Timer 0 interrupt service routine can be used to alert the host microcontroller of an SCL Low Timeout. After an SCL Low Timeout, the SMBus slave will reset its internal state machine and will be ready to respond to new transfers. On reset or wake-up from ULP mode, Timer 0 is enabled and configured for SCL Low Timeout detection. The SCL Low Timeout may be disabled by clearing the SMBTOE bit in the SMB0CF register. This allows full software control of Timer 0.

15.3.4. SCL High (SMBus Free) Timeout

The SMBus specification stipulates that if the SCL and SDA lines remain high for more that 50 µs, the bus is designated as free. When the SMBFTE bit in SMB0CF is set, the bus will be considered free if SCL and SDA remain high for more than 1250 system clock periods. After an SCL High Timeout, the SMBus slave will reset its internal state machine and will be ready to respond to new transfers.

15.3.5. Slave Address Selection

CP2400/1/2/3 devices can have one of 2 possible 7-bit, left-justified slave addresses: 0x74 and 0x76. The least significant bit of the slave address is set by the SMBA0 pin. The remaining bits in the slave address are fixed. The bit following the least significant address bit is used to indicate whether the current transfer is a read or a write.

Not Recommended for New Designs

SFR Definition 15.1. SMBCF: SMBus Clock/Configuration

Bit	7	6	5	4	3	2	1	0
Name	ENSMB	INH	BUSY	EXTHOLD	SMBTOE	SMBFTE	Reserved	
Type	R/W	R/W	R	R/W	R/W	R/W	R/W	
Reset (CP2400/2)	0	0	0	0	0	0	0	0
Reset (CP2401/3)	1	0	0	1	1	1	0	0

Address: 0x68

Bit	Name	Function
7	ENSMB	**SMBus Enable.** This bit enables the SMBus interface when set to 1. When enabled, the interface constantly monitors the SDA and SCL pins.
6	INH	**SMBus Slave Inhibit.** When this bit is set to logic 1, the SMBus does not generate an interrupt when slave events occur. This effectively removes the SMBus slave from the bus.
5	BUSY	**SMBus Busy Indicator.** This bit is set to logic 1 by hardware when a transfer is in progress. It is cleared to logic 0 when a STOP or free-timeout is sensed.
4	EXTHOLD	**SMBus Setup and Hold Time Extension Enable.** This bit controls the SDA setup and hold times. 0: Setup time is 4 system clocks and hold time is 3 system clocks. 1: Setup time is 11 system clocks and hold time is 12 system clocks.
3	SMBTOE	**SMBus SCL Timeout Detection Enable.** This bit enables SCL low timeout detection. If set to logic 1, the SMBus forces Timer 0 to reload while SCL is high and allows Timer 0 to count when SCL goes low. The Timer 0 reload value should be set to overflow the timer after 25 ms.
2	SMBFTE	**SMBus Free Timeout Detection Enable.** When this bit is set to logic 1, the bus will be considered free if SCL and SDA remain high for more than 50 µs.
1:0	Reserved	Read = 00b. Must write 00b.
Note: This register has a reset value of 0x00 in devices that do not support SMBus.		

Not Recommended for New Designs

DOCUMENT CHANGE LIST

Revision 1.0 to Revision 1.1

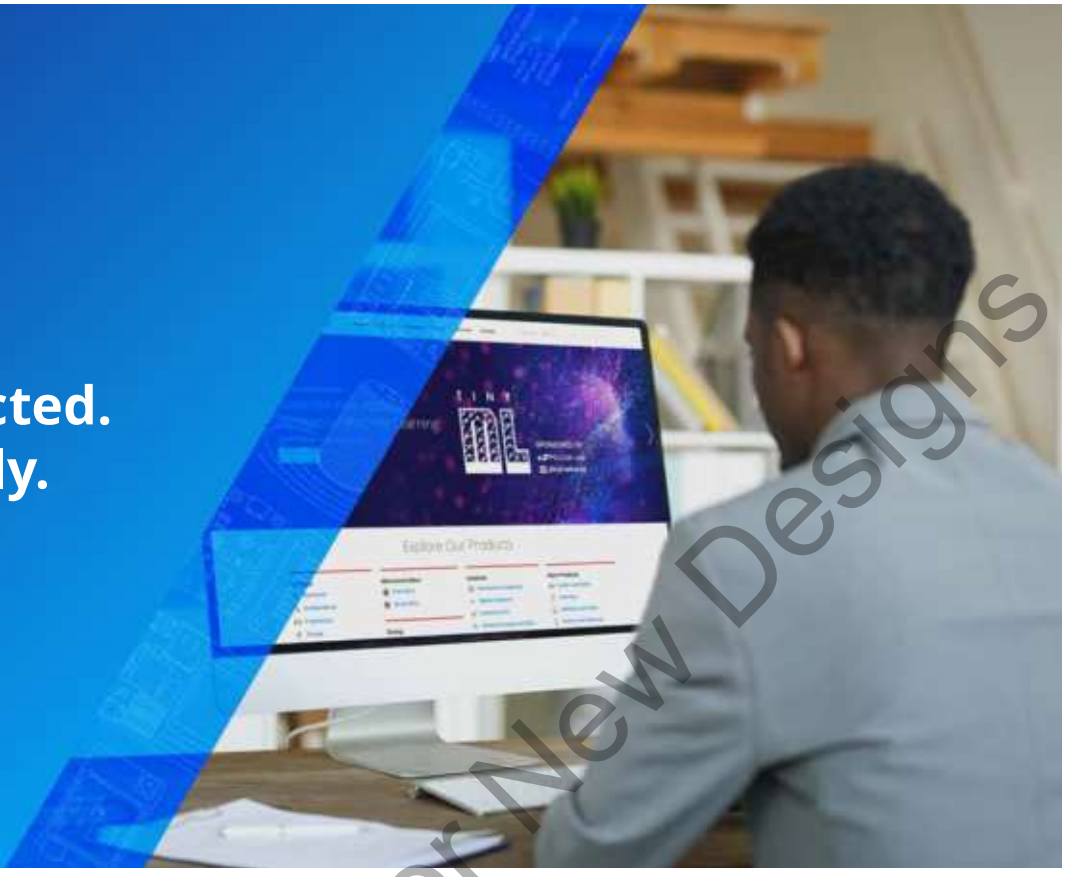
- Applied End of Life (EOL) designation to specific part numbers on the front page.

Revision 0.2 to Revision 1.0

- Updated Electrical Specifications to remove TBDs and specify min/max parameters.
- Updated Reset Values for various registers.
- Updated Register Description for LCD0PWR register.

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