

Features

- Small 16-pin SOIC or DFN package
- DFN package printed-circuit board footprint is 60 percent smaller than the SOIC version, 40 percent smaller than fourth generation EMR solutions.
- Monolithic IC reliability
- Low, matched R_{ON}
- Eliminates the need for zero-cross switching
- Flexible switch timing for transition from ringing mode to idle/talk mode.
- Clean, bounce-free switching
- Tertiary protection consisting of integrated current limiting, thermal shutdown for SLIC protection
- 5 V operation with power consumption < 10 mW
- Intelligent battery monitor
- Latched logic-level inputs, no external drive circuitry required
- SOIC package pin-compatible with Legerity product

Applications

- Central office (CO)
- Digital Loop Carrier (DLC)
- PBX Systems
- Digitally Added Main Line (DAML)
- Hybrid Fiber Coax (HFC)
- Fiber in the Loop (FITL)
- Pair Gain System
- Channel Banks

Description

The CPC7581 is a monolithic solid-state four-pole switch in a 16-pin package. It provides the necessary functions to replace a 2-Form-C electromechanical relay on traditional analog and integrated voice and data (IVD) line cards found in central office, access, and PBX equipment. The CPC7581 contains solid-state switches for tip and ring lead line break and ringing injection/ringing return. The device requires only a +5 V supply and offers break-before-make and make-before-break operation using logic-level inputs.

The CPC7581xA versions include an SCR that provides protection to the SLIC and subsequent circuitry during a fault condition. The CPC7581xC versions are functionally identical to the CPC7581xA versions, but with higher SCR hold current.

Ordering Information

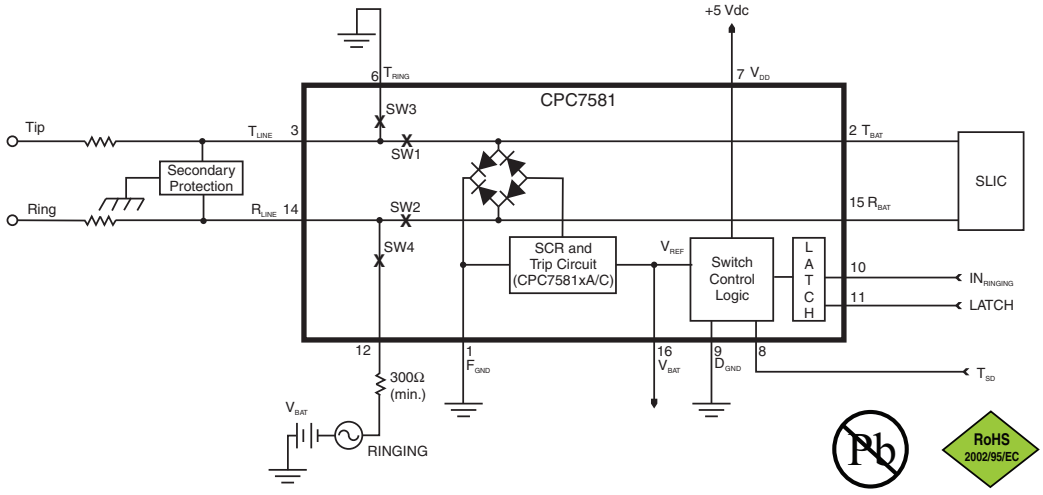
CPC7581 part numbers are specified as shown here:

B - 16-pin SOIC delivered 50/Tube, 1000/Reel
M - 16-pin DFN delivered 52/Tube, 1000/Reel

CPC7581 x x xx — TR - Add for Tape & Reel Version

A - With Protection SCR
B - Without Protection SCR
C - With Protection SCR and higher SCR hold current

Figure 1. CPC7581 Block Diagram



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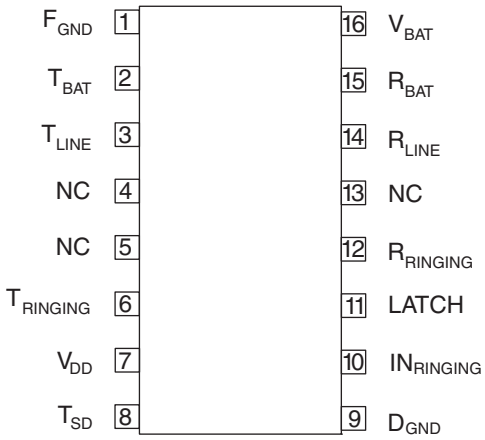
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1. Specifications

1.1 Package Pinout

CPC7581



1.2 Pinout

Pin	Name	Description
1	F_{GND}	Fault ground
2	T_{BAT}	Tip lead of the SLIC
3	T_{LINE}	Tip lead of the line side
4	NC	No connection
5	NC	No connection
6	$T_{RINGING}$	Ringing generator return
7	V_{DD}	+5 V supply
8	T_{SD}	Temperature shutdown pin
9	D_{GND}	Digital ground
10	$IN_{RINGING}$	Logic control input
11	LATCH	Data latch enable control input
12	$R_{RINGING}$	Ringing generator source
13	NC	No connection
14	R_{LINE}	Ring lead of the line side
15	R_{BAT}	Ring lead of the SLIC
16	V_{BAT}	Battery supply

1.3 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
+5 V power supply (V_{DD})	-0.3	7	V
Battery Supply	-	-85	V
D_{GND} to F_{GND} Separation	-5	+5	V
Logic input voltage	-0.3	V_{DD} + 0.3	V
Logic input to switch output isolation	-	320	V
Switch open-contact isolation (SW1, SW2, SW3)	-	320	V
Switch open-contact isolation (SW4)	-	465	V
Operating relative humidity	5	95	%
Operating temperature	-40	+110	°C
Storage temperature	-40	+150	°C

Absolute maximum electrical ratings are at 25°C.

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied. Exposure of the device to the absolute maximum ratings for an extended period may degrade the device and affect its reliability.

1.4 ESD Rating

ESD Rating (Human Body Model)
1000 V

1.5 General Conditions

Unless otherwise specified, minimum and maximum values are production testing requirements.

Typical values are characteristic of the device at 25°C and are the result of engineering evaluations. They are provided for informational purposes only and are not part of the manufacturing testing requirements.

Specifications cover the operating temperature range T_A = -40°C to +85°C. Also, unless otherwise specified all testing is performed with V_{DD} = +5V_{dc}, logic low input voltage is 0V_{dc} and logic high input voltage is +5V_{dc}.

1.6 Switch Specifications

1.6.1 Break Switches, SW1 and SW2

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-state leakage current						
+25° C	V_{SW} (differential) = -320 V to gnd V_{SW} (differential) = +260 V to -60 V	I_{SW}	-	0.1	1	µA
+85° C	V_{SW} (differential) = -330 V to gnd V_{SW} (differential) = +270 V to -60 V			0.3		
-40° C	V_{SW} (differential) = -310 V to gnd V_{SW} (differential) = +250 V to -60 V			0.1		
R_{ON}						
+25° C	I_{SW} = ±10 mA, ±40 mA, R_{BAT} and T_{BAT} = -2 V	R_{ON}	-	14.5	-	Ω
+85° C				20.5	28	
-40° C				10.5	-	
R_{ON} match	Per on-resistance test condition of SW1, SW2. Magnitude R_{ON} SW1-R_{ON} SW2	Δ R_{ON}	-	0.15	0.8	
DC current limit						
+25° C	V_{SW} (on) = ±10 V	I_{SW}	-	300	-	mA
+85° C			80	160	-	
-40° C			-	400	425	
Dynamic current limit ($t \leq 0.5$ µs)	Break switches on, all other switches off, apply ±1 kV at 10x1000 µs pulse, with appropriate protection in place.		-	2.5	-	A
Logic input to switch output isolation						
+25° C	V_{SW} (T_{LINE}, R_{LINE}) = ±320 V, logic inputs = gnd	I_{SW}	-	0.1	1	µA
+85° C	V_{SW} (T_{LINE}, R_{LINE}) = ±330 V, logic inputs = gnd			0.3		
-40° C	V_{SW} (T_{LINE}, R_{LINE}) = ±310 V, logic inputs = gnd			0.1		
dv/dt sensitivity	-	-		200	-	V/µs

1.6.2 Ringing Return Switch, SW3

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-state leakage current						
+25° C	V_{SW} (differential) = -320 V to gnd V_{SW} (differential) = +260 V to -60 V	I_{SW}	-	0.1	1	µA
+85° C	V_{SW} (differential) = -330 V to gnd V_{SW} (differential) = +270 V to -60 V			0.3		
-40° C	V_{SW} (differential) = -310 V to gnd V_{SW} (differential) = +250 V to -60 V			0.1		
R_{ON}						
+25° C	I_{SW} (on) = ±0 mA, ±10 mA	R_{ON}	-	60	-	Ω
+85° C				85	100	
-40° C				45	-	
DC current limit						
+25° C	V_{SW} (on) = ±10 V	I_{SW}	-	135	-	mA
+85° C			70	85		
-40° C			-	210		
Dynamic current limit ($t \leq 0.5$ µs)	Ringing switches on, all other switches off, apply ±1 kV at 10x1000 µs pulse, with appropriate protection in place.			2.5		A
Logic input to switch output isolation						
+25° C	V_{SW} ($T_{RINGING}$, T_{LINE}) = ±320 V, logic inputs = gnd	I_{SW}	-	0.1	1	µA
+85° C	V_{SW} ($T_{RINGING}$, T_{LINE}) = ±330 V, logic inputs = gnd			0.3		
-40° C	V_{SW} ($T_{RINGING}$, T_{LINE}) = ±310 V, logic inputs = gnd			0.1		
dv/dt sensitivity	-	-		200	-	V/µs

1.6.3 Ringing Switch, SW4

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-state leakage current						
+25° C	V_{SW} (differential) = -255 V to +210 V V_{SW} (differential) = +255 V to -210 V	I_{SW}	-	0.05	1	µA
+85° C	V_{SW} (differential) = -270 V to +210 V V_{SW} (differential) = +270 V to -210 V			0.1		
-40° C	V_{SW} (differential) = -245 V to +210 V V_{SW} (differential) = +245 V to -210 V			0.05		
On Voltage	I_{SW} (on) = ± 1 mA	-		1.5	3	V
Ringing generator current to ground during ringing	V_{DD} = 5 V, $IN_{RINGING}$ = 0	$I_{RINGING}$		0.1	0.25	mA
On steady-state current*	Inputs set for ringing mode	I_{SW}		-	150	mA
Surge current*	Ringing switches on, all other switches off, apply ±1 kV at 10x1000 µs pulse, with appropriate protection in place.	-		-	2	A
Release current	-	$I_{RINGING}$		300	-	µA
R_{ON}	I_{SW} (on) = ±70 mA, ±80 mA	R_{ON}		10	15	Ω
Logic input to switch output isolation						
+25° C	V_{SW} ($R_{RINGING}$, R_{LINE}) = ±320 V, logic inputs = gnd	I_{SW}	-	0.1	1	µA
+85° C	V_{SW} ($R_{RINGING}$, R_{LINE}) = ±330 V, logic inputs = gnd			0.3		
-40° C	V_{SW} ($R_{RINGING}$, R_{LINE}) = ±310 V, logic inputs = gnd			0.1		
dv/dt sensitivity	-	-		200	-	V/µs

**Secondary protection and ringing source current limiting must prevent exceeding this parameter.*

1.7 Additional Electrical Characteristics

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Digital input characteristics						
Input low voltage	-	V_{IL}	-	2.2	1.5	V
Input high voltage	-	V_{IH}	3.5	2.3	-	
Input leakage current (high)	V_{DD} = 5.5 V, V_{BAT} = -75 V, V_{IH} = 5 V	I_{IH}	-	0.1	1	µA
Input leakage current (low)	V_{DD} = 5.5 V, V_{BAT} = -75 V, V_{IL} = 0 V	I_{IL}	-	0.1	1	
Voltage Requirements						
V_{DD}	-	V_{DD}	4.5	5.0	5.5	V
V_{BAT}[1]	-	V_{BAT}	-19	-48	-72	V
[1] V_{BAT} is used only for internal protection circuitry. If V_{BAT} goes more positive than -10 V, the device will enter the all-off state and will remain in the all-off state until the battery goes more negative than -15 V						
Power requirements						
Power consumption in talk and all-off states	V_{DD} = 5 V, V_{BAT} = -48 V, measure I_{DD} and I_{BAT}	P	-	5.5	10	mW
Power consumption in ringing state				6.5	10	
V_{DD} current in talk and all-off states	V_{DD} = 5 V, V_{BAT} = -48 V	I_{DD}	-	1.1	2.0	mA
V_{DD} current in ringing state			-	1.3	2.0	
V_{BAT} current in any state		I_{BAT}	-	0.1	10	µA
Temperature Shutdown Requirements (temperature shutdown flag is active low)						
Shutdown activation temperature	-	-	110	125	150	°C
Shutdown circuit hysteresis			10	-	25	
Temperature shutdown requirements are not production tested, but rather guaranteed by design.						

1.8 Protection Circuitry Electrical Specifications

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Parameters Related to the Diodes in the Diode Bridge						
Voltage drop at continuous current (50/60 Hz)	Apply ± dc current limit of break switches	Forward Voltage	-	2.1	3	V
Voltage drop at surge current	Apply ± dynamic current limit of break switches	Forward Voltage	-	5	-	
Parameters Related to the Protection SCR						
Surge current	-	-	-	-	*	A
Trigger current	T=+25°C	I_{TRIG}	-	60 (CPC7581xA) 70 (CPC7581xC)	-	mA
	T=+85°C			35 (CPC7581xA) 40 (CPC7581xC)		
Hold current	T=+25°C	I_{HOLD}		110 (CPC7581xA) 135 (CPC7581xC)		
	T=+85°C		60 (CPC7581xA) 110 (CPC7581xC)	70 (CPC7581xA) 115 (CPC7581xC)		
Gate trigger voltage	$I_{GATE} = I_{TRIGGER}$**	V_{TBAT} or V_{RBAT}	V_{BAT} -4	-	V_{BAT} -2	V
Reverse leakage current	V_{BAT} = -48 V	I_{VBAT}	-	-	1.0	µA
On-state voltage	0.5 A, t = 0.5 µs	V_{TBAT} or V_{RBAT}	-	-3	-	V
	2.0 A, t = 0.5 µs		-	-5	-	V

*Passes GR1089 and ITU-T K.20 with appropriate secondary protection in place.
**V_{BAT} must be capable of sourcing $I_{TRIGGER}$ for the internal SCR to activate.

1.9 Truth Table

State	$IN_{RINGING}$	Latch	T_{SD}	Break Switches	Ringing Switches
Talk	0	0	Z[1]	On	Off
Ringing	1			Off	On
Latched	X	1		Unchanged	
All-Off	X	X	0	Off	Off

[1] Z = High Impedance. Because T_{SD} has an internal pull up at this pin, it should be controlled with an open-collector or open-drain type device.

2. Functional Description

2.1 Introduction

The CPC7581 has three states:

- **Talk**. Line break switches SW1 and SW2 closed, ringing switches SW3 and SW4 open.
- **Ringing**. Ringing switches SW3 and SW4 closed, line break switches SW1 and SW2 open.
- **All-off**. All switches open.

See "Truth Table" on page 9 for more information.

The CPC7581 offers break-before-make and make-before-break switching from the ringing state to the talk state with simple logic-level input control. Solid-state switch construction means no impulse noise is generated when switching during ring cadence or ring trip, eliminating the need for external zero-cross switching circuitry. State control is via logic-level input so no additional driver circuitry is required. The line break switches SW1 and SW2 are linear switches that have exceptionally low R_{ON} and excellent matching characteristics. The ringing switch SW4 has a breakdown voltage rating of 465V @ 25°C. This is sufficiently high, with proper protection, to prevent breakdown in the presence of a transient fault condition (i.e., passing the transient on to the ringing generator).

Integrated into the CPC7581 is a over voltage clamping circuit, active current limiting, and a thermal shutdown mechanism to provide protection to the SLIC device during a fault condition. Positive and negative surges are reduced by the current limiting circuitry and hazardous potentials are steered to ground via diodes and, in CPC7581xA and CPC7581xC parts, an integrated SCR. Power-cross potentials are also reduced by the current limiting and thermal shutdown circuits.

To protect the CPC7581 from an overvoltage fault condition, the use of a secondary protector is required. The secondary protector must limit the voltage seen at the tip and ring terminals to a level below the maximum breakdown voltage of the switches. To minimize the stress on the solid-state contacts, use of a foldback or crowbar type secondary protector is recommended. With proper selection of the secondary protector, a line card using the CPC7581 will meet all relevant ITU, LSSGR, TIA/EIA and IEC protection requirements.

The CPC7581 operates from a +5 V supply only. This gives the device extremely low idle and active power consumption and allows use with virtually any range of battery voltage. Battery voltage is also used by the CPC7581 as a reference for the integrated protection circuit. In the event of a loss of battery voltage, the CPC7581 enters the all-off state.

2.2 Switch Logic

The CPC7581 provides, when switching from the ringing state to the talk state, the ability to control the release timing of the ringing switches SW3 and SW4 relative to the state of the line break switches SW1 and SW2 using simple logic-level input. This is called make-before-break or break-before-make operation. When the line break switch contacts (SW1 and SW2) are closed (or made) before the ringing switch contacts (SW3 and SW4) are opened (or broken), this is called make-before-break operation.
Break-before-make operation occurs when the ringing contacts (SW3 and SW4) are opened (broken) before the line break contacts (SW1 and SW2) are closed (made).

To use make-before-break ringing switch release timing, de-assert $IN_{RINGING}$ during ringing. This causes the operational sequence shown in "Make-Before-Break Operation Logic Table (Ringing to Talk Transition)" on page 11 to occur.

2.2.1 Make-Before-Break Operation Logic Table (Ringing to Talk Transition)

State	$IN_{RINGING}$	Latch	T_{SD}	Timing	Break Switches	Ringing Return Switch (SW3)	Ringing Switch (SW4)
Ringing	1	0	Z	-	Off	On	On
Make-Before-Break	0			SW4 waiting for next zero-current crossing to turn off. Maximum time is one-half of the ringing cycle. In this transition state, current that is limited to the dc break switch current limit value will be sourced from the ring node of the SLIC.	On	Off	On
Talk	0			Zero-cross current has occurred	On	Off	Off

To use break-before-make ringing switch release timing, assert T_{SD} during ringing. This causes the operational sequence shown in **"Break-Before-Make Operation Logic Table (Ringing to Talk Transition)" on page 11** to occur.

2.2.2 Break-Before-Make Operation Logic Table (Ringing to Talk Transition)

State	$IN_{RINGING}$	Latch	T_{SD}	Timing	Break Switches	Ringing Return Switch (SW3)	Ringing Switch (SW4)
Ringing	1	0	Z	-	Off	On	On
All-off	1		0	Hold this state for one-half of the ringing cycle. SW4 waiting for zero current to turn off.	Off	Off	On
All-off	1			Zero current has occurred. SW4 has opened	Off	Off	Off
Talk	0		Z	Release break switches	On	Off	Off

Logic states and explanations are given in **"Truth Table" on page 9**.

2.3 Data Latch

The CPC7581 has an integrated data latch. The latch operation is controlled by logic-level input pin 11 (LATCH). The data input of the latch is pin 10 ($IN_{RINGING}$), while the output of the data latch is an internal node used for state control. When the LATCH control pin is at logic 0, the data latch is transparent and data control signals flow directly through to state control. A change in input will be reflected in a change is switch state. When the LATCH control pin is at logic 1, the data latch is active and a change in input control will not affect switch state. The switches will remain in the position they were in when the LATCH changed from logic 0 to logic 1 and will not respond to changes in input as long as the latch is at logic 1. The T_{SD} input is not tied to the data latch. Therefore, T_{SD} is not affected by the LATCH input and the T_{SD} input will override state control.

2.4 T_{SD}

The thermal shutdown mechanism activates when the device die temperature reaches a minimum of 110° C, placing the device in the all-off state regardless of logic input. During thermal shutdown mode, pin 8 (T_{SD}) will read a nominal 0 V. Normal output of T_{SD} is typically equal to V_{DD}.

If presented with a short duration transient such as a lightning event, the thermal shutdown feature will typically not activate. But in an extended power-cross event, the device temperature will rise and the thermal shutdown will activate forcing the switches to the all-off state. At this point the current measured through the break switches (SW1 and SW2) will drop to zero. Once the device enters thermal shutdown it will remain in the all-off state until the temperature of the device drops below the de-activation level of the thermal shutdown circuit. This permits the device to

return to normal operation. If the transient has not passed, current will flow at the value allowed by the dynamic DC current limiting of the switches and heating will begin again, reactivating the thermal shutdown mechanism. This cycle of entering and exiting the thermal shutdown mode will continue as long as the fault condition persists. If the magnitude of the fault condition is great enough, the external secondary protector could activate and shunt all current to ground.

The T_{SD} pin is a pull-up current source with a nominal value of 300 µA biased from V_{DD}. For applications using low-voltage logic devices (lower than V_{DD}), Clare recommends the use of an open-drain type output to control T_{SD}. This avoids sinking the T_{SD} bias current to ground during normal operation when the all-off state is not required.

2.5 Ringing Switch Zero-Cross Current Turn Off

After the application of a logic input to turn SW4 off, the ringing switch is designed to delay the change in state until the next zero-crossing. Once on, the switch requires a zero-current cross to turn off, and therefore should not be used to switch a pure DC signal. The switch will remain in the on state no matter the logic input until the next zero crossing. These switching characteristics will reduce and possibly eliminate overall system impulse noise normally associated with ringing switches. See Clare application note **AN-144, Impulse Noise Benefits of Line Card Access Switches** for more information. The attributes of ringing switch SW4 may make it possible to eliminate the need for a zero-cross switching scheme. A minimum impedance of 300 Ω in series with the ring generator is recommended.

2.6 Power Supplies

Both a +5 V supply and battery voltage are connected to the CPC7581. CPC7581 switch state control is powered exclusively by the +5 V supply. As a result, the CPC7581 exhibits extremely low power dissipation during both active and all-off states.

The battery voltage is not used for switch control but rather as a supply for the integrated secondary protection circuitry. The integrated SCR is designed to trigger when pin 2 (T_{BAT}) or pin 15 (R_{BAT}) drops 2 to 4 V below the voltage on pin 16 (V_{BAT}). This trigger prevents a fault-induced overvoltage event at the T_{BAT} or R_{BAT} nodes.

2.7 Battery Voltage Monitor

The CPC7581 also uses the V_{BAT} voltage to monitor battery voltage. If system battery voltage is lost, the CPC7581 immediately enters the all-off state. It remains in this state until the battery voltage is restored. The device also enters the all-off state if the system battery voltage goes more positive than –10 V, and remains in the all-off state until the battery voltage goes more negative than –15 V. This battery monitor feature draws a small current from the battery (less than 1 µA typical) and adds slightly to the device's overall power dissipation.

Due to the nature of the internal protection circuitry, the V_{BAT} pin can be biased via potentials applied to T_{BAT} or R_{BAT}. This allows the CPC7581 switches to operate, but offers no transient protection. The supply voltage applied to V_{BAT} should therefor be the same supply voltage applied to the line driver device.

2.8 Protection

2.8.1 Diode Bridge/SCR

The CPC7581 uses a combination of current limited break switches, a diode bridge/SCR clamping circuit, and a thermal shutdown mechanism to protect the SLIC device or other associated circuitry from damage during line transient events such as lightning. During a positive transient condition, the fault current is conducted through the diode bridge to ground via F_{GND}. Voltage is clamped to a diode drop above ground. During a negative transient of 2 to 4 V more negative than the battery, the SCR conducts and faults are shunted to F_{GND} via the SCR or the diode bridge.

In order for the SCR to crowbar (or foldback), the on voltage (see **"Protection Circuitry Electrical Specifications" on page 9**) of the SCR must be less negative than the battery reference voltage. If the battery voltage is less negative than the SCR on voltage, or if the V_{BAT} supply is unable to source the trigger current, the SCR will not crowbar.

For power induction or power-cross fault conditions, the positive cycle of the transient is clamped to a diode drop above ground and the fault current directed to ground. The negative cycle of the transient will cause the SCR to conduct when the voltage exceeds the

battery reference voltage by two to four volts, steering the current to ground.

Note: The CPC7581xB does not contain the protection SCR.

2.8.2 Current Limiting function

If a lightning strike transient occurs when the device in the talk state, the current is passed along the line to the integrated protection circuitry and limited by the dynamic current limit response of break switches SW1 and SW2. When a 1000V 10x1000 μs pulse (GR-1089-CORE lightning) is applied to the line though a properly clamped external protector, the current seen through the break switches will be a pulse with a typical magnitude of 2.5 A and a duration of less than 0.5 μs.

If a power-cross fault occurs with the device in the talk state, the current is passed though the break switches SW1 and SW2 on to the integrated protection circuit and is limited by the dynamic DC current limit response of the two break switches. The DC current limit, specified over temperature, is between 80 mA and 425 mA, and the circuitry has a negative temperature coefficient. As a result, if the device is subjected to extended heating due to power cross fault, the measured current through the break switches (SW1 and SW2) will decrease as the device temperature increases. If the device temperature rises sufficiently, the temperature shutdown mechanism will activate and the device will enter the all-off state.

2.9 External Protection Elements

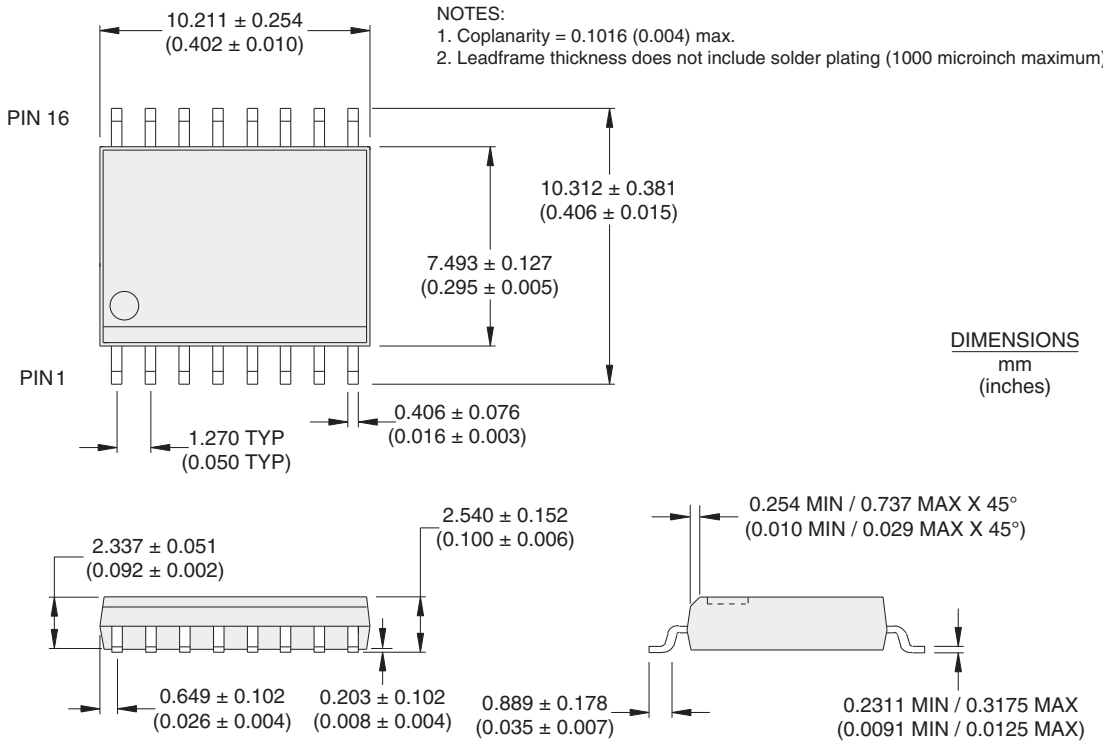
The CPC7581 requires only overvoltage secondary protection on the loop side of the device. The integrated protection feature described above negates the need for protection on the other (usually SLIC) side. The secondary protector limits voltage transients to levels that do not exceed the breakdown voltage or input-output isolation barrier of the CPC7581. A foldback or crowbar type protector is recommended to minimize stresses on the device.

Consult Clare's application note, AN-100, "Designing Surge and Power Fault Protection Circuits for Solid State Subscriber Line Interfaces" for equations related to the specifications of external secondary protectors, fused resistors and PTCs.

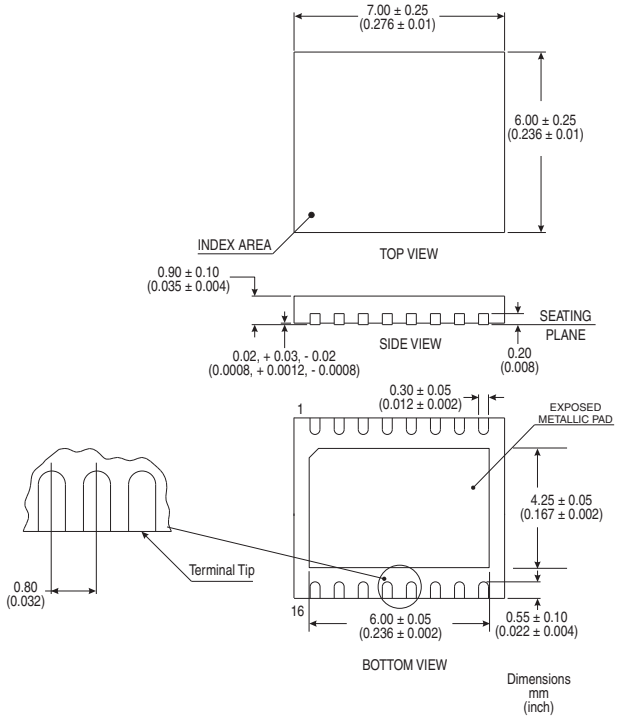
3. Manufacturing Information

3.1 Mechanical Dimensions

3.1.1 SOIC

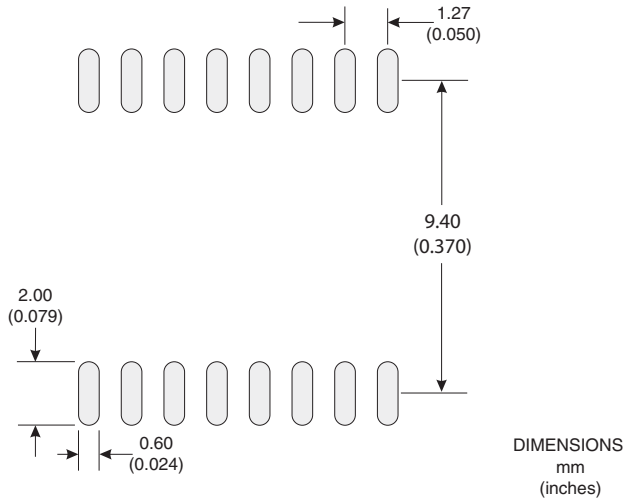


3.1.2 DFN

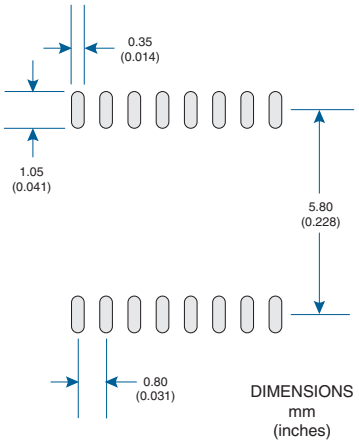


3.2 Printed-Circuit Board Layout

3.2.1 SOIC



3.2.2 DFN

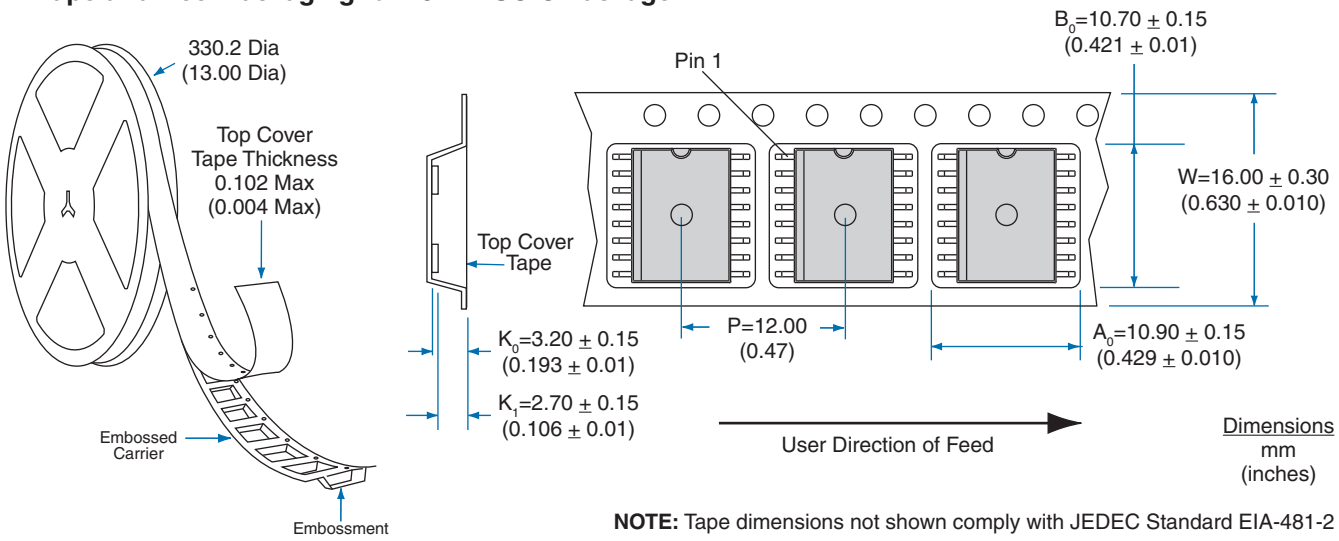


As the metallic pad on the bottom of the DFN package is connected to the substrate of the die, Clare recommends that no printed circuit board traces or vias be placed under this area.

3.3 Tape and Reel Packaging

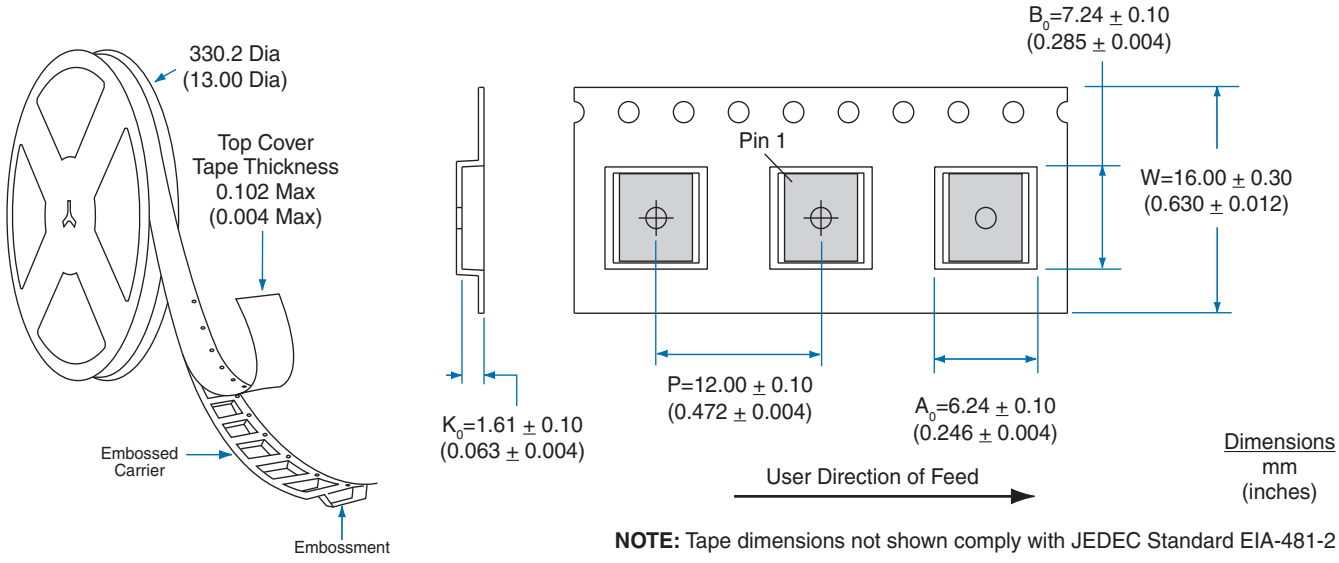
3.3.1 SOIC

Tape and Reel Packaging for 16-Pin SOIC Package



NOTE: Tape dimensions not shown comply with JEDEC Standard EIA-481-2

3.3.2 DFN



NOTE: Tape dimensions not shown comply with JEDEC Standard EIA-481-2

3.4 Soldering

3.4.1 Moisture Reflow Sensitivity

Clare has characterized the moisture reflow sensitivity for this product using IPC/JEDEC standard J-STD-020. Moisture uptake from atmospheric humidity occurs by diffusion. During the solder reflow process, in which the component is attached to the PCB, the whole body of the component is exposed to high process temperatures. The combination of moisture uptake and high reflow soldering temperatures may lead to moisture induced delamination and cracking of the component. To prevent this, this component must be handled in accordance with IPC/JEDEC standard J-STD-033 per the labeled moisture sensitivity level (MSL), level 1 for the SOIC package, and level 3 for the DFN package.

3.4.2 Reflow Profile

For proper assembly, this component must be processed in accordance with the current revision of IPC/JEDEC standard J-STD-020. Failure to follow the recommended guidelines may cause permanent damage to the device resulting in impaired performance and/or a reduced lifetime expectancy.

3.5 Washing

Clare does not recommend ultrasonic cleaning of this part.



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