CS3002

Precision Low-voltage Amplifier; DC to 2kHz

Features

- Low Offset: 10µV Max
- Low Drift: 0.05µV/°C Max
- Low Noise
  - 6nV/√Hz @ 0.5Hz
  - 0.1 to 10Hz = 125nVpp
  - 1/f corner @ 0.08Hz
- Open-loop Voltage Gain
  - 300dB Typical
  - 200dB Minimum
- Rail-to-rail Output Swing
- Slew Rate: 5V/µs

Applications

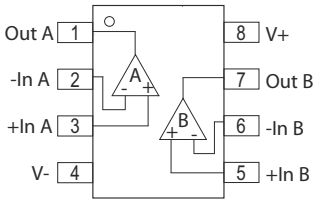
- Thermocouple/Thermopile Amplifiers
- Load Cell and Bridge Transducer Amplifiers
- Precision Instrumentation
- Battery-powered Systems

Description

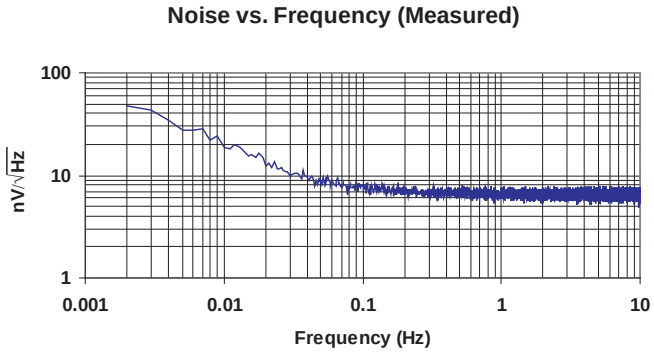
The CS3002 dual amplifier is designed for precision amplification of low-level signals and is ideally suited for applications that require very high closed-loop gains. These amplifiers achieve excellent offset stability, super-high open-loop gain, and low noise over time and temperature. The devices also exhibit excellent CMRR and PSRR. The common mode input range includes the negative supply rail. The amplifiers operate with any total supply voltage from 2.7V to 6.7V (±1.35V to ±3.35V).

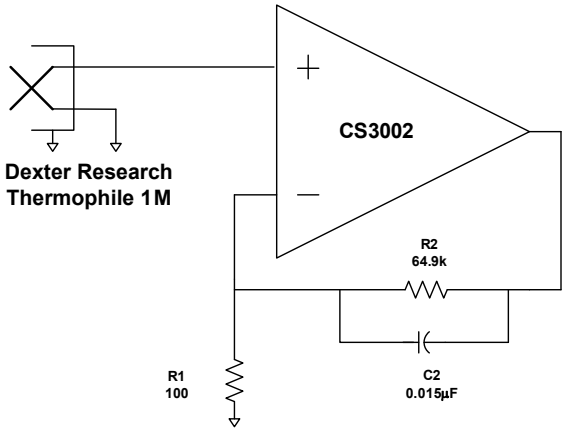
Pin Configuration

CS3002



8-lead SOIC





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1. CHARACTERISTICS AND SPECIFICATIONS

1.1 Electrical Characteristics

Typical characteristics conditions:
- T_A = 25 °C, V+ = +5 V, V- = 0 V, VCM = 2.5V
- All voltages are measured with respect to V-

Minimum/Maximum characteristics conditions:
- T_J = -40 °C to +125 °C, V+ = +5 V, V- = 0 V, VCM = 2.5V

Parameter	Condition	Min	Typ	Max	Unit
Input Offset Voltage (Note 1)		-	-	±10	µV
Average Input Offset Drift (Note 1)		-	±0.01	±0.05	µV/ºC
Long Term Input Offset Voltage Stability			(Note 2)		
Input Bias Current	T_A = 25ºC	- -	±100 -	- ±1000	pA pA
Input Offset Current	T_A = 25ºC	- -	±200 -	- ±2000	pA pA
Input Noise Voltage Density	R_S = 100Ω, f_0 = 1Hz R_S = 100Ω, f_0 = 1kHz	- -	6 6		nV/$\sqrt{Hz}$ nV/$\sqrt{Hz}$
Input Noise Voltage	0.1 to 10Hz	-	125		nV_{pp}
Input Noise Current Density	f_0 = 1Hz	-	100		fA/$\sqrt{Hz}$
Input Noise Current	0.1 to 10Hz	-	1.9		pA_{p-p}
Input Common Mode Voltage Range		-0.1	-	(V+)-1.25	V
Common Mode Rejection Ratio (DC) (Note 3)		115	120	-	dB
Power Supply Rejection Ratio		120	136	-	dB
Large Signal Voltage Gain (Note 4)	R_L = 2kΩ to V+/2	200	300	-	dB
Output Voltage Swing	R_L = 2kΩ to V+/2 R_L = 100kΩ to V+/2	+4.7	- +4.99	-	V V
Slew Rate	R_L = 2k, 100pF		5	-	V/µs
Overload Recovery Time		-	100	-	µs
$\overline{PWDN}$ Threshold (Note 5)		(V+) -1.0	-	-	V
Start-up Time (Note 5)		-	9	12	ms

Notes:
1. This parameter is guaranteed by design and laboratory characterization. Thermocouple effects prohibit accurate measurement of these parameters in automatic test systems.
2. 1000-hour life test data @ 125 °C indicates randomly distributed variation approximately equal to measurement repeatability of 1µV.
3. Measured within the specified common mode range limits.
4. Guaranteed within the output limits of (V+ - 0.3V) to (V- + 0.3V). Tested with proprietary production test method.
5. The device has a controlled start-up behavior due to its complex open-loop gain characteristics. Start-up time applies when supply voltage is applied or when $\overline{PDWN}$ is released.

1.2 Absolute Maximum Ratings

Parameter	Min	Typ	Max	Unit
Supply Voltage [(V+) - (V-)]			6.8	V
Input Voltage	(V-) - 0.3		(V+) + 0.3	V
Storage Temperature Range	-65		+150	ºC

2. TYPICAL PERFORMANCE PLOTS

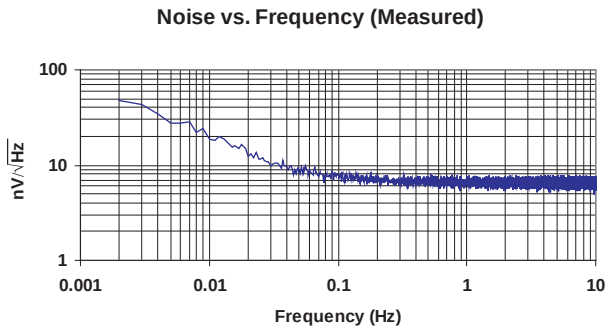


Figure 1. Noise vs. Frequency (Measured)

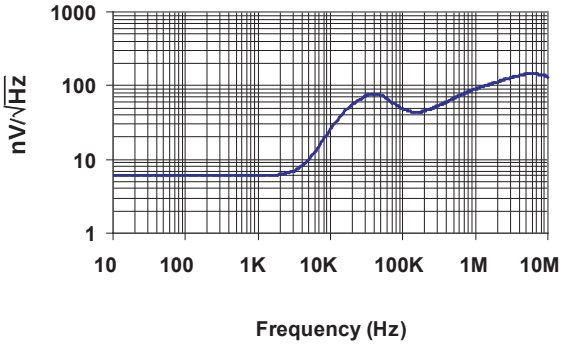


Figure 2. Noise vs. Frequency

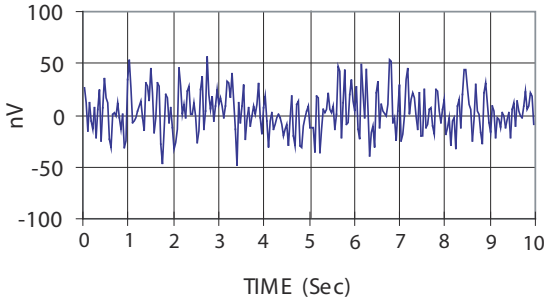


Figure 3. 0.01 Hz to 10 Hz Noise

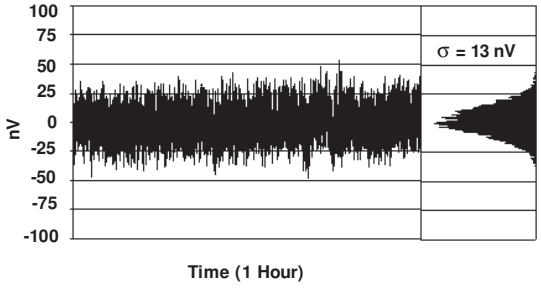


Figure 4. Offset Voltage Stability (DC to 3.2 Hz)

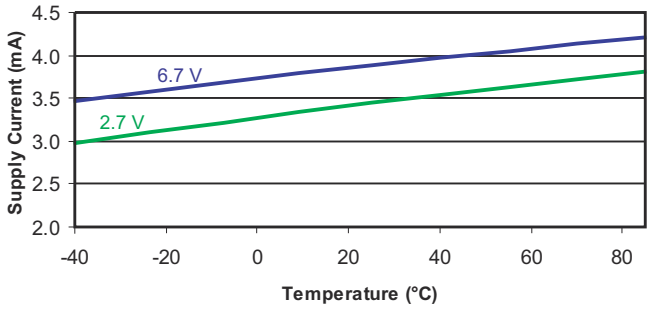


Figure 5. Supply Current vs. Temperature

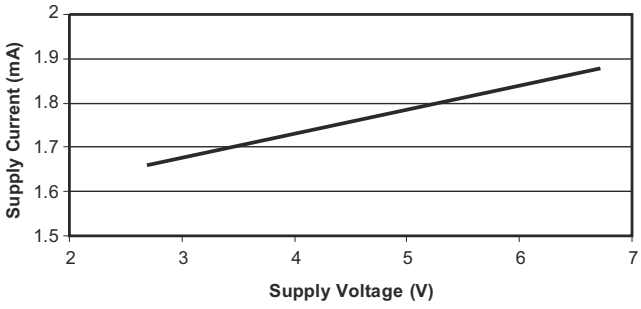


Figure 6. Supply Current vs. Supply Voltage

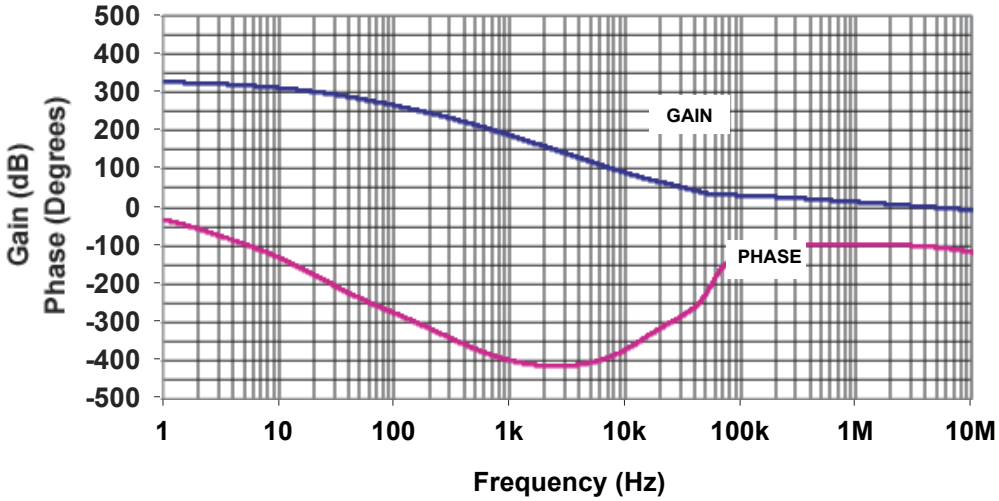


Figure 7. Open-loop Gain and Phase vs. Frequency

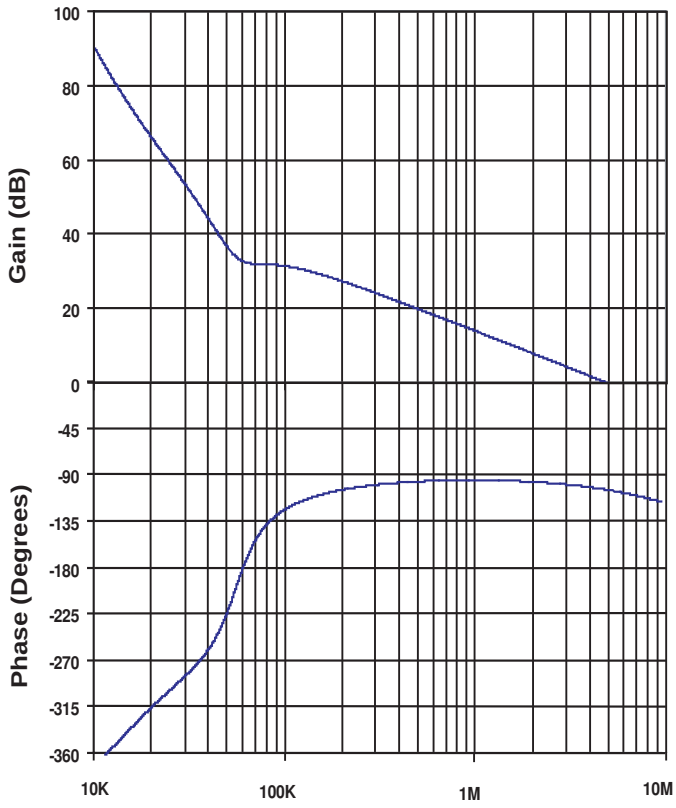


Figure 8. Open-loop Gain and Phase vs. Frequency (Expanded)

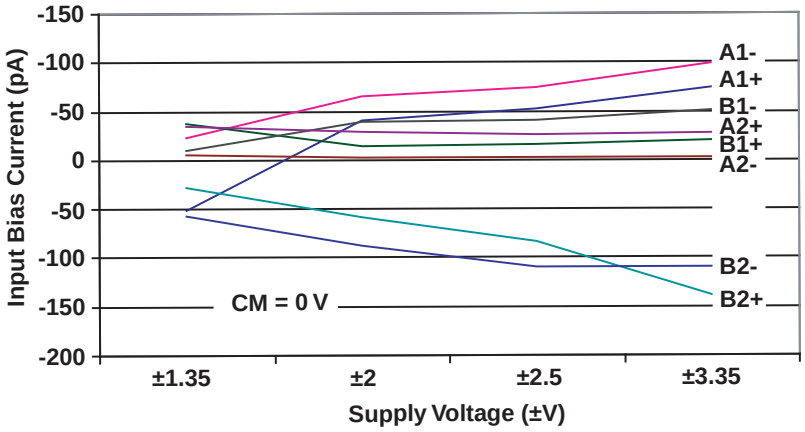


Figure 9. Input Bias Current vs. Supply Voltage

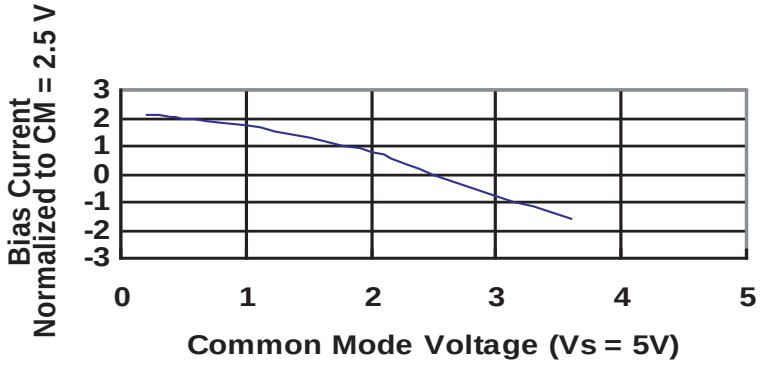


Figure 10. Input Bias Current vs. Common Mode Voltage

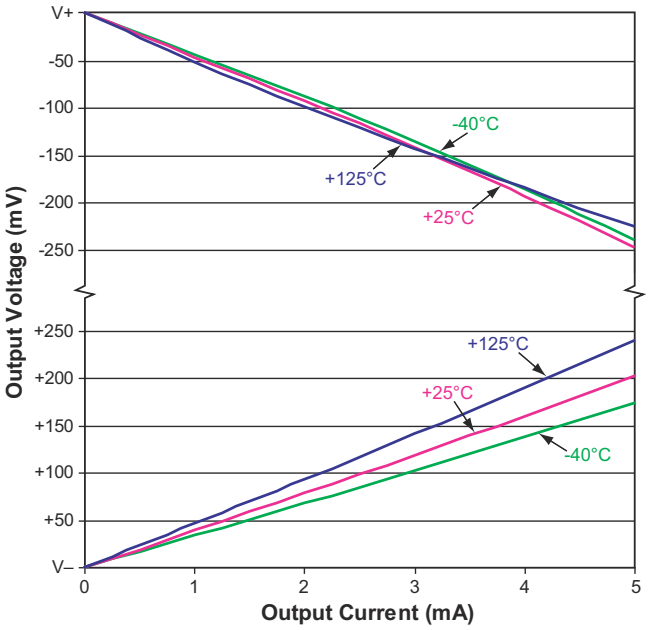


Figure 11. Voltage Swing vs. Output Current

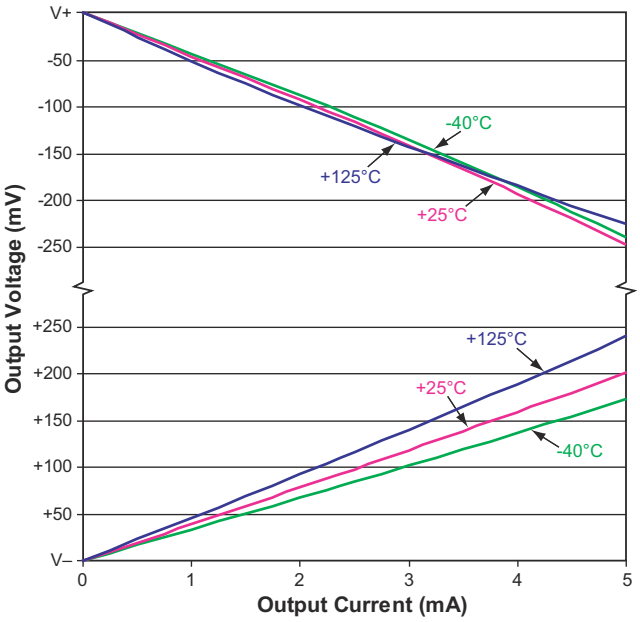


Figure 12. Voltage Swing vs. Output Current (5V)

3. OVERVIEW

The CS3002 amplifiers are designed for precision measurement of signals from DC to 2kHz when operating from a supply voltage of +2.7V to +6.7V (±1.35V to ±3.35V). The amplifiers are designed with a patented architecture that utilizes multiple amplifier stages to yield very high open-loop gain at frequencies of 10 kHz and below.

The amplifiers yield low noise and low offset drift while consuming relatively low supply current. An increase in noise floor above 2kHz is the result of intermediate stages of the amplifier being operated at very low currents. The amplifiers are intended for amplifying small signals with large gains in applications where the output of the amplifier can be band-limited to frequencies below 2kHz.

3.1 Open-loop Gain and Phase Response

Figure 13 illustrates the open-loop gain and phase response of the CS3002. The gain slope of the amplifier is approximately -100dB/decade between 500Hz and 60kHz and transitions to -20dB/decade between 60kHz and its unity gain crossover frequency at approximately 4.8MHz. Phase margin at unity gain is about 70° and the gain margin is approximately 20dB.

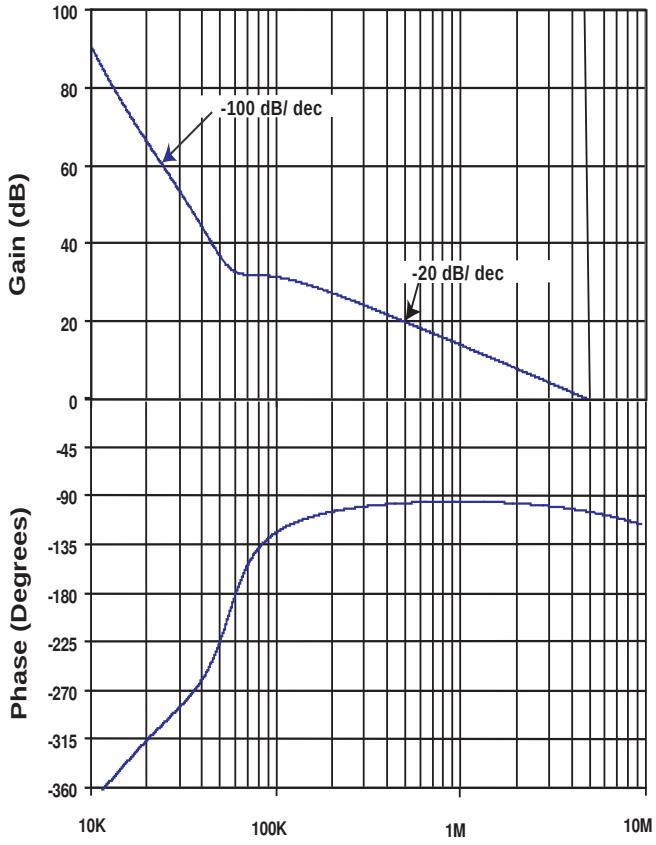


Figure 13. Open-loop Gain and Phase Response

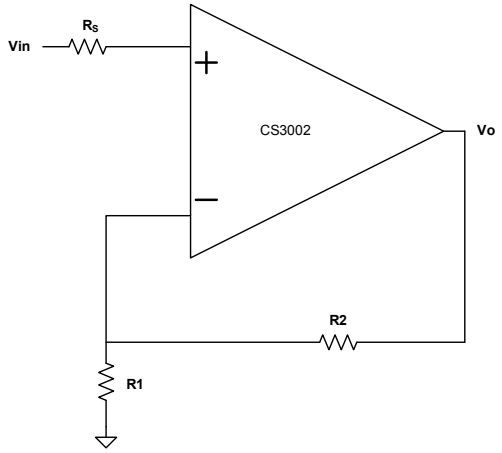


Figure 14. Non-inverting Gain Configuration

3.2 Open-loop Gain and Stability

3.2.1 Discussion

The CS3002 achieves ultra-high open-loop gain. Figure 14 illustrates the amplifier in a non-inverting gain configuration. The open-loop gain and phase plots indicate that the amplifier is stable for closed-loop gains less than 50 V/V and R1 ≤ 100 Ω. For a gain of 50, the phase margin is between 40° and 60° depending upon the loading conditions. As shown in Figure 15, on page 9, the operational amplifier has an input capacitance at the + and – signal inputs of typically 50 pF. This capacitance adds an additional pole in the loop gain transfer function at a frequency defined using Equation 1:

$$f = \frac{1}{2\pi R \times C_{in}} \qquad \text{[Eq. 1]}$$

where

R = R1 || R2; the parallel combination of R1 and R2

A higher value for R produces a pole at a lower frequency, thus reducing the phase margin. Resistor R1 is recommended to be less than or equal to 100 Ω, which results in a pole at 30 MHz or higher. If a higher value of R1 is desired, compensation capacitor C2 should be added in parallel with resistor R2. Capacitor C2 should be chosen using Equation 2:

$$R2 \times C2 \geq R1 \times C_{in} \qquad \text{[Eq. 2]}$$

The feedback capacitor C2 is required for closed-loop gains greater than 50 V/V. The capacitor introduces a pole P_1 and a zero Z_1 in the loop gain transfer function T(s), see Equation 3

$$T(s) = \left[\frac{-\left(1+\frac{s}{Z_1}\right)}{\left(1+\frac{s}{P_1}\right)}\right] \times A_{ol} \qquad \text{[Eq. 3]}$$

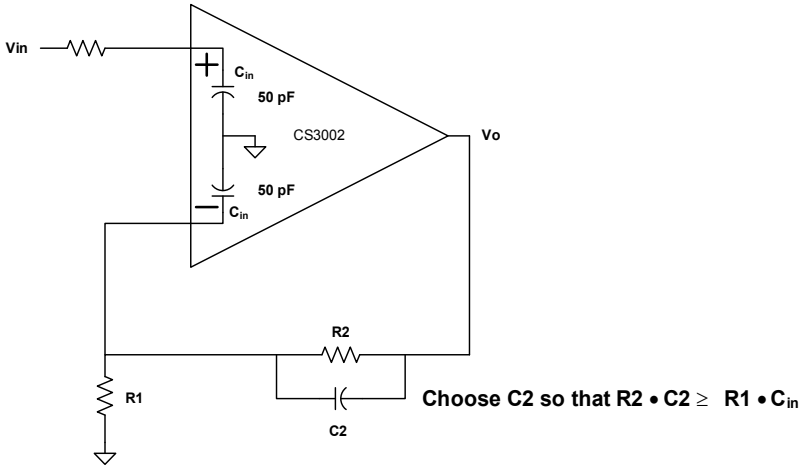


Figure 15. Non-inverting Gain Configuration with Compensation

Equation 4 is used to determine transfer function zero Z_1.

$$Z_1 = \frac{1}{2\pi \times (A \times R1) \times C2} \quad \text{[Eq. 4]}$$

where

$|A| = R2/R1$

Substituting A into Equation 4 then zero Z_1 is:

$$Z_1 = \frac{1}{2\pi \times R2 \times C2} \quad \text{[Eq. 5]}$$

Equation 6 is used to determine the transfer function pole P_1.

$$P_1 = \frac{1}{2\pi \times (R1 \parallel R2) \times C2} \cong \frac{1}{2\pi \times R1 \times C2} \quad \text{[Eq. 6]}$$

where

$R2 >> R1$

This indicates that the separation of the pole and the zero is governed by the closed loop gain. It is required that the zero falls on the steep slope (-100dB/decade) of the loop gain plot so that there is some gain higher than 0dB (typically 20dB) at the hand-over frequency (the frequency at which the slope changes from -100dB/decade to -20dB/decade). The loop gain plot shown in Figure 16 illustrates the unity gain configuration, and indicates how this is modified when using the amplifier in a higher gain configuration with compensation. If it is configured for higher gain, for example, 60dB, the x-axis will move up by 60dB (line B). Capacitor C2 adds a zero and a pole. The modified plot indicates the effects of introducing the pole and zero due to capacitor C2. The pole can be located at any frequency higher than the hand-over frequency, the zero has to be at a frequency lower than the hand-over frequency so as to provide adequate gain margin. The separation between the pole and the zero is governed by the closed loop gain. The zero (Z_1) occurs at the intersection of the -100dB/decade and -80dB/decade slopes. The point X in the figure should be at closed loop gain plus 20dB gain margin. The value for capacitor C2 is determined by Equation 7. Setting the

$$C2 = \frac{1}{2\pi \times R1 \times P_1} \quad \text{[Eq. 7]}$$

pole of the filter to P_1 = 1MHz works very well and is independent of gain. As the closed loop gain is changed, the zero location is also modified if R1 remains fixed. Capacitor C2 can be increased in value to limit the amplifier's rising noise above 2kHz.

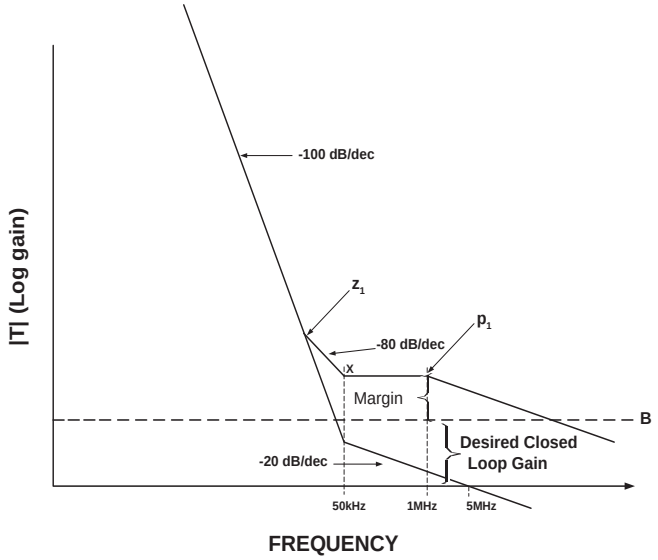


Figure 16. Loop Gain Plot: Unity Gain and with Pole-zero Compensation

3.2.2 Gain Calculation Recommendations

Condition 1: |Av| ≤ 50 and R1 ≤ 100Ω

The op amp is inherently stable for |Av| ≤ 50 and R1 ≤ 100Ω. Capacitor C2 is not required for compensation across resistor R2.

1) |Av| = 1 configuration has 70° phase margin and 20dB gain margin.
2) |Av| = 50 configuration has phase margin between 40° for C_{LOAD} ≤ 100 pF and 60° for C_{LOAD} = 0pF.

Condition 2: |Av| ≤ 50 and R1 > 100Ω

Compensation capacitor C2 across resistor R2 is required. Calculate C2 using Equation 8:

$$C2 \geq \frac{(R1 \times C_{in})}{R2} \quad \text{[Eq. 8]}$$

where

C_{in} = 50pF

Condition 3: |Av| > 50

Compensation capacitor C2 across resistor R2 is required. Calculate and verify a value for C2 using the following steps.

Calculate the Compensation Capacitor Value:

1) Calculate a value for C2 using Equation 9:

$$C2 = \frac{1}{[2\pi(R1 \parallel R2) \times P_1]} \quad \text{[Eq. 9]}$$

where

P_1 = 1MHz

To simplify the calculation, set the pole of the filter to P_1 = 1MHz. Pole P_1 must be set higher than the op amp's internal 50kHz crossover frequency.

2) Calculate a second value for C2 using Equation 10:

$$C2 \geq \frac{(R1 \times C_{in})}{R2} \quad \text{[Eq. 10]}$$

where

C_{in} = 50pF

3) Use the larger of the two values calculated in steps 1 and 2.

Verify the Op Amp Compensation:

Verify the op amp compensation using the open-loop gain and phase response Bode plot in Figure 13. Plot the calculated closed loop gain transfer function and verify the following design criteria are met:

1) Pole P_1 > op amp internal 50kHz crossover frequency

$$P_1 = \frac{1}{2\pi(R1 \parallel R2) \times C2} \quad \text{[Eq. 11]}$$

where

P_1 = 1MHz

To simplify the calculation, set the pole to P_1 = 1MHz.

2) Z1 < op amp internal 50kHz crossover frequency

$$Z_1 = \frac{1}{2\pi(R2 \times C2)} \quad \text{[Eq. 12]}$$

3) Gain margin above the open-loop gain transfer function is required. A gain margin of +20dB above the open-loop gain transfer function is optimal.

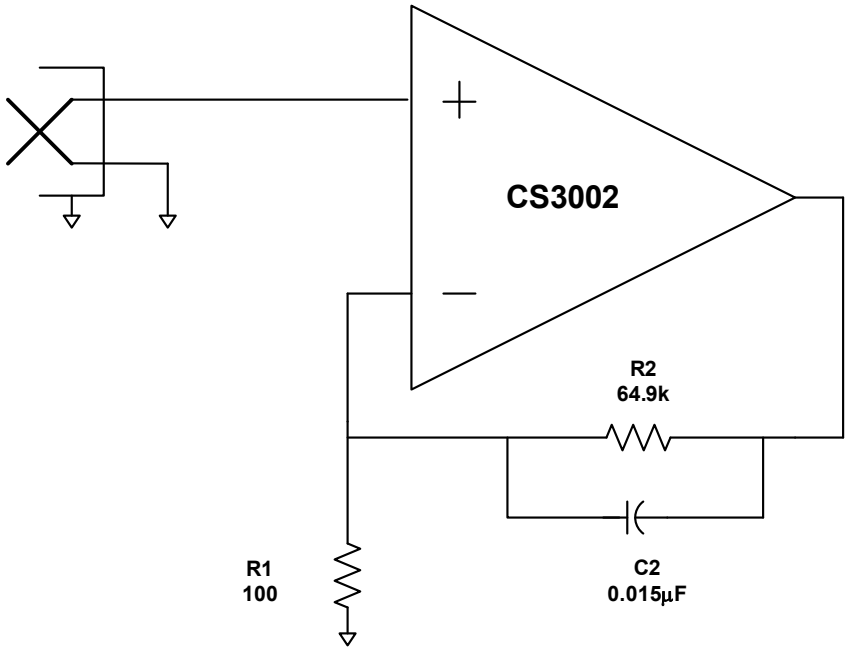


Figure 17. Thermopile Amplifier with a Gain of 650V/V

3.3 Applications

The CS3002 amplifiers are optimum for applications that require high gain and low drift. Figure 17 illustrates a thermopile amplifier with a gain of 650V/V. The thermopile outputs only a few millivolts when subjected to infrared radiation. The amplifier is compensated and bandlimited by capacitor C2 in combination with resistor R2.

Figure 18, on page 12 illustrates a load cell bridge amplifier with a gain of 768V/V. The load cell is excited with +5V and has a 1mV/V sensitivity. Its full scale output signal is amplified to produce a fully differential ±3.8V into the CS5510/12 A/D converter. This circuit operates from +5V.

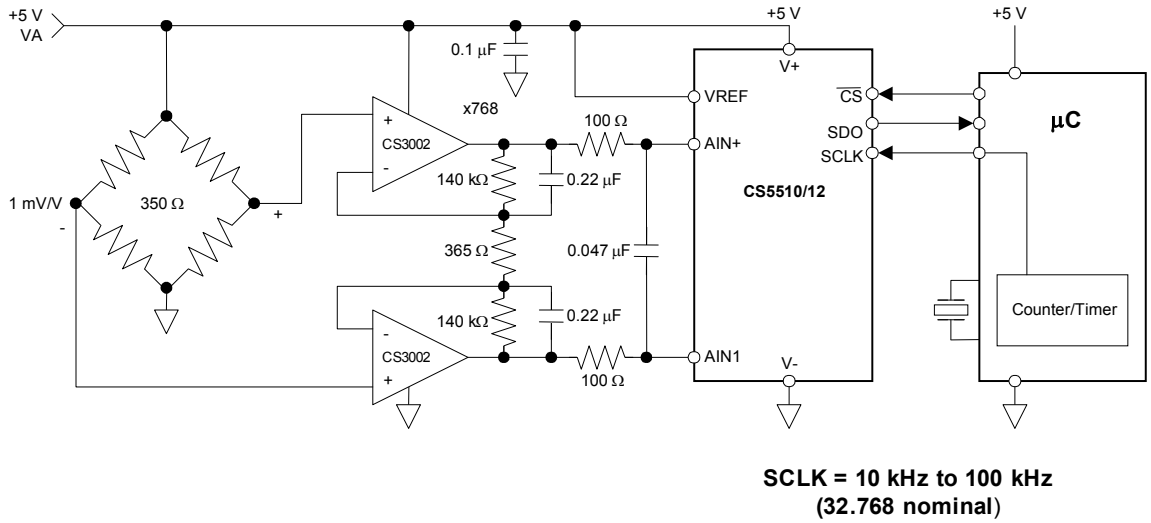
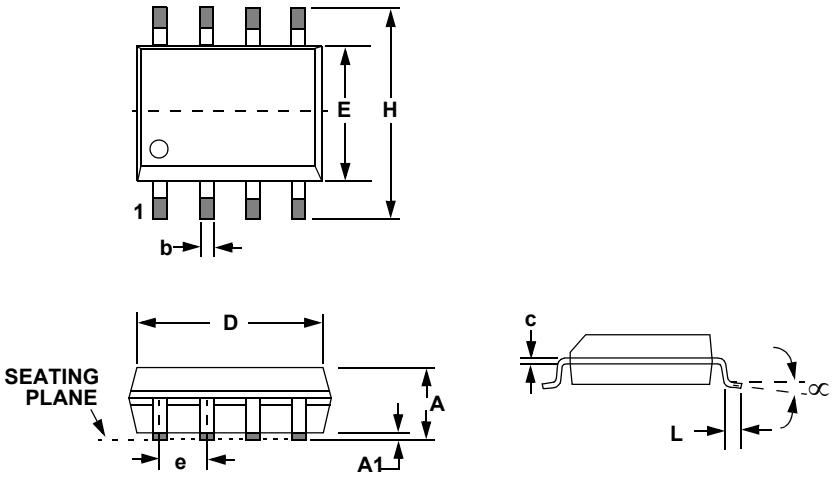


Figure 18. Load Cell Bridge Amplifier and A/D Converter

4. PACKAGE DRAWING

8L SOIC (150 MIL BODY) PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
e	0.040	0.060	1.02	1.52
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
∝	0°	8°	0°	8°

JEDEC #: MS-012

5. ORDERING INFORMATION

Model	Container	Temperature	Package
CS3002-ISZ (lead free)	Bulk	-40 to +85 °C	8-pin SOIC (Lead Free)
CS3002-ISZR (lead free)	Tape & Reel		

6. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS3002-ISZ (lead free)	260 °C	2	365 Days

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

7. REVISION HISTORY

Revision	Date	Changes
F3	OCT 2004	Added lead-free device ordering information.
F4	AUG 2005	Added MSL specifications. Updated legal notice. Added leaded (Pb) devices.
F5	AUG 2006	Updated *Typical Performance Plots*.
F6	SEP 2006	Corrected error in Ordering Information section.
F7	NOV 2007	Added additional information regarding open-loop and gain stability compensation.
F8	OCT 2008	Minor, cosmetic correction to caption for Figure 10.
F9	JUL 2009	Removed lead-containing devices from ordering information.
F10	DEC 2012	Removed CS3001 and corrected typographical errors.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find the one nearest to you go to www.cirrus.com

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