CS3301A

Low-noise, Programmable Gain, Differential Amplifier

Features

- Signal Bandwidth: DC to 2 kHz
- Selectable Gain: x1, x2, x4, x8, x16, x32, x64
- Differential Inputs, Differential Outputs
  - Multiplexed inputs: INA, INB, 800Ω termination
  - Rough / fine outputs for CS5371A / 72A / 73A
  - Max signal amplitude: 5 V_{pp} differential
  - Low input bias: 1 nA typical
- Outstanding Noise Performance
  - 8.5 nV/$\sqrt{Hz}$ from 0.1 Hz to 2 kHz
  - 0.180 μV_{p-p} between 0.1 Hz and 10 Hz
- Low Total Harmonic Distortion
  - -121 dB THD typical (0.0000891%)
  - -112 dB THD maximum (0.0002512%)
- Low Power Consumption
  - Normal operation: 5.5 mA typical
  - Power down: 10 µA typical
- Small 24-pin SSOP Package
- Bipolar Power Supply Configuration
  - VA+ = +2.5 V; VA- = -2.5 V; VD = +3.3 V

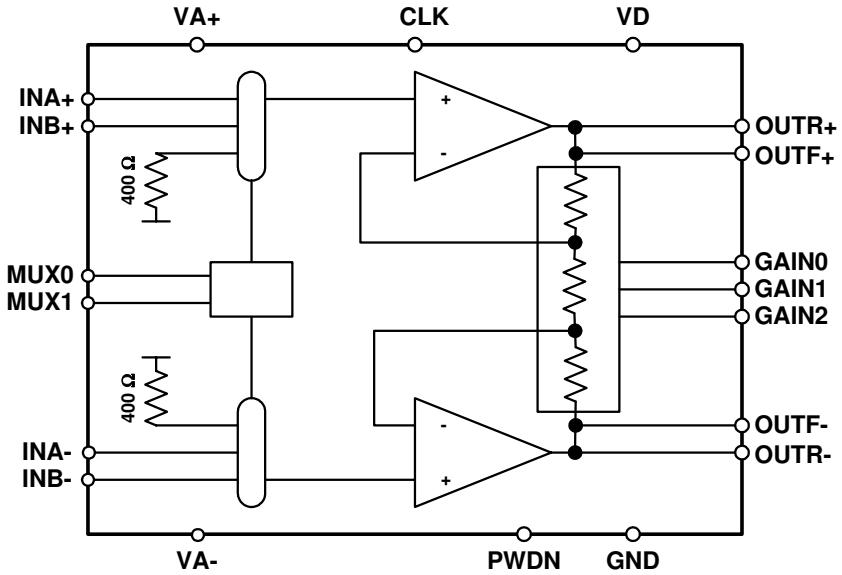
Description

The CS3301A is a low-noise differential input, differential output amplifier with programmable gain, optimized for amplifying signals from low-impedance sensors such as geophones. The gain settings are binary weighted (x1, x2, x4, x8, x16, x32, x64) and are selected using simple pin settings. Two sets of external inputs, INA and INB, simplify system design as inputs from a sensor and test DAC. An internal 800 Ω termination can also be selected for noise tests.

Amplifier noise performance is outstanding with a noise density of 8.5 nV/$\sqrt{Hz}$ over the 0.1 Hz to 2 kHz bandwidth. Distortion performance is also extremely good, typically -121 dB THD at x1 gain. Flat noise down to 0.1 Hz and low total harmonic distortion make this amplifier ideal for low-frequency, low-amplitude, differential signals requiring maximum dynamic range.

ORDERING INFORMATION

See page 15.



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1. CHARACTERISTICS AND SPECIFICATIONS

- Min / Max characteristics and specifications are guaranteed over the Specified Operating Conditions.
- Typical performance characteristics and specifications are measured at nominal supply voltages and T_A = 25°C.
- GND = 0 V. Single-ended voltages with respect to GND, differential voltages with respect to opposite half.
- Device is connected as shown in Figure 5 on page 12 unless otherwise noted.

SPECIFIED OPERATING CONDITIONS

Parameter		Symbol	Min	Nom	Max	Unit
Bipolar Power Supplies						
Positive Analog	± 2%	VA+	2.45	2.50	2.55	V
Negative Analog	(Note 1) ± 2%	VA-	-2.55	-2.50	-2.45	V
Positive Digital	(Note 2) ± 3%	VD	3.20	3.30	3.40	V
Thermal						
Ambient Operating Temperature	Industrial (-IS, -ISZ)	T_A	-40	25	85	°C

Notes: 1. VA- must be the most negative voltage to avoid potential SCR latch-up conditions.
2. VD must conform to Digital Supply Differential under Absolute Maximum Ratings.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Parameter
DC Power Supplies	Positive Analog Negative Analog Digital	VA+ VA- VD	-0.5 -6.8 -0.5	6.8 0.5 6.8	V V V
Analog Supply Differential	[(VA+) - (VA-)]	VA_{DIFF}	-	6.8	V
Digital Supply Differential	[(VD) - (VA-)]	VD_{DIFF}	-	6.8	V
Input Current, Power Supplies	(Note 3)	I_{PWR}	-	±50	mA
Input Current, Any Pin Except Supplies	(Note 3)	I_{IN}	-	±10	mA
Output Current	(Note 3)	I_{OUT}	-	±25	mA
Power Dissipation		PD	-	500	mW
Analog Input Voltages		V_{INA}	(VA-) - 0.5	(VA+) + 0.5	V
Digital Input Voltages		V_{IND}	-0.5	(VD) + 0.5	V
Storage Temperature Range		T_{STG}	-65	150	ºC

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 3. Transient currents up to ±100 mA will not cause SCR latch-up.

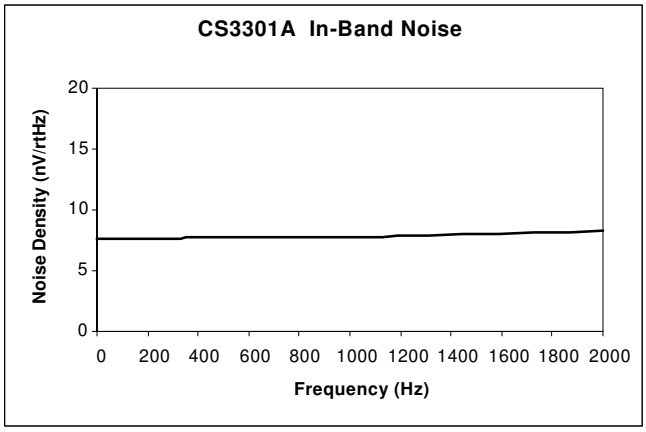
TEMPERATURE CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Operating Temperature	T_A	-40	-	85	ºC
Storage Temperature Range	T_{STR}	-65	-	150	ºC
Allowable Junction Temperature	T_{JCT}	-	-	125	ºC
Junction to Ambient Thermal Impedance	Θ_{JA}	-	65	-	ºC / W

ANALOG CHARACTERISTICS

Parameter		Symbol	CS3301A Min	Typ	Max	Unit
Noise Performance						
Input Voltage Noise	f_0 = 0.1 Hz to 10 Hz	VN_{PP}	-	0.18	0.40	μV_{p-p}
Input Voltage Noise Density	f_0 = 0.1 Hz to 2 kHz	VN_D	-	8.5	12.0	$nV/\sqrt{Hz}$
Input Current Noise Density	(Note 4)	IN_D	-	100	-	$fA/\sqrt{Hz}$
Distortion Performance						
Total Harmonic Distortion (Note 5)	x1	THD	-	-121	-112	dB
	x2		-	-120	-	
	x4		-	-120	-	
	x8		-	-120	-	
	x16		-	-120	-	
	x32		-	-119	-	
	x64		-	-116	-	
Linearity (Note 5)	x1	LIN	-	0.0000891	0.0002512	%
	x2		-	0.0001000	-	
	x4		-	0.0001000	-	
	x8		-	0.0001000	-	
	x16		-	0.0001000	-	
	x32		-	0.0001122	-	
	x64		-	0.0001585	-	

Notes: 4. Guaranteed by design and/or characterization.
5. Tested with a full scale input signal of 31.25 Hz.



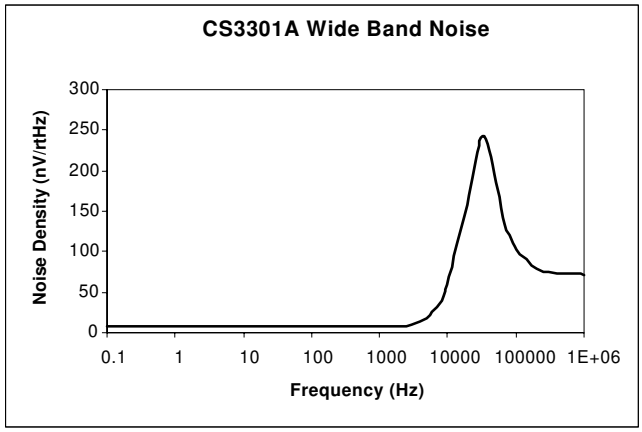


Figure 1. CS3301A Noise Performance

ANALOG CHARACTERISTICS (CONT.)

Parameter			Symbol	CS3301A Min	CS3301A Typ	CS3301A Max	Unit
Gain							
Gain, Differential			GAIN	x1	-	x64	
Gain, Common Mode	(Note 6)		$GAIN_{CM}$	-	x1	-	
Gain Accuracy, Absolute	(Note 7)		$GAIN_{ABS}$	-	±1	±2	%
Gain Accuracy, Relative	(Note 8)	2x	$GAIN_{REL}$	-0.4	-0.2	0	%
		4x		-	-0.2	-	
		8x		-	-0.2	-	
		16x		-	-0.2	-	
		32x		-	-0.3	-	
		64x		-	-0.3	-	
Gain Drift	(Note 4, 9)		$GAIN_{TC}$	-	5	-	ppm / ºC
Offset							
Offset Voltage, Input Referred	(Note 10)		OFST	-	±5	±15	µV
Offset After Calibration, Absolute	(Note 11)		$OFST_{CAL}$	-	±1	-	µV
Offset Calibration Range	(Note 12)		$OFST_{RNG}$	-	100	-	% FS
Offset Voltage Drift	(Note 4, 9)		$OFST_{TC}$	-	0.1	-	µV / ºC

6. Common mode signals pass unchanged through the differential amplifier architecture and are rejected by the CS5371A / 72A / 73A modulator CMRR.
7. Absolute gain accuracy tests the matching of x1 gain across multiple CS3301A devices.
8. Relative gain accuracy tests the tracking of x2, x4, x8, x16, x32, x64 gain relative to x1 gain on a single CS3301A device.
9. Specification is for the parameter over the specified temperature range and is for the CS3301A device only. It does not include the effects of external components.
10. Offset voltage is tested with the amplifier inputs connected to the internal 800 Ω termination.
11. The absolute offset after calibration specification applies to the effective offset voltage of the CS3301A output when used with the CS5371A / 72A / 73A modulator and CS5376A / 78 digital filter, and is measured from the digitally calibrated output codes of the digital filter.
12. The CS3301A offset calibration is performed digitally with the CS5371A / 72A / 73A modulator and CS5376A / 78 digital filter and includes the full scale signal range. Calibration offsets of greater than ± 5% of full scale will begin to subtract from system dynamic range.

ANALOG CHARACTERISTICS (CONT.)

Parameter		Symbol	CS3301A Min	Typ	Max	Unit
Analog Input Characteristics						
Input Signal Frequencies		BW	DC	-	2000	Hz
Input Voltage Range (Vcm ± Signal)	x1 x2 to x64	V_{IN}	(VA-)+0.7 (VA-)+0.7	- -	(VA+)-1.25 (VA+)-1.75	V
Full Scale Input, Differential	x1 x2 x4 x8 x16 x32 x64	V_{INFS}	- - - - - - -	- - - - - - -	5 2.5 1.25 625 312.5 156.25 78.125	V_{p-p} V_{p-p} V_{p-p} mV_{p-p} mV_{p-p} mV_{p-p} mV_{p-p}
Input Impedance, Differential		Z_{INDIFF}	-	1, 50	-	GΩ, pF
Input Impedance, Common Mode		Z_{INCM}	-	1	-	MΩ
Input Bias Current		I_{IN}	-	1	2	nA
Crosstalk, Multiplexed Inputs	(Note 4)	XT	-	-130	-	dB
Common to Differential Mode Rejection	(Note 4, 7, 13)	CDMR	95	120	-	dB
Analog Output Characteristics						
Full Scale Output, Differential		V_{OUT}	-	-	5	V_{p-p}
Output Voltage Range (Vcm ± Signal)		V_{RNG}	(VA-)+0.5	-	(VA+)-0.5	V
Output Impedance	(Note 14)	Z_{OUT}	-	40	-	Ω
Output Impedance Drift	(Note 14)	Z_{TC}	-	0.24	-	Ω/°C
Output Current		I_{OUT}	-	-	±25	mA
Load Capacitance		C_L	-	-	1	nF

Notes: 13. Ratio of input common mode amplitude vs. output differential mode amplitude for a perfectly matched common mode input signal. Characterized with a 50 Hz, 500 mV_{peak} common mode sine wave applied to the analog inputs.

14. Output impedance characteristics are approximate and can vary up to ±30% depending on process parameters.

DIGITAL CHARACTERISTICS

Parameter	Symbol	CS3301A Min	Typ	Max	Unit
Digital Characteristics					
High Level Input Drive Voltage (Note 15)	V_{IH}	0.6*VD	-	VD	V
Low Level Input Drive Voltage (Note 15)	V_{IL}	0.0	-	0.8	V
Input Leakage Current	I_{IN}	-	±1	±10	µA
Digital Input Capacitance	C_{IN}	-	9	-	pF
Rise Times, Digital Inputs Except CLK	t_{RISE}	-	-	100	ns
Fall Times, Digital Inputs Except CLK	t_{FALL}	-	-	100	ns
Master Clock Specifications					
Master Clock Frequency (Note 16)	f_{CLK}	2.0	2.048	2.2	MHz
Master Clock Duty Cycle	f_{DTY}	40	-	60	%
Master Clock Rise Time	t_{RISE}	-	-	25	ns
Master Clock Fall Time	t_{FALL}	-	-	25	ns
Master Clock Jitter (In-Band or Aliased In-Band)	JTR_{IB}	-	-	300	ps
Master Clock Jitter (Out-of-Band)	JTR_{OB}	-	-	1	ns

Notes: 15. Device is intended to be driven with CMOS logic levels.

16. When CLK is tied to GND, an internal oscillator provides a master clock at approximately 2 MHz. CLK should be driven for synchronous system operation.

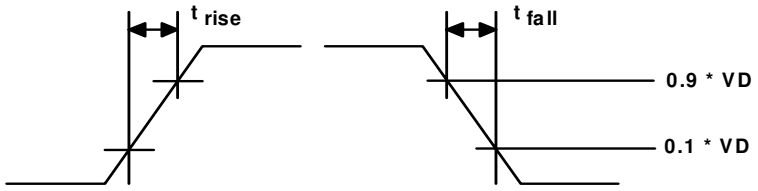


Figure 2. Digital Input Rise and Fall Times

Input Selection	MUX1	MUX0
800 Ω termination	0	0
INA only	1	0
INB only	0	1
INA + INB	1	1

Gain Selection	GAIN2	GAIN1	GAIN0
x1	0	0	0
x2	0	0	1
x4	0	1	0
x8	0	1	1
x16	1	0	0
x32	1	0	1
x64	1	1	0
reserved	1	1	1

Table 1. Digital Selections for Gain and Input Mux Control

POWER SUPPLY CHARACTERISTICS

Parameter	Symbol	CS3301A Min	Typ	Max	Unit
Power Supply Current, Normal					
Analog Power Supply Current (Note 17)	I_A	-	5.5	6.8	mA
Digital Power Supply Current (Note 17)	I_D	-	0.2	0.25	mA
Power Supply Current, Power Down (PWDN=1)					
Analog Power Supply Current (Note 17)	I_A	-	8	12	µA
Digital Power Supply Current (Note 17)	I_D	-	2	8	µA
Power Supply Rejection					
Power Supply Rejection Ratio (Note 4, 18)	PSRR	100	120	-	dB

Notes: 17. All outputs unloaded. Analog inputs connected to the internal 800 Ω termination. Digital inputs forced to VD or GND respectively.

18. Power supply rejection characterized with a 50 Hz, 400 mVp-p sine wave applied separately to each supply.

2. GENERAL DESCRIPTION

The CS3301A is a low-noise chopper-stabilized CMOS differential input, differential output amplifier for precision analog signals between DC and 2 kHz. It has multiplexed inputs, rough / fine outputs and programmable gains of x1, x2, x4, x8, x16, x32, and x64.

The amplifier's performance makes it ideal for low-frequency, high dynamic range applications requiring low distortion and minimal power consumption. It's optimized for use in acquisition systems designed around the CS5371A/72A single/dual ΔΣ modulators and the CS5376A quad digital filter or the CS5373A ΔΣ modulator and CS5378 digital filter.

Figure 3 on page 9 shows the system architecture of a 4-channel acquisition system using four CS3301A, two CS5372A, one CS4373A, and one CS5376A. Figure 4 on page 10 shows the system architecture of a single channel acquisition system using a CS3301A, CS5373A, and CS5378.

2.1 Analog Signals

2.1.1 Analog Inputs

The amplifier analog inputs are designed for differential sensors. Input multiplexing simplifies system connections by providing separate inputs for a sensor and test DAC (INA, INB) as well as an internal termination for noise tests. The MUX0, MUX1 digital pins determine which multiplexed input is connected to the amplifier.

2.1.2 Analog Outputs

The amplifier analog outputs are separated into rough charge / fine charge signals to easily connect to the CS5371A/72A/73A modulator inputs. Each differential output requires two series resistors and a differential capacitor to create the modulator anti-alias RC filter.

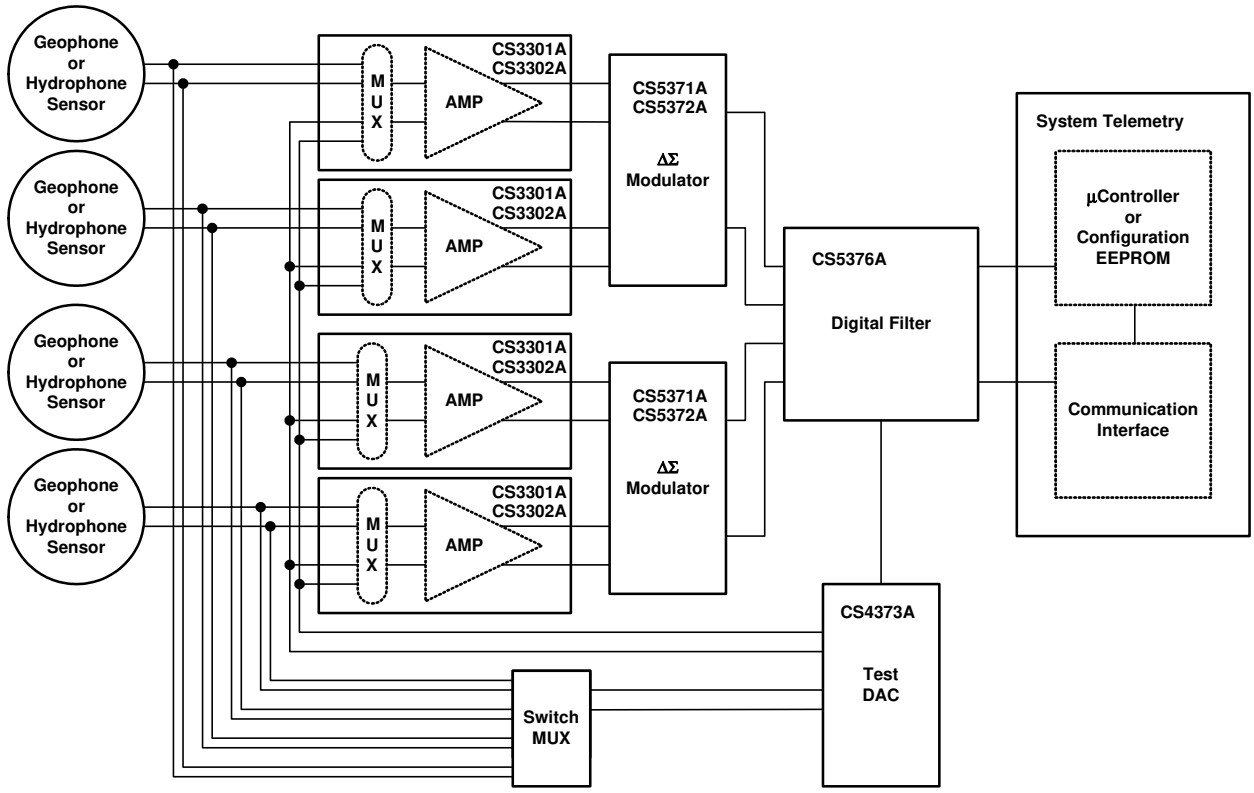


Figure 3. Multi-Channel System Architecture

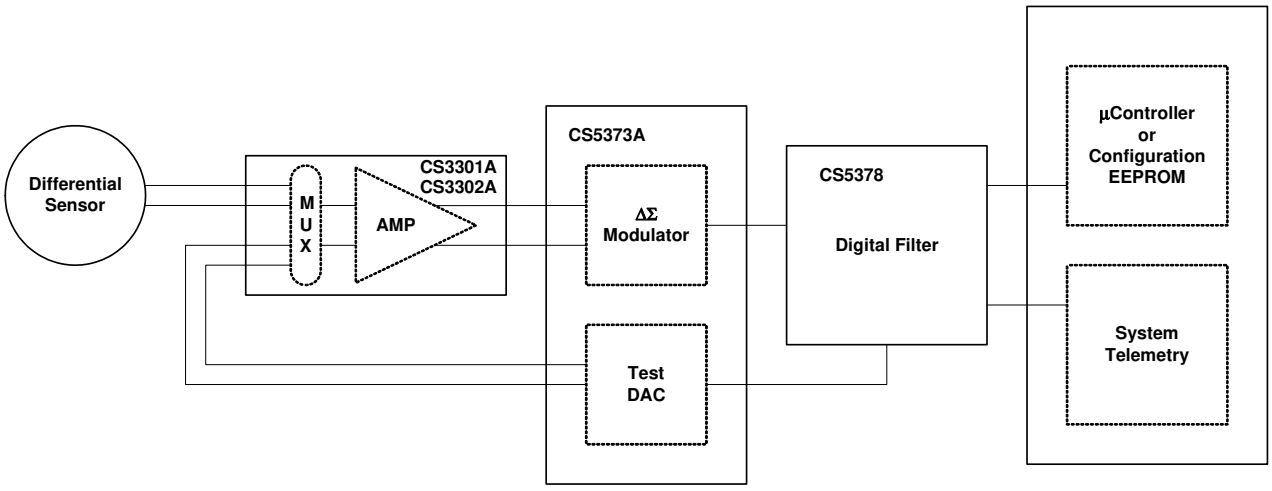


Figure 4. Single-Channel System Architecture

2.1.3 Differential Signals

Analog signals into and out of the CS3301A are differential, consisting of two halves with equal but opposite magnitude varying about a common mode voltage.

A full scale 5 Vpp differential signal centered on a -0.15 V common mode can have:

SIG+ = -0.15 V + 1.25 V = 1.1 V

SIG- = -0.15 V - 1.25 V = -1.4 V

SIG+ is +2.5 V relative to SIG-

For the reverse case:

SIG+ = -0.15 V - 1.25 V = -1.4 V

SIG- = -0.15 V + 1.25 V = 1.1 V

SIG+ is -2.5 V relative to SIG-

The total swing for SIG+ relative to SIG- is (+2.5 V) - (-2.5 V) = 5 V_{pp}. A similar calculation can be done for SIG- relative to SIG+. Note that a 5 V_{pp} differential signal centered on a -0.15 V common mode voltage never exceeds 1.1 V and never drops below -1.4 V on either half of the signal.

By definition, differential voltages are to be measured with respect to the opposite half, not relative to ground. A multimeter differentially measuring between SIG+ and SIG- in this example would properly read 1.767 V_{rms}, or 5 V_{pp}.

2.2 Digital Signals

2.2.1 Clock Input

The clock signal is used by the chopper-stabilization circuitry of the amplifier analog inputs. The CLK pin can be driven by an external clock source for synchronous operation, or CLK can be grounded to run from its own internally generated clock signal. The CLK pin is connected to a clock detect circuit which will disable the internal clock and use an external clock if one is supplied. If the internal clock signal is to be used, the CLK pin should be connected to GND.

2.2.2 Gain Selection

The CS3301A supports gain ranges of x1, x2, x4, x8, x16, x32, and x64. They are selected using the GAIN0, GAIN1, and GAIN2 pins as shown in Table 1 on page 7.

2.2.3 Mux Selection

The analog inputs to the amplifier are multiplexed, with external signals applied to the INA+, INA- or INB+, INB- pins. An internal termination is also available for noise tests. Input mux selection is

made using the MUX0 and MUX1 pins as shown in Table 1 on page 7.

Although a mux selection is provided to enable the INA and INB switches simultaneously, signal current should not be driven through them in this mode. The CS3301A mux switches will maintain good linearity only with minimal signal currents.

2.2.4 Power Down Selection

A power-down mode is available to shut down the amplifier when not in use. When enabled, all internal circuitry is disabled, the analog inputs and outputs go high-impedance, and the device enters a micro-power state. Power down mode is selected using the PWDN pin, which is active high.

2.3 Power Supplies

2.3.1 Analog Power Supplies

The analog power pins of the CS3301A are specified to run from bipolar ±2.5 V power supplies. When using bipolar power supplies, the analog signal common mode voltage should be biased to 0 V. The analog power supplies are recommended to be bypassed to system ground using 0.1 µF X7R type capacitors.

The VA- supply is connected to the CMOS substrate and as such must remain the most negative applied voltage. It is recommended to clamp the VA- supply to system ground using a reversed biased Schottky diode to prevent possible damage related to mis-matched power supply initialization.

2.3.2 Digital Power Supplies

The digital voltage across the VD and GND pins is specified for a +3.3 V power supply. The digital power supply should be bypassed to system ground using a 0.01 µF X7R type capacitor.

2.4 Connection Diagram

Figure 5 on page 12 shows a connection diagram for the CS3301A amplifier when used with the CS5372A dual ΔΣ modulator, the CS4373A Test DAC, and the CS5376A digital filter. The diagram shows differential sensors and test DAC inputs, and analog outputs with anti-alias RC components; power supply connections including recommended bypassing; and digital control connections back to the CS5376A GPIO pins.

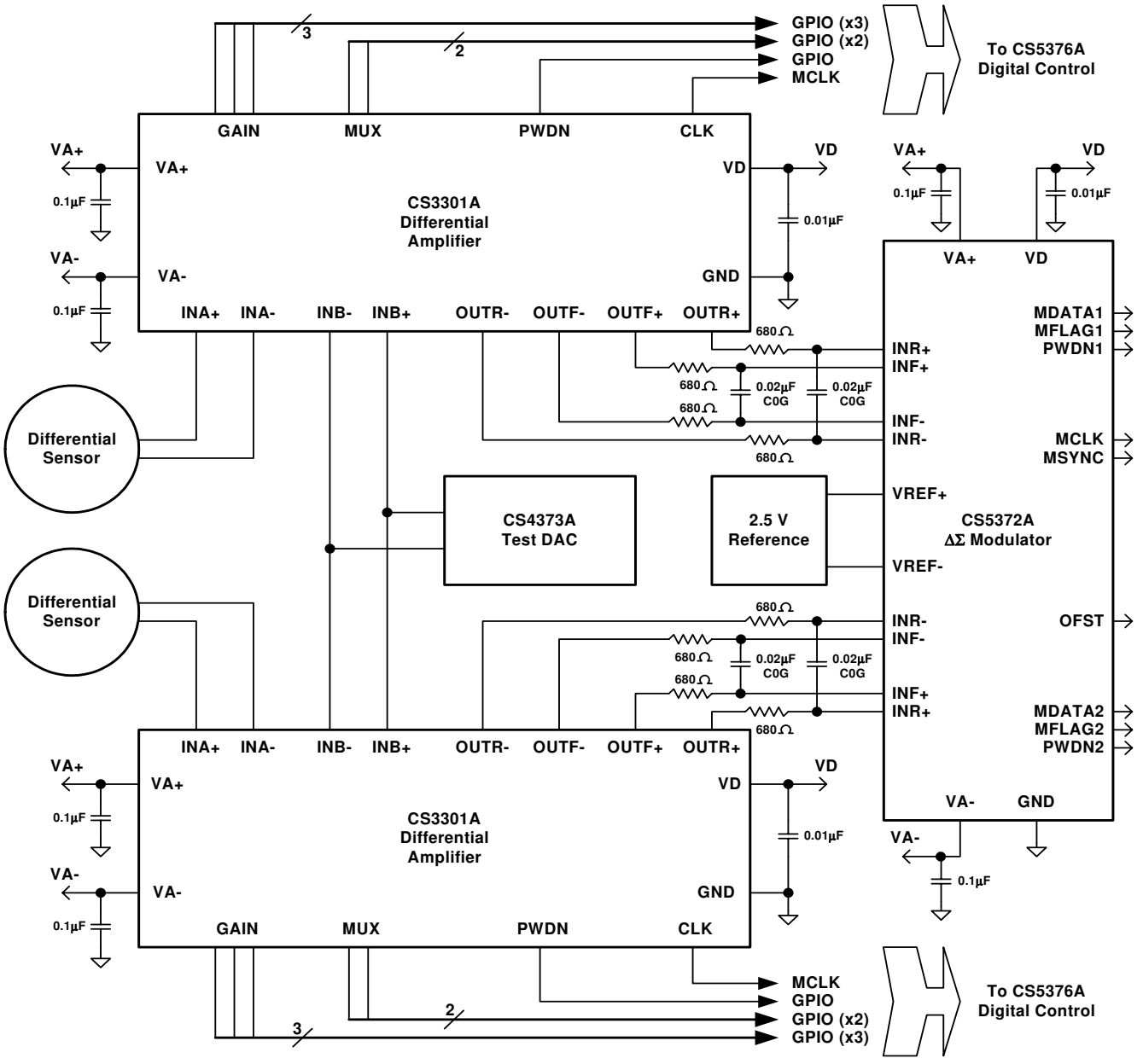


Figure 5. CS3301A Amplifier Connections

3. PIN DESCRIPTION

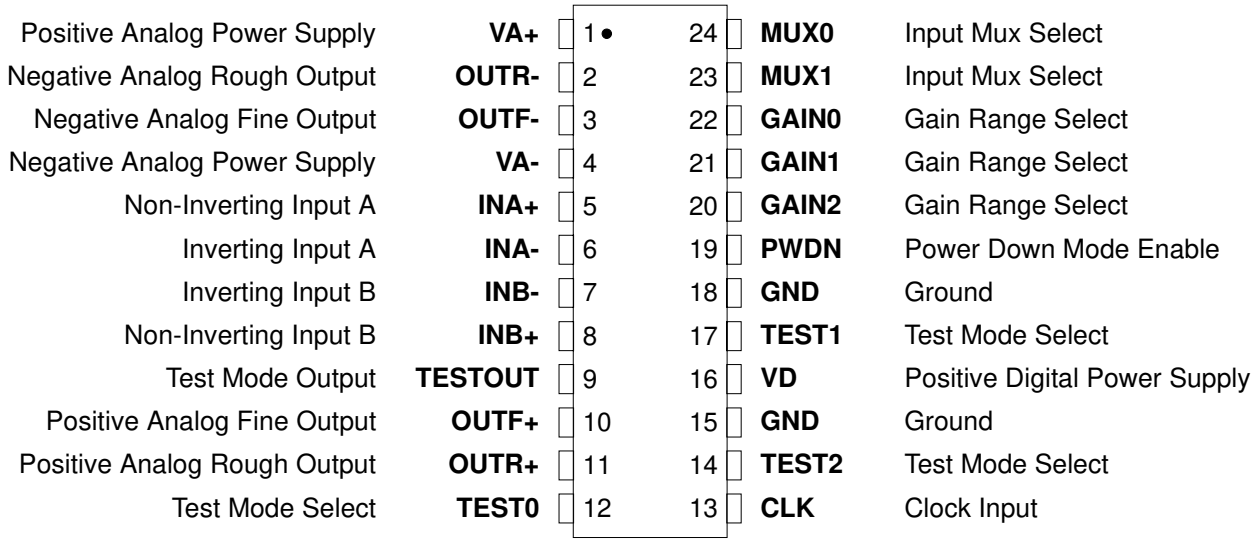


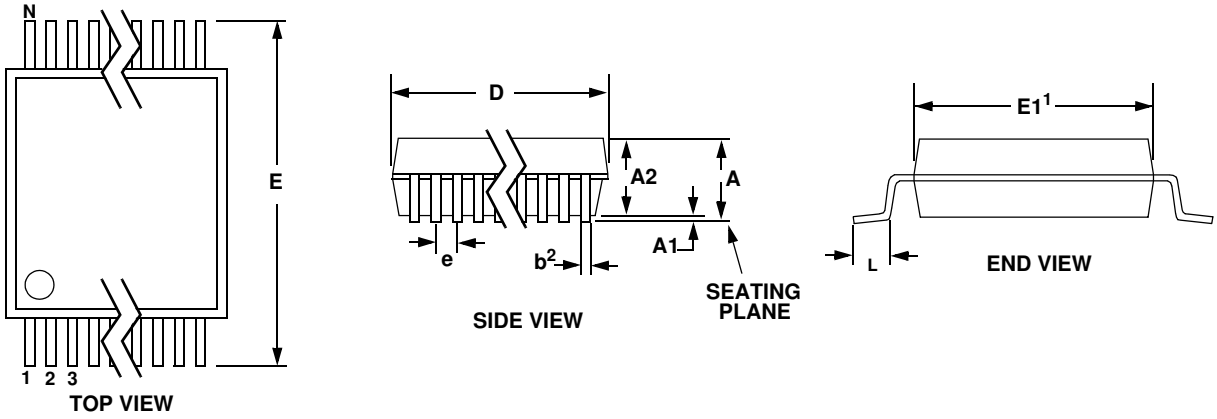
Figure 6. CS3301A Pin Assignments

Pin Name	Pin #	I/O	Pin Description
VA+	1	I	Positive analog supply voltage.
VA-	4	I	Negative analog supply voltage.
VD	16	I	Positive digital supply voltage.
GND	15, 18	I	Ground.
INA+, INA-	5, 6	I	Channel A differential analog inputs. Selected via MUX pins.
INB+, INB-	8, 7	I	Channel B differential analog inputs. Selected via MUX pins.
OUTR+, OUTR-	11, 2	O	Rough charge differential analog outputs.
OUTF+, OUTF-	10, 3	O	Fine charge differential analog outputs.
GAIN0, GAIN1, GAIN2	22, 21, 20	I	Gain range select. See Gain Selection table in Digital Characteristics section.
CLK	13	I	Master clock input. Connect to GND to use internal oscillator.
PWDN	19	I	Power down mode enable. Active high.
MUX0, MUX1	24, 23	I	Analog input select. See Input Selection table in Digital Characteristics section.
TEST0	12	I	Test mode select, factory use only. Connect to VA- during normal operation.
TEST1, TEST2	17, 14	I	Test mode select, factory use only. Connect to GND during normal operation.
TESTOUT	9	O	Test mode output, factory use only. No connect during normal operation.

Table 2. Pin Descriptions

4. PACKAGE DIMENSIONS

24 PIN SSOP PACKAGE DRAWING



	INCHES		MILLIMETERS		NOTE
DIM	MIN	MAX	MIN	MAX	
A	--	0.084	--	2.13	
A1	0.002	0.010	0.05	0.25	
A2	0.064	0.074	1.62	1.88	
b	0.009	0.015	0.22	0.38	2,3
D	0.311	0.335	7.90	8.50	1
E	0.291	0.323	7.40	8.20	
E1	0.197	0.220	5.00	5.60	1
e	0.024	0.027	0.61	0.69	
L	0.025	0.040	0.63	1.03	
∝	0°	8°	0°	8°	

Notes: 1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

5. ORDERING INFORMATION

Model	Temperature	Package
CS3301A-IS	-40 to +85 °C	24-pin SSOP
CS3301A-ISZ (lead free)		

6. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS3301A-IS	240 °C	2	365 Days
CS3301A-ISZ (lead free)	260 °C	3	7 Days

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

7. REVISION HISTORY

Revision	Date	Changes
PP1	FEB 2007	Preliminary release.
F1	MAR 2007	Updated to final for QPL (Quality Process Level).

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
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