CS42435

108 dB, 192 kHz 4-In, 8-Out TDM CODEC

FEATURES

- Four 24-bit A/D, Eight 24-bit D/A Converters
- ADC Dynamic Range
  - 105 dB Differential
  - 102 dB Single-Ended
- DAC Dynamic Range
  - 108 dB Differential
  - 105 dB Single-Ended
- ADC/DAC THD+N
  - -98 dB Differential
  - -95 dB Single-Ended
- Compatible with Industry-Standard Time Division Multiplexed (TDM) Serial Interface
- DAC Sampling Rates up to 192 kHz
- ADC Sampling Rates up to 96 kHz
- Programmable ADC High-Pass Filter for DC Offset Calibration
- Logarithmic Digital Volume Control
- Hardware Mode or Software I²C™ & SPI™
- Supports Logic Levels Between 5 V and 1.8 V

GENERAL DESCRIPTION

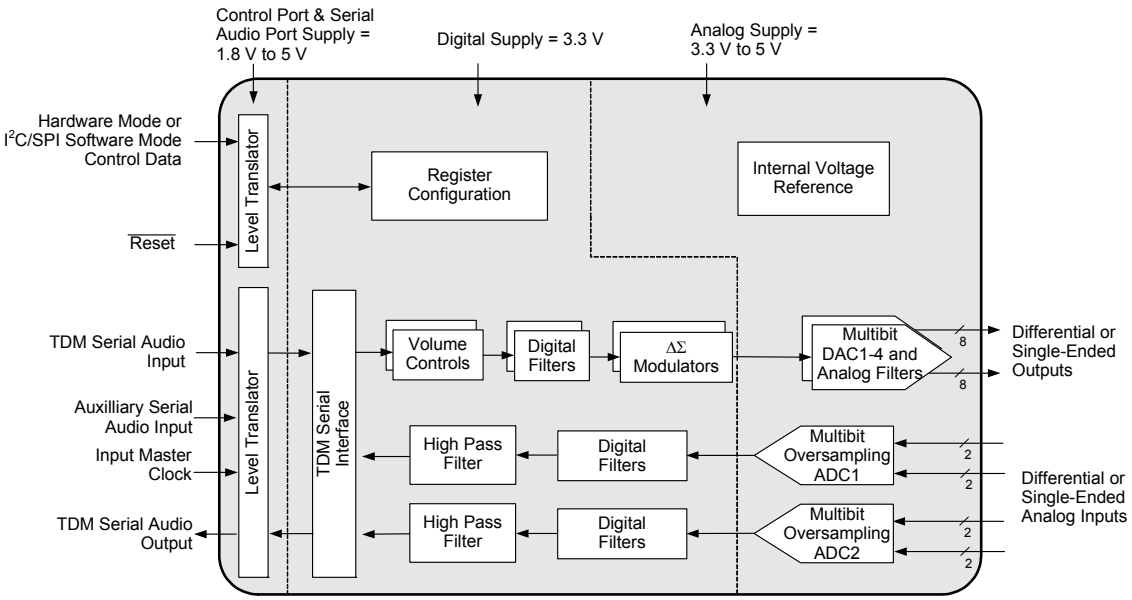
The CS42435 CODEC provides four multi-bit analog-to-digital and eight multi-bit digital-to-analog delta-sigma converters. The CODEC is capable of operation with either differential or single-ended inputs and outputs, in a 52-pin MQFP package.

Four fully differential, or single-ended, inputs are available on stereo ADC1 and ADC2. Digital volume control is provided for each ADC channel, with selectable overflow detection. An auxiliary serial input is available for an additional two channels of PCM data.

All eight DAC channels provide digital volume control and can operate with differential or single-ended outputs.

The CS42435 is available in a 52-pin MQFP package in Commercial (-40°C to +85°C) and Automotive (-40°C to +105°C) grades. The CDB42438 Customer Demonstration Board is also available for device evaluation and implementation suggestions. Please refer to "Ordering Information" on page 57 for complete ordering information.

The CS42435 is ideal for audio systems requiring wide dynamic range, negligible distortion and low noise, such as A/V receivers, DVD receivers, and automotive audio systems.



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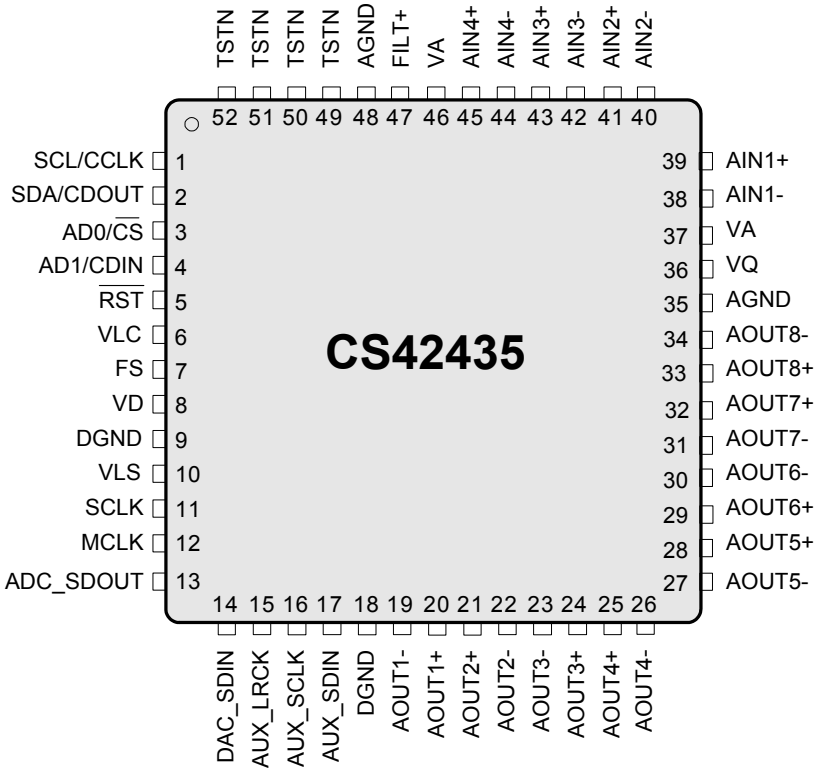
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1. PIN DESCRIPTIONS - SOFTWARE MODE



Pin Name	#	Pin Description
SCL/CCLK	1	**Serial Control Port Clock** (*Input*) - Serial clock for the control port interface.
SDA/CDOUT	2	**Serial Control Data I/O** (*Input/Output*) - Input/Output for I²C data. Output for SPI data.
AD0/$\overline{CS}$	3	**Address Bit [0]/ Chip Select** (*Input*) - Chip address bit in I²C Mode. Control signal used to select the chip in SPI Mode.
AD1/CDIN	4	**Address Bit [1]/ SPI Data Input** (*Input*) - Chip address bit in I²C Mode. Input for SPI data.
$\overline{RST}$	5	**$\overline{Reset}$** (*Input*) - The device enters a low-power mode and all internal registers are reset to their default settings when low.
VLC	6	**Control Port Power** (*Input*) **-** Determines the required signal level for the control port interface. See "Digital I/O Pin Characteristics" on page 8.
FS	7	**Frame Sync** (*Input*) - Signals the start of a new TDM frame in the TDM digital interface format.
VD	8	**Digital Power** (*Input*) - Positive power supply for the digital section.
DGND	9,18	**Digital Ground** (*Input*) - Ground reference for the digital section.
VLS	10	**Serial Port Interface Power** (*Input*) - Determines the required signal level for the serial port interfaces. See "Digital I/O Pin Characteristics" on page 8.
SCLK	11	**Serial Clock** *(Input)* - Serial clock for the serial audio interface. Input frequency must be 256 x Fs.
MCLK	12	**Master Clock** (*Input*) - Clock source for the delta-sigma modulators and digital filters.
ADC_SDOUT	13	**Serial Audio Data Output** *(Output)* - TDM output for two's complement serial audio data.
DAC_SDIN	14	**DAC Serial Audio Data Input** (*Input*) - TDM Input for two's complement serial audio data.
AUX_LRCK	15	**Auxiliary Left/Right Clock** (*Output*) - Determines which channel, Left or Right, is currently active on the Auxiliary serial audio data line.

AUX_SCLK	16	**Auxiliary Serial Clock** *(Output)* - Serial clock for the Auxiliary serial audio interface.
AUX_SDIN	17	**Auxiliary Serial Input** (*Input*) - The CS42435 provides an additional serial input for two's complement serial audio data.
AOUT1 +,- AOUT2 +,- AOUT3 +,- AOUT4 +,- AOUT5 +,- AOUT6 +,- AOUT7 +,- AOUT8 +,-	20,19 21,22 24,23 25,26 28,27 29,30 32,31 33,34	**Differential Analog Output** (*Output*) - The full-scale differential analog output level is specified in the Analog Characteristics specification table. Each positive leg of the differential outputs may also be used single-ended.
TSTN	49,50 51,52	**Test In** - These pins are inputs used for test purposes only. They must be tied to ground for normal operation.
AGND	35,48	**Analog Ground** (*Input*) - Ground reference for the analog section.
VQ	36	**Quiescent Voltage** (*Output*) **-** Filter connection for internal quiescent reference voltage.
VA	37,46	**Analog Power** (*Input*) - Positive power supply for the analog section.
AIN1 +,- AIN2 +,- AIN3 +,- AIN4 +,-	39,38 41,40 43,42 45,44	**Differential Analog Input** (*Input*) - Signals are presented differentially to the delta-sigma modulators. The full-scale input level is specified in the Analog Characteristics specification table.
FILT+	47	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits.

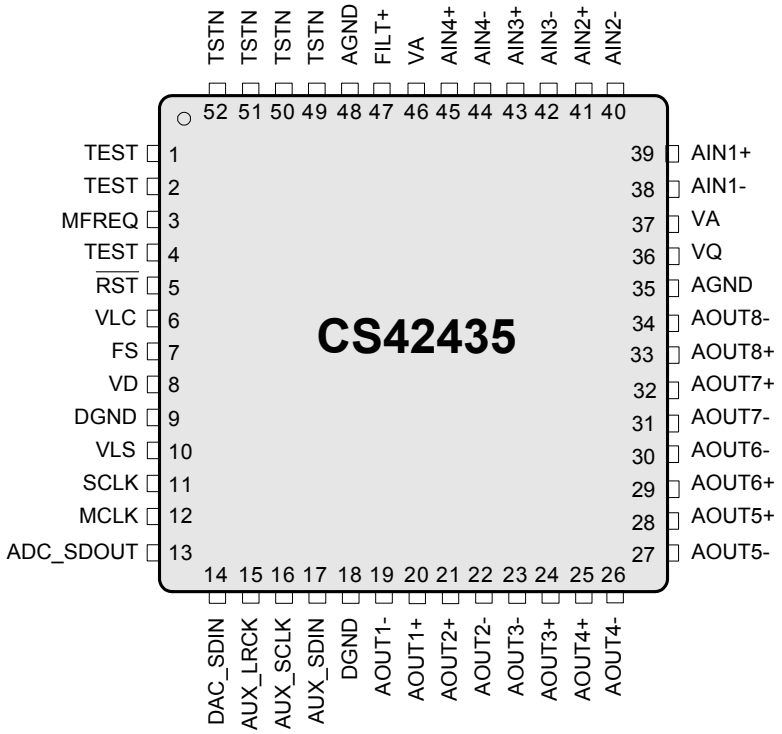
1.1 Digital I/O Pin Characteristics

Various pins on the CS42435 are powered from separate power supply rails. The logic level for each input should adhere to the corresponding power rail and should not exceed the maximum ratings.

Power Rail	Pin Name SW/(HW)	I/O	Driver	Receiver
VLC	$\overline{\text{RST}}$	Input	-	1.8 V - 5.0 V, CMOS
	SCL/CCLK (TEST)	Input	-	1.8 V - 5.0 V, CMOS, with Hysteresis
	SDA/CDOUT (TEST)	Input/ Output	1.8 V - 5.0 V, CMOS/Open Drain	1.8 V - 5.0 V, CMOS, with Hysteresis
	AD0/$\overline{\text{CS}}$ (MFREQ)	Input	-	1.8 V - 5.0 V, CMOS
	AD1/CDIN (TEST)	Input	-	1.8 V - 5.0 V, CMOS
VLS	MCLK	Input	-	1.8 V - 5.0 V, CMOS
	LRCK	Input	-	1.8 V - 5.0 V, CMOS
	SCLK	Input	-	1.8 V - 5.0 V, CMOS
	ADC_SDOUT	Input/ Output	1.8 V - 5.0 V, CMOS	-
	DAC_SDIN	Input	-	1.8 V - 5.0 V, CMOS
	AUX_LRCK	Output	1.8 V - 5.0 V, CMOS	-
	AUX_SCLK	Output	1.8 V - 5.0 V, CMOS	-
	AUX_SDIN	Input	-	1.8 V - 5.0 V, CMOS

Table 1. I/O Power Rails

2. PIN DESCRIPTIONS - HARDWARE MODE



Pin Name	#	Pin Description
TEST	1,2,4	**Test** - These pins are inputs used for test purposes only. They must be tied high or low.
MFREQ	3	**MCLK Frequency** (*Input*) - Sets the required frequency range of the input master clock.
$\overline{\text{RST}}$	5	**$\overline{\text{Reset}}$** (*Input*) - The device enters a low-power mode and all internal registers are reset to their default settings when low.
VLC	6	**Control Port Power** (*Input*) **-** Determines the required signal level for the control port interface. See "Digital I/O Pin Characteristics" on page 8.
FS	7	**Frame Sync** (*Input*) - Signals the start of a new TDM frame in the TDM digital interface format.
VD	8	**Digital Power** (*Input*) - Positive power supply for the digital section.
DGND	9,18	**Digital Ground** (*Input*) - Ground reference for the digital section.
VLS	10	**Serial Port Interface Power** (*Input*) - Determines the required signal level for the serial port interfaces. See "Digital I/O Pin Characteristics" on page 8.
SCLK	11	**Serial Clock** *(Input)* - Serial clock for the serial audio interface. Input frequency must be 256 x Fs.
MCLK	12	**Master Clock** (*Input*) - Clock source for the delta-sigma modulators and digital filters.
ADC_SDOUT	13	**Serial Audio Data Output** *(Output)* - TDM output for two's complement serial audio data.
DAC_SDIN	14	**DAC Serial Audio Data Input** (*Input*) - TDM Input for two's complement serial audio data.
AUX_LRCK	15	**Auxiliary Left/Right Clock** (*Output*) - Determines which channel, Left or Right, is currently active on the Auxiliary serial audio data line.
AUX_SCLK	16	**Auxiliary Serial Clock** *(Output)* - Serial clock for the Auxiliary serial audio interface.
AUX_SDIN	17	**Auxiliary Serial Input** (*Input*) - The CS42435 provides an additional serial input for two's complement serial audio data.

AOUT1 +,- AOUT2 +,- AOUT3 +,- AOUT4 +,- AOUT5 +,- AOUT6 +,- AOUT7 +,- AOUT8 +,-	20,19 21,22 24,23 25,26 28,27 29,30 32,31 33,34	**Differential Analog Output** (*Output*) - The full-scale differential analog output level is specified in the Analog Characteristics specification table. Each positive leg of the differential outputs may also be used single-ended.
AGND	35,48	**Analog Ground** (*Input*) - Ground reference for the analog section.
VQ	36	**Quiescent Voltage** (*Output*) **-** Filter connection for internal quiescent reference voltage.
VA	37,46	**Analog Power** (*Input*) - Positive power supply for the analog section.
AIN1 +,- AIN2 +,- AIN3 +,- AIN4 +,-	39,38 41,40 43,42 45,44	**Differential Analog Input** (*Input*) - Signals are presented differentially to the delta-sigma modulators. The full-scale input level is specified in the Analog Characteristics specification table.
FILT+	47	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits.
TSTN	49,50 51,52	**Test In** - These pins are inputs used for test purposes only. They must be tied to ground for normal operation.

3. TYPICAL CONNECTION DIAGRAMS

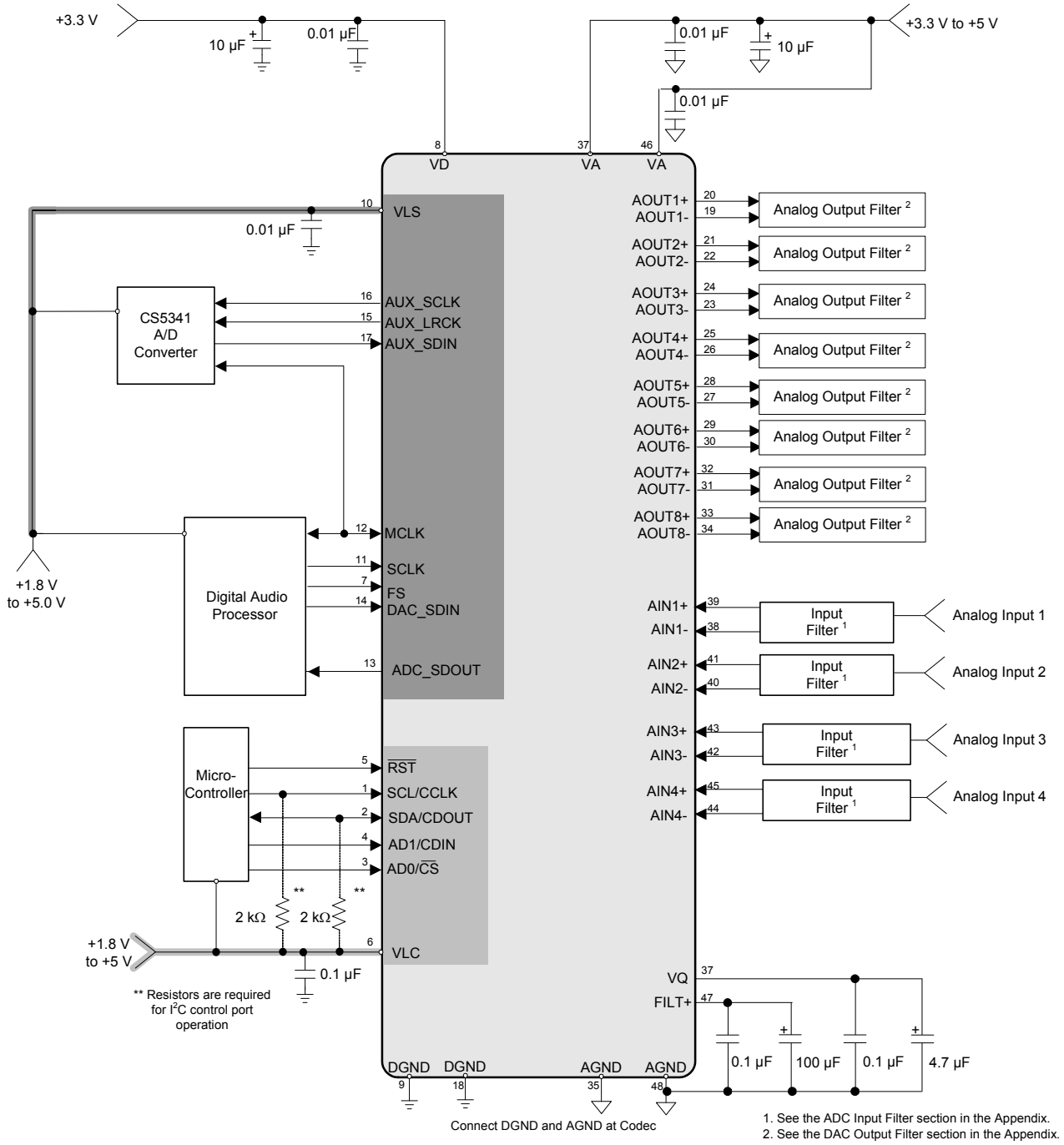


Figure 1. Typical Connection Diagram (Software Mode)

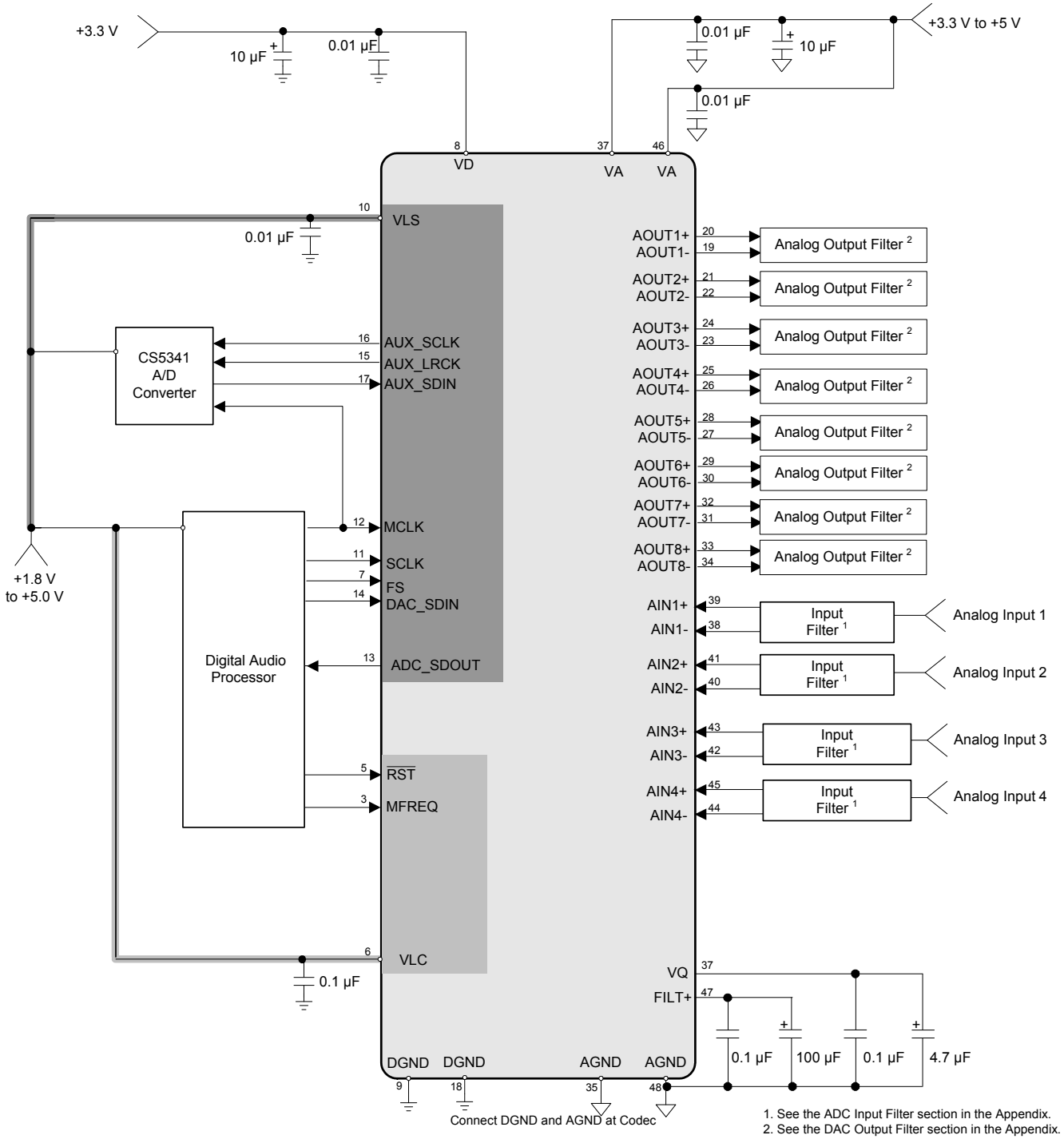


Figure 2. Typical Connection Diagram (Hardware Mode)

4. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

(AGND=DGND=0 V, all voltages with respect to ground.)

Parameters		Symbol	Min	Max	Units
DC Power Supply					
Analog	(Note 1)	VA	3.14	5.25	V
Digital		VD	3.14	3.47	V
Serial Audio Interface	(Note 2)	VLS	1.71	5.25	V
Control Port Interface		VLC	1.71	5.25	V
Ambient Temperature					
Commercial Automotive	-CMZ -DMZ	T_A	-40 -40	+85 +105	°C °C

ABSOLUTE MAXIMUM RATINGS

(AGND = DGND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Max	Units
DC Power Supply	Analog	VA	-0.3	6.0	V
	Digital	VD	-0.3	6.0	V
	Serial Port Interface	VLS	-0.3	6.0	V
	Control Port Interface	VLC	-0.3	6.0	V
Input Current	(Note 3)	I_{in}	-	±10	mA
Analog Input Voltage	(Note 4)	V_{IN}	AGND-0.7	VA+0.7	V
Digital Input Voltage (Note 4)	Serial Port Interface	V_{IND-S}	-0.3	VLS+ 0.4	V
	Control Port Interface	V_{IND-C}	-0.3	VLC+ 0.4	V
Ambient Operating Temperature (power applied)		T_A	-50	+125	°C
Storage Temperature		T_{stg}	-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:

1. Typical Analog input/output performance will slightly degrade at VA = 3.3 V.
2. The ADC_SDOUT may not meet timing requirements in Double-Speed Mode.
3. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.
4. The maximum over/under voltage is limited by the input current.

ANALOG INPUT CHARACTERISTICS (COMMERCIAL)

(Test Conditions (unless otherwise specified): VA = 5 V, VD = VLS = VLC = 3.3 V, and TA = 25°C. Full-scale input sine wave: 1 kHz through the active input filter in Figure 20 on page 48 and Figure 20 on page 48; Measurement Bandwidth is 10 Hz to 20 kHz.)

Parameter		Differential			Single-Ended			Unit
		Min	Typ	Max	Min	Typ	Max	
Fs=48 kHz, 96 kHz								
Dynamic Range	A-weighted	99	105	-	96	102	-	dB
	unweighted	96	102	-	93	99	-	dB
40 kHz bandwidth	unweighted	-	99	-		96	-	dB
Total Harmonic Distortion + Noise	-1 dB	-	-98	-92	-	-95	-89	dB
(Note 5)	-20 dB	-	-82	-	-	-79	-	dB
	-60 dB	-	-42	-	-	-39	-	dB
40 kHz bandwidth	-1 dB	-	-90	-	-	-90	-	dB
ADC1-2 Interchannel Isolation		-	90	-	-	90	-	dB
DC Accuracy								
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Analog Input								
Full-Scale Input Voltage		1.06*VA	1.12*VA	1.18*VA	0.53*VA	0.56*VA	0.59*VA	Vpp
Differential Input Impedance (Note 6)		23	29	32	-	-	-	kΩ
Single-Ended Input Impedance (Note 7)		-	-	-	23	29	32	kΩ
Common Mode Rejection Ratio (CMRR)		-	82	-	-	-	-	dB

ANALOG INPUT CHARACTERISTICS (AUTOMOTIVE)

(Test Conditions (unless otherwise specified): VA = 5 V±5%, VD = VLS = VLC = 3.3 V±5% and TA = -40° to +85°C. Full-scale input sine wave: 1 kHz through the active input filter in Figure 20 on page 48 and Figure 19 on page 48; Measurement Bandwidth is 10 Hz to 20 kHz.)

Parameter		Differential			Single-Ended			Unit
		Min	Typ	Max	Min	Typ	Max	
Fs=48 kHz, 96 kHz								
Dynamic Range	A-weighted	97	105	-	94	102	-	dB
	unweighted	94	102	-	91	99	-	dB
40 kHz bandwidth	unweighted	-	99	-	-	96	-	dB
Total Harmonic Distortion + Noise	-1 dB	-	-98	-90	-	-95	-87	dB
(Note 5)	-20 dB	-	-82	-	-	-79	-	dB
	-60 dB	-	-42	-	-	-39	-	dB
40 kHz bandwidth	-1 dB	-	-87	-	-	-87	-	dB
ADC1-2 Interchannel Isolation		-	90	-	-	90	-	dB
DC Accuracy								
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Analog Input								
Full-Scale Input Voltage		1.04*VA	1.12*VA	1.20*VA	0.52*VA	0.56*VA	0.60*VA	Vpp
Differential Input Impedance	(Note 6 & 8)	23	29	32	-	-	-	kΩ
Single-Ended Input Impedance	(Note 7 & 8)	-	-	-	23	29	32	kΩ
Common Mode Rejection Ratio (CMRR)		-	82	-	-	-	-	dB

Notes:

5. Referred to the typical full-scale voltage.
6. Measured between AINx+ and AINx-.
7. Measured between AINxx and AGND.
8. The input impedance scales inversely proportionate to the sample rate of the ADC modulator.

ADC DIGITAL FILTER CHARACTERISTICS

Parameter (Notes 9, 10)		Min	Typ	Max	Unit
Single-Speed Mode (Note 10)					
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.4896	Fs
Passband Ripple		-	-	0.08	dB
Stopband		0.5688	-	-	Fs
Stopband Attenuation		70	-	-	dB
Total Group Delay		-	12/Fs	-	s
Double-Speed Mode (Note 10)					
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.4896	Fs
Passband Ripple		-	-	0.16	dB
Stopband		0.5604	-	-	Fs
Stopband Attenuation		69	-	-	dB
Total Group Delay		-	9/Fs	-	s
High-Pass Filter Characteristics					
Frequency Response	-3.0 dB -0.13 dB	-	1 20	- -	Hz Hz
Phase Deviation	@ 20 Hz	-	10	-	Deg
Passband Ripple		-	-	0	dB
Filter Settling Time		-	10^5/Fs	0	s

Notes:

9. Filter response is guaranteed by design.
10. Response is clock-dependent and will scale with Fs. Note that the response plots (Figures 25 to 32) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.

ANALOG OUTPUT CHARACTERISTICS (COMMERCIAL)

(Test Conditions (unless otherwise specified): VA = 5 V, VD = VLS = VLC = 3.3 V, and TA = 25° C. Full-scale 997 Hz output sine wave (see Note 12) into passive filter in Figure 25 on page 51 and active filter in Figure 25 on page 51; Measurement Bandwidth is 10 Hz to 20 kHz.)

Parameter		Differential Min	Differential Typ	Differential Max	Single-Ended Min	Single-Ended Typ	Single-Ended Max	Unit
Fs = 48 kHz, 96 kHz, 192 kHz								
Dynamic Range								
18 to 24-Bit	A-weighted	102	108	-	99	105	-	dB
	unweighted	99	105	-	96	102	-	dB
16-Bit	A-weighted	-	99	-	-	96	-	dB
	unweighted	-	96	-	-	93	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-98	-92	-	-95	-89	dB
	-20 dB	-	-85	-	-	-82	-	dB
	-60 dB	-	-45	-	-	-42	-	dB
16-Bit	0 dB	-	-93	-	-	-90	-	dB
	-20 dB	-	-76	-	-	-73	-	dB
	-60 dB	-	-36		-	-33	-	dB
Interchannel Isolation	(1 kHz)	-	100	-	-	100	-	dB
Analog Output								
Full-Scale Output		1.235•VA	1.300•VA	1.365•VA	0.618•VA	0.650•VA	0.683•VA	Vpp
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Output Impedance		-	100	-	-	100	-	Ω
DC Current draw from an AOUT pin	(Note 11)	-	-	10	-	-	10	µA
AC-Load Resistance (R_L)	(Note 13)	3	-	-	3	-	-	kΩ
Load Capacitance (C_L)	(Note 13)	-	-	100	-	-	100	pF

ANALOG OUTPUT CHARACTERISTICS (AUTOMOTIVE)

(Test Conditions (unless otherwise specified): VA = 5 V±5%, VD = VLS = VLC = 3.3 V±5% and TA = -40 to +85×C. Full-scale 997 Hz output sine wave (see Note 12) in Figure 25 on page 51 and Figure 25 on page 51; Measurement Bandwidth is 10 Hz to 20 kHz.)

Parameter		Differential Min	Differential Typ	Differential Max	Single-Ended Min	Single-Ended Typ	Single-Ended Max	Unit
Fs = 48 kHz, 96 kHz, 192 kHz								
Dynamic Range								
18 to 24-Bit	A-weighted	100	108	-	97	105	-	dB
	unweighted	97	105	-	94	102	-	dB
16-Bit	A-weighted	-	99	-	-	96	-	dB
	unweighted	-	96	-	-	93	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-98	-90	-	-95	-87	dB
	-20 dB	-	-85	-	-	-82	-	dB
	-60 dB	-	-45	-	-	-42	-	dB
16-Bit	0 dB	-	-93	-	-	-90	-	dB
	-20 dB	-	-76	-	-	-73	-	dB
	-60 dB	-	-36	-	-	-33	-	dB
Interchannel Isolation	(1 kHz)	-	100	-	-	100	-	dB
Analog Output								
Full-Scale Output		1.210•VA	1.300•VA	1.392•VA	0.605•VA	0.650•VA	0.696•VA	Vpp
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Output Impedance		-	100	-	-	100	-	Ω
DC Current draw from an AOUT pin (Note 11)		-	-	10	-	-	10	µA
AC-Load Resistance (R_L) (Note 13)		3	-	-	3	-	-	kΩ
Load Capacitance (C_L) (Note 13)		-	-	100	-	-	100	pF

Notes:

11. Guaranteed by design. The DC current draw represents the allowed current draw from the AOUT pin due to typical leakage through the electrolytic DC-blocking capacitors.
12. One LSB of triangular PDF dither is added to data.
13. Guaranteed by design. See Figure 3. R_L and C_L reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. In this circuit topology, C_L will effectively move the dominant pole of the two-pole amp in the output stage. Increasing this value beyond the recommended 100 pF can cause the internal op-amp to become unstable. See "External Filters" on page 48 for a recommended output filter.

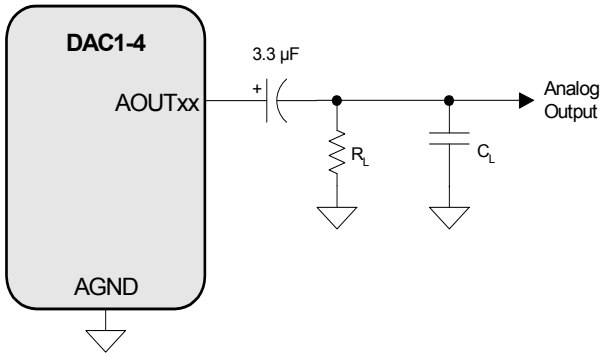


Figure 3. Output Test Circuit for Maximum Load

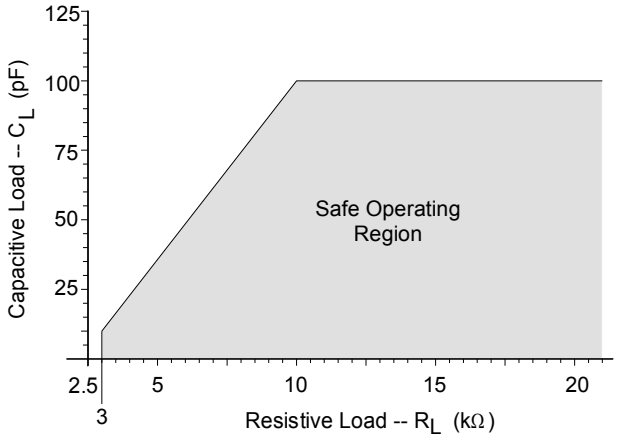


Figure 4. Maximum Loading

COMBINED DAC INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

Parameter (Notes 9, 14)		Min	Typ	Max	Unit
Single-Speed Mode					
Passband (Frequency Response)	to -0.05 dB corner	0	-	0.4780	Fs
	to -3 dB corner	0	-	0.4996	Fs
Frequency Response 10 Hz to 20 kHz		-0.2	-	+0.08	dB
StopBand		0.5465	-	-	Fs
StopBand Attenuation	(Note 15)	50	-	-	dB
Group Delay		-	10/Fs	-	s
De-emphasis Error (Note 16)	Fs = 32 kHz	-	-	+1.5/+0	dB
	Fs = 44.1 kHz	-	-	+0.05/-0.25	dB
	Fs = 48 kHz	-	-	-0.2/-0.4	dB
Double-Speed Mode					
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.4650	Fs
	to -3 dB corner	0	-	0.4982	Fs
Frequency Response 10 Hz to 20 kHz		-0.2	-	+0.7	dB
StopBand		0.5770	-	-	Fs
StopBand Attenuation	(Note 15)	55	-	-	dB
Group Delay		-	5/Fs	-	s
Quad-Speed Mode					
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.397	Fs
	to -3 dB corner	0	-	0.476	Fs
Frequency Response 10 Hz to 20 kHz		-0.2	-	+0.05	dB
StopBand		0.7	-	-	Fs
StopBand Attenuation	(Note 15)	51	-	-	dB
Group Delay		-	2.5/Fs	-	s

Notes:

14. Response is clock-dependent and will scale with Fs. Note that the response plots (Figures 33 to 44) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
15. Single- and Double-Speed Mode Measurement Bandwidth is from Stopband to 3 Fs. Quad-Speed Mode Measurement Bandwidth is from Stopband to 1.34 Fs.
16. De-emphasis is only available in Single-Speed Mode.

SWITCHING SPECIFICATIONS - ADC/DAC PORT

(Inputs: Logic 0 = DGND, Logic 1 = VLS, ADC_SDOUT C_{LOAD} = 15 pF.)

Parameters		Symbol	Min	Max	Units
Slave Mode					
$\overline{\text{RST}}$ pin Low Pulse Width	(Note 17)		1	-	ms
MCLK Frequency			0.512	50	MHz
MCLK Duty Cycle	(Note 18)		45	55	%
Input Sample Rate (FS pin)	Single-Speed Mode	F_s	4	50	kHz
	Double-Speed Mode (Note 19)	F_s	50	100	kHz
	Quad-Speed Mode (Note 20)	F_s	100	200	kHz
SCLK Duty Cycle			45	55	%
SCLK High Time		t_{sckh}	8	-	ns
SCLK Low Time		t_{sckl}	8	-	ns
FS Rising Edge to SCLK Rising Edge		t_{fss}	5	-	ns
SCLK Rising Edge to FS Falling Edge		t_{fsh}	16	-	ns
DAC_SDIN Setup Time Before SCLK Rising Edge		t_{ds}	3	-	ns
DAC_SDIN Hold Time After SCLK Rising Edge		t_{dh}	5	-	ns
DAC_SDIN Hold Time After SCLK Rising Edge		t_{dh1}	5	-	ns
ADC_SDOUT Hold Time After SCLK Rising Edge		t_{dh2}	10	-	ns
ADC_SDOUT Valid Before SCLK Rising Edge		t_{dval}	15	-	ns

Notes:

17. After powering up the CS42435, $\overline{\text{RST}}$ should be held low after the power supplies and clocks are settled.
18. See Table 5 on page 41 for suggested MCLK frequencies.
19. VLS is limited to nominal 2.5 V to 5.0 V operation only.
20. ADC does not meet timing specification for Quad-Speed Mode.

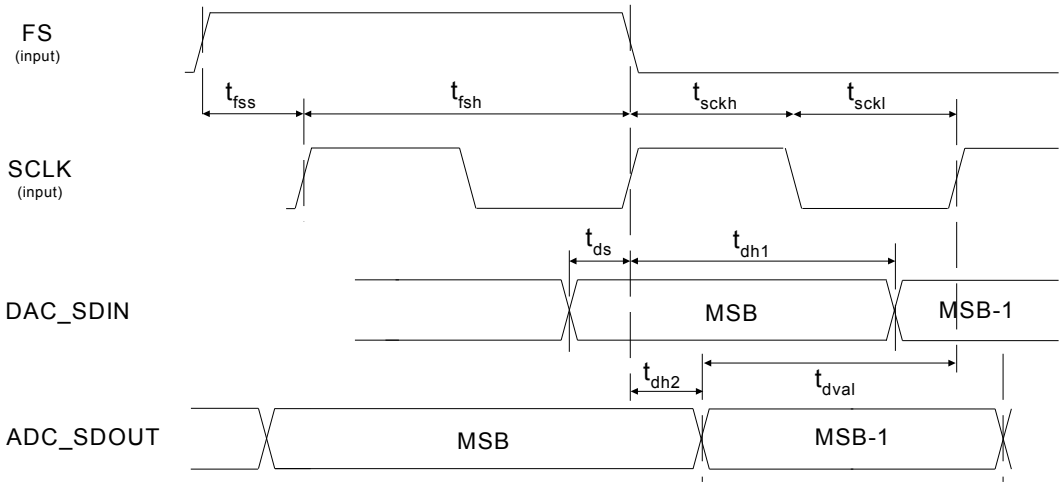


Figure 5. TDM Serial Audio Interface Timing

SWITCHING CHARACTERISTICS - AUX PORT

(Inputs: Logic 0 = DGND, Logic 1 = VLS.)

Parameters		Symbol	Min	Max	Units
Master Mode					
Output Sample Rate (AUX_LRCK)	All Speed Modes	F_s	-	FS	kHz
AUX_SCLK Frequency			-	64•FS	kHz
AUX_SCLK Duty Cycle			45	55	%
AUX_LRCK Edge to SCLK Rising Edge		t_{lcks}	-	5	ns
AUX_SDIN Setup Time Before SCLK Rising Edge		t_{ds}	3	-	ns
AUX_SDIN Hold Time After SCLK Rising Edge		t_{dh}	5	-	ns

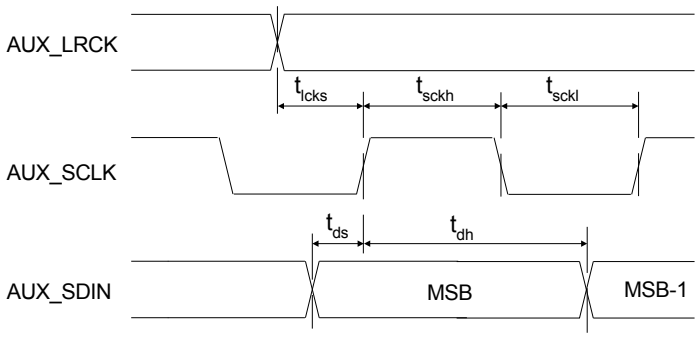


Figure 6. Serial Audio Interface Slave Mode Timing

SWITCHING SPECIFICATIONS - CONTROL PORT - I²C MODE

(VLC = 1.8 V - 5.0 V, VLS = VD = 3.3 V, VA = 5.0 V; Inputs: Logic 0 = DGND, Logic 1 = VLC, SDA C_L = 30 pF)

Parameter		Symbol	Min	Max	Unit
SCL Clock Frequency		f_{scl}	-	100	kHz
$\overline{RST}$ Rising Edge to Start		t_{irs}	500	-	ns
Bus Free Time Between Transmissions		t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)		t_{hdst}	4.0	-	µs
Clock Low time		t_{low}	4.7	-	µs
Clock High Time		t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition		t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling	(Note 21)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising		t_{sud}	250	-	ns
Rise Time of SCL and SDA	(Note 22)	t_{rc}	-	1	µs
Fall Time SCL and SDA	(Note 22)	t_{fc}	-	300	ns
Setup Time for Stop Condition		t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling		t_{ack}	300	1000	ns

Notes:

21. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.
22. Guaranteed by design.

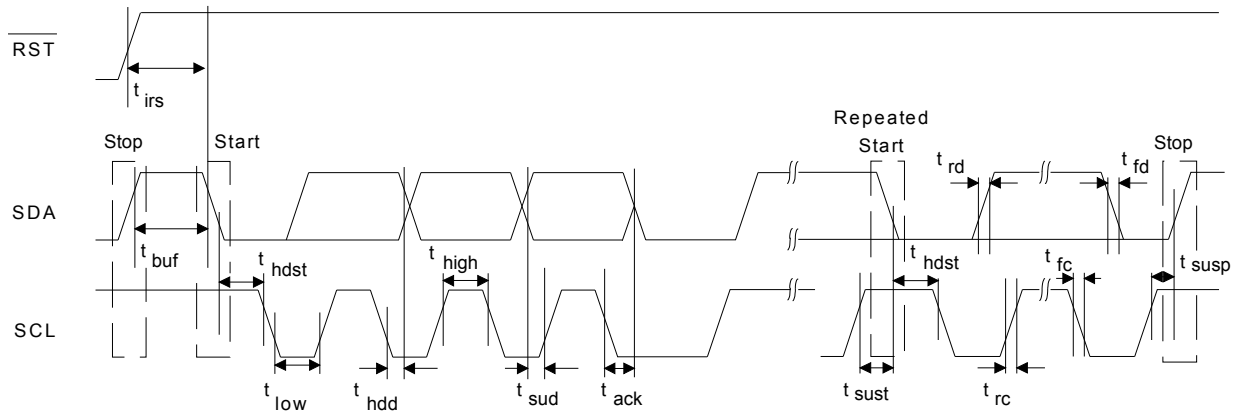


Figure 7. Control Port Timing - I²C Format

SWITCHING SPECIFICATIONS - CONTROL PORT - SPI FORMAT

(VLC = 1.8 V - 5.0 V, VLS = VD = 3.3 V, VA = 5.0 V; Inputs: Logic 0 = DGND, Logic 1 = VLC, CDOUT C_L = 30 pF)

Parameter		Symbol	Min	Max	Units
CCLK Clock Frequency		f_{sck}	0	6.0	MHz
$\overline{RST}$ Rising Edge to $\overline{CS}$ Falling		t_{srs}	20	-	ns
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	ns
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 23)	t_{dh}	15	-	ns
CCLK Falling to CDOUT Stable		t_{pd}	-	50	ns
Rise Time of CDOUT		t_{r1}	-	25	ns
Fall Time of CDOUT		t_{f1}	-	25	ns
Rise Time of CCLK and CDIN	(Note 24)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 24)	t_{f2}	-	100	ns

Notes:

23. Data must be held for sufficient time to bridge the transition time of CCLK.
24. For f_{sck} <1 MHz.

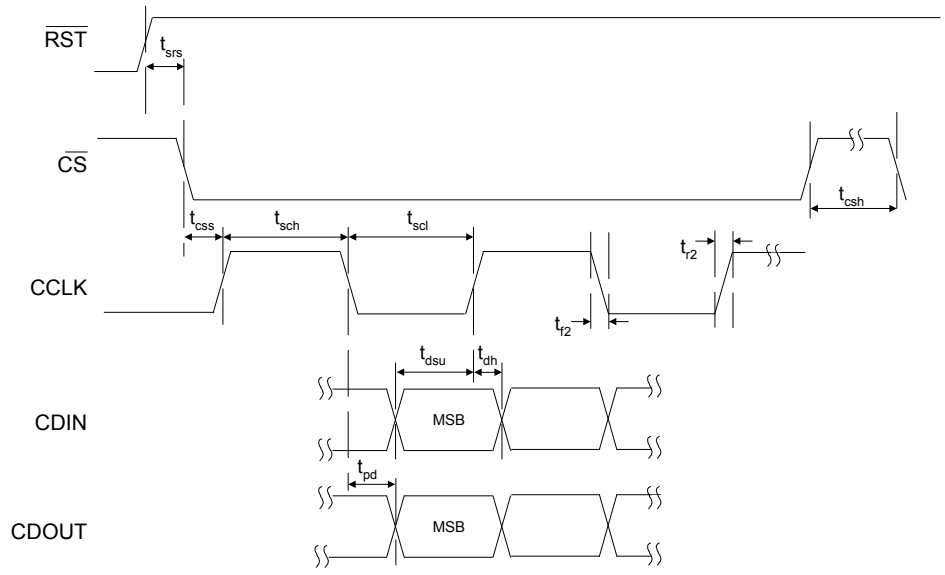


Figure 8. Control Port Timing - SPI Format

DC ELECTRICAL CHARACTERISTICS

(AGND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Typ	Max	Units
Normal Operation (Note 25)						
Power Supply Current	VA = 5.0 V	I_A	-	80	-	mA
	VLS = VLC = VD = 3.3 V					
	(Note 26)	I_{DT}	-	60.6	-	mA
Power Dissipation	VLS = VLC = VD = 3.3 V,5 V		-	600	850	mW
Power Supply Rejection Ratio	1 kHz	PSRR	-	60	-	dB
(Note 27)	60 Hz		-	40	-	dB
Power-Down Mode (Note 28)						
Power Dissipation	VLS = VLC = VD = 3.3 V,VA = 5 V		-	1.25	-	mW
VQ Characteristics						
Nominal Voltage			-	0.5•VA	-	V
Output Impedance			-	23	-	kΩ
DC Current Source/Sink (Note 29)			-	-	10	µA
FILT+ Nominal Voltage			-	VA	-	V

Notes:

25. Normal operation is defined as $\overline{RST}$ = HI with a 997 Hz, 0 dBFS input to the DAC and AUX port, and a 1 kHz, -1 dB analog input to the ADC port sampled at the highest F_s for each speed mode. DAC outputs are open, unless otherwise specified.
26. I_{DT} measured with no external loading on pin (SDA).
27. Valid with the recommended capacitor values on FILT+ and VQ. Increasing the capacitance will also increase the PSRR.
28. Power-Down Mode is defined as $\overline{RST}$ = LO with all clocks and data lines held static and no analog input.
29. Guaranteed by design. The DC current draw represents the allowed current draw from the VQ pin due to typical leakage through the electrolytic de-coupling capacitors.

DIGITAL INTERFACE SPECIFICATIONS & CHARACTERISTICS

Parameters (Note 30)		Symbol	Min	Typ	Max	Units
High-Level Output Voltage at I_o=2 mA	Serial Port		VLS-1.0	-	-	V
	Control Port	V_{OH}	VLC-1.0	-	-	V
Low-Level Output Voltage at I_o=2 mA	Serial Port		-	-	0.4	V
	Control Port	V_{OL}	-	-	0.4	V
High-Level Input Voltage	Serial Port		0.7xVLS	-	-	V
	Control Port	V_{IH}	0.7xVLC	-	-	V
Low-Level Input Voltage	Serial Port		-	-	0.2xVLS	V
	Control Port	V_{IL}	-	-	0.2xVLC	V
Leakage Current		I_{in}	-	-	±10	µA
Input Capacitance (Note 22)			-	-	10	pF

Notes:

30. See "Digital I/O Pin Characteristics" on page 8 for serial and control port power rails.

5. APPLICATIONS

5.1 Overview

The CS42435 is a highly integrated mixed signal 24-bit audio CODEC comprised of 4 analog-to-digital converters (ADC) implemented using multi-bit delta-sigma techniques and 8 digital-to-analog converters (DAC) also implemented using multi-bit delta-sigma techniques.

Other functions integrated within the CODEC include independent digital volume controls for each DAC, digital de-emphasis filters for the DAC, digital volume control with gain on each ADC channel, ADC high-pass filters, and an on-chip voltage reference.

The serial audio interface ports allow up to 8 DAC channels and 6 ADC channels in a Time-Division Multiplexed (TDM) interface format. The CS42435 features an Auxiliary Port used to accommodate an additional two channels of PCM data on the ADC_SDOUT data line in the TDM digital interface format. See "AUX Port Digital Interface Formats" on page 32 for details.

The CS42435 operates in one of three oversampling modes based on the input sample rate. Mode selection is determined automatically based on the MCLK frequency setting. Single-Speed Mode (SSM) supports input sample rates up to 50 kHz and uses a 128x oversampling ratio. Double-Speed Mode (DSM) supports input sample rates up to 100 kHz and uses an oversampling ratio of 64x. Quad-Speed Mode (QSM) supports input sample rates up to 200 kHz and uses an oversampling ratio of 32x (**Note:** QSM for the ADC is only supported in the I²S, Left-Justified, Right-Justified interface formats. QSM is not supported for the ADC in the TDM interface format). **Note:** QSM is only available in Software Mode (see "System Clocking" on page 31 for details).

All functions can be configured through software via a serial control port operable in SPI Mode or in I²C Mode. A Hardware, Stand-Alone Mode is also available, allowing configuration of the CODEC on a more limited basis. See Table 2 for the default configuration in Hardware Mode.

Figure 1 on page 11 and Figure 2 on page 12 show the recommended connections for the CS42435 in Software and Hardware Mode, respectively. See "Register Description" on page 39 for the default register settings and options in Software Mode.

Hardware Mode Feature Summary			
Function	**Default Configuration**	**Hardware Control**	**Note**
Power Down ADC	All ADC's are enabled	-	-
Power Down DAC	All DAC's are enabled	-	-
Power Down Device	Device is powered up	-	-
MCLK Frequency Select	Selectable between 256Fs and 512Fs	"MFREQ" pin 3	see Section 5.4
Freeze Control	N/A	-	-
AUX Serial Port Interface Format	Left-Justified	-	-
ADC1 High Pass Filter Freeze	High Pass Filter is always enabled	-	-
DAC De-Emphasis	No De-Emphasis applied	-	-
ADC1 Single-Ended Mode	Disabled	-	-
DAC Volume Control/Mute/Invert	All DAC Volume = 0 dB, un-muted, not inverted	-	-
ADC Volume Control	All ADC Volume = 0 dB	-	-
DAC Soft Ramp/Zero Cross	Immediate Change	-	-
ADC Soft Ramp/Zero Cross	Immediate Change	-	-

Table 2. Hardware Configurable Settings

Hardware Mode Feature Summary			
Function	**Default Configuration**	**Hardware Control**	**Note**
DAC Auto-Mute	Enabled	-	-
Status Interrupt	N/A	-	-

Table 2. Hardware Configurable Settings (Continued)

5.2 Analog Inputs

5.2.1 Line-Level Inputs

AINx+ and AINx- are the line-level differential analog inputs internally biased to VQ, approximately VA/2. Figure 9 on page 27 shows the full-scale analog input levels. The CS42435 also accommodates single-ended signals on all inputs, AIN1-AIN4. See "ADC Input Filter" on page 48 for the recommended input filters.

5.2.1.1 Hardware Mode

AIN Volume Control and ADC Overflow status are not accessible in Hardware Mode.

5.2.1.2 Software Mode

For single-ended operation on ADC1-ADC2 (AIN1 to AIN4), the ADCx_SINGLE bit in the register "ADC Control & DAC De-Emphasis (Address 05h)" on page 42 must be set appropriately (see Figure 20 on page 48 for required external components).

The gain/attenuation of the signal can be adjusted for each AINx independently through the "AINX Volume Control (Address 11h-14h)" on page 45. The ADC output data is in 2's complement binary format. For differential inputs above positive full scale or below negative full scale, the ADC will output 7FFFFFH or 800000H, respectively, and cause the ADC Overflow bit in the register "Status (Address 19h) (Read Only)" on page 46 to be set to a '1'. For single-ended inputs, the analog input level must remain at or below full scale to avoid wraparound of the resulting ADC codes. The ADC Overflow bit is reserved in single-ended mode.

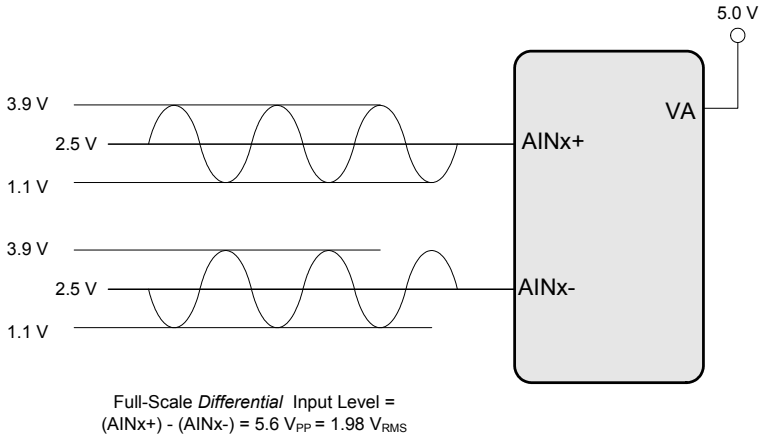


Figure 9. Full-Scale Input

5.2.2 High-Pass Filter and DC Offset Calibration

The high-pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. If the high-pass filter is disabled during normal operation, the current value of the DC offset for the corresponding channel is frozen and this DC offset will continue to be subtracted from the conversion result. This feature makes it possible to perform a system DC offset calibration by:

1. Running the CS42435 with the high-pass filter enabled until the filter settles. See the Digital Filter Characteristics for filter settling time.
2. Disabling the high-pass filter and freezing the stored DC offset.

5.2.2.1 Hardware Mode

The high pass filters for ADC1 and ADC2 are permanently enabled in Hardware Mode. Software Mode. The high-pass filter for ADC1/ADC2 can be enabled and disabled. The high-pass filters are controlled using the HPF_FREEZE bit in the register “ADC Control & DAC De-Emphasis (Address 05h)” on page 42.

5.3 Analog Outputs

5.3.1 Initialization

The initialization and Power-Down sequence flow chart is shown in Figure 10 on page 29. The CS42435 enters a power-down state upon initial power-up. The interpolation and decimation filters, delta-sigma modulators and control port registers are reset. The internal voltage reference, multi-bit digital-to-analog and analog-to-digital converters and switched-capacitor low-pass filters are powered down.

The device remains in the power-down state until the RST pin is brought high. The control port is accessible once RST is high, and the desired register settings can be loaded per the interface descriptions in the “Control Port Description and Timing” on page 33. In Hardware Mode operation, the Hardware Mode pins must be set up before RST is brought high. All features will default to the Hardware Mode defaults as listed in Table 2.

VQ will quickly charge to VA/2 upon initial power up. Once MCLK is valid and the PDN bit is set to ‘0’b, the internal voltage reference, FILT+, will ramp up to approximately VA. Power is applied to the D/A converters and switched-capacitor filters, and the analog outputs are clamped to the quiescent voltage, VQ. Once LRCK is valid, MCLK occurrences are counted over one LRCK period to determine the MCLK/LRCK frequency ratio. After an approximate 2000 sample period delay, normal operation begins.

5.3.2 Line-Level Outputs and Filtering

The CS42435 contains on-chip buffer amplifiers capable of producing line-level differential as well as single-ended outputs on AOUT1-AOUT8. These amplifiers are biased to a quiescent DC level of approximately VQ.

The delta-sigma conversion process produces high-frequency noise beyond the audio passband, most of which is removed by the on-chip analog filters. The remaining out-of-band noise can be attenuated using an off-chip low-pass filter.

See “DAC Output Filter” on page 50 for recommended output filter. The active filter configuration accounts for the normally differing AC loads on the AOUTx+ and AOUTx- differential output pins. Also shown is a passive filter configuration which minimizes costs and the number of components.

Figure 11 shows the full-scale analog output levels. All outputs are internally biased to VQ, approximately VA/2.

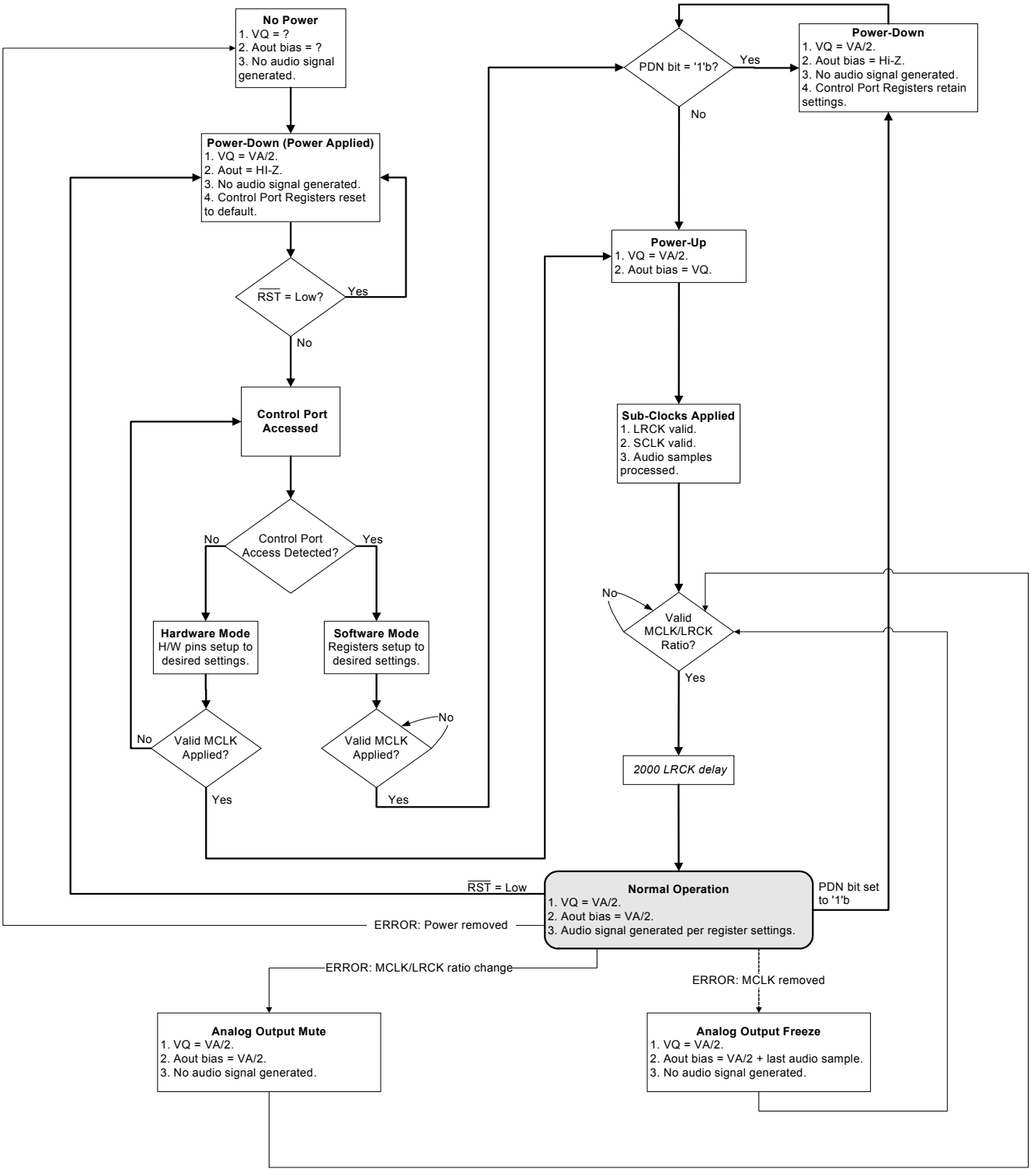


Figure 10. Audio Output Initialization Flow Chart

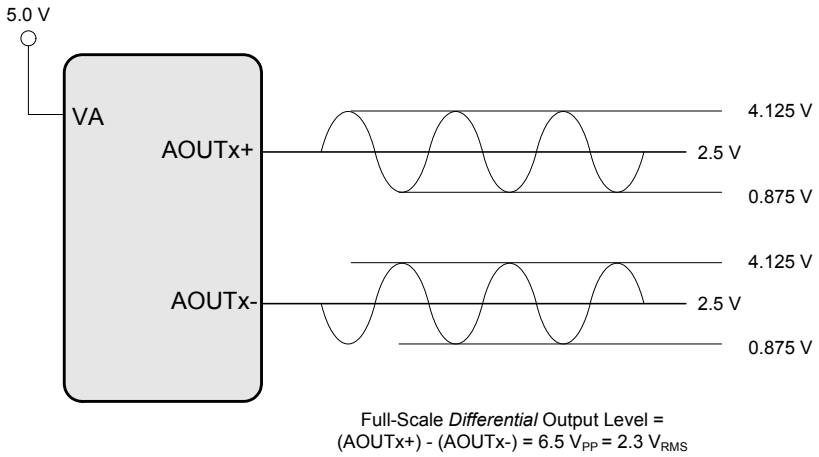


Figure 11. Full-Scale Output

5.3.3 Digital Volume Control

5.3.3.1 Hardware Mode

DAC Volume Control and Mute are not accessible in Hardware Mode.

5.3.3.2 Software Mode

Each DAC's output level is controlled via the Volume Control registers operating over the range of 0 to -127.5 dB attenuation with 0.5 dB resolution. See "AOUTX Volume Control (Addresses 08h- 0Fh)" on page 45. Volume control changes are programmable to ramp in increments of 0.125 dB at the rate controlled by the SZC[1:0] bits in the Digital Volume Control register. See "Transition Control (Address 06h)" on page 43.

Each output can be independently muted via mute control bits in the register "DAC Channel Mute (Address 07h)" on page 44. When enabled, each AOUTx_MUTE bit attenuates the corresponding DAC to its maximum value (-127.5 dB). When the AOUTx_MUTE bit is disabled, the corresponding DAC returns to the attenuation level set in the Volume Control register. The attenuation is ramped up and down at the rate specified by the SZC[1:0] bits.

5.3.4 De-Emphasis Filter

The CS42435 includes on-chip digital de-emphasis optimized for a sample rate of 44.1 kHz. The filter response is shown in Figure 12. The de-emphasis feature is included to accommodate audio recordings that utilize 50/15 µs pre-emphasis equalization as a means of noise reduction.

De-emphasis is only available in Single-Speed Mode. Please see "DAC De-Emphasis Control (DAC_DEM)" on page 42 for de-emphasis control.

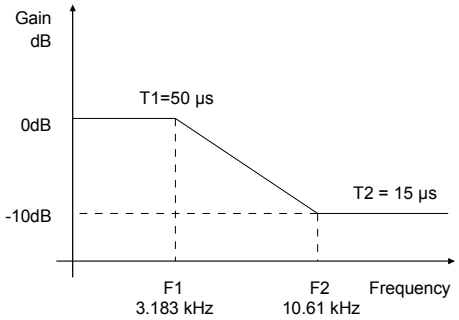


Figure 12. De-Emphasis Curve

5.4 System Clocking

The CODEC serial audio interface ports operate as a slave and accept externally generated clocks.

The CODEC requires external generation of the master clock (MCLK). The frequency of this clock must be an integer multiple of, and synchronous with, the system sample rate, Fs.

5.4.1 Hardware Mode

The allowable ratios include 256Fs and 512Fs in Single-Speed Mode and 256Fs in Double-Speed Mode. The frequency of MCLK must be specified using the MFREQ (pin 3). See Table 3 for the required frequency range.

		Ratio (xFs)		
MFREQ	**Description**	**SSM**	**DSM**	**QSM**
0	1.5360 MHz to 12.8000 MHz	256	N/A	N/A
1	2.0480 MHz to 25.6000 MHz	512	256	N/A

Table 3. MCLK Frequency Settings

5.4.2 Software Mode

The frequency range of MCLK must be specified using the MFREQ bits in register “MCLK Frequency (MFREQ[2:0])” on page 41.

5.5 CODEC Digital Interface

The ADC and DAC serial ports operate as a slave and support the TDM digital interface formats with varying bit depths from 16 to 32 as shown in Figure 13 on page 32. Data is clocked out of the ADC on the falling edge of SCLK and clocked into the DAC on the rising edge.

TDM is the only interface supported in Hardware and Software Mode.

5.5.1 TDM

TDM data is received most significant bit (MSB) first, on the second rising edge of the SCLK occurring after an FS rising edge. All data is valid on the rising edge of SCLK. The AIN1 MSB is transmitted early, but is guaranteed valid for a specified time after SCLK rises. All other bits are transmitted on the falling edge of SCLK. Each time slot is 32 bits wide, with the valid data sample left justified within the time slot. Valid data lengths are 16, 18, 20, or 24.

SCLK must operate at 256Fs. FS identifies the start of a new frame and is equal to the sample rate, Fs.

FS is sampled as valid on the rising SCLK edge preceding the most significant bit of the first data sample and must be held valid for at least 1 SCLK period.

Note: The ADC does not meet the timing requirements for proper operation in Quad-Speed Mode.

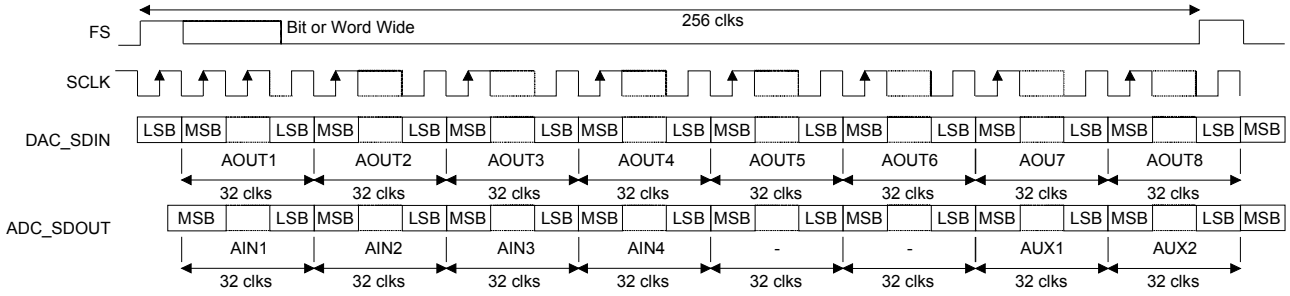


Figure 13. TDM Serial Audio Format

5.5.2 I/O Channel Allocation

Digital Input/Output	Interface Format	Analog Output/Input Channel Allocation from/to Digital I/O
DAC_SDIN	TDM	AOUT 1,2,3,4,5,6,7,8
ADC_SDOUT	TDM	AIN 1,2,3,4 (2 additional channels from AUX_SDIN)

Table 4. Serial Audio Interface Channel Allocations

5.6 AUX Port Digital Interface Formats

These serial data lines are used when supporting the TDM Mode of operation with an external ADC or S/PDIF receiver attached. The AUX serial port operates only as a clock master. The AUX_SCLK will operate at 64xFs, where Fs is equal to the ADC sample rate (FS on the TDM interface). If the AUX_SDIN signal is not being used, it should be tied to AGND via a pull-down resistor.

5.6.1 Hardware Mode

The AUX port will only operate in the Left-Justified digital interface format and supports bit depths ranging from 16 to 24 bits (see Figure 17 on page 34 for timing relationship between AUX_LRCK and AUX_SCLK).

5.6.2 Software Mode

The AUX port will operate in either the Left-Justified or I²S digital interface format with bit depths ranging from 16 to 24 bits. Settings for the AUX port are made through the register "Miscellaneous Control (Address 04h)" on page 41.

5.6.3 I²S

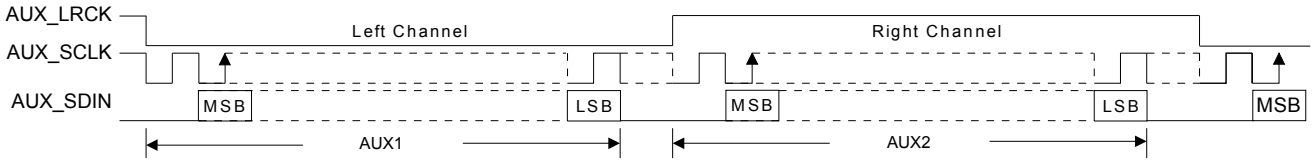


Figure 14. AUX I²S Format

5.6.4 Left-Justified

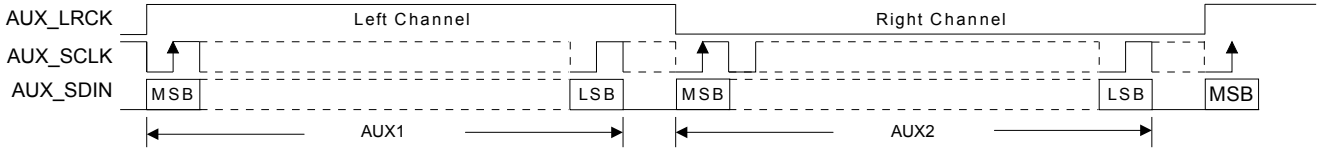


Figure 15. AUX Left-Justified Format

5.7 Control Port Description and Timing

The control port is used to access the registers, in Software Mode, allowing the CS42435 to be configured for the desired operational modes and formats. The operation of the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port has two modes: SPI and I²C, with the CS42435 acting as a slave device. SPI Mode is selected if there is a high-to-low transition on the AD0/$\overline{CS}$ pin, after the $\overline{RST}$ pin has been brought high. I²C Mode is selected by connecting the AD0/$\overline{CS}$ pin through a resistor to VLC or DGND, thereby permanently selecting the desired AD0 bit address state.

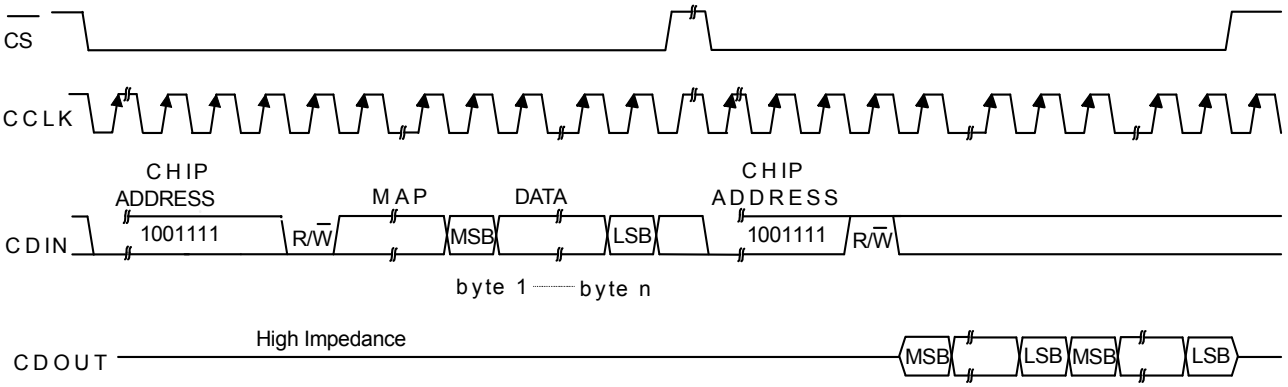
5.7.1 SPI Mode

In SPI Mode, $\overline{CS}$ is the CS42435 chip-select signal, CCLK is the control port bit clock (input into the CS42435 from the microcontroller), CDIN is the input data line from the microcontroller, CDOUT is the output data line to the microcontroller. Data is clocked in on the rising edge of CCLK and out on the falling edge.

Figure 16 shows the operation of the control port in SPI Mode. To write to a register, bring $\overline{CS}$ low. The first seven bits on CDIN form the chip address and must be 1001111. The eighth bit is a read/write indicator (R/$\overline{W}$), which should be low to write. The next eight bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next eight bits are the data which will be placed into the register designated by the MAP. During writes, the CDOUT output stays in the Hi-Z state. It may be externally pulled high or low with a 47 kΩ resistor, if desired.

There is a MAP auto-increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, the MAP will stay constant for successive read or writes. If INCR is set to a 1, the MAP will auto-increment after each byte is read or written, allowing block reads or writes of successive registers.

To read a register, the MAP has to be set to the correct address by executing a partial write cycle which finishes ($\overline{CS}$ high) immediately after the MAP byte. The MAP auto-increment bit (INCR) may be set or not, as desired. To begin a read, bring $\overline{CS}$ low, send out the chip address and set the read/write bit (R/$\overline{W}$) high. The next falling edge of CCLK will clock out the MSB of the addressed register (CDOUT will leave the high impedance state). If the MAP auto-increment bit is set to 1, the data for successive registers will appear consecutively.



MAP = Memory Address Pointer, 8 bits, MSB first

Figure 16. Control Port Timing in SPI Mode

5.7.2 I²C Mode

In I²C Mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL. There is no CS pin. Pins AD0 and AD1 form the two least-significant bits of the chip address and should be connected through a resistor to VLC or DGND as desired. The state of the pins is sensed while the CS42435 is being reset.

The signal timings for a read and write cycle are shown in Figure 17 and Figure 18. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS42435 after a Start condition consists of a 7-bit chip address field and a R/W bit (high for a read, low for a write). The upper 5 bits of the 7-bit address field are fixed at 10010. To communicate with a CS42435, the chip address field, which is the first byte sent to the CS42435, should match 10010 followed by the settings of the AD1 and AD0. The eighth bit of the address is the R/W bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto-increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS42435 after each input byte is read, and is input to the CS42435 from the microcontroller after each transmitted byte.

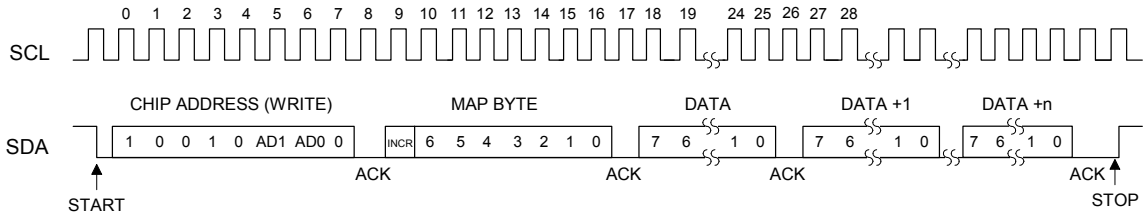


Figure 17. Control Port Timing, I²C Write

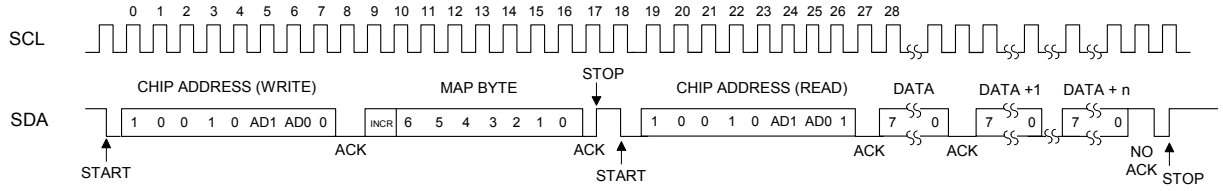


Figure 18. Control Port Timing, I²C Read

Since the read operation cannot set the MAP, an aborted write operation is used as a preamble. As shown in Figure 18, the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

Send start condition.

Send 10010xx0 (chip address & write operation).

Receive acknowledge bit.

Send MAP byte, auto increment off.

Receive acknowledge bit.

Send stop condition, aborting write.

Send start condition.

Send 10010xx1(chip address & read operation).

Receive acknowledge bit.

Receive byte, contents of selected register.

Send acknowledge bit.

Send stop condition.

Setting the auto-increment bit in the MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

5.8 Recommended Power-Up Sequence

5.8.1 Hardware Mode

1. Hold $\overline{\text{RST}}$ low until the power supply, clocks and hardware control pins are stable. In this state, the control port is reset to its default settings and VQ will remain low.
2. Bring $\overline{\text{RST}}$ high. The device will initially be in a low power state with VQ low.
3. The device will initiate the Hardware Mode power up sequence. All features will default to the Hardware Mode defaults as listed in Table 2 on page 26 according to the Hardware Mode control pins. VQ will quick-charge to approximately VA/2 and the analog output bias will clamp to VQ.
4. Following approximately 2000 sample periods, the device is initialized and ready for normal operation.

Note: During the Hardware Mode power-up sequence, there must be no transitions on any of the hardware control pins.

5.8.2 Software Mode

1. Hold $\overline{\text{RST}}$ low until the power supply and clocks are stable. In this state, the control port is reset to its default settings and VQ will remain low.
2. Bring $\overline{\text{RST}}$ high. The device will initially be in a low power state with VQ low. All features will default as described in the "Register Quick Reference" on page 37.
3. Perform a write operation to the Power Control register ("Power Control (Address 02h)" on page 40) to set bit 0 to a '1'b. This will place the device in a power down state.
4. Load the desired register settings while keeping the PDN bit set to '1'b.
5. Mute all DACs. Muting the DACs suppresses any noise associated with the CODEC's first initialization after power is applied.
6. Set the PDN bit in the power control register to '0'b.Following approximately 2000 LRCK cycles, the device is initialized and ready for normal operation.
7. After the CODEC is initialized, wait ~90 LRCK cycles (~1.9 ms @48 kHz) and then unmute the DACs.
8. Normal operation begins.

5.9 Reset and Power-Up

It is recommended that reset be activated if the analog or digital supplies drop below the recommended operating condition to prevent power-glitch-related issues.

The delta-sigma modulators settle in a matter of microseconds after the analog section is powered, either through the application of power or by setting the $\overline{\text{RST}}$ pin high. However, the voltage reference will take much longer to reach a final value due to the presence of external capacitance on the FILT+ pin. A time delay of approximately 400 ms is required after applying power to the device or after exiting a reset state. During this voltage reference ramp delay, all serial ports and DAC outputs will be automatically muted.

5.10 Power Supply, Grounding, and PCB Layout

As with any high-resolution converter, the CS42435 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 and Figure 2 show the recommended power arrangements, with VA connected to clean supplies. VD, which powers the digital circuitry, may be run from the system logic supply.

Extensive use of power and ground planes, ground plane fill in unused areas and surface mount decoupling capacitors are recommended. Decoupling capacitors should be as near to the pins of the CS42435 as possible. The low value ceramic capacitor should be the nearest to the pin and should be mounted on the same side of the board as the CS42435 to minimize inductance effects. All signals, especially clocks, should be kept away from the FILT+, VQ pins in order to avoid unwanted coupling into the modulators. The FILT+ and VQ decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from FILT+ and AGND. The CS42435 evaluation board demonstrates the optimum layout and power supply arrangements.

For optimal heat dissipation from the package, it is recommended that the area directly under the part be filled with copper and tied to the ground plane. The use of vias connecting the topside ground to the backside ground is also recommended.

6. REGISTER QUICK REFERENCE

Software Mode register defaults are as shown. **Note**: The default value in all “Reserved” registers must be preserved.

Addr	Function	7	6	5	4	3	2	1	0
01h	ID	Chip_ID3	Chip_ID2	Chip_ID1	Chip_ID0	Rev_ID3	Rev_ID2	Rev_ID1	Rev_ID0
	p 39 default	0	0	0	1	0	0	0	1
02h	Power Control	Reserved	PDN_ADC2	PDN_ADC1	PDN_DAC4	PDN_DAC3	PDN_DAC2	PDN_DAC1	PDN
	p 40 default	0	0	0	0	0	0	0	0
03h	Functional Mode	Reserved	Reserved	Reserved	Reserved	MFreq2	MFreq1	MFreq0	Reserved
	p 41 default	1	1	1	1	0	0	0	0
04h	Misc Control	FREEZE	AUX_DIF	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	p 41 default	0	0	1	1	0	1	1	0
05h	ADC Control (w/DAC_DEM)	ADC1-2_HPF FREEZE	Reserved	DAC_DEM	ADC1 SINGLE	ADC2 SINGLE	Reserved	Reserved	Reserved
	p 42 default	0	0	0	0	0	0	0	0
06h	Transition Control	DAC_SNG VOL	DAC_SZC1	DAC_SZC0	AMUTE	MUTE ADC_SP	ADC_SNG VOL	ADC_SZC1	ADC_SZC0
	p 43 default	0	0	0	1	0	0	0	0
07h	Channel Mute	AOUT8 MUTE	AOUT7 MUTE	AOUT6 MUTE	AOUT5 MUTE	AOUT4 MUTE	AOUT3 MUTE	AOUT2 MUTE	AOUT1 MUTE
	p 44 default	0	0	0	0	0	0	0	0
08h	Vol. Control AOUT1	AOUT1 VOL7	AOUT1 VOL6	AOUT1 VOL5	AOUT1 VOL4	AOUT1 VOL3	AOUT1 VOL2	AOUT1 VOL1	AOUT1 VOL0
	p 45 default	0	0	0	0	0	0	0	0
09h	Vol. Control AOUT2	AOUT2 VOL7	AOUT2 VOL6	AOUT2 VOL5	AOUT2 VOL4	AOUT2 VOL3	AOUT2 VOL2	AOUT2 VOL1	AOUT2 VOL0
	p 45 default	0	0	0	0	0	0	0	0
0Ah	Vol. Control AOUT3	AOUT3 VOL7	AOUT3 VOL6	AOUT3 VOL5	AOUT3 VOL4	AOUT3 VOL3	AOUT3 VOL2	AOUT3 VOL1	AOUT3 VOL0
	p 45 default	0	0	0	0	0	0	0	0
0Bh	Vol. Control AOUT4	AOUT4 VOL7	AOUT4 VOL6	AOUT4 VOL5	AOUT4 VOL4	AOUT4 VOL3	AOUT4 VOL2	AOUT4 VOL1	AOUT4 VOL0
	p 45 default	0	0	0	0	0	0	0	0
0Ch	Vol. Control AOUT5	AOUT5 VOL7	AOUT5 VOL6	AOUT5 VOL5	AOUT5 VOL4	AOUT5 VOL3	AOUT5 VOL2	AOUT5 VOL1	AOUT5 VOL0
	p 45 default	0	0	0	0	0	0	0	0
0Dh	Vol. Control AOUT6	AOUT6 VOL7	AOUT6 VOL6	AOUT6 VOL5	AOUT6 VOL4	AOUT6 VOL3	AOUT6 VOL2	AOUT6 VOL1	AOUT6 VOL0
	p 45 default	0	0	0	0	0	0	0	0
0Eh	Vol. Control AOUT7	AOUT7 VOL7	AOUT7 VOL6	AOUT7 VOL5	AOUT7 VOL4	AOUT7 VOL3	AOUT7 VOL2	AOUT7 VOL1	AOUT7 VOL0
	p 45 default	0	0	0	0	0	0	0	0
0Fh	Vol. Control AOUT8	AOUT8 VOL7	AOUT8 VOL6	AOUT8 VOL5	AOUT8 VOL4	AOUT8 VOL3	AOUT8 VOL2	AOUT8 VOL1	AOUT8 VOL0
	p 45 default	0	0	0	0	0	0	0	0
10h	DAC Channel Invert	INV_AOUT8	INV_AOUT7	INV_AOUT6	INV_AOUT5	INV_AOUT4	INV_AOUT3	INV_AOUT2	INV_AOUT1
	p 45 default	0	0	0	0	0	0	0	0

Addr	Function	7	6	5	4	3	2	1	0
11h	Vol. Control AIN1	AIN1 VOL7	AIN1 VOL6	AIN1 VOL5	AIN1 VOL4	AIN1 VOL3	AIN1 VOL2	AIN1 VOL1	AIN1 VOL0
	p 45 default	0	0	0	0	0	0	0	0
12h	Vol. Control AIN2	AIN2 VOL7	AIN2 VOL6	AIN2 VOL5	AIN2 VOL4	AIN2 VOL3	AIN2 VOL2	AIN2 VOL1	AIN2 VOL0
	p 45 default	0	0	0	0	0	0	0	0
13h	Vol. Control AIN3	AIN3 VOL7	AIN3 VOL6	AIN3 VOL5	AIN3 VOL4	AIN3 VOL3	AIN3 VOL2	AIN3 VOL1	AIN3 VOL0
	p 45 default	0	0	0	0	0	0	0	0
14h	Vol. Control AIN4	AIN4 VOL7	AIN4 VOL6	AIN4 VOL5	AIN4 VOL4	AIN4 VOL3	AIN4 VOL2	AIN4 VOL1	AIN4 VOL0
	p 45 default	0	0	0	0	0	0	0	0
15h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	0	0	0	0	0	0	0	0
16h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	0	0	0	0	0	0	0	0
17h	ADC Channel Invert	Reserved	Reserved	Reserved	Reserved	INV_A4	INV_A3	INV_A2	INV_A1
	p 45 default	0	0	0	0	0	0	0	0
18h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	0	0	0	0	0	0	0	0
19h	Status	Reserved	Reserved	Reserved	Reserved	CLK Error	Reserved	ADC2 OVFL	ADC1 OVFL
	p 46 default	0	0	0	X	X	X	X	X
1Ah	Status Mask	Reserved	Reserved	Reserved	Reserved	CLK Error_M	Reserved	ADC2_ OVFL_M	ADC1_ OVFL_M
	p 47 default	0	0	0	0	0	0	0	0

7. REGISTER DESCRIPTION

All registers are read/write except for the I.D. and Revision Register and Interrupt Status Register which are read only. See the following bit-definition tables for bit assignment information. The default state of each bit after a power-up sequence or reset is listed in each bit description.

7.1 Memory Address Pointer (MAP)

Not a register

7	6	5	4	3	2	1	0
INCR	MAP6	MAP5	MAP4	MAP3	MAP2	MAP1	MAP0

7.1.1 Increment (INCR)

Default = 1

Function:

Memory address pointer auto increment control
0 - MAP is not incremented automatically.
1 - Internal MAP is automatically incremented after each read or write.

7.1.2 Memory Address Pointer (MAP[6:0])

Default = 0000001

Function:

Memory address pointer (MAP). Sets the register address that will be read or written by the control port.

7.2 Chip I.D. and Revision Register (Address 01h) (Read Only)

7	6	5	4	3	2	1	0
Chip_ID3	Chip_ID2	Chip_ID1	Chip_ID0	Rev_ID3	Rev_ID2	Rev_ID1	Rev_ID0

7.2.1 Chip I.D. (CHIP_ID[3:0])

Default = 0001

Function:

I.D. code for the CS42435. Permanently set to 0000.

7.2.2 Chip Revision (REV_ID[3:0])

Default = xxxx

Function:

CS42435 revision level. Revision A is coded as 0001.

7.3 Power Control (Address 02h)

7	6	5	4	3	2	1	0
Reserved	PDN_ADC2	PDN_ADC1	PDN_DAC4	PDN_DAC3	PDN_DAC2	PDN_DAC1	PDN

7.3.1 Power Down ADC Pairs (PDN_ADCX)

Default = 0

0 - Disable
1 - Enable

Function:

When enabled, the respective ADC channel pair (ADC1 - AIN1/AIN2; and ADC2 - AIN3/AIN4) will remain in a reset state.

7.3.2 Power Down DAC Pairs (PDN_DACX)

Default = 0

0 - Disable
1 - Enable

Function:

When enabled, the respective DAC channel pair (DAC1 - AOUT1/AOUT2; DAC2 - AOUT3/AOUT4; DAC3 - AOUT5/AOUT6; and DAC4 - AOUT7/AOUT8) will remain in a reset state. It is advised that any change of these bits be made while the DACs are muted or the power down bit (PDN) is enabled to eliminate the possibility of audible artifacts.

7.3.3 Power Down (PDN)

Default = 0

0 - Disable
1 - Enable

Function:

The entire device will enter a low-power state when this function is enabled. The contents of the control registers are retained in this mode.

7.4 Functional Mode (Address 03h)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	MFreq2	MFreq1	MFreq0	Reserved

7.4.1 MCLK Frequency (MFREQ[2:0])

Default = 000

Function:

Sets the appropriate frequency for the supplied MCLK. For TDM operation, SCLK must equal 256Fs. MCLK can be equal to or greater than SCLK.

				Ratio (xFs)		
MFreq2	**MFreq1**	**MFreq0**	**Description**	**SSM**	**DSM**	**QSM**
0	0	0	1.0290 MHz to 12.8000 MHz	256	N/A	N/A
0	0	1	Reserved			
0	1	0	2.0480 MHz to 25.6000 MHz	512	256	N/A
0	1	1	Reserved			
1	X	X	4.0960 MHz to 51.2000 MHz	1024	512	256

Table 5. MCLK Frequency Settings

7.5 MISCELLANEOUS CONTROL (Address 04h)

7	6	5	4	3	2	1	0
FREEZE	AUX_DIF	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

7.5.1 Freeze Controls (FREEZE)

Default = 0

Function:

This function will freeze the previous settings of, and allow modifications to be made to the channel mutes, the DAC and ADC Volume Control/Channel Invert registers without the changes taking effect until the FREEZE is disabled. To have multiple changes in these control port registers take effect simultaneously, enable the FREEZE bit, make all register changes, then disable the FREEZE bit.

7.5.2 Auxiliary Digital Interface Format (AUX_DIF)

Default = 0

0 - Left Justified
1 - I²S

Function:

This bit selects the digital interface format used for the AUX Serial Port. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in Figures 16-17.

7.6 ADC Control & DAC De-Emphasis (Address 05h)

7	6	5	4	3	2	1	0
ADC1-2_HPF FREEZE	Reserved	DAC_DEM	ADC1 SINGLE	ADC2 SINGLE	Reserved	Reserved	Reserved

7.6.1 ADC1-2 High-Pass Filter Freeze (ADC1-2_HPF FREEZE)

Default = 0

Function:

When this bit is set, the internal high-pass filter will be disabled for ADC1 and ADC2.The current DC offset value will be frozen and continue to be subtracted from the conversion result. See “ADC Digital Filter Characteristics” on page 16.

7.6.2 DAC De-Emphasis Control (DAC_DEM)

Default = 0

0 - No De-Emphasis
1 - De-Emphasis Enabled (Auto-Detect Fs)

Function:

Enables the digital filter to maintain the standard 15μs/50μs digital de-emphasis filter response at the auto-detected sample rate of either 32, 44.1, or 48 kHz. De-emphasis will not be enabled, regardless of this register setting, at any other sample rate.

7.6.3 ADC1 Single-Ended Mode (ADC1 SINGLE)

Default = 0

0 - Disabled; Differential input to ADC1
1 - Enabled; Single-Ended input to ADC1

Function:

When enabled, this bit allows the user to apply a single-ended input to the positive terminal of ADC1. A +6 dB digital gain is automatically applied to the serial audio data of ADC1. The negative leg must be driven to the common mode of the ADC. See Figure 20 on page 48 for a graphical description, and Sections 5.2.1 and 7.13.2.

7.6.4 ADC2 Single-Ended Mode (ADC2 SINGLE)

Default = 0

0 - Disabled; Differential input to ADC2
1 - Enabled; Single-Ended input to ADC2

Function:

When enabled, this bit allows the user to apply a single-ended input to the positive terminal of ADC2. A +6 dB digital gain is automatically applied to the serial audio data of ADC2. The negative leg must be driven to the common mode of the ADC. See Figure 20 on page 48 for a graphical description, and Sections 5.2.1 and 7.13.2.

7.7 Transition Control (Address 06h)

7	6	5	4	3	2	1	0
DAC_SNGVOL	DAC_SZC1	DAC_SZC0	AMUTE	MUTE ADC_SP	ADC_SNGVOL	ADC_SZC1	ADC_SZC0

7.7.1 Single Volume Control (DAC_SNGVOL, ADC_SNGVOL)

Default = 0

Function:

The individual channel volume levels are independently controlled by their respective Volume Control registers when this function is disabled. When enabled, the volume on all channels is determined by the AOUT1 and AIN1 Volume Control register and the other Volume Control registers are ignored.

7.7.2 Soft Ramp and Zero Cross Control (ADC_SZC[1:0], DAC_SZC[1:0])

Default = 00

00 - Immediate Change
01 - Zero Cross
10 - Soft Ramp
11 - Soft Ramp on Zero Crossings

Function:

Immediate Change

When Immediate Change is selected, all volume-level changes will take effect immediately in one step.

Zero Cross

Zero Cross Enable dictates that signal level changes, either by gain changes, attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Soft Ramp

Soft Ramp allows level changes, either by gain changes, attenuation changes or muting, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods.

Soft Ramp on Zero Crossing

Soft Ramp and Zero Cross Enable dictates that signal level changes, either by gain changes, attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

7.7.3 Auto-Mute (AMUTE)

Default = 1

0 - Disabled
1 - Enabled

Function:

The Digital-to-Analog converters of the CS42435 will mute the output following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-static data will release the mute. Detection and muting is done independently for each channel. The quiescent voltage on the output will be retained during the mute period. The muting function is affected, similar to volume control changes, by the Soft and Zero Cross bits (SZC[1:0]).

7.7.4 Mute ADC Serial Port (MUTE ADC_SP)

Default = 0

0 - Disabled
1 - Enabled

Function:

When enabled, the ADC Serial Port will be muted.

7.8 DAC Channel Mute (Address 07h)

7	6	5	4	3	2	1	0
AOUT8_MUTE	AOUT7_MUTE	AOUT6_MUTE	AOUT5_MUTE	AOUT4_MUTE	AOUT3_MUTE	AOUT2_MUTE	AOUT1_MUTE

7.8.1 Independent Channel Mute (AOUTX_MUTE)

Default = 0

0 - Disabled
1 - Enabled

Function:

The respective Digital-to-Analog converter outputs of the CS42435 will mute when enabled. The quiescent voltage on the outputs will be retained. The muting function is affected by the DAC Soft and Zero Cross bits (DAC_SZC[1:0]).

7.9 AOUTX Volume Control (Addresses 08h- 0Fh)

7	6	5	4	3	2	1	0
AOUTx_VOL7	AOUTx_VOL6	AOUTx_VOL5	AOUTx_VOL4	AOUTx_VOL3	AOUTx_VOL2	AOUTx_VOL1	AOUTx_VOL0

7.9.1 Volume Control (AOUTX_VOL[7:0])

Default = 00h

Function:

The AOUTx Volume Control registers allow independent setting of the signal levels in 0.5 dB increments from 0 dB to -127.5 dB. Volume settings are decoded as shown in Table 6. The volume changes are implemented as dictated by the Soft and Zero Cross bits (DAC_SZC[1:0]). All volume settings less than -127.5 dB are equivalent to enabling the AOUTx_MUTE bit for the given channel.

Binary Code	Volume Setting
00000000	0 dB
00101000	-20 dB
01010000	-40 dB
01111000	-60 dB
10110100	-90 dB

Table 6. Example AOUT Volume Settings

7.10 DAC Channel Invert (Address 10h)

7	6	5	4	3	2	1	0
INV_AOUT8	INV_AOUT7	INV_AOUT6	INV_AOUT5	INV_AOUT4	INV_AOUT3	INV_AOUT2	INV_AOUT1

7.10.1 Invert Signal Polarity (INV_AOUTX)

Default = 0

0 - Disabled
1 - Enabled

Function:

When enabled, these bits will invert the signal polarity of their respective channels.

7.11 AINX Volume Control (Address 11h-14h)

7	6	5	4	3	2	1	0
AINx_VOL7	AINx_VOL6	AINx_VOL5	AINx_VOL4	AINx_VOL3	AINx_VOL2	AINx_VOL1	AINx_VOL0

7.11.1 AINX Volume Control (AINX_VOL[7:0])

Default = 00h

Function:

The level of the analog inputs can be adjusted in 0.5 dB increments as dictated by the ADC Soft and Zero Cross bits (ADC_SZC[1:0]) from +24 to -64 dB. Levels are decoded in two's complement, as shown in Table 7.

Binary Code	Volume Setting
0111 1111	+24 dB
...	...
0011 0000	+24 dB
...	...
0000 0000	0 dB
1111 1111	-0.5 dB
1111 1110	-1 dB
...	...
1000 0000	-64 dB

Table 7. Example AIN Volume Settings

7.12 ADC Channel Invert (Address 17h)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	INV_A4	INV_A3	INV_A2	INV_A1

7.12.1 Invert Signal Polarity (INV_AINX)

Default = 0

0 - Disabled
1 - Enabled

Function:

When enabled, these bits will invert the signal polarity of their respective channels.

7.13 Status (Address 19h) (Read Only)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	CLK Error	Reserved	ADC2_OVFL	ADC1_OVFL

For all bits in this register, a “1” means the associated error condition has occurred at least once since the register was last read. A”0” means the associated error condition has NOT occurred since the last reading of the register. Reading the register resets all bits to 0. Status bits that are masked off in the associated mask register will always be “0” in this register.

7.13.1 Clock Error (CLK ERROR)

Default = x

Function:

Indicates an invalid MCLK to FS ratio. This status flag is set to “Level Active Mode” and becomes active *during* the error condition. See “System Clocking” on page 31 for valid clock ratios.

7.13.2 ADC Overflow (ADCX_OVFL)

Default = x

Function:

Indicates that there is an over-range condition anywhere in the CS42435 signal path of each of the associated ADCs. This status flag becomes active on the *arrival* of the error condition. This bit is reserved when analog inputs are driven as single-ended.

7.14 Status Mask (Address 1Ah)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	CLK Error_M	Reserved	ADC2_OVFL_M	ADC1_OVFL_M

Default = 0000

Function:

The bits of this register serve as a mask for the error sources found in the register “Status (Address 19h) (Read Only)” on page 46. If a mask bit is set to 1, the error is unmasked, meaning that its occurrence will affect the status register. If a mask bit is set to 0, the error is masked, meaning that its occurrence will not affect status register. The bit positions align with the corresponding bits in the Status register.

8. EXTERNAL FILTERS

8.1 ADC Input Filter

The analog modulator samples the input at 6.144 MHz (internal MCLK=12.288 MHz). The digital filter will reject signals within the stopband of the filter. However, there is no rejection for input signals which are multiples of the digital passband frequency (n × 6.144 MHz), where n=0,1,2,... Refer to Figures 19 and 20 for a recommended analog input filter that will attenuate any noise energy at 6.144 MHz, in addition to providing the optimum source impedance for the modulators. Refer to Figures 21 and 22 for low-cost, low-component-count passive input filters. The use of capacitors that have a large voltage coefficient (such as general-purpose ceramics) must be avoided since these can degrade signal linearity

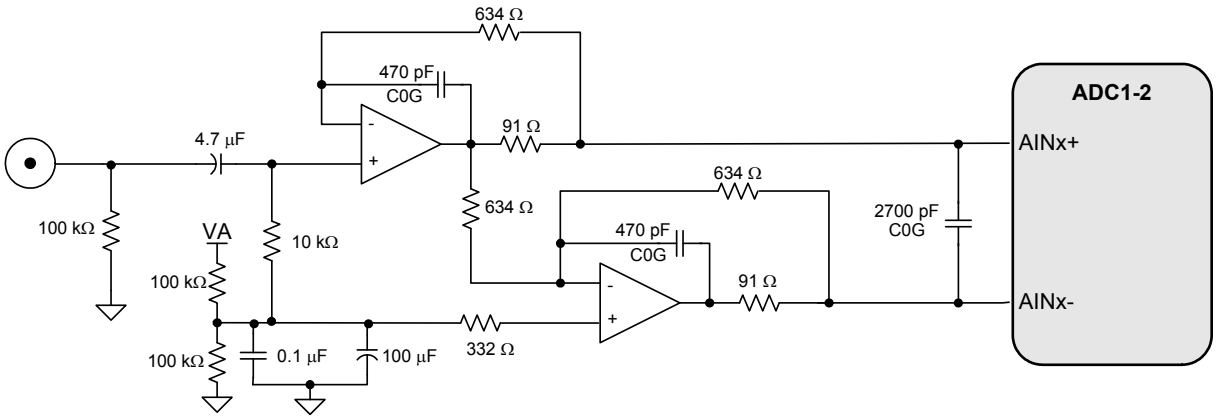


Figure 19. Single-to-Differential Active Input Filter

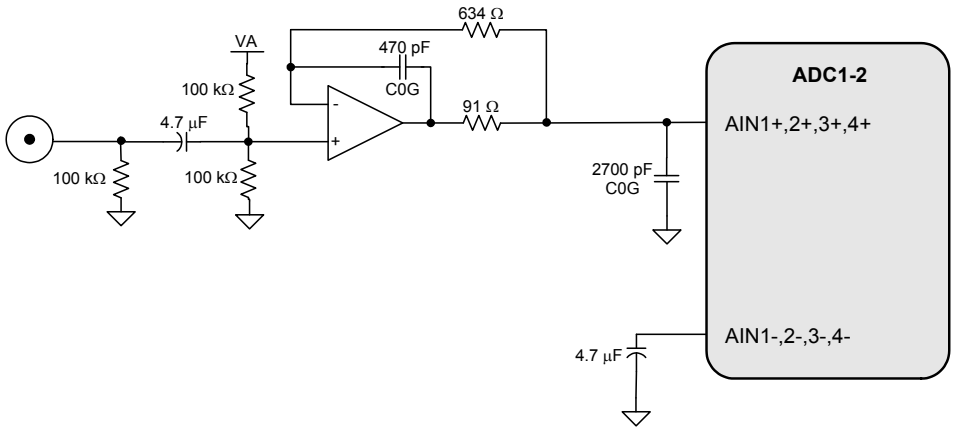


Figure 20. Single-Ended Active Input Filter

8.1.1 Passive Input Filter

The passive filter implementation shown in Figure 21 will attenuate any noise energy at 6.144 MHz but will not provide optimum source impedance for the ADC modulators. Full analog performance will therefore not be realized using a passive filter. Figure 21 illustrates the unity gain, passive input filter solution. In this topology the distortion performance is affected, but the dynamic range performance is not limited.

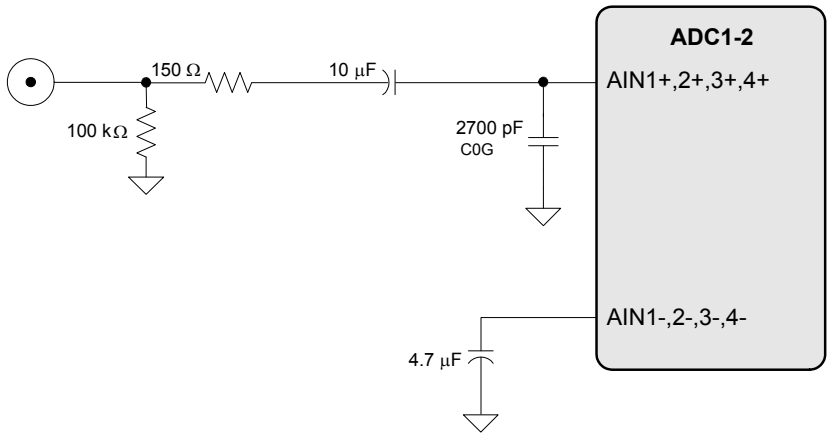


Figure 21. Passive Input Filter

8.1.2 Passive Input Filter w/Attenuation

Some applications may require signal attenuation prior to the ADC. The full-scale input voltage will scale with the analog power supply voltage. For VA = 5.0 V, the full-scale input voltage is approximately 2.8 Vpp, or 1 Vrms (most consumer audio line-level outputs range from 1.5 to 2 Vrms).

Figure 22 shows a passive input filter with 6 dB of signal attenuation. Due to the relatively high input impedance on the analog inputs, the full distortion performance cannot be realized. Also, the resistor divider circuit will determine the input impedance into the input filter. In the circuit shown in Figure 22, the input impedance is approximately 5 kΩ. By doubling the resistor values, the input impedance will increase to 10 kΩ. However, in this case the distortion performance will drop due to the increase in series resistance on the analog inputs.

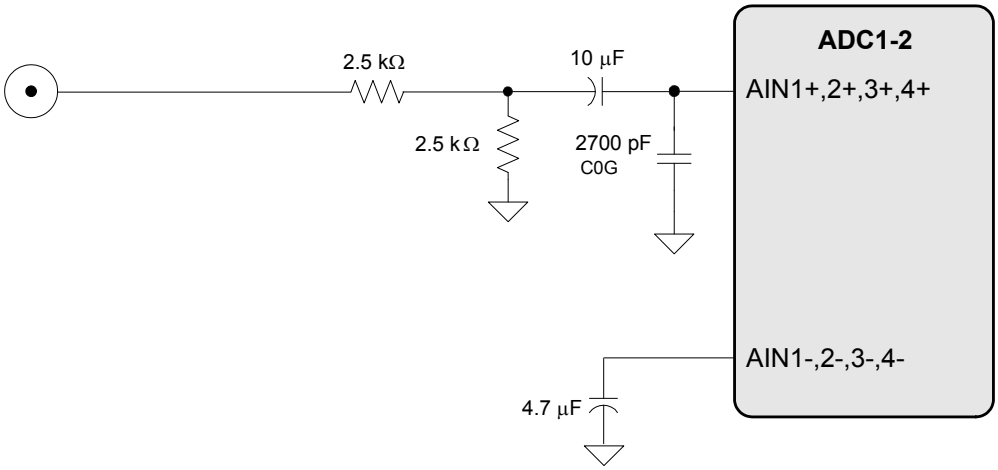


Figure 22. Passive Input Filter w/Attenuation

8.2 DAC Output Filter

The recommended active and passive output filters are shown below.

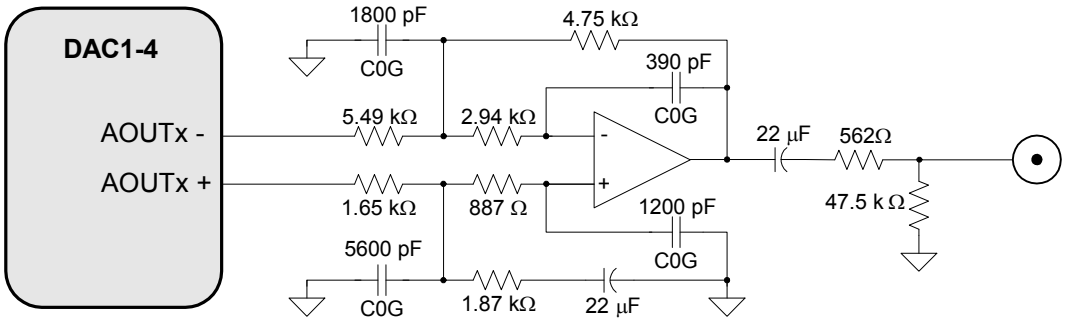


Figure 23. Active Analog Output Filter

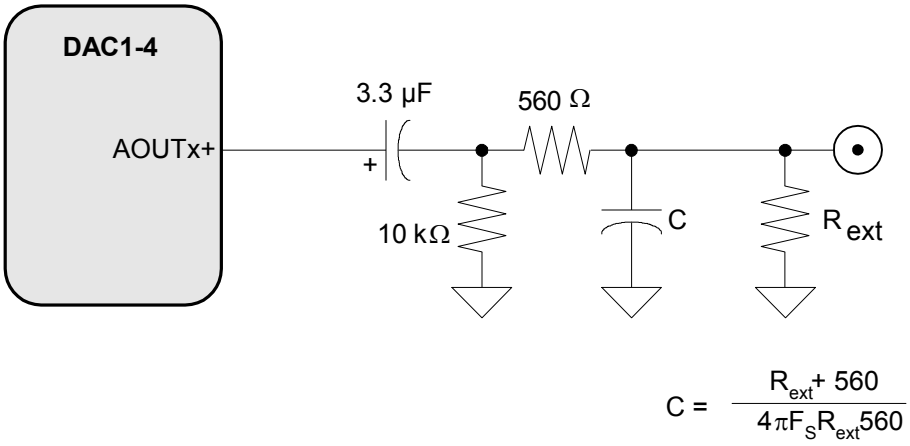


Figure 24. Passive Analog Output Filter

9. ADC FILTER PLOTS

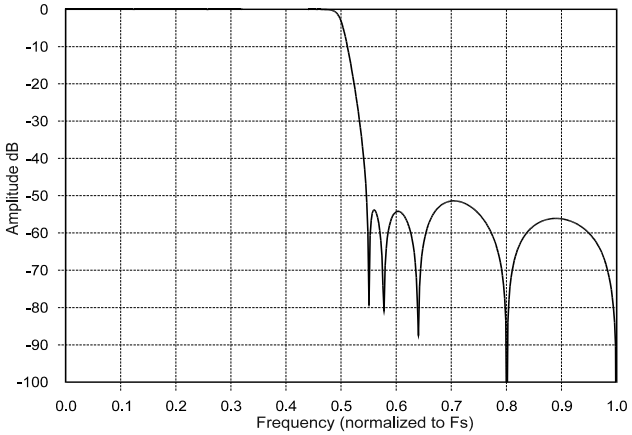


Figure 25. SSM Stopband Rejection

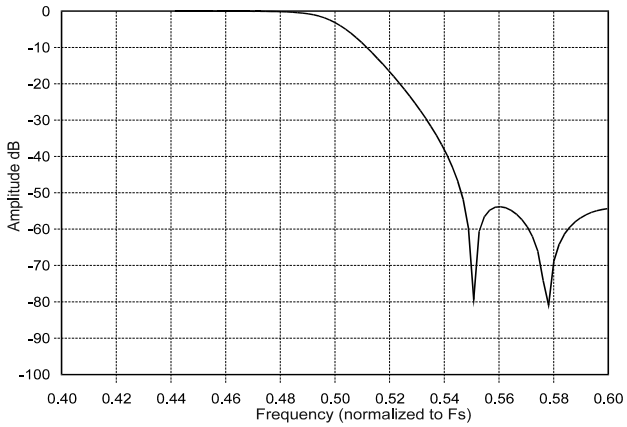


Figure 26. SSM Transition Band

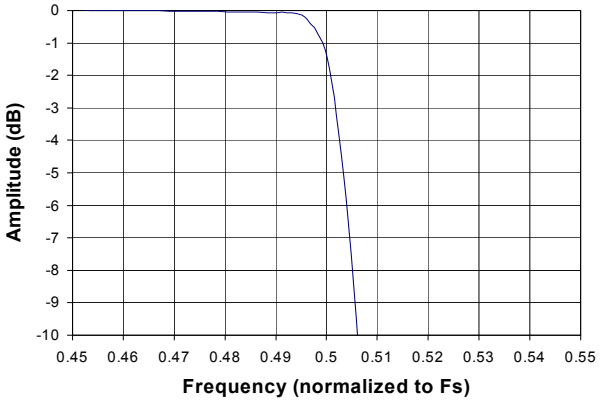


Figure 27. SSM Transition Band (Detail)

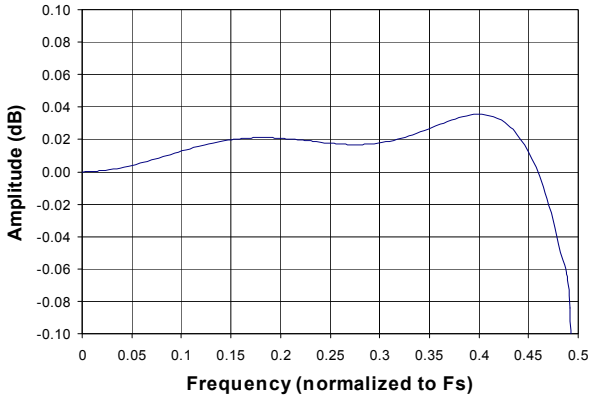


Figure 28. SSM Passband Ripple

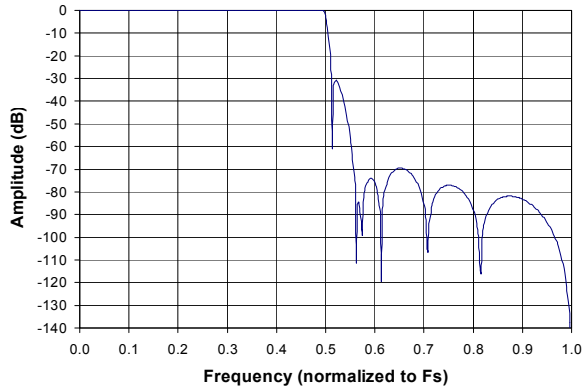


Figure 29. DSM Stopband Rejection

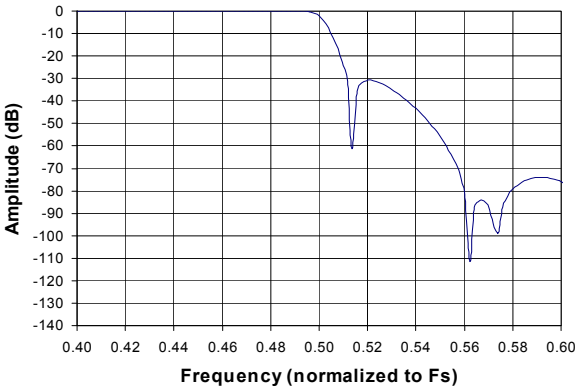


Figure 30. DSM Transition Band

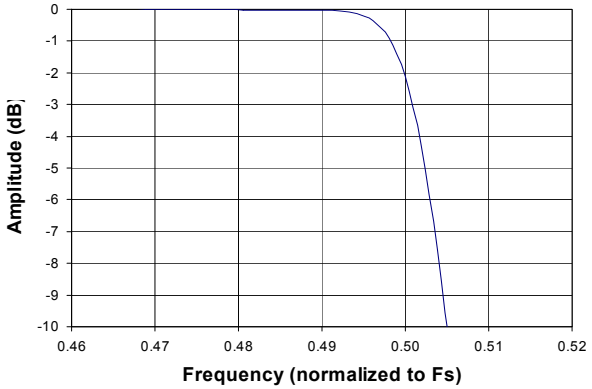


Figure 31. DSM Transition Band (Detail)

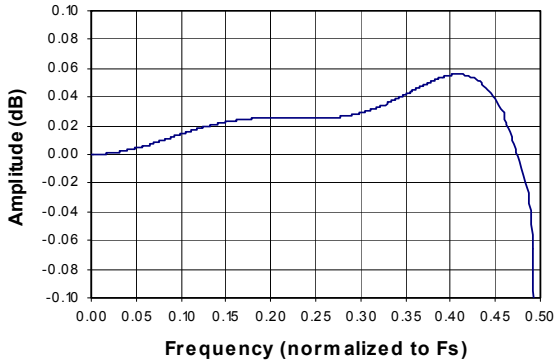


Figure 32. DSM Passband Ripple

10.DAC FILTER PLOTS

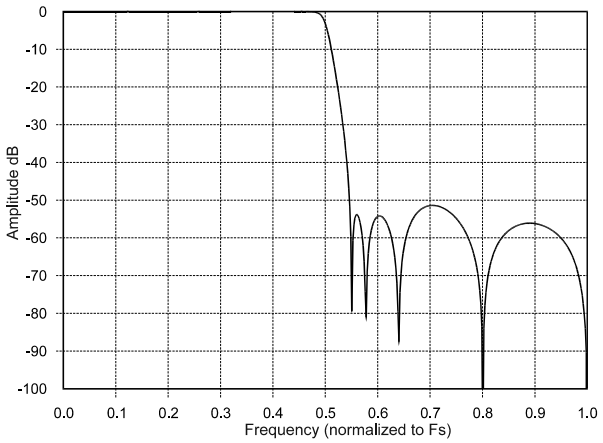


Figure 33. SSM Stopband Rejection

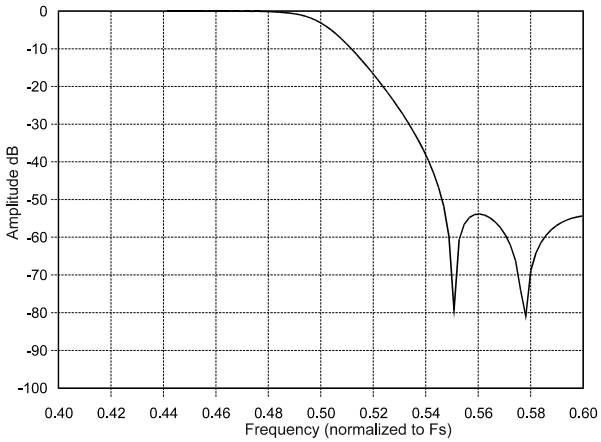


Figure 34. SSM Transition Band

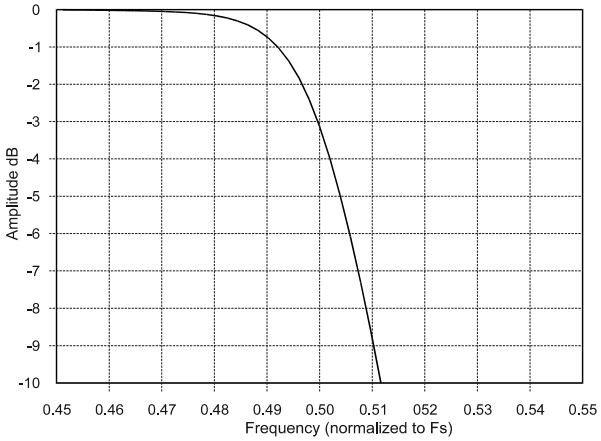


Figure 35. SSM Transition Band (detail)

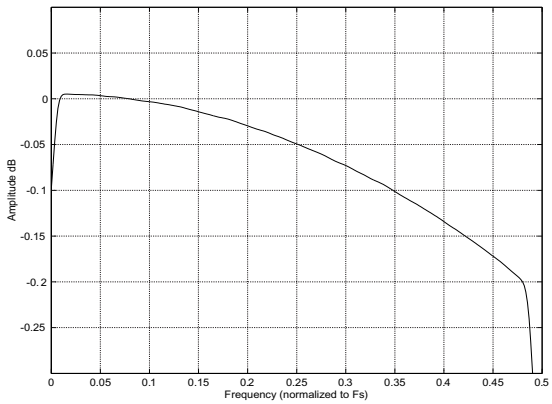


Figure 36. SSM Passband Ripple

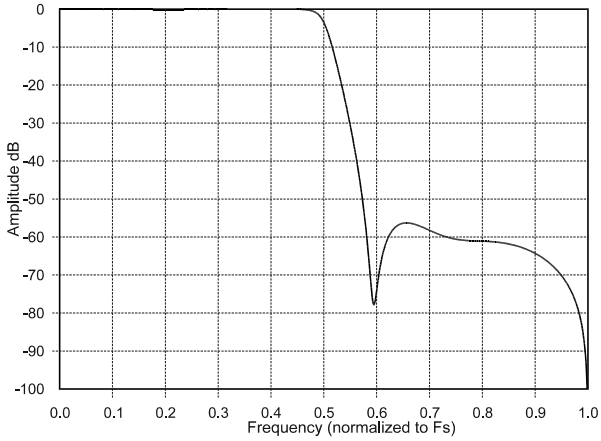


Figure 37. DSM Stopband Rejection

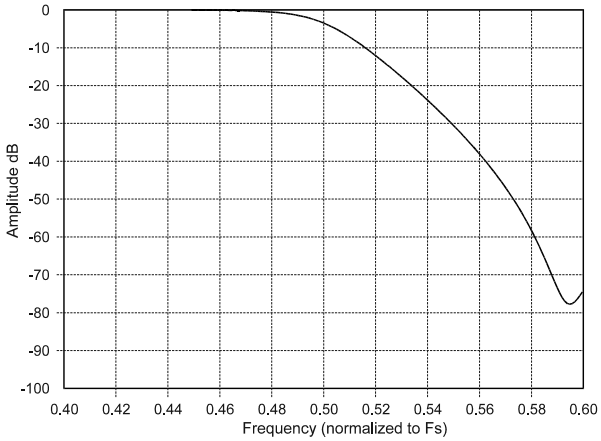


Figure 38. DSM Transition Band

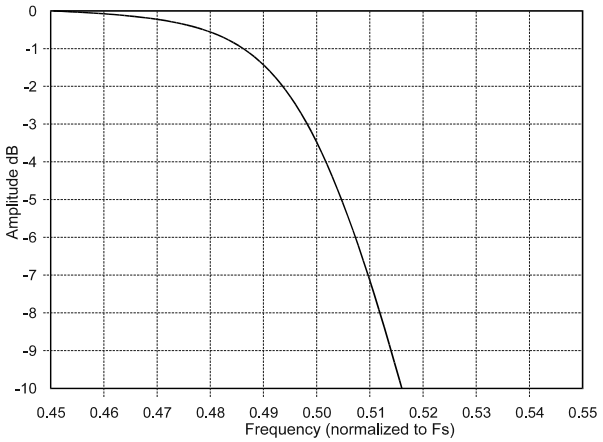


Figure 39. DSM Transition Band (detail)

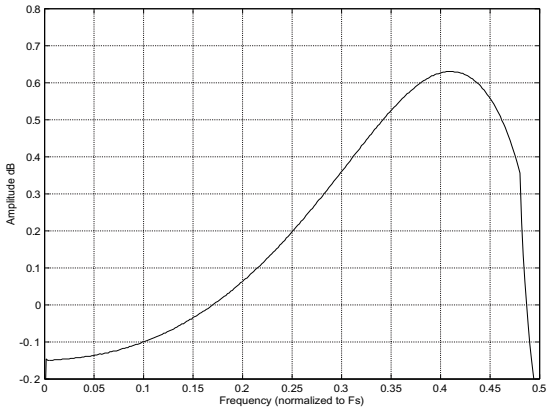


Figure 40. DSM Passband Ripple

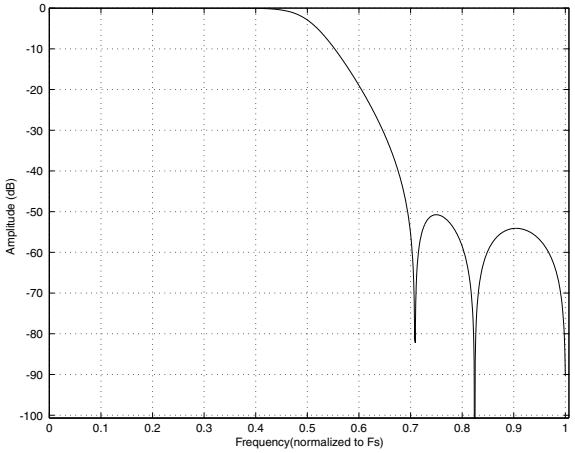


Figure 41. QSM Stopband Rejection

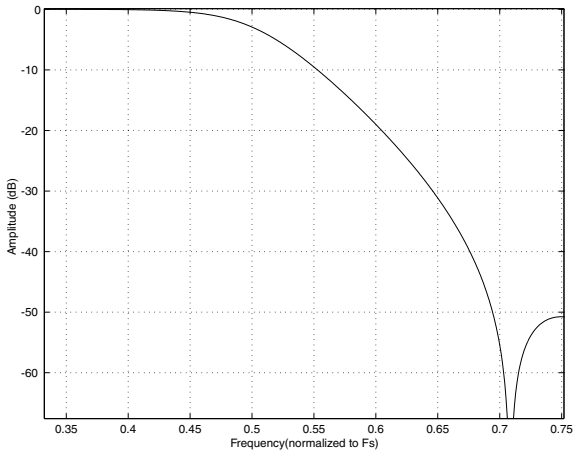


Figure 42. QSM Transition Band

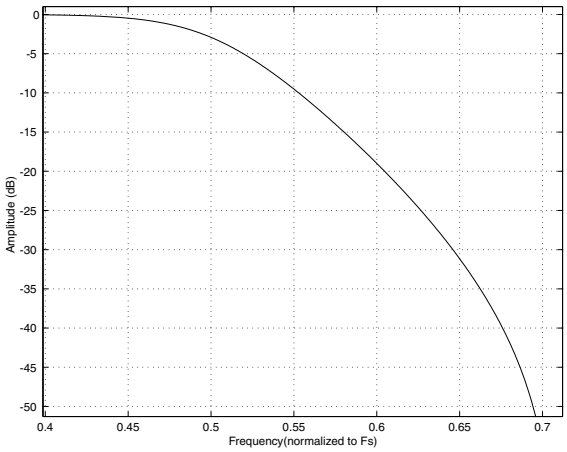


Figure 43. QSM Transition Band (detail)

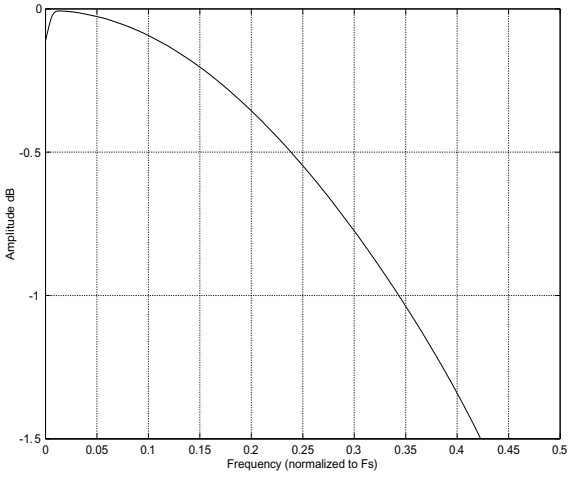


Figure 44. QSM Passband Ripple

11.PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified band width made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channel pairs. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channel pairs. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

Offset Error

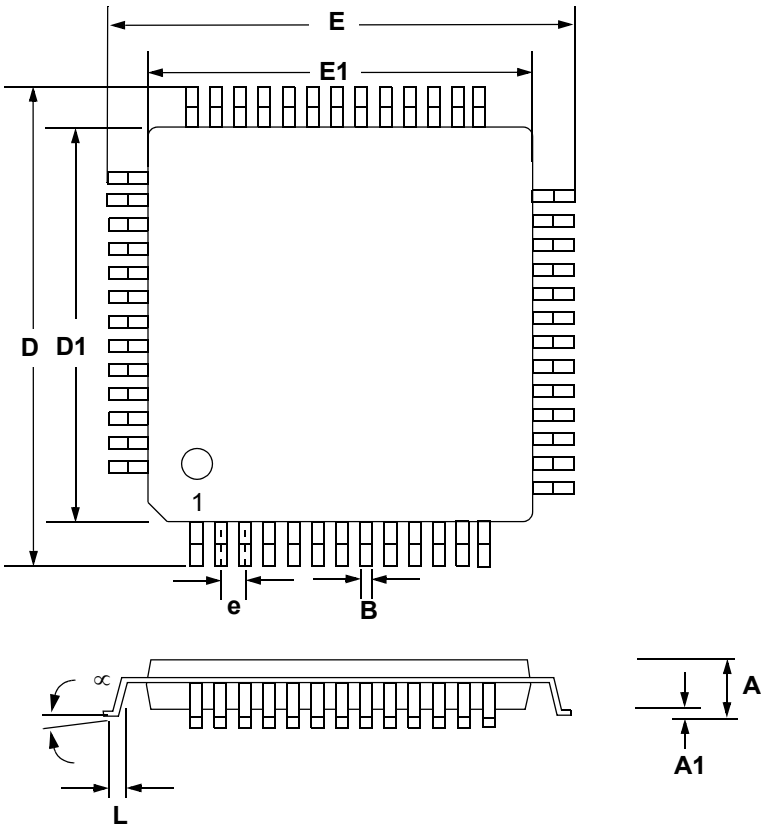
The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

12.REFERENCES

1. Cirrus Logic, *Techniques to Measure and Maximize the Performance of a 120 dB, 96 kHz A/D Converter Integrated Circuit*, by Steven Harris, Steven Green and Ka Leung. Presented at the 103rd Convention of the Audio Engineering Society, September 1997.
2. Cirrus Logic, *The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADC's*, by Steven Harris. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.
3. Philips Semiconductor, *The I²C-Bus Specification: Version 2.1*, January 2000. http://www.semiconductors.philips.com

13.PACKAGE INFORMATION

52L MQFP PACKAGE DRAWING



	INCHES			MILLIMETERS		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	0.096	---	---	2.45
A1	0.000	---	0.010	0.00	---	0.25
B	0.009	---	0.016	0.22	---	0.40
D	---	0.519	---	---	13.20 BSC	---
D1	---	0.394	---	---	10.00 BSC	---
E	---	0.519	---	---	13.20 BSC	---
E1	---	0.394	---	---	10.00 BSC	---
e*	---	0.026	---	---	0.65 BSC	---
L	0.029	0.035	0.041	0.73	0.88	1.03
µ	0.00°	4°	7.00°	0.00°	4°	7.00°

* Nominal pin pitch is 0.65 mm
Controlling dimension is mm.
JEDEC Designation: MS022

13.1 Thermal Characteristics

Parameter		Symbol	Min	Typ	Max	Units
Junction to Ambient Thermal Impedance	2 Layer Board	θ_{JA}	-	47	-	°C/Watt
	4 Layer Board	θ_{JA}	-	38	-	°C/Watt

14.ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS42435	4-in, 8-out, TDM CODEC for Surround Sound Apps	52L-MQFP	YES	Commercial	-40°C to +85°C	Rail	CS42435-CMZ
						Tape & Reel	CS42435-CMZR
				Automotive	-40°C to +105°C	Rail	CS42435-DMZ
						Tape & Reel	CS42435-DMZR
CDB42438	CS42435 evaluation board	-	-	-	-	-	CDB42438

15.REVISION HISTORY

Revision	Changes
F1	Initial Release
F2	Pin labels for Pins 3 and 4 were corrected in Figure 1. "Pin Descriptions - Software Mode" on page 6. Updated input impedance specification for Differential and Single-Ended Inputs in “Analog Input Characteristics (Commercial)” section on page 14 and “Analog Input Characteristics (Automotive)” section on page 15.
F3	Added Note 8 “The input impedance scales inversely proportionate to the sample rate of the ADC modulator” to “Analog Input Characteristics (Automotive)” section on page 15.
F4	• Updated Note 12 to regarding the triangular PDF dither in “Analog Output Characteristics (Automotive)” on page 18. • Updated MFreq2:0 == 001 and MFreq2:0 == 011 (ratios of 384x and 768x) to "Reserved" in Table 5.
F5	Updates to clarify the behavior of the ADC Overflow bit; full-scale signal with single-ended input. • Explanatory text preceding Figure 9 on page 27. • Explanatory text, “ADC Overflow (ADCX_OVFL)” on page 46

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.

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