CS4299

# CrystalClear® SoundFusion™ Audio Codec '97

## Features

- AC '97 2.1 Compatible
- Industry Leading Mixed Signal Technology
- 20-bit Stereo Digital-to-Analog Converters
- 18-bit Stereo Analog-to-Digital Converters
- Sample Rate Converters
- Four Analog Line-level Stereo Inputs for LINE_IN, CD, VIDEO, and AUX
- Two Analog Line-level Mono Inputs for Modem and Internal PC Beep
- Dual Stereo Line-level Outputs for LINE_OUT and ALT_LINE_OUT
- Dual Microphone Inputs
- High Quality Pseudo-Differential CD Input
- Extensive Power Management Support
- Meets or Exceeds the Microsoft® PC 99 Audio Performance Requirements
- S/PDIF Digital Audio Output
- CrystalClear® 3D Stereo Enhancement

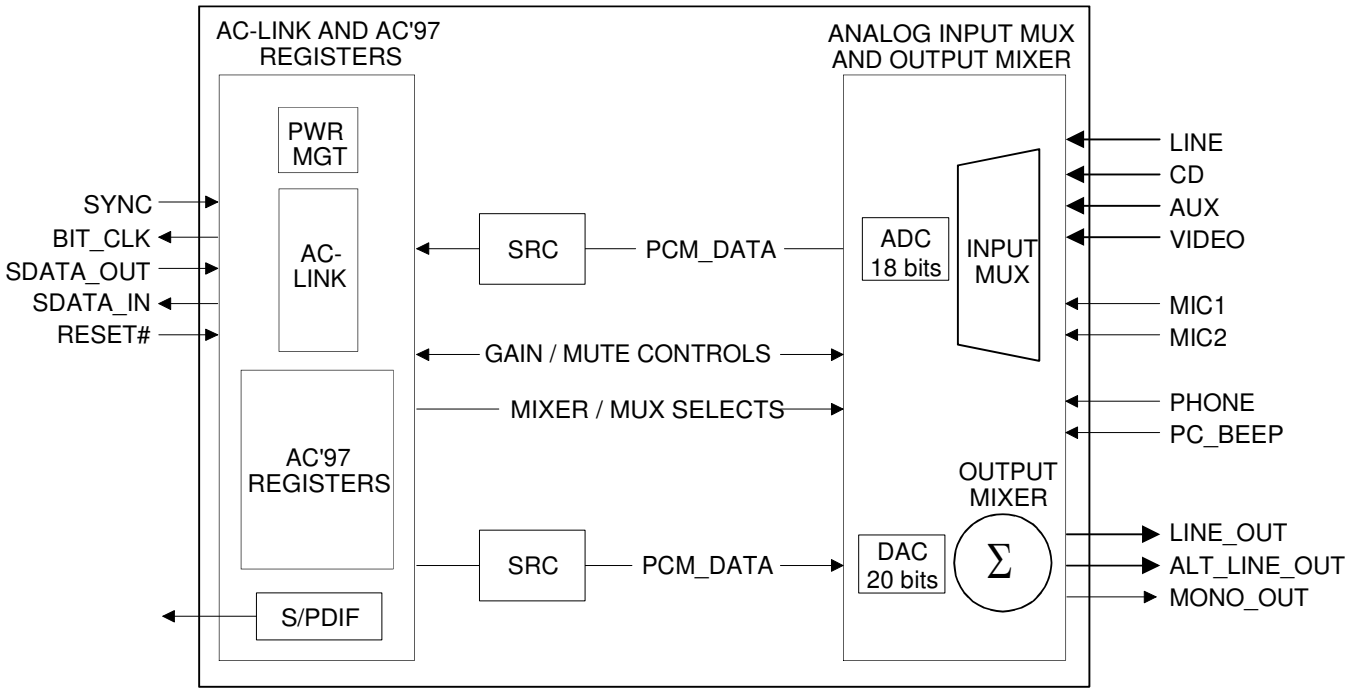
## Description

The CS4299 is an AC '97 2.1 compatible stereo audio codec designed for PC multimedia systems. Using the industry leading CrystalClear® delta-sigma and mixed signal technology, the CS4299 enables the design of PC 99-compliant desktop, portable, and entertainment PCs.

Coupling the CS4299 with a PCI audio accelerator or core logic supporting the AC '97 interface, implements a cost effective, superior quality, audio solution. The CS4299 surpasses PC 99 and AC '97 2.1 audio quality standards.

**ORDERING INFO**

CS4299-BQZ lead-free 48-pin LQFP 9x9x1.4 mm
CS4299-JQZ lead-free 48-pin LQFP 9x9x1.4 mm






Copyright © Cirrus Logic, Inc. 2001–2015
(All Rights Reserved)

# Table of Contents

**1 Characteristics and specifications ..... 4**
**2 General Description ..... 9**
2.1 AC-Link ..... 9
2.2 Control registers ..... 9
2.3 Sample Rate Converters ..... 9
2.4 Output Mixer ..... 10
2.5 Input Mux ..... 10
2.6 Volume Control ..... 10
**3 AC Link Frame Definition ..... 11**
3.1 AC-Link Serial Data Output Frame ..... 12
3.2 AC-Link Audio Input Frame ..... 14
3.3 AC-Link Protocol Violation - Loss of SYNC ..... 16
**4 Register Interface ..... 17**
**5 Power Management ..... 31**
5.1 AC '97 Reset Modes ..... 31
5.1.1 Cold AC '97 Reset ..... 31
5.1.2 Warm AC '97 Reset ..... 31
5.1.3 Register AC '97 Reset ..... 31
5.2 Powerdown Controls ..... 32
**6 Analog Hardware Description ..... 34**
6.1 Analog Inputs ..... 34
6.1.1 Line-Level Inputs ..... 34
6.1.2 CD Input ..... 34
6.1.3 Microphone Inputs ..... 35
6.1.4 PC Beep Input ..... 35
6.1.5 Phone Input ..... 36
6.2 Analog Outputs ..... 36
6.2.1 Stereo Outputs ..... 36
6.2.2 Mono Output ..... 37
6.3 Miscellaneous Analog Signals ..... 37
6.4 Power Supplies ..... 37
6.5 Reference Design ..... 37
**7 Sony/Philips Digital Interface (S/PDIF) ..... 38**
**8 Grounding and Layout ..... 38**
**9 Pin Descriptions ..... 40**
**10 Parameter and Term Definitions ..... 45**
**11 Reference Design ..... 47**
**12 References ..... 48**
**13 Package Dimensions ..... 49**
**14 Revision History ..... 50**

## List of Figures

Figure 1-1. Power Up Timing ..... 7
Figure 1-2. Codec Ready from Startup or Fault Condition ..... 7
Figure 1-3. Clocks ..... 7
Figure 1-4. Data Setup and Hold ..... 8
Figure 1-5. PR4 Powerdown and Warm Reset ..... 8
Figure 1-6. Test Mode ..... 8
Figure 2-1. AC-link Connections ..... 9
Figure 2-2. Mixer Diagram ..... 10
Figure 3-1. AC-link Input and Output Framing ..... 11
Figure 6-1. Differential 2 VRMS CD Input ..... 34
Figure 6-2. Differential 1 VRMS CD Input ..... 34
Figure 6-3. Microphone Input ..... 35
Figure 6-4. Microphone Pre-amplifier ..... 35
Figure 6-5. PC_BEEP Input ..... 35
Figure 6-6. Modem Connection ..... 36
Figure 6-7. Alternate Line Output as Headphone Output ..... 36
Figure 6-8. Stereo Output ..... 36
Figure 6-9. Voltage Regulator ..... 37
Figure 7-1. S/PDIF Output ..... 38
Figure 8-1. Conceptual Layout for the CS4299 ..... 39
Figure 9-1. Pin Locations for the CS4299 ..... 40
Figure 11-1. CS4299 Reference Design ..... 47

## List of Tables

Table 4-1. Mixer Registers ..... 17
Table 4-2. Analog Mixer Output Attenuation ..... 19
Table 4-3. Microphone Input Gain Values ..... 21
Table 4-4. Analog Mixer Input Gain Values ..... 22
Table 4-5. Stereo Volume Register Index ..... 22
Table 4-6. Input Mux Selection ..... 23
Table 4-7. Standard Sample Rates ..... 27
Table 4-8. Slot Mapping ..... 28
Table 4-9. Device ID with Corresponding Part Number ..... 30
Table 4-10. Revision Values ..... 30
Table 5-1. Powerdown PR Bit Functions ..... 32
Table 5-2. Powerdown PR Function Matrix ..... 32
Table 5-3. Power Consumption by Powerdown Mode ..... 33

# 1 Characteristics and specifications

**ANALOG CHARACTERISTICS** Standard test conditions unless otherwise noted: $T_{ambient}$ = 25° C, AVdd = 5.0 V ±5%, DVdd = 3.3 V ±5%; 1 kHz Input Sine wave; Sample Frequency, Fs = 48 kHz; $Z_{AL}$=100 kΩ/ 1000 pF load, $C_{DL}$ = 18 pF load (Note 1); Measurement bandwidth is 20 Hz - 20 kHz, 18-bit linear coding for ADC functions, 20-bit linear coding for DAC functions; Mixer registers set for unity gain.

| Parameter (Note 2) | Symbol | Path (Note 3) | CS4299-BQZ | | | CS4299-JQZ | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| Full Scale Input Voltage | | | | | | | | | |
| Line Inputs | | A-D | - | 1.00 | - | 0.91 | 1.00 | - | $V_{RMS}$ |
| Mic Inputs | | A-D | - | 1.00 | - | 0.91 | 1.00 | - | $V_{RMS}$ |
| Mic Inputs (20 dB internal gain) | | A-D | - | 0.10 | - | 0.091 | 0.10 | - | $V_{RMS}$ |
| Full Scale Output Voltage | | | | | | | | | |
| Line,Alternate Line, and Mono Outputs | | D-A | 0.85 | 1.0 | 1.15 | 0.91 | 1.0 | 1.13 | $V_{RMS}$ |
| Frequency Response (Note 4) | FR | | | | | | | | |
| Analog Ac = ± 0.25 dB | | A-A | 20 | - | 20,000 | 20 | - | 20,000 | Hz |
| DAC Ac = ± 0.25 dB | | D-A | 20 | - | 20,000 | 20 | - | 20,000 | Hz |
| ADC Ac = ± 0.25 dB | | A-D | 20 | - | 20,000 | 20 | - | 20,000 | Hz |
| Dynamic Range | DR | | | | | | | | |
| Stereo Analog inputs to LINE_OUT | | A-A | - | 90 | - | - | 90 | - | dB FS A |
| Mono Analog inputs to LINE_OUT | | A-A | - | 85 | - | - | 85 | - | dB FS A |
| DAC Dynamic Range | | D-A | - | 85 | - | - | 87 | - | dB FS A |
| ADC Dynamic Range | | A-D | - | 80 | - | - | 85 | - | dB FS A |
| DAC SNR (-20 dB FS input w/ CCIR-RMS filter on output) | SNR | D-A | - | 70 | - | - | - | - | dB |
| Total Harmonic Distortion + Noise (-3 dB FS input signal): | THD+N | | | | | | | | |
| Line/Alternate Line Output | | A-A | - | - | -72 | - | - | -74 | dB FS |
| DAC | | D-A | - | - | -72 | - | - | -74 | dB FS |
| ADC (all inputs except phone/mic) | | A-D | - | - | -72 | - | - | -74 | dB FS |
| ADC (phone/mic) | | A-D | - | - | -72 | - | - | -74 | dB FS |
| Power Supply Rejection Ratio (1 kHz, 0.5 $V_{RMS}$ w/ 5 V DC offset) (Note 4) | | | - | 40 | - | - | 40 | - | dB |
| Interchannel Isolation | | | - | 60 | - | - | 88 | - | dB |
| Spurious Tone (Note 4) | | | - | -100 | - | - | -100 | - | dB FS |
| Input Impedance (Note 4) | | | 10 | - | - | 10 | - | - | kΩ |
| External Load Impedance | | | 10 | - | - | 10 | - | - | kΩ |
| Output Impedance (Note 4) | | | - | 730 | - | - | 730 | - | Ω |
| Input Capacitance (Note 4) | | | - | 5 | - | - | 5 | - | pF |
| Vrefout | | | 2.0 | 2.28 | 2.5 | 2.0 | 2.28 | 2.5 | V |

**Notes:**

1. $Z_{AL}$ refers to the analog output pin loading and $C_{DL}$ refers to the digital output pin loading.
2. Parameter definitions are given in the Section 10, *Parameter and Term Definitions*.
3. Path refers to the signal path used to generate this data. These paths are defined in the Section 10, *Parameter and Term Definitions*.
4. This specification is guaranteed by silicon characterization, it is not production tested.

## ABSOLUTE MAXIMUM RATINGS (AVss1 = AVss2 = DVss1 = DVss2 = 0 V)

| Parameter | | Min | Min -BQZ | Typ | Max | Max -BQZ | Unit |
|---|---|---|---|---|---|---|---|
| Power Supplies | +3.3 V Digital | -0.3 | -0.3 | - | 6.0 | 6.0 | V |
| | +5 V Digital | -0.3 | -0.3 | - | 6.0 | 6.0 | V |
| | Analog | -0.3 | -0.3 | - | 6.0 | 6.0 | V |
| Total Power Dissipation | (Supplies, Inputs, Outputs) | - | - | - | 1.25 | 1.25 | W |
| Input Current per Pin | (Except Supply Pins) | -10 | -10 | - | 10 | 10 | mA |
| Output Current per Pin | (Except Supply Pins) | -15 | -15 | - | 15 | 15 | mA |
| Analog Input voltage | | -0.3 | -0.3 | - | AVdd+ 0.3 | AVdd+ 0.3 | V |
| Digital Input voltage | | -0.3 | -0.3 | - | DVdd + 0.3 | DVdd + 0.3 | V |
| Ambient Temperature | (Power Applied) | -55 | -40 | - | 110 | 85 | °C |
| Storage Temperature | | -65 | -65 | - | 150 | 150 | °C |

## RECOMMENDED OPERATING CONDITIONS (AVss1 = AVss2 = DVss1 = DVss2 = 0 V)

| Parameter | | Symbol | Min | Min -BQZ | Typ | Max | Max -BQZ | Unit |
|---|---|---|---|---|---|---|---|---|
| Power Supplies | +3.3 V Digital | DVdd1, DVdd2 | 3.135 | 3.135 | 3.3 | 3.465 | 3.465 | V |
| | +5 V Digital | DVdd1, DVdd2 | 4.75 | 4.75 | 5 | 5.25 | 5.25 | V |
| | Analog | AVdd1, AVdd2 | 4.75 | 4.75 | 5 | 5.25 | 5.25 | V |
| Operating Ambient Temperature | | | 0 | -40 | - | 70 | 85 | °C |

## DIGITAL CHARACTERISTICS (AVss = DVss = 0 V)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Low level input voltage | $V_{il}$ | - | - | 0.8 | V |
| High level input voltage | $V_{ih}$ | 0.65 x DVdd | - | - | V |
| High level output voltage | $V_{oh}$ | 0.90 x DVdd | 0.99 x DVdd | - | V |
| Low level output voltage | $V_{ol}$ | - | 0.03 | 0.10 x DVdd | V |
| Input Leakage Current (AC-link inputs) | | -10 | - | 10 | µA |
| Output Leakage Current (Tri-stated AC-link outputs) | | -10 | - | 10 | µA |
| Output buffer drive current | | | | | |
| BIT_CLK, S/PDIF_OUT | | - | 24 | - | mA |
| SDATA_IN, EAPD (Note 4) | | - | 4 | - | mA |

## AC '97 SERIAL PORT TIMING

Standard test conditions unless otherwise noted: $T_{ambient}$ = 25° C, AVdd = 5.0 V, DVdd = 3.3 V; $C_L$ = 55 pF load.

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ***RESET Timing*** | | | | | |
| RESET# active low pulse width | $T_{rst_low}$ | 1.0 | - | - | µs |
| RESET# inactive to BIT_CLK start-up delay | $T_{rst2clk}$ | - | 40.0 | - | µs |
| 1st SYNC active to CODEC READY set | $T_{sync2crd}$ | - | 62.5 | - | µs |
| Vdd stable to Reset inactive | $T_{vdd2rst\#}$ | 100 | - | - | µs |
| ***Clocks*** | | | | | |
| BIT_CLK frequency | $F_{clk}$ | - | 12.288 | - | MHz |
| BIT_CLK period | $T_{clk_period}$ | - | 81.4 | - | ns |
| BIT_CLK output jitter (depends on XTAL_IN source) | | - | - | 750 | ps |
| BIT_CLK high pulse width | $T_{clk_high}$ | 36 | 40.7 | 45 | ns |
| BIT_CLK low pulse width | $T_{clk_low}$ | 36 | 40.7 | 45 | ns |
| SYNC frequency | $F_{sync}$ | - | 48 | - | kHz |
| SYNC period | $T_{sync_period}$ | - | 20.8 | - | µs |
| SYNC high pulse width | $T_{sync_high}$ | - | 1.3 | - | µs |
| SYNC low pulse width | $T_{sync_low}$ | - | 19.5 | - | µs |
| ***Data Setup and Hold*** | | | | | |
| Output Propagation delay from rising edge of BIT_CLK | $T_{co}$ | 8 | 10 | 12 | ns |
| Input setup time from falling edge of BIT_CLK | $T_{isetup}$ | 10 | - | - | ns |
| Input hold time from falling edge of BIT_CLK | $T_{ihold}$ | 0 | - | - | ns |
| Input Signal rise time | $T_{irise}$ | 2 | - | 6 | ns |
| Input Signal fall time | $T_{ifall}$ | 2 | - | 6 | ns |
| Output Signal rise time (Note 4) | $T_{orise}$ | 2 | 4 | 6 | ns |
| Output Signal fall time (Note 4) | $T_{ofall}$ | 2 | 4 | 6 | ns |
| ***Misc. Timing Parameters*** | | | | | |
| End of Slot 2 to BIT_CLK, SDATA_IN low (PR4) | $T_{s2_pdown}$ | - | .28 | 1.0 | µs |
| SYNC pulse width (PR4) Warm Reset | $T_{sync_pr4}$ | 1.0 | - | - | µs |
| SYNC inactive (PR4) to BIT_CLK start-up delay | $T_{sync2clk}$ | 162.8 | 285 | - | ns |
| Setup to trailing edge of RESET# (ATE test mode) (Note 4) | $T_{setup2rst}$ | 15 | - | - | ns |
| Rising edge of RESET# to Hi-Z delay (Note 4) | $T_{off}$ | - | - | 25 | ns |

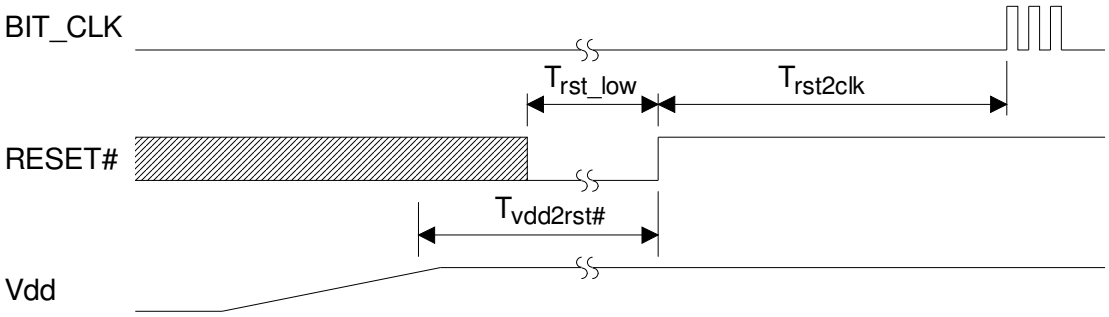



**Figure 1-1. Power Up Timing**

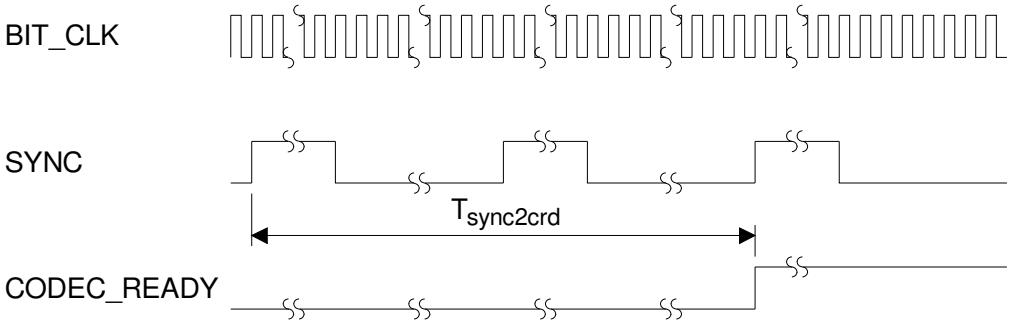



**Figure 1-2. Codec Ready from Startup or Fault Condition**

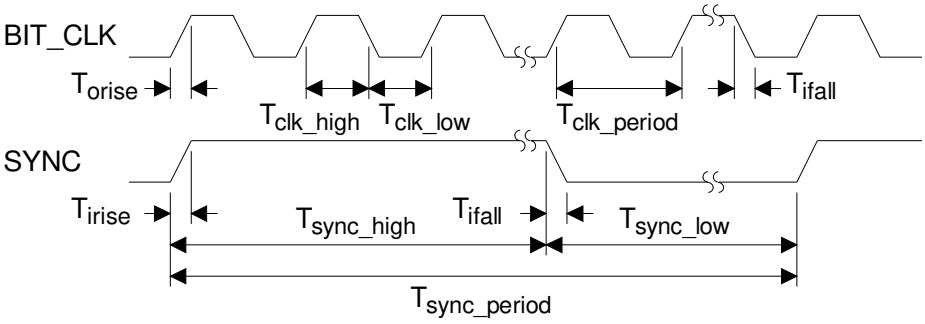



**Figure 1-3. Clocks**

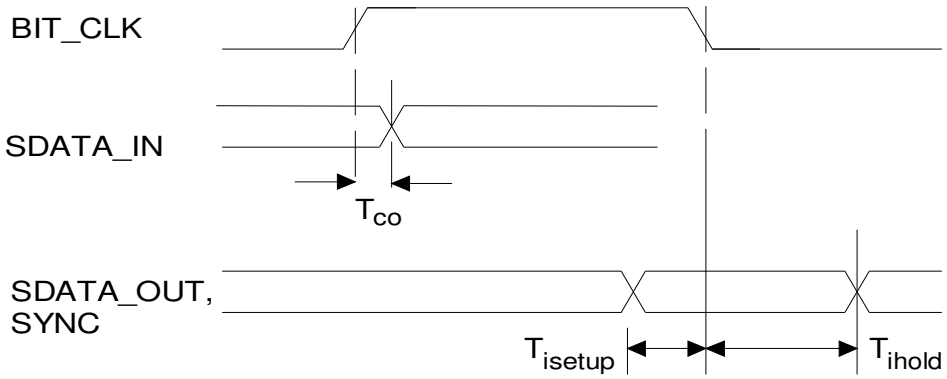



**Figure 1-4. Data Setup and Hold**

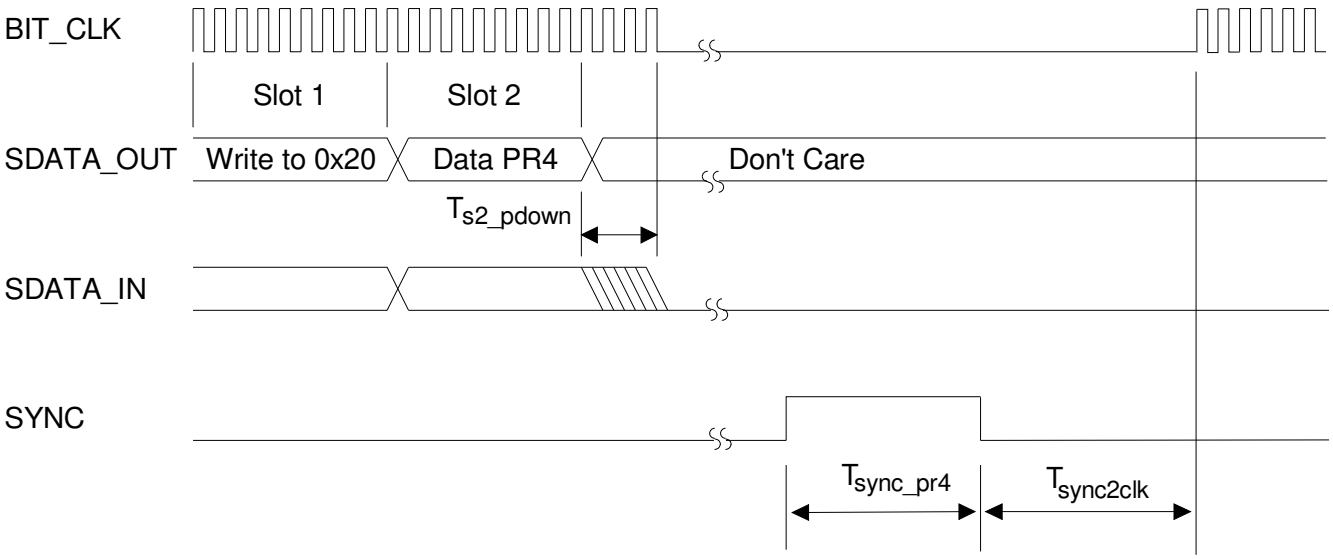



**Figure 1-5. PR4 Powerdown and Warm Reset**

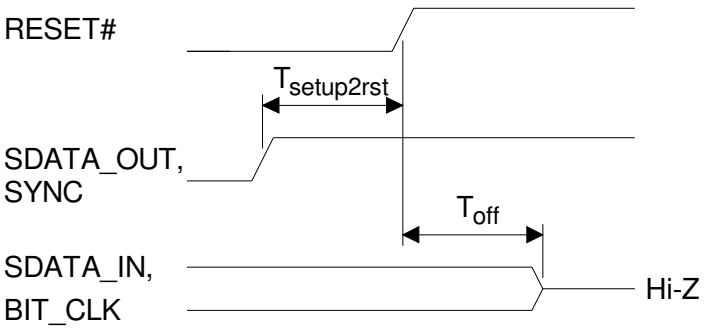



**Figure 1-6. Test Mode**

# 2 General Description

The CS4299 is a mixed-signal serial audio Codec compliant to the Intel® *Audio Codec '97 Specification*, revision 2.1 [1]. It is designed to be paired with a digital controller, typically located on the PCI bus or integrated within the system core logic chip set. The controller is responsible for all communications between the CS4299 and the remainder of the system. The CS4299 contains two distinct functional sections: digital and analog. The digital section includes the AC-link interface, S/PDIF interface, serial data port, Sample Rate Converters, and power management support. The analog section includes the analog input multiplexer (mux), stereo output mixer, mono output mixer, stereo Analog-to-Digital Converters (ADCs), stereo Digital-to-Analog Converters (DACs), and their associated volume controls.

## 2.1 AC-Link

All communication with the CS4299 is established with a 5-wire digital interface to the controller, as shown in Fig. 2-1. This interface is called the AC-link. All clocking for the serial communication is synchronous to the BIT_CLK signal. BIT_CLK is generated by the primary audio codec and is used to clock the controller and any secondary audio codecs. Both input and output AC-link audio frames are organized as a sequence of 256 serial bits forming 13 groups referred to as 'slots'. During each audio frame, data is passed bi-directionally between the CS4299 and the controller. The input frame is driven from the CS4299 on the SDATA_IN line. The output frame is driven from the controller on the SDATA_OUT line. The controller is also responsible for issuing reset commands via the RESET# signal. Following a Cold Reset, the CS4299 is responsible for notifying the controller that it is ready for operation after synchronizing its internal functions. The CS4299 AC-link signals must use the same digital supply voltage as the controller chip, either +5 V or +3.3 V. See Section 3, *AC Link Frame Definition*, for detailed AC-link information.

## 2.2 Control registers

The CS4299 contains a set of AC '97 compliant control registers and a set of Cirrus Logic defined control registers. These registers control the basic functions and features of the CS4299. Read accesses of the control registers by the AC '97 controller are accomplished with the requested register index in Slot 1 of a SDATA_OUT frame. The following SDATA_IN frame will contain the read data in its Slot 2. Write operations are similar, with the register index in Slot 1 and the write data in Slot 2 of a SDATA_OUT frame. The function of each input and output frame is detailed in Section 3, *AC Link Frame Definition*. Individual register descriptions are found in Section 4, *Register Interface*.

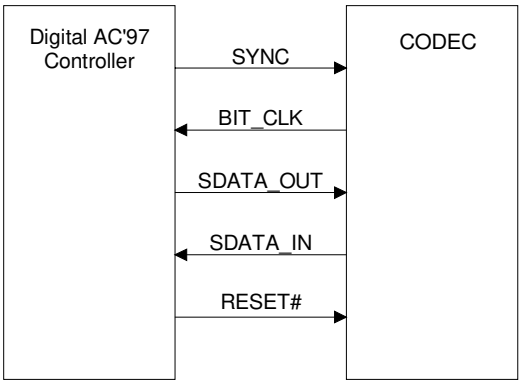



**Figure 2-1. AC-link Connections**

## 2.3 Sample Rate Converters

The Sample Rate Converters (SRCs) provide high accuracy digital filters supporting sample frequencies other than 48 kHz to be captured from the CS4299 or played from the controller. AC '97 requires support for two audio rates (44.1 and 48kHz). In addition, the Intel® I/O Controller Hub (ICHx) specification requires support for five more audio rates (8, 11.025, 16, 22.05, and 32). The CS4299 supports all these rate, as shown in Table 4-7 on page 27.

## 2.4 Output Mixer

The CS4299 has two output mixers, illustrated in Fig. 2-2. The stereo output mixer sums together the analog inputs to the CS4299, including the PC_BEEP and PHONE signals, according to the settings in the volume control registers. The stereo output mix is sent to the LINE_OUT and ALT_LINE_OUT pins on the CS4299. The mono output mixer generates a monophonic sum of the left and right channels from the stereo input mixer. The mono output mix is sent to the MONO_ OUT output pin on the CS4299.

## 2.5 Input Mux

The input multiplexer controls which analog input is sent to the ADCs. The output of the input mux is converted to stereo 18-bit digital PCM data and sent to the controller by means of the AC-link SDATA_IN signal.

## 2.6 Volume Control

The CS4299 volume registers control analog input levels to the input mixer and analog output levels, including the master volume level, and the alternate volume level. The PC_BEEP volume control uses 3 dB steps with a range of 0 dB to -45 dB attenuation. All other analog volume controls use 1.5 dB steps. The analog inputs have a mixing range of +12 dB signal gain to -34.5 dB signal attenuation. The analog output volume controls have from 0 dB to -94.5 dB attenuation for LINE_ OUT and from 0 dB to -46.5 dB attenuation for ALT_LINE_OUT and MONO_OUT.

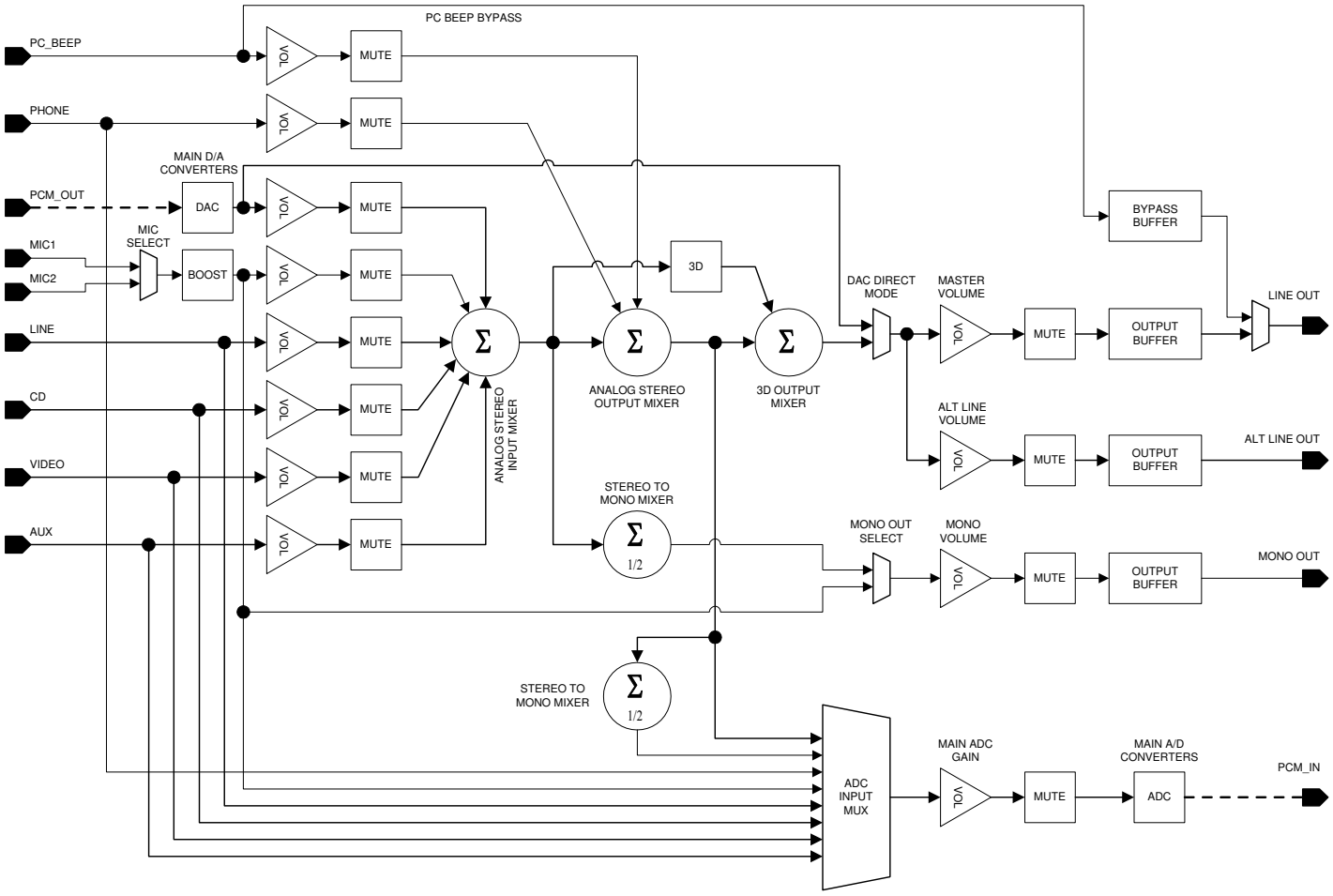



**Figure 2-2. Mixer Diagram**

# 3 AC Link Frame Definition

The AC-link is a bidirectional serial port with data organized into frames consisting of one 16-bit and twelve 20-bit time-division multiplexed slots. The first slot, called the tag slot, contains bits indicating if the CS4299 is ready to receive data (input frame) and which, if any, other slots contain valid data. Slots 1 through 12 contain audio or control/status data. Both the serial data output and input frames are defined from the controller perspective, not from the CS4299 perspective.

The controller synchronizes the beginning of a frame with the assertion of the SYNC signal. Fig. 3-1 shows the position of each bit location within the frame. The first bit position in a new serial data frame is F0 and the last bit position in the serial data frame is F255. When SYNC goes active (high) and is sampled active by the CS4299 (on the falling edge of BIT_CLK), both devices are synchronized to a new serial data frame. The data on the SDATA_OUT pin at this clock edge is the final bit of the previous frame's serial data. On the next rising edge of BIT_CLK, the first bit of Slot 0 is driven by the controller on the SDATA_OUT pin. On the next falling edge of BIT_CLK, the CS4299 latches this data in, as the first bit of the frame.

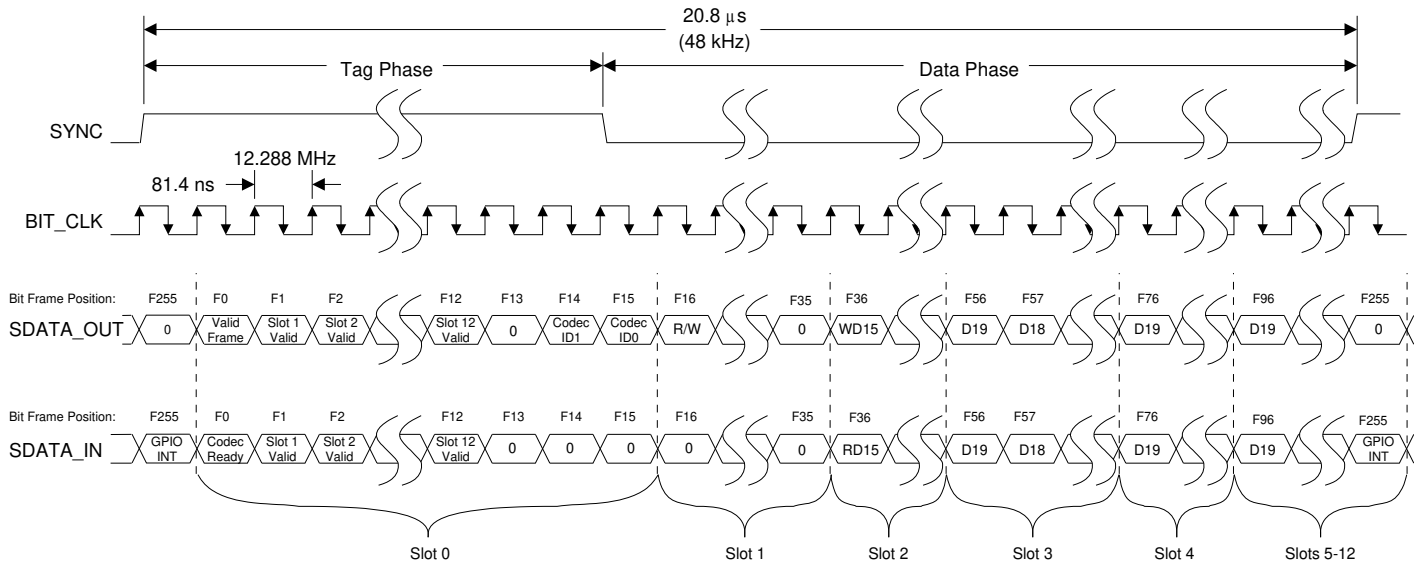



**Figure 3-1. AC-link Input and Output Framing**

## 3.1 AC-Link Serial Data Output Frame

In the serial data output frame, data is passed on the SDATA_OUT pin to the CS4299 from the AC '97 controller. Fig. 3-1 illustrates the serial port timing.

The PCM playback data being passed to the CS4299 is shifted out MSB first in the most significant bits of each slot. Any PCM data from the AC '97 controller that is not 20 bits wide should be left justified in its corresponding slot and dithered or zero-padded in the unused bit positions.

Bits that are reserved should always be 'cleared' by the AC '97 controller.

### *3.1.1 Serial Data Output Slot Tags (Slot 0)*

| Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Valid Frame | Slot 1 Valid | Slot 2 Valid | Slot 3 Valid | Slot 4 Valid | Slot 5 Valid | Slot 6 Valid | Slot 7 Valid | Slot 8 Valid | Slot 9 Valid | Slot 10 Valid | Reserved | | | Codec ID1 | Codec ID0 |

Valid Frame — The Valid Frame bit determines if any of the following slots contain either valid playback data for the CS4299 DACs or data for read/write operations. When 'set', at least one of the other AC-link slots contain valid data. If this bit is 'clear', the remainder of the frame is ignored.

Slot [1:2] Valid — The Slot [1:2] Valid bits indicate the validity of data in their corresponding serial data output slots. If a bit is 'set', the corresponding output slot contains valid data. If a bit is 'cleared', the corresponding slot will be ignored.

Slot [3:10] Valid — The Slot [3:10] Valid bits indicate Slot [3:10] contains valid playback data for the CS4299. If a Slot Valid bit is 'set', the named slot contains valid audio data. If the bit is 'clear', the slot will be ignored. The CS4299 supports alternate slot mapping as defined in the AC '97 2.1 specification. For more information, see the *AC Mode Control Register (Index 5Eh)*.

Codec ID[1:0] — The Codec ID[1:0] bits display the Codec ID of the audio codec being accessed during the current AC-link frame. Codec ID[1:0] = 00 indicates the primary codec is being accessed. Codec ID[1:0] = 01, 10, or 11 indicates one of three possible secondary codecs is being accessed. A non-zero value of one or more of the Codec ID bits indicates a valid Read or Write Address in Slot 1, and the Slot 1 R/W bit indicates presence or absence of valid Data in Slot 2.

### 3.1.2 Command Address Port (Slot 1)

| Bit 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R/$\overline{W}$ | RI6 | RI5 | RI4 | RI3 | RI2 | RI1 | RI0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

R/$\overline{W}$ — Read/$\overline{Write}$. When this bit is 'set', a read of the AC '97 register specified by the register index bits will occur in the AC '97 2.1 audio codec. When the bit is 'cleared', a write will occur. For any read or write access to occur, the Frame Valid bit (F0) must be 'set' and the Codec ID[1:0] bits (F[14:15]) must match the Codec ID of the AC '97 2.1 audio codec being accessed. Additionally, for a primary codec, the Slot 1 Valid bit (F1) must be 'set' for a read access and both the Slot 1 Valid bit (F1) and the Slot 2 Valid bit (F2) must be 'set' for a write access. For a secondary codec, both the Slot 1 Valid bit (F1) and the Slot 2 Valid bit (F2) must be 'cleared' for read and write accesses. See Fig. 3-1 for bit frame positions.

RI[6:0] — Register Index. The RI[6:0] bits contain the 7-bit register index to the AC '97 registers in the CS4299. All registers are defined at word addressable boundaries. The RI0 bit must be 'clear' to access CS4299 registers.

### 3.1.3 Command Data Port (Slot 2)

| Bit 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| WD15 | WD14 | WD13 | WD12 | WD11 | WD10 | WD9 | WD8 | WD7 | WD6 | WD5 | WD4 | WD3 | WD2 | WD1 | WD0 | Reserved | | | |

WD[15:0] — Write Data. The WD[15:0] bits contain the 16-bit value to be written to the register. If an access is a read, this slot is ignored.

NOTE: For any write to an AC '97 register, the write is defined to be an 'atomic' access. This means that when the Slot 1 Valid bit in output Slot 0 is 'set', the Slot 2 Valid bit in output slot 0 should always be 'set' during the same audio frame. No write access may be split across 2 frames.

### 3.1.4 PCM Playback Data (Slots 3-10)

| Bit 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PD19 | PD18 | PD17 | PD16 | PD15 | PD14 | PD13 | PD12 | PD11 | PD10 | PD9 | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |

PD[19:0] — Playback Data. The PD[19:0] bits contain the 20-bit PCM playback (2's complement) data for the left and right DACs and/or the S/PDIF transmitter. Table 4-8 on page 28 lists a cross reference for each function and its respective slot. The mapping of a given slot to a DAC is determined by the state of the ID[1:0] bits in the *Extended Audio ID Register (Index 28h)* and by the SM[1:0] and AMAP bits in the *AC Mode Control Register (Index 5Eh).*

## 3.2 AC-Link Audio Input Frame

In the serial data input frame, data is passed on the SDATA_IN pin from the CS4299 to the AC '97 controller. The data format for the input frame is very similar to the output frame. Fig. 3-1 illustrates the serial port timing.

The PCM capture data from the CS4299 is shifted out MSB first in the most significant 18 bits of each slot. The least significant 2 bits in each slot will be 'cleared'. If the host requests PCM data from the AC '97 Controller that is less than 18 bits wide, the controller should dither and round or just round (but not truncate) to the desired bit depth.

Bits that are reserved or not implemented in the CS4299 will always be returned 'cleared'.

### *3.2.1 Serial Data Input Slot Tag Bits (Slot 0)*

| Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Codec Ready | Slot 1 Valid | Slot 2 Valid | Slot 3 Valid | Slot 4 Valid | Slot 5 Valid | Slot 6 Valid | Slot 7 Valid | Slot 8 Valid | Slot 9 Valid | Slot 10 Valid | 0 | 0 | 0 | 0 | 0 |

Codec Ready — The Codec Ready bit indicates the readiness of the CS4299 AC-link. Immediately after a Cold Reset this bit will be 'clear'. Once the CS4299 clocks and voltages are stable, this bit will be 'set'. Until the Codec Ready bit is 'set', no AC-link transactions should be attempted by the controller. The Codec Ready bit does not indicate readiness of the DACs, ADCs, Vref, or any other analog function. Those must be checked in the *Powerdown Control/Status Register (Index 26h)* by the controller before any access is made to the mixer registers. Any accesses to the CS4299 while Codec Ready is 'clear' are ignored.

Slot 1 Valid — When 'set', the Slot 1 Valid bit indicates Slot 1 contains a valid read back address.

Slot 2 Valid — When 'set', the Slot 2 Valid bit indicates Slot 2 contains valid register read data.

Slot [3:10] Valid — When 'set', the Slot [3:10] Valid bits indicate Slot [3:10] contains valid capture data from the CS4299 ADCs. Only if a Slot [3:10] Valid bit is 'set' will the corresponding input slot contain valid data.

### *3.2.2 Status Address Port (Slot 1)*

| Bit 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | RI6 | RI5 | RI4 | RI3 | RI2 | RI1 | RI0 | SR3 | SR4 | SR5 | SR6 | SR7 | SR8 | SR9 | SR10 | 0 | Reserved | | |

RI[6:0] — Register Index. The RI[6:0] bits echo the AC '97 register address when a register read has been requested in the previous frame. The CS4299 will only echo the register index for a read access. Write accesses will not return valid data in Slot 1.

SR[3:10] — Slot Request. If SRx is 'set', this indicates the CS4299 SRC does not need a new sample on the next AC-link frame for that particular slot. If SRx is 'clear', the SRC indicates a new sample is needed on the following frame. If the VRA bit in the *Extended Audio Status/Control Register (Index 2Ah)* is 'clear', the SR[3:10] bits are always 0. When VRA is 'set', the SRC is enabled and the SR[3:10] bits are used to request data.

### *3.2.3 Status Data Port (Slot 2)*

| Bit 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RD15 | RD14 | RD13 | RD12 | RD11 | RD10 | RD9 | RD8 | RD7 | RD6 | RD5 | RD4 | RD3 | RD2 | RD1 | RD0 | Reserved | | | |

RD[15:0] Read Data. The RD[15:0] bits contain the register data requested by the controller from the previous read request. All read requests will return the read address in the input Slot 1 and the register data in the input Slot 2 on the following serial data frame.

### *3.2.4 PCM Capture Data (Slot 3-10)*

| Bit 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD17 | CD16 | CD15 | CD14 | CD13 | CD12 | CD11 | CD10 | CD9 | CD8 | CD7 | CD6 | CD5 | CD4 | CD3 | CD2 | CD1 | CD0 | 0 | 0 |

CD[17:0] Capture Data. The D[17:0] bits contain 18-bit PCM (2's complement) capture data. The mapping of a given slot to an ADC is determined by the state of the ID[1:0] bits in the *Extended Audio ID Register (Index 28h)* and the SM[1:0] and AMAP bits in the *AC Mode Control Register (Index 5Eh).* The definition of each slot can be found in Table 4-8 on page 28.

## 3.3 AC-Link Protocol Violation - Loss of SYNC

The CS4299 is designed to handle SYNC protocol violations. The following are situations where the SYNC protocol has been violated:

- The SYNC signal is not sampled high for exactly 16 BIT_CLK clock cycles at the start of an audio frame.
- The SYNC signal is not sampled high on the 256th BIT_CLK clock period after the previous SYNC assertion.
- The SYNC signal goes active high before the 256th BIT_CLK clock period after the previous SYNC assertion.

Upon loss of synchronization with the controller, the CS4299 will 'clear' the Codec Ready bit in the serial data input frame until two valid frames are detected. During this detection period, the CS4299 will ignore all register reads and writes and will discontinue the transmission of PCM capture data. In addition, if the LOSM bit in the *Misc. Crystal Control Register (Index 60h)* is 'set' (default), the CS4299 will mute all analog outputs. If the LOSM bit is 'clear', the analog outputs will not be muted.

# 4 Register Interface

**Table 4-1. Mixer Registers**

| Reg | Register Name | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 00h | Reset | 0 | SE4 | SE3 | SE2 | SE1 | SE0 | 0 | ID8 | ID7 | 0 | 0 | ID4 | 0 | 0 | 0 | 0 | 1990h |
| 02h | Master Volume | Mute | 0 | ML5 | ML4 | ML3 | ML2 | ML1 | ML0 | 0 | 0 | MR5 | MR4 | MR3 | MR2 | MR1 | MR0 | 8000h |
| 04h | Alternate Volume | Mute | 0 | ML5 | ML4 | ML3 | ML2 | ML1 | ML0 | 0 | 0 | MR5 | MR4 | MR3 | MR2 | MR1 | MR0 | 8000h |
| 06h | Mono Volume | Mute | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MM5 | MM4 | MM3 | MM2 | MM1 | MM0 | 8000h |
| 0Ah | PC_BEEP Volume | Mute | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PV3 | PV2 | PV1 | PV0 | 0 | 0000h |
| 0Ch | Phone Volume | Mute | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | GN4 | GN3 | GN2 | GN1 | GN0 | 8008h |
| 0Eh | Mic Volume | Mute | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 20dB | 0 | GN4 | GN3 | GN2 | GN1 | GN0 | 8008h |
| 10h | Line In Volume | Mute | 0 | 0 | GL4 | GL3 | GL2 | GL1 | GL0 | 0 | 0 | 0 | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h |
| 12h | CD Volume | Mute | 0 | 0 | GL4 | GL3 | GL2 | GL1 | GL0 | 0 | 0 | 0 | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h |
| 14h | Video Volume | Mute | 0 | 0 | GL4 | GL3 | GL2 | GL1 | GL0 | 0 | 0 | 0 | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h |
| 16h | Aux Volume | Mute | 0 | 0 | GL4 | GL3 | GL2 | GL1 | GL0 | 0 | 0 | 0 | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h |
| 18h | PCM Out Volume | Mute | 0 | 0 | GL4 | GL3 | GL2 | GL1 | GL0 | 0 | 0 | 0 | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h |
| 1Ah | Record Select | 0 | 0 | 0 | 0 | 0 | SL2 | SL1 | SL0 | 0 | 0 | 0 | 0 | 0 | SR2 | SR1 | SR0 | 0000h |
| 1Ch | Record Gain | Mute | 0 | 0 | 0 | GL3 | GL2 | GL1 | GL0 | 0 | 0 | 0 | 0 | GR3 | GR2 | GR1 | GR0 | 8000h |
| 20h | General Purpose | 0 | 0 | 3D | 0 | 0 | 0 | MIX | MS | LPBK | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000h |
| 22h | 3D Control | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | S3 | S2 | S1 | S0 | 0000h |
| 26h | Powerdown Ctrl/Stat | EAPD | PR6 | PR5 | PR4 | PR3 | PR2 | PR1 | PR0 | 0 | 0 | 0 | 0 | REF | ANL | DAC | ADC | 000Fh |
| 28h | Extended Audio ID | ID1 | ID0 | 0 | 0 | 0 | 0 | AMAP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VRA | 0201h |
| 2Ah | Extended Audio Ctrl/Stat | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VRA | 0000h |
| 2Ch | PCM Front DAC Rate | SR15 | SR14 | SR13 | SR12 | SR11 | SR10 | SR9 | SR8 | SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 | BB80h |
| 32h | PCM L/R ADC Rate | SR15 | SR14 | SR13 | SR12 | SR11 | SR10 | SR9 | SR8 | SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 | BB80h |
| **Cirrus Logic Defined Registers**: | | | | | | | | | | | | | | | | | | |
| 5E | AC Mode Control | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DDM | AMAP | 0 | SM1 | SM0 | 0 | 0 | 0 | 0 | 0080h |
| 60 | Misc. Crystal Control | 0 | 0 | 0 | 0 | Reserved | | | | 0 | 0 | Reserved | | 0 | Reserved | | LOSM | 0023h |
| 68 | S/PDIF Control | SPEN | Val | 0 | Fs | L | CC6 | CC5 | CC4 | CC3 | CC2 | CC1 | CC0 | Emph | Copy | /Audio | Pro | 0000h |
| 7Ch | Vendor ID1(CR) | F7 | F6 | F5 | F4 | F3 | F4 | F1 | F0 | S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 | 4352h |
| 7Eh | Vendor ID2(Y-) | T7 | T6 | T5 | T4 | T3 | T2 | T1 | T0 | 0 | DID2 | DID1 | DID0 | 0 | REV2 | REV1 | REV0 | 5931h |

### 4.1 Reset Register (Index 00h)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | SE4 | SE3 | SE2 | SE1 | SE0 | 0 | ID8 | ID7 | 0 | 0 | ID4 | 0 | 0 | 0 | 0 |

SE[4:0] Crystal 3D Stereo Enhancement. SE[4:0] = 00110, indicating this feature is present.

ID8 18-bit ADC Resolution. The ID8 bit is 'set', indicating this feature is present.

ID7 20-bit DAC resolution. The ID7 bit is 'set', indicating this feature is present.

ID4 Headphone Output (Alt Line Out). The ID4 bit is 'set', indicating this feature is present.

Default 1990h. The data in this register is read-only data.

Any write to this register causes a Register Reset to the default state of the audio *(Index 00h - 38h)* and vendor specific *(Index 5Ah - 7Ah)* registers. A read from this register returns configuration information about the CS4299.

### 4.2 Master Volume Register (Index 02h)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Mute | 0 | ML5 | ML4 | ML3 | ML2 | ML1 | ML0 | 0 | 0 | MR5 | MR4 | MR3 | MR2 | MR1 | MR0 |

Mute Master Mute. Setting this bit mutes the LINE_OUT_L/R output signals.

ML[5:0] Master Volume Left. These bits control the left master output volume. Each step corresponds to 1.5 dB gain adjustment, with 00000 = 0 dB. The total range is 0 dB to -94.5 dB attenuation.

MR[5:0] Master Volume Right. These bits control the right master output volume. Each step corresponds to 1.5 dB gain adjustment, with 00000 = 0 dB. The total range is 0 dB to -94.5 dB attenuation.

Default 8000h. This value corresponds to 0 dB attenuation and Mute 'set'.

### 4.3 Alternate Volume Register (Index 04h)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Mute | 0 | ML5 | ML4 | ML3 | ML2 | ML1 | ML0 | 0 | 0 | MR5 | MR4 | MR3 | MR2 | MR1 | MR0 |

Mute — Alternate Mute. Setting this bit mutes the ALT_LINE_OUT_L/R output signals.

ML[4:0] — Alternate Volume Left. These bits control the left alternate output volume. Each step corresponds to 1.5 dB gain adjustment, with 00000 = 0 dB. The total range is 0 dB to -46.5 dB attenuation. See Table 4-2 for further attenuation levels.

ML5 — Alternate Volume Left Max Attenuation. Setting ML5 sets the left channel attenuation to -46.5 dB by forcing ML[4:0] to a '1' state. ML[5:0] will read back 011111 when ML5 has been 'set'. Table 4-2 summarizes this behavior.

MR[4:0] — Alternate Volume Right. These bits control the right alternate output volume. Each step corresponds to 1.5 dB gain adjustment, with 00000 = 0 dB. The total range is 0 dB to -46.5 dB attenuation. See Table 4-2 for further attenuation levels.

MR5 — Alternate Volume Right Max Attenuation. Setting MR5 sets the right channel attenuation to -46.5 dB by forcing MR[4:0] to a '1' state. MR[5:0] will read back 011111 when MR5 has been 'set'. Table 4-2 summarizes this behavior.

Default — 8000h. This value corresponds to 0 dB attenuation and Mute 'set'.

**Table 4-2. Analog Mixer Output Attenuation**

| Mx[5:0] Write | Mx[5:0] Read | Gain Level |
|---|---|---|
| 000000 | 000000 | 0 dB |
| 000001 | 000001 | -1.5 dB |
| … | … | ... |
| 011111 | 011111 | -46.5 dB |
| 100000 | 011111 | -46.5 dB |
| ... | ... | ... |
| 111111 | 011111 | -46.5 dB |

### 4.4 Mono Volume Register (Index 06h)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Mute | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MM5 | MM4 | MM3 | MM2 | MM1 | MM0 |

Mute — Mono Mute. Setting this bit mutes the MONO_OUT signal.

MM[5:0] — Mono Volume. These bits control the mono output volume. Each step corresponds to 1.5 dB gain adjustment, with a total available range from 0 dB to -46.5 dB attenuation. See Table 4-2 for further attenuation levels.

MM5 — Mono Volume Max Attenuation. Setting the MM5 bit sets the mono attenuation to -46.5 dB by forcing MM[4:0] to a '1' state. MM[5:0] will read back 011111 when MM5 has been 'set'. Table 4-2 summarizes this behavior.

Default — 8000h. This value corresponds to 0 dB attenuation and Mute 'set'.

### 4.5 PC_BEEP Volume Register (Index 0Ah)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Mute | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PV3 | PV2 | PV1 | PV0 | 0 |

Mute — PC_BEEP Mute. Setting this bit mutes the PC_BEEP input signal.

PV[3:0] — PC_BEEP Volume Control. The PV[3:0] bits are used to control the gain levels of the PC_BEEP input source to the Input Mixer. Each step corresponds to 3 dB gain adjustment, with 0000 = 0 dB. The total range is 0 dB to -45 dB attenuation.

Default — 0000h. This value corresponds to 0 dB attenuation and Mute ‘clear’.

This register has no effect on the PC_BEEP volume during RESET#.

### 4.6 Phone Volume Register (Index 0Ch)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Mute | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | GN4 | GN3 | GN2 | GN1 | GN0 |

Mute — Phone Mute. Setting this bit mutes the Phone input signal.

GN[4:0] — Phone Volume Control. The GN[4:0] bits are used to control the gain levels of the Phone input source to the Input Mixer. Each step corresponds to 1.5 dB gain adjustment, with 01000 = 0 dB. The total range is +12 dB to -34.5 dB gain. See Table 4-4 on page 22 for further details.

Default — 8008h. This value corresponds to 0 dB gain and Mute ‘set’.

## 4.7 *Microphone Volume Register (Index 0Eh)*

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Mute | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 20dB | 0 | GN4 | GN3 | GN2 | GN1 | GN0 |

Mute — Microphone Mute. Setting this bit mutes the MIC1 or MIC2 signal. The selection of the MIC1 or MIC2 input pin is controlled by the MS bit in the *General Purpose Register (Index 20h)*.

GN[4:0] — Microphone Volume Control. The GN[4:0] bits are used to control the gain level of the Microphone input source to the Input Mixer. Each step corresponds to 1.5 dB gain adjustment, with 01000 = 0 dB. The total range is +12 dB to -34.5 dB gain. See Table 4-3 for further details.

20dB — Microphone 20 dB Boost. When ‘set’, the 20dB bit enables the +20 dB microphone boost block. This bit allows for variable boost of 0 dB or +20 dB. Table 4-3 summarizes this behavior.

Default — 8008h. This value corresponds to 0 dB gain and Mute ‘set’.

**Table 4-3. Microphone Input Gain Values**

| GN[4:0] | Gain Level | |
|---|---|---|
| | 20 dB = 0 | 20 dB = 1 |
| 00000 | +12.0 dB | +32.0 dB |
| 00001 | +10.5 dB | +30.5 dB |
| … | … | ... |
| 00111 | +1.5 dB | +21.5 dB |
| 01000 | 0.0 dB | +20.0 dB |
| 01001 | -1.5 dB | +18.5 dB |
| … | … | ... |
| 11111 | -34.5 dB | -14.5 dB |

## 4.8 *Stereo Analog Mixer Input Gain Registers (Index 10h - 18h)*

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Mute | 0 | 0 | GL4 | GL3 | GL2 | GL1 | GL0 | 0 | 0 | 0 | GR4 | GR3 | GR2 | GR1 | GR0 |

Mute — Stereo Input Mute. Setting this bit mutes the respective input signal, both right and left inputs.

GL[4:0] — Left Volume Control. The GL[4:0] bits are used to control the gain level of the left analog input source to the Input Mixer. Each step corresponds to 1.5 dB gain adjustment, with 01000 = 0 dB. The total range is +12 dB to -34.5 dB gain. See Table 4-4 for further details.

GR[4:0] — Right Volume Control. The GR[4:0] bits are used to control the gain level of the right analog input source to the Input Mixer. Each step corresponds to 1.5 dB gain adjustment, with 01000 = 0 dB. The total range is +12 dB to -34.5 dB gain. See Table 4-4 for further details.

Default — 8808h. This value corresponds to 0 dB gain and Mute 'set'.

The Stereo Analog Mixer Input Gain Registers are listed in Table 4-5.

**Table 4-4. Analog Mixer Input Gain Values**

| Gx[4:0] | Gain Level |
|---|---|
| 00000 | +12.0 dB |
| 00001 | +10.5 dB |
| … | … |
| 00111 | +1.5 dB |
| 01000 | 0.0 dB |
| 01001 | -1.5 dB |
| … | … |
| 11111 | -34.5 dB |

**Table 4-5. Stereo Volume Register Index**

| Register Index | Function |
|---|---|
| 10h | Line In Volume |
| 12h | CD Volume |
| 14h | Video Volume |
| 16h | Aux Volume |
| 18h | PCM Out Volume |

### 4.9 *Input Mux Select Register (Index 1Ah)*

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | SL2 | SL1 | SL0 | 0 | 0 | 0 | 0 | 0 | SR2 | SR1 | SR0 |

SL[2:0] Left Channel Source. The SL[2:0] bits select the left channel source to pass to the ADCs for recording. See Table 4-6 for possible values.

SR[2:0] Right Channel Source. The SR[2:0] bits select the right channel source to pass to the ADCs for recording. See Table 4-6 for possible values.

Default 0000h. This value selects the Mic input for both channels.

**Table 4-6. Input Mux Selection**

| Sx[2:0] | Record Source |
|---|---|
| 000 | Mic |
| 001 | CD Input |
| 010 | Video Input |
| 011 | Aux Input |
| 100 | Line Input |
| 101 | Stereo Mix |
| 110 | Mono Mix |
| 111 | Phone Input |

### 4.10 *Record Gain Register (Index 1Ch)*

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Mute | 0 | 0 | 0 | GL3 | GL2 | GL1 | GL0 | 0 | 0 | 0 | 0 | GR3 | GR2 | GR1 | GR0 |

Mute Record Gain Mute. Setting this bit mutes the input to the L/R ADCs.

GL[3:0] Left ADC Gain. The GL[3:0] bits control the input gain on the left channel of the analog source, applied after the input mux and before the ADCs. Each step corresponds to 1.5 dB gain adjustment, with 0000 = 0 dB. The total range is 0 dB to +22.5 dB gain.

GR[3:0] Right ADC Gain. The GR[3:0] bits control the input gain on the right channel of the analog source, applied after the input mux and before the ADCs. Each step corresponds to 1.5 dB gain adjustment, with 0000 = 0 dB. The total range is 0 dB to +22.5 dB gain.

Default 8000h. This value corresponds to 0 dB gain and Mute ‘set’.

### 4.11 General Purpose Register (Index 20h)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 3D | 0 | 0 | 0 | MIX | MS | LPBK | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

3D — 3D Enable. When 'set', the 3D bit enables the CrystalClear™ 3D stereo enhancement. This function is not available in DAC Direct Mode (DDM).

MIX — Mono Output Select. The MIX bit selects the source for the Mono Out output. When 'set', the microphone input is selected. When 'clear', the stereo-to-mono mixer is selected.

MS — Microphone Select. The MS bit determines which of the two Mic inputs are passed to the mixer. When 'set', the MIC2 input is selected. When 'clear', the MIC1 input is selected.

LPBK — Loopback Enable. When 'set', the LPBK bit enables the ADC/DAC Loopback Mode. This bit routes the output of the ADCs to the input of the DACs without involving the AC-link.

Default — 0000h

### 4.12 3D Control Register (Index 22h)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | S3 | S2 | S1 | S0 |

S[3:0] — Spacial Enhancement Depth. These bits control the amount of "space" added to the output stereo signal. When S[3:0] = 0000, the minimum amount of spatial enhancement is added. When S[3:0] = 1111, the maximum amount of spatial enhancement is added. The 3D function is enabled and disabled by the 3D bit in the *General Purpose Register (Index 20h)*.

Default — 0000h. This value corresponds to minimum spatial enhancement added to the output signal.

### 4.13 *Powerdown Control/Status Register (Index 26h)*

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| EAPD | PR6 | PR5 | PR4 | PR3 | PR2 | PR1 | PR0 | 0 | 0 | 0 | 0 | REF | ANL | DAC | ADC |

EAPD — External Amplifier Power Down. The EAPD pin follows this bit and is generally used to power down external amplifiers.

PR6 — Alternate Line Out Powerdown. When ‘set’, the alternate line out buffer is powered down.

PR5 — Internal Clock Disable. When ‘set’, this bit completely powers down both the analog and digital sections of the CS4299. The only way to recover from setting this bit is through a Cold Reset (driving the RESET# signal active).

PR4 — AC-link Powerdown. When ‘set’, the AC link is powered down (BIT_CLK off). The AC-link can be restarted through a Warm Reset using the SYNC signal, or a Cold Reset using the RESET# signal (primary audio codec only).

PR3 — Analog Mixer Powerdown (Vref off). When ‘set’, the analog mixer and voltage reference are powered down. When clearing this bit, the ANL, ADC, and DAC bits should be checked before writing any mixer registers.

PR2 — Analog Mixer Powerdown (Vref on). When ‘set’, the analog mixer is powered down (the voltage reference is still active). When clearing this bit, the ANL bit should be checked before writing any mixer registers.

PR1 — Front DACs Powerdown. When ‘set’, the DACs are powered down. When clearing this bit, the DAC bit should be checked before sending any data to the DACs.

PR0 — L/R ADCs and Input Mux Powerdown. When ‘set’, the ADCs and the ADC input muxes are powered down. When clearing this bit, no valid data will be sent down the AC link until the ADC bit goes high.

REF — Voltage Reference Ready Status. When ‘set’, indicates the voltage reference is at a nominal level.

ANL — Analog Ready Status. When ‘set’, the analog output mixer, input multiplexer, and volume controls are ready. When clear, no volume control registers should be written.

DAC — Front DAC Ready Status. When ‘set’, the DACs are ready to receive data across the AC link. When clear, the DACs will not accept any valid data.

ADC — L/R ADC Ready Status. When ‘set’, the ADCs are ready to send data across the AC link. When clear, no data will be sent to the Controller.

Default — 0000h. This value indicates all blocks are powered on. The lower four bits will change as the CS4299 finishes an initialization and calibration sequence.

The PR[6:0] and the EAPD bits are powerdown control for different sections of the CS4299 as well as external amplifiers. The REF, ANL, DAC, and ADC bits are read-only status bits which, when ‘set’, indicate that a particular section of the CS4299 is ready. After the controller receives the Codec Ready bit in input Slot 0, these status bits must be checked before writing to any mixer registers. See Section 5, *Power Management*, for more information on the powerdown functions.

### 4.14 Extended Audio ID Register (Index 28h)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID1 | ID0 | 0 | 0 | 0 | 0 | AMAP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VRA |

ID[1:0] Codec Configuration ID. When ID[1:0] = 00, the CS4299 is the primary audio codec. When ID[1:0] = 01, 10, or 11, the CS4299 is a secondary audio codec. The state of the ID[1:0] bits is determined at power-up from the ID[1:0]# pins.

AMAP Audio Slot Mapping. The AMAP bit indicates whether the optional AC '97 2.1 compliant AC-link slot to audio DAC mapping is supported. This bit is a shadow of the AMAP bit in the *AC Mode Control Register (Index 5Eh)*. The PCM playback and capture slots are mapped according to Table 4-8 on page 28.

VRA Variable Rate PCM Audio. The VRA bit indicates whether variable rate PCM audio is supported. This bit always returns '1', indicating that variable rate PCM audio is available.

Default x201h. Where x is determined by the state of ID[1:0]# input pins. The *Extended Audio ID Register (Index 28h)* is a read only register.

### 4.15 Extended Audio Status/Control Register (Index 2Ah)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VRA |

VRA Enable Variable Rate Audio. When 'set', the VRA bit allows access to the *PCM Front DAC Rate Register (Index 2Ch)* and the *PCM L/R ADC Rate Register (Index 32h)*. The bit must be 'set' in order to use variable PCM playback or capture rates. The VRA bit also serves as a powerdown for the DAC and ADC SRC blocks. Clearing VRA will reset the *PCM Front DAC Rate Register (Index 2Ch)* and the *PCM L/R ADC Rate Register (Index 32h)* to their default values. The SRC data path is flushed and the Slot Request bits for the currently active DAC slots will be fixed at '0'.

Default 0000h

### 4.16 PCM Front DAC Rate Register (Index 2Ch)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SR15 | SR14 | SR13 | SR12 | SR11 | SR10 | SR9 | SR8 | SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 |

SR[15:0] Front DAC Sample Rate. The SR[15:0] bits can only be written when the VRA bit of the *Extended Audio Status/Control Register (Index 2Ah)* is 'set'. If the VRA bit is 'clear', all writes are ignored and the register reads back BB80h; corresponding to a 48 kHz sample rate. If the VRA bit is 'set', seven standard sample rates are available. If a sample rate written to the register is not directly supported, the attempted value to be written will be decoded according to the ranges indicated in Table 4-7. All register read transactions will reflect the actual value stored (column 2 in Table 4-7) and not the one attempted to be written.

Default BB80h. This value corresponds to 48 kHz sample rate..

**Table 4-7. Standard Sample Rates**

| Sample rate (Hz) | SR[15:0] | SR[15:12] Decode Range |
|---|---|---|
| 8,000 | 1F40 | 0 or 1 |
| 11,025 | 2B11 | 2 |
| 16,000 | 3E80 | 3 |
| 22,050 | 5622 | 4 or 5 |
| 32,000 | 7D00 | 6 or 7 |
| 44,100 | AC44 | 8, 9, or Ah |
| 48,000 | BB80 | Bh, Ch, Dh, Eh, or Fh |

### 4.17 PCM L/R ADC Rate Register (Index 32h)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SR15 | SR14 | SR13 | SR12 | SR11 | SR10 | SR9 | SR8 | SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 |

SR[15:0] Left/Right ADC Sample Rate. The SR[15:0] bits can only be written when the VRA bit of the *Extended Audio Status/Control Register (Index 2Ah)* is 'set'. If the VRA bit is 'clear', all writes are ignored and the register reads back BB80h; corresponding to a 48 kHz sample rate. If the VRA bit is 'set', seven standard sample rates are available. If a sample rate written to the register is not directly supported, the attempted value to be written will be decoded according to the ranges indicated in Table 4-7. All register read transactions will reflect the actual value stored (column 2 in Table 4-7) and not the one attempted to be written.

Default BB80h. This value corresponds to 48 kHz sample rate.

### 4.18 AC Mode Control Register (Index 5Eh)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | DDM | AMAP | 0 | SM1 | SM0 | 0 | 0 | 0 | 0 |

DDM — DAC Direct Mode. This bit controls the source to the line and alternate line output drivers. When 'set', the L/R DACs directly drive the line and alternate line outputs by bypassing the audio mixer. When 'clear', the audio mixer is the source for the line and alternate line outputs.

AMAP — Audio Slot Mapping. This read/write bit controls whether the CS4299 responds to the Codec ID based slot mapping as outlined in the AC '97 2.1 specification. The bit is shadowed in the *Extended Audio ID Register (Index 28h)*. Refer to Table 4-8 for the slot mapping configurations.

SM[1:0] — Slot Map. The SM[1:0] bits define the Slot Mapping for the CS4299 when the AMAP bit is 'cleared'. Refer to Table 4-8 for the slot mapping configurations.

Default — 0080h

**Table 4-8. Slot Mapping**

| Slot Assignment Mode | Codec ID | | Slot Map | | AMAP | Slot Assignments | | | |
|---|---|---|---|---|---|---|---|---|---|
| | ID1 | ID0 | SM1 | SM0 | | DAC, SPDIF | | ADC | |
| | | | | | | L | R | L | R |
| AMAP Mode 0 | 0 | 0 | X | X | 1 | 3 | 4 | 3 | 4 |
| AMAP Mode 1 | 0 | 1 | X | X | 1 | 3 | 4 | 3 | 4 |
| AMAP Mode 2 | 1 | 0 | X | X | 1 | 7 | 8 | 7 | 8 |
| AMAP Mode 3 | 1 | 1 | X | X | 1 | 6 | 9 | 6 | 9 |
| Slot Map Mode 0 | X | X | 0 | 0 | 0 | 3 | 4 | 3 | 4 |
| Slot Map Mode 1 | X | X | 0 | 1 | 0 | 5 | 6 | 5 | 6 |
| Slot Map Mode 2 | X | X | 1 | 0 | 0 | 7 | 8 | 7 | 8 |
| Slot Map Mode 3 | X | X | 1 | 1 | 0 | 9 | 10 | 9 | 10 |

### 4.19 Misc. Crystal Control Register (Index 60h)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Reserved | | | | 0 | 0 | Reserved | | 0 | Reserved | | LOSM |

LOSM — Loss of SYNC Mute Enable. The LOSM bit controls the loss of SYNC mute function. If this bit is 'set', the CS4299 will mute all analog outputs for the duration of loss of SYNC. If this bit is 'cleared', the mixer will continue to function normally during loss of SYNC. The CS4299 expects to sample SYNC 'high' for 16 consecutive BIT_CLK periods and then 'low' for 240 consecutive BIT_CLK periods, otherwise loss of SYNC becomes true.

Default — 0023h

### 4.20 S/PDIF Control Register (Index 68h)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SPEN | Val | 0 | Fs | L | CC6 | CC5 | CC4 | CC3 | CC2 | CC1 | CC0 | Emph | Copy | /Audio | Pro |

SPEN — S/PDIF Enable. The SPEN bit enables S/PDIF data transmission on the S/PDIF_OUT pin. The SPEN bit routes the left and right channel data from the AC '97 controller, the digital mixer, or the digital effects engine to the S/PDIF transmitter block. The actual data routed to the S/PDIF block is controlled through the AMAP/SM[1:0] configuration in the *AC Mode Control Register (Index 5Eh)*.

Val — Validity. The V bit is mapped to the V bit (bit 28) of every *sub-frame*. If this bit is '0', the signal is suitable for conversion or processing.

Fs — Sample Rate. The Fs bit indicates the sampling rate for the S/PDIF data. The inverse of this bit is mapped to bit 25 of the channel status block. When the Fs bit is 'clear', the sampling frequency is 48 kHz. When 'set', the sampling frequency is 44.1 kHz. The actual rate at which S/PDIF data are being transmitted solely depends on the master clock frequency of the CS4299. The Fs bit is merely an indicator to the S/PDIF receiver.

L — Generation Status. The L bit is mapped to bit 15 of the channel status block. For category codes 001xxxx, 0111xxx and 100xxxx, a value of '0' indicates original material and a value of '1' indicates a copy of original material. For all other category codes the definition of the L bit is reversed.

CC[6:0] — Category Code. The CC[6:0] bits are mapped to bits 8-14 of the channel status block.

Emph — Data Emphasis. The Emph bit is mapped to bit 3 of the channel status block. If the Emph bit is '1', 50/15us filter pre-emphasis is indicated. If the bit is '0', no pre-emphasis is indicated.

Copy — Copyright. The Copy bit is mapped to bit 3 of the channel status block. If the Copy bit is '1' copyright is not asserted and copying is permitted.

/Audio — Audio / Non-Audio. The /Audio bit is mapped to bit 1 of the channel status block. If the /Audio bit is '0', the data transmitted over S/PDIF is assumed to be digital audio. If the /Audio bit is '1', non-audio data is assumed.

Pro — Professional/Consumer. The Pro bit is mapped to bit 0 of the channel status block. If the Pro bit is '0', consumer use of the audio control block is indicated. If the bit is '1', professional use is indicated.

Default — 0000h

For a further discussion of the proper use of the channel status bits see application note *AN22: Overview of Digital Audio Interface Data Structures* [3].

### 4.21 Vendor ID1 Register (Index 7Ch)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| F7 | F6 | F5 | F4 | F3 | F2 | F1 | F0 | S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 |

F[7:0] First Character of Vendor ID. With a value of F[7:0] = 43h, these bits define the ASCII ‘C’ character.

S[7:0] Second Character of Vendor ID. With a value of S[7:0] = 52h, these bits define the ASCII ‘R’ character.

Default 4352h. This register contains read-only data.

### 4.22 Vendor ID2 Register (Index 7Eh)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| T7 | T6 | T5 | T4 | T3 | T2 | T1 | T0 | 0 | DID2 | DID1 | DID0 | 0 | REV2 | REV1 | REV0 |

T[7:0] Third Character of Vendor ID. With a value of T[7:0] = 59h, these bits define the ASCII ‘Y’ character.

DID[2:0] Device ID. With a value of DID[2:0] = 011, these bits specify the audio codec is a CS4299.

REV[2:0] Revision. With a value of REV[2:0] = 001, these bits specify the audio codec revision is ‘A’.

Default 593xh. This register contains read-only data.

The two Vendor ID registers provide a means to determine the manufacturer of the AC ’97 audio codec. The first three bytes of the Vendor ID registers contain the ASCII code for the first three letters of Crystal (CRY). The final byte of the Vendor ID registers is divided into a Device ID field and a Revision field. Table 4-9 lists the currently defined Device ID’s. Table 4-10 lists the current revisions of the CS4299.

**Table 4-9. Device ID with Corresponding Part Number**

| DID[2:0] | Part Name |
|---|---|
| 000 | CS4297 |
| 001 | CS4297A |
| 010 | CS4294/CS4298 |
| 011 | CS4299 |
| 100 | CS4201 |
| 101 | CS4205 |

**Table 4-10. Revision Values**

| REV[2:0] | Revision |
|---|---|
| 001 | A |
| 010 | B |
| 011 | C |
| 100 | D, E, F, G, H |
| 101 | K |
| 110 | L |

# 5 Power Management

## 5.1 AC ’97 Reset Modes

The CS4299 supports three reset methods, as defined in the AC ’97 Specification: *Cold AC ’97 Reset*, *Warm AC ’97 Reset*, *Register AC ’97 Reset*. A Cold Reset results in all AC ’97 logic (registers included) initialized to its default state. A Warm Reset leaves the contents of the AC ’97 register set unaltered. A Register Reset initializes only the AC ’97 registers to their default states.

### 5.1.1 Cold AC ‘97 Reset

A Cold Reset is achieved by asserting RESET# for a minimum of 1 µs after the power supply rails have stabilized. This is done in accordance with the minimum timing specifications in the *AC ’97 Serial Port Timing* section on page 6. Once deasserted, all of the CS4299 registers will be reset to their default power-on states and the BIT_CLK and SDATA_IN signals will be reactivated.

### 5.1.2 Warm AC ’97 Reset

A Warm Reset allows the AC-link to be reactivated without losing information in the CS4299 registers. A Warm Reset is required to resume from a $D3_{hot}$ state, where the AC-link had been halted yet full power had been maintained. A primary codec Warm Reset is initiated when the SYNC signal is driven high for at least 1 µs and then driven low in the absence of the BIT_CLK clock signal. The BIT_CLK clock will not restart until at least 2 normal BIT_CLK clock periods (162.8 ns) after the SYNC signal is deasserted. A Warm Reset of the secondary codec is recognized when the primary codec on the AC-link resumes BIT_CLK generation. The CS4299 will wait for BIT_CLK to be stable to restore SDATA_IN activity and/or S/PDIF transmission on the following frame.

### 5.1.3 Register AC ’97 Reset

The third reset mode provides a Register Reset to the CS4299. This is available only when the CS4299 AC-link is active and the Codec Ready bit is ‘set’. The audio (including extended audio) registers *(Index 00h - 38h)* and the vendor specific registers *(Index 5Ah - 7Ah)* are reset to their default states by a write of any value to the *Reset Register (Index 00h)*.

## 5.2 Powerdown Controls

The *Powerdown Control/Status Register (Index 26h)* controls the power management functions. The PR[6:0] bits in this register control the internal powerdown states of the CS4299. Powerdown control is available for individual subsections of the CS4299 by asserting any PRx bit or any combination of PRx bits. Most powerdown states can be resumed by clearing the corresponding PRx bit. Table 5-1 shows the mapping of the power control bits to the functions they manage.

When PR0 is 'set', the L/R ADCs and the Input Mux are shut down and the ADC bit in the *Powerdown Control/Status Register (Index 26h)* is 'cleared' indicating the ADCs are no longer in a ready state. The same is true for the DACs, the analog mixers, and the reference voltage (Vrefout). When the PR2 or PR3 bit of the mixer is 'cleared', the mixer section will begin a power-on process, and the corresponding powerdown status bit will be 'set' when the hardware is ready.

Shutting down the AC-link by 'setting' PR4 causes the primary Codec to turn off the BIT_CLK and drive SDATA_IN low. It also ignores SYNC and SDATA_OUT in their normal capacities. Either a Cold Reset or a Warm Reset is required to restore operation to the CS4299. A Cold Reset will restore all mixer registers to their power-on default values. A Warm Reset will not alter the values of any mixer register, except clearing the PR4 bit in *Powerdown Control/Status Register (Index 26h)*.

The PR5 bit powers down all analog and digital subsections of the device. A Cold Reset is the only way to restore operation to the CS4299 after a PR5 global powerdown.

The CS4299 does not automatically mute any input or output when the powerdown bits are 'set'. The software driver controlling the AC '97 device must manage muting the input and output analog signals before putting the part into any power management state. The definition of each PRx bit may affect a single subsection or a combination of subsections within the CS4299. Table 5-2 contains the matrix of subsections affected by the respective PRx function. Table 5-3 shows the different operating power consumptions levels for different powerdown functions.

**Table 5-1. Powerdown PR Bit Functions**

| PR Bit | Function |
|---|---|
| PR0 | L/R ADCs and Input Mux Powerdown |
| PR1 | Front DACs Powerdown |
| PR2 | Analog Mixer Powerdown (Vref on) |
| PR3 | Analog Mixer Powerdown (Vref off) |
| PR4 | AC-link Powerdown (BIT_CLK off)* |
| PR5 | Internal Clock Disable |
| PR6 | Alternate Line Out Powerdown |
| * Applies only to primary codec | |

**Table 5-2. Powerdown PR Function Matrix**

| PR Bit | ADCs | DACs | Mixer | Alternate Line Out | Analog Reference | AC Link | Internal Clock Off |
|---|---|---|---|---|---|---|---|
| PR0 | • | | | | | | |
| PR1 | | • | | | | | |
| PR2 | | • | • | • | | | |
| PR3 | • | • | • | • | • | | |
| PR4 | | | | | | • | |
| PR5 | • | • | • | • | • | • | • |
| PR6 | | | | • | | | |

**Table 5-3. Power Consumption by Powerdown Mode**

| Power State | $I_{DVdd}$ (mA) [DVdd=3.3 V] | $I_{DVdd}$ (mA) [DVdd=5 V] | $I_{AVdd}$ (mA) |
|---|---|---|---|
| Full Power + SRC's | 29.1 | 50.2 | 37.9 |
| Full Power + S/PDIF[1] | 30.1 | 49.4 | 37.9 |
| Full Power | 24.5 | 43.4 | 37.9 |
| ADCs off (PR0) | 21.0 | 38.1 | 29.0 |
| DACs off (PR1) | 22.1 | 39.6 | 31.3 |
| Audio off (PR2) | 22.1 | 39.9 | 10.7 |
| Vref off (PR3) | 18.9 | 34.8 | 45 µA |
| AC-Link off (PR4) | 19.3 | 35.5 | 37.9 |
| Internal Clocks off (PR5) | 11 µA | 27 µA | 45 µA |
| Alt line out off (PR6) | 24.5 | 43.4 | 36.2 |
| RESET | 11 µA | 27 µA | 450 µA |

1. Assuming standard resistive load for transformer coupled coaxial S/PDIF output (Rload = 292 Ohm, DVdd = 3.3 V) (Rload = 415 Ohm, DVdd = 5 V).
General: $I_{DVdd\ S/PDIF} = I_{DVdd} + DVdd/Rload/2$

# 6 Analog Hardware Description

The analog line-level input hardware consists of four stereo inputs (LINE_IN_L/R, CD_L/GND/R, VIDEO_L/R, and AUX_L/R), two selectable mono microphone inputs (MIC1 and MIC2), and two mono inputs (PC_BEEP and PHONE). The analog line-level output hardware consists of a mono output (MONO_OUT), and dual stereo line outputs (LINE_OUT_L/R and ALT_LINE_OUT_L/R). This section describes the analog hardware needed to interface with these pins. The designs presented in this section comply with specifications detailed in Chapter 17 of the Microsoft® *PC Design Guidelines* [7] (referred to as PC 99). For EMI reduction techniques refer to the application note *N165: CS4297A/CS4299 EMI Reduction Techniques* [5].

## 6.1 Analog Inputs

All analog inputs to the CS4299, including CD_GND, should be capacitively coupled to the input pins. Unused analog inputs should be tied together and connected through a capacitor to analog ground or tied to the Vrefout pin directly. The maximum allowed voltage for analog inputs, except the microphone input, is 1 $V_{RMS}$. For the microphone input the maximum allowed voltage depends on the selected boost setting.

### 6.1.1 Line-Level Inputs

Fig. 6-1 shows circuitry for a line-level stereo input. Replicate this circuit for the Line, Video and Aux inputs. This design attenuates the input by 6 dB, bringing the signal from the PC 99 specified 2 $V_{RMS}$, to the CS4299 maximum allowed 1 $V_{RMS}$.

### 6.1.2 CD Input

The CD line-level input has an extra pin, CD_GND, providing a pseudo-differential input for both CD_L and CD_R. This pin takes the common-mode noise out of the CD inputs when connected to the CD analog source ground. Following the reference designs in Fig. 6-1 and Fig. 6-2 provides extra attenuation of common mode noise coming from the CD-ROM drive, thereby producing a higher quality signal. One percent resistors are recommended since closely matched resistor values provide better common-mode attenuation of unwanted signals. The circuit shown in Fig. 6-1 can be used to attenuate a 2 $V_{RMS}$ CD input signal by 6 dB. The circuit shown in Fig. 6-2 can be used for a 1 $V_{RMS}$ CD input signal.

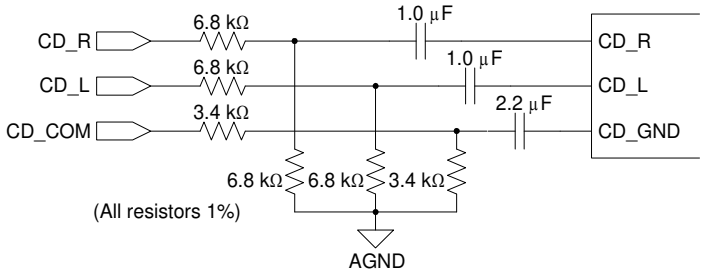



**Figure 6-1. Differential 2 $V_{RMS}$ CD Input**

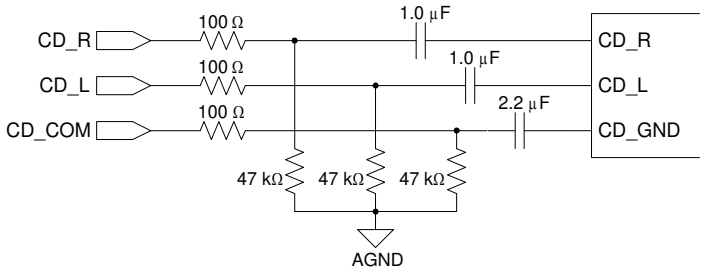



**Figure 6-2. Differential 1 $V_{RMS}$ CD Input**

### 6.1.3 Microphone Inputs

Fig. 6-3 illustrates an input circuit suitable for dynamic and electret microphones. Electret, or phantom-powered, microphones use the right channel (ring) of the jack for power. The design also supports the recommended advanced frequency response for voice recognition as specified in PC 99. Note the microphone input to the CS4299 has an integrated pre-amplifier. Using the 20 dB bit in the *Microphone Volume Register (Index 0Eh)* the pre-amplifier gain can be set to 0 dB or 20 dB. Fig. 6-4 shows an external pre-amplifier circuit for an additional 18 dB gain.

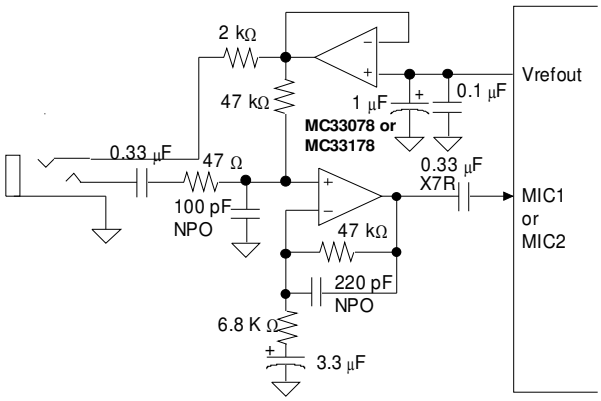



**Figure 6-3. Microphone Input**

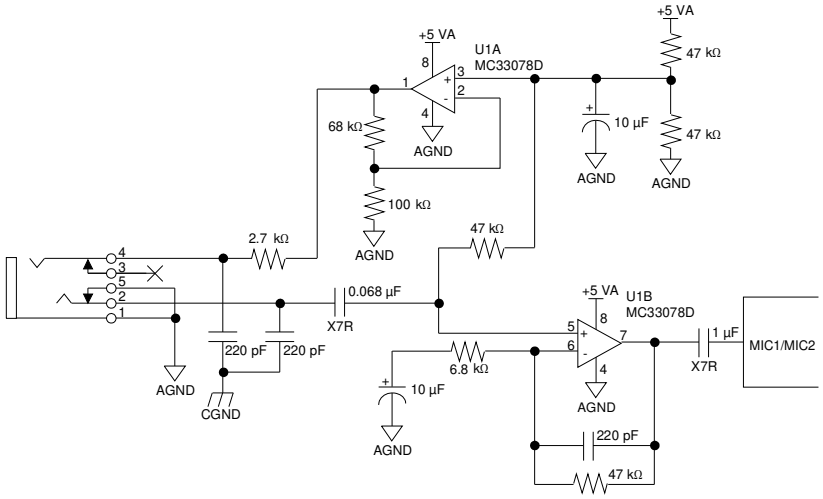



**Figure 6-4. Microphone Pre-amplifier**

### 6.1.4 PC Beep Input

The PC_BEEP input is useful for mixing the output of the “beeper” (timer chip), provided in most PCs, with the other audio signals. When the CS4299 is held in reset, PC_BEEP is passed directly to the line output. This allows the system sounds or “beeps” to be available before the AC ’97 interface has been activated. Fig. 6-5 illustrates a typical input circuit for the PC_BEEP input. If PC_BEEP is driven from a CMOS gate, the 4.7 kΩ resistor should be tied to analog ground instead of +5VA. Although this input is described for a low-quality “beeper”, it is of the same high-quality as all other analog inputs and may be used for other purposes.

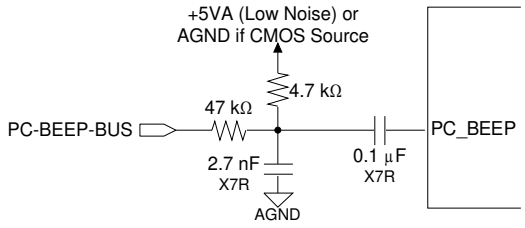



**Figure 6-5. PC_BEEP Input**

### 6.1.5 Phone Input

One application of the PHONE input is to interface to the output of a modem analog front end (AFE) device so that modem dialing signals and protocol negotiations may be monitored through the audio system. Fig. 6-6 shows a design for a modem connection where the output is fed from the CS4299 MONO_OUT pin through a divider. The divider ratio shown does not attenuate the signal, providing an output voltage of 1 $V_{RMS}$. If a lower output voltage is desired, the resistors can be replaced with appropriate values, as long as the total load on the output is kept greater than 10 kΩ. The PHONE input is divided by 6 dB to accommodate a line-level source of 2 $V_{RMS}$.

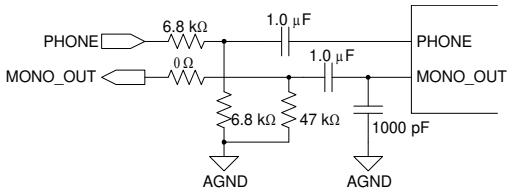



**Figure 6-6. Modem Connection**

## 6.2 Analog Outputs

The analog line-level output section provides two stereo outputs and a mono output. The LINE_OUT_L/R, ALT_LINE_OUT_L/R, and MONO_OUT pins require 680 pF to 1000 pF NPO capacitors between the corresponding pin and analog ground. Each analog output is DC-biased up to the Vrefout signal reference, nominally 2.3 V. This requires the outputs be AC-coupled to external circuitry (AC load must be greater than 10 kΩ) or DC coupled to a buffer op-amp biased at Vrefout.

### 6.2.1 Stereo Outputs

See Fig. 6-7 for a recommended headphone stereo output reference design. See Fig. 6-8 for a line-level stereo output reference design.

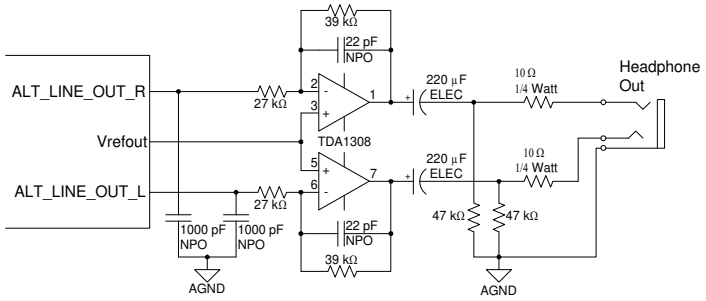



**Figure 6-7. Alternate Line Output as Headphone Output**

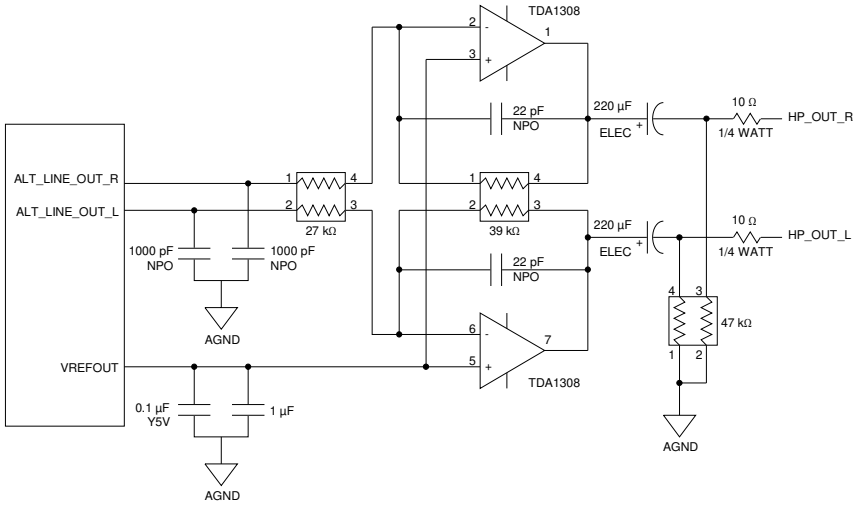



**Figure 6-8. Stereo Output**

### 6.2.2 Mono Output

The mono output, MONO_OUT, can be either a sum of the left and right output channels, attenuated by 6 dB to prevent clipping at full scale, or the selected Mic signal. The mono out channel can drive the PC internal mono speaker using an appropriate buffer circuit

## 6.3 Miscellaneous Analog Signals

The AFLT1 and AFLT2 pins must have a 1000 pF NPO capacitor to analog ground. These capacitors provide a single-pole low-pass filter at the inputs to the ADCs. This makes low-pass filters at each analog input pin unnecessary.

The REFFLT pin must have a 1 µF and a 0.1 µF capacitor connected to analog ground with a short, wide trace to this pin (see Fig. 8-1 in Section 8, *Grounding and Layout*, for an example). The 1 µF capacitor must not be replaced with any value higher than 1 µF. No other connection should be made, as any coupling onto this pin will degrade the analog performance of the CS4299. Likewise, digital signals should be kept away from REFFLT for similar reasons.

The Vrefout pin is typically 2.3 V and provides a common mode signal for single-supply external circuits. Vrefout only supports light DC loads and should be buffered if AC loading is needed. For typical use the Vrefout pin should have a 1 µF and a 0.1 µF capacitor connected to analog ground.

## 6.4 Power Supplies

The power supplies providing analog power should be as clean as possible to minimize coupling into the analog section which could degrade analog performance. The analog power pins, AVdd1 and AVdd2, supply power to all the analog circuitry on the CS4299. The +5 V analog supply should be generated from a linear voltage regulator (7805 type) connected to a +12 V supply. This helps isolate the analog circuitry from noise typically found on +5 V digital supplies. A typical voltage regulator circuit for analog power using a MC78M05CDT +5 V regulator is shown in Fig. 6-9. The digital power pins, DVdd1 and DVdd2, should be connected to the same digital supply as the controller AC-link interface. The digital interface on the CS4299 may operate at either +3.3 V or +5 V and proper connection of these pins will depend on the digital power supply of the controller.

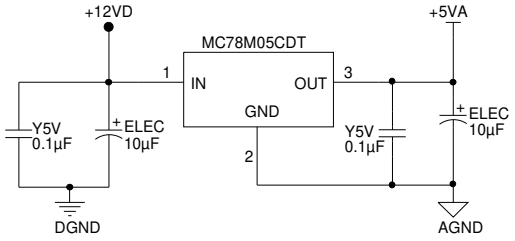


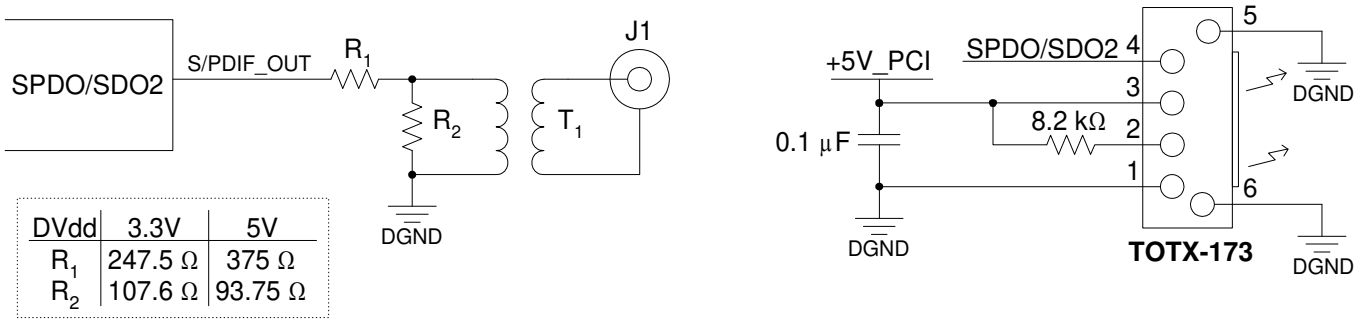

**Figure 6-9. Voltage Regulator**

## 6.5 Reference Design

See Section 11 for a CS4299 reference design.

# 7 Sony/Philips Digital Interface (S/PDIF)

The S/PDIF digital output is used to interface the CS4299 to consumer audio equipment external to the PC. This output provides an interface for storing digital audio data or playing digital audio data to digital speakers. Fig. 7-1 illustrates the circuits necessary for implementing the IEC-958 optical or consumer interface. For further information on S/PDIF operation see application note *AN22: Overview of Digital Audio Interface Data Structures* [3]. For further information on S/PDIF recommended transformers see application note *AN134: AES and S/PDIF Recommended Transformers* [4].




| DVdd | 3.3V | 5V |
|---|---|---|
| $R_1$ | 247.5 Ω | 375 Ω |
| $R_2$ | 107.6 Ω | 93.75 Ω |

**Figure 7-1. S/PDIF Output**

# 8 Grounding and Layout

Fig. 8-1 shows the conceptual layout for the CS4299. The decoupling capacitors should be located physically as close to the pins as possible. Also note the connection of the REFFLT decoupling capacitors to the ground return trace connected directly to the ground return pin, AVss1.

It is strongly recommended that separate analog and digital ground planes be used. Separate ground planes keep digital noise and return currents from modulating the CS4299 ground potential and degrading performance. The digital ground pins should be connected to the digital ground plane and kept separate from the analog ground connections of the CS4299 and any other external analog circuitry. All analog components and traces should be located over the analog ground plane and all digital components and traces should be located over the digital ground plane.

The common connection point between the two ground planes (required to maintain a common ground voltage potential) should be located under the CS4299. The AC-link digital interface connection traces should be routed such that the digital ground plane lies underneath these signals (on the internal ground layer). This applies along the entire length of these traces from the AC ’97 controller to the CS4299.

Refer to the Application Note *AN18: Layout and Design Rules for Data Converters and Other Mixed Signal Devices* [2] for more information on layout and design rules.

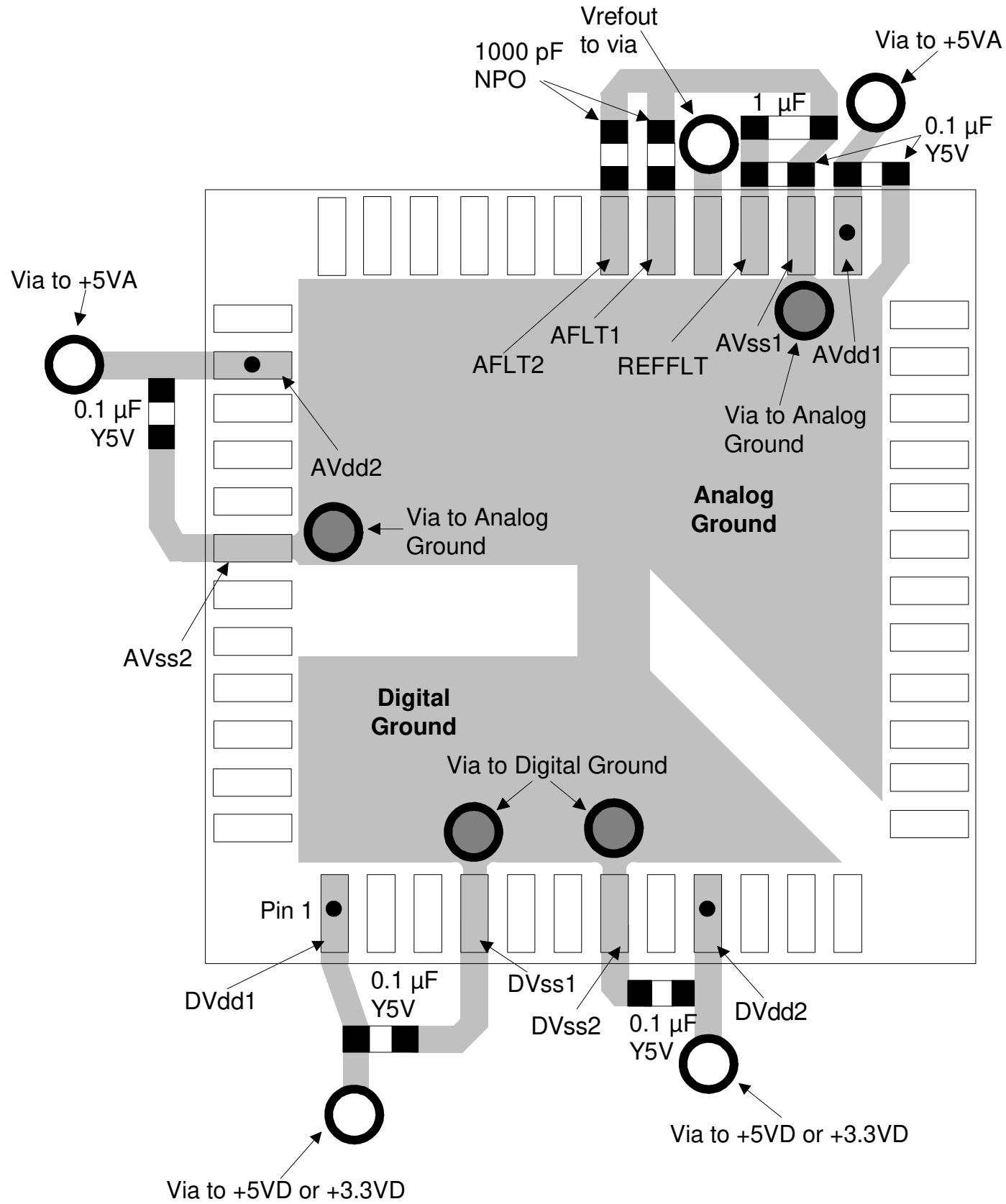



**Figure 8-1. Conceptual Layout for the CS4299**

# 9 Pin Descriptions

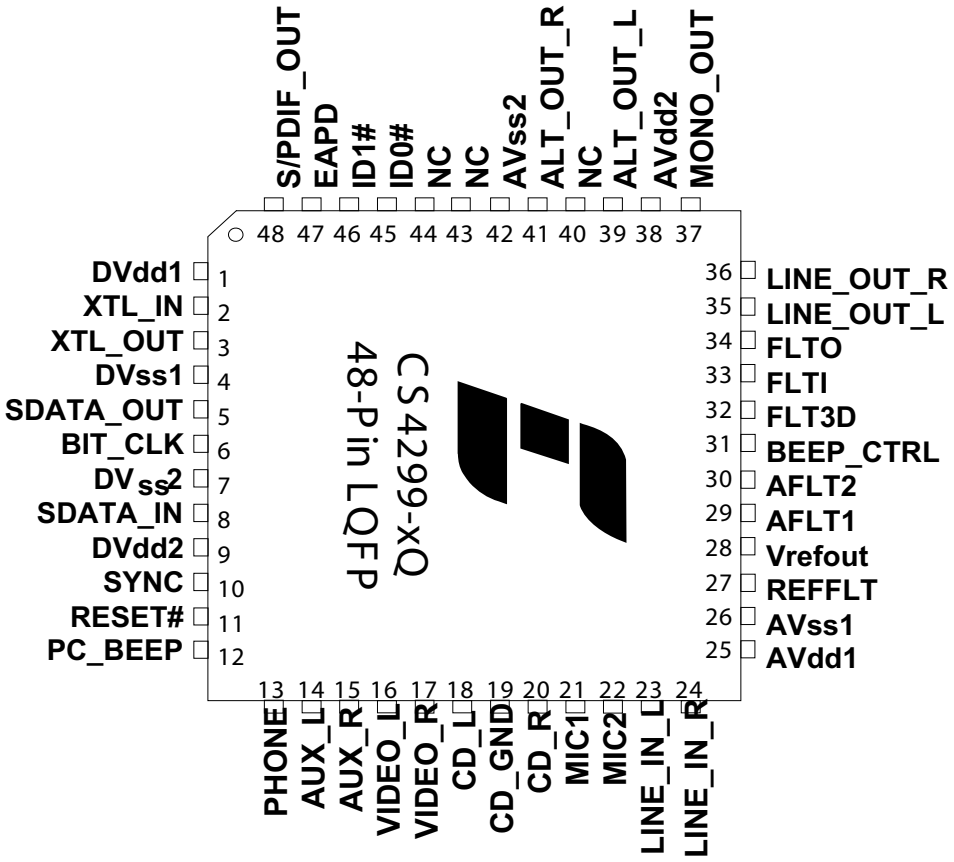



**Figure 9-1. Pin Locations for the CS4299**

*Audio I/O*

**PC_BEEP - Analog Mono Source, Input, Pin 12**

The PC_BEEP input is intended to allow the PC system POST (Power On Self-Test) tones to pass through to the audio subsystem. The PC_BEEP input has two connections: the first connection is to the analog output mixer, the second connection is directly to the LINE_OUT stereo outputs. While the RESET# pin is actively being asserted and the BCFG pin is left floating, the PC_BEEP bypass path to the LINE_OUT outputs is enabled. While the CS4299 is in normal operation mode, with RESET# deasserted or BCFG grounded, PC_BEEP is a monophonic source to the analog output mixer. The maximum allowable input is 1 $V_{RMS}$ (sinusoidal). This input is internally biased at the Vrefout voltage reference and requires AC-coupling to external circuitry. If this input is not used, it should be connected to the Vrefout pin or AC-coupled to analog ground.

**PHONE - Analog Mono Source, Input, Pin 13**

This analog input is a monophonic source to the analog output mixer. It is intended to be used as a modem subsystem input to the audio subsystem. The maximum allowable input is 1 $V_{RMS}$ (sinusoidal). This input is internally biased at the Vrefout voltage reference and requires AC-coupling to external circuitry. If this input is not used, it should be connected to the Vrefout pin or AC-coupled to analog ground.

**MIC1 - Analog Mono Source, Input, Pin 21**

This analog input is a monophonic source to the analog output mixer. It is intended to be used as a desktop microphone connection to the audio subsystem. The CS4299 internal mixer's microphone input is MUX selectable with either MIC1 or MIC2 as the input. The maximum allowable input is 1 $V_{RMS}$ (sinusoidal). This input is internally biased at the Vrefout voltage reference and requires AC-coupling to external circuitry. If this input is not used, it should be connected to the Vrefout pin or AC-coupled to analog ground.

**MIC2 - Analog Mono Source, Input, Pin 22**

This analog input is a monophonic source to the analog output mixer. It is intended to be used as an alternate microphone connection to the audio subsystem. The CS4299 internal mixer's microphone input is MUX selectable with either MIC1 or MIC2 as the input. The maximum allowable input is 1 $V_{RMS}$ (sinusoidal). This input is internally biased at the Vrefout voltage reference and requires AC-coupling to external circuitry. If this input is not used, it should be connected to the Vrefout pin or AC-coupled to analog ground.

**LINE_IN_L, LINE_IN_R - Analog Line Source, Inputs, Pins 23 and 24**

These inputs form a stereo input pair to the CS4299. The maximum allowable input is 1 $V_{RMS}$ (sinusoidal). These inputs are internally biased at the Vrefout voltage reference and require AC-coupling to external circuitry. If these inputs are not used, they should both be connected to the Vrefout pin or both AC-coupled, with separate AC-coupling caps, to analog ground.

**CD_L, CD_R - Analog CD Source, Inputs, Pins 18 and 20**

These inputs form a stereo input pair to the CS4299. It is intended to be used for the Red Book CD audio connection to the audio subsystem. The maximum allowable input is 1 $V_{RMS}$ (sinusoidal). These inputs are internally biased at the Vrefout voltage reference and require AC-coupling to external circuitry. If these inputs are not used, they should both be connected to the Vrefout pin or both AC-coupled, with separate AC-coupling caps, to analog ground.

**CD_GND - Analog CD Common Source, Input, Pin 19**

This analog input is used to remove common mode noise from Red Book CD audio signals. The impedance on the input signal path should be one half the impedance on the CD_L and CD_R input paths. This pin requires AC-coupling to external circuitry. If this input is not used, it should be connected to the Vrefout pin or AC-coupled to analog ground.

**VIDEO_L, VIDEO_R - Analog Video Audio Source, Inputs, Pins 16 and 17**

These inputs form a stereo input pair to the CS4299. It is intended to be used for the audio signal output of a video device. The maximum allowable input is 1 $V_{RMS}$ (sinusoidal). These inputs are internally biased at the Vrefout voltage reference and require AC-coupling to external circuitry. If these inputs are not used, they should both be connected to the Vrefout pin or both AC-coupled, with separate AC-coupling caps, to analog ground.

**AUX_L, AUX_R - Analog Auxiliary Source, Inputs, Pins 14 and 15**

These inputs form a stereo input pair to the CS4299. The maximum allowable input is 1 $V_{RMS}$ (sinusoidal). These inputs are internally biased at the Vrefout voltage reference and require AC-coupling to external circuitry. If these inputs are not used, they should both be connected to the Vrefout pin or both AC-coupled, with separate AC-coupling caps, to analog ground.

**LINE_OUT_L, LINE_OUT_R - Analog Line-Level, Outputs, Pins 35 and 36**

These signals are analog outputs from the stereo output mixer. The full-scale output voltage for each output is nominally 1 $V_{RMS}$ (sinusoidal). These outputs are internally biased at the Vrefout voltage reference and require either AC-coupling to external circuitry or DC-coupling to a buffer op-amp biased at the Vrefout voltage. These pins need a 680-1000 pF NPO capacitor attached to analog ground.

**ALT_LINE_OUT_L, ALT _LINE_OUT_R - Analog Alternate Line-Level, Outputs, Pins 39 and 41**

These signals are analog outputs from the stereo output mixer. The full-scale output voltage for each output is nominally 1 $V_{RMS}$ (sinusoidal). These outputs are internally biased at the Vrefout voltage reference and require either AC-coupling to external circuitry or DC-coupling to a buffer op-amp biased at the Vrefout voltage. These pins need a 680-1000 pF NPO capacitor attached to analog ground.

**MONO_OUT - Analog Mono Line-Level, Output, Pin 37**

This signal is an analog output from the stereo-to-mono mixer or MIC1/2. The full-scale output voltage for this output is nominally 1 $V_{RMS}$ (sinusoidal). This output is internally biased at the Vrefout voltage reference and requires either AC-coupling to external circuitry or DC-coupling to a buffer op-amp biased at the Vrefout voltage. This pin needs a 680-1000 pF NPO capacitor attached to analog ground.

## *Clock and Configuration*

**XTL_IN - Crystal Input/Clock Input, Pin 2**

In primary mode this pin requires either a 24.576 MHz crystal, with the other pin attached to XTL_OUT, or an external CMOS clock. The crystal frequency must be 24.576 MHz and designed for fundamental mode, parallel resonance operation. If an external CMOS clock is used to drive this pin, it must run at 24.576 MHz. In secondary mode all timing is derived from the BIT_CLK input signal and this pin should be left floating.

**XTL_OUT - Crystal Output, Pin 3**

This pin is used when a crystal is placed between XTL_OUT and XLT_IN. If an external 24.576 MHz clock is used on XTL_IN, this pin must be left floating with no traces or components connected to it. In secondary mode this pin should be left floating.

**ID1#, ID0# - Codec ID, Inputs, Pins 45 and 46**

These pins select the Codec ID and mode of operation for the CS4299. They are only sampled after the rising edge of RESET#. These pins are internally pulled up to the digital supply voltage and should be left floating for logic ‘0’ or tied to digital ground for logic ‘1’. When both pins are left floating the CS4299 is the primary codec. If either or both pins are tied to ground the CS4299 is a secondary codec.

*Analog Reference, Filters, and Configuration*

**REFFLT - Internal Reference Voltage, Input, Pin 27**

This signal is the voltage reference used internal to the CS4299. A 0.1 µF and a 1.0 µF (must not be larger than 1 µF) capacitor with short, wide traces must be connected to this pin. No other connections should be made to this pin.

**Vrefout - Voltage Reference, Output, Pin 28**

All analog inputs and outputs are centered around Vrefout, nominally 2.3 Volts. This pin may be used to level shift external circuitry. This pin cannot drive any DC loads, thus any external loading must be buffered.

**AFLT1 - Left ADC Channel Antialiasing Filter, Input, Pin 29**

This pin needs a 1000 pF NPO capacitor connected to analog ground.

**AFLT2 - Right ADC Channel Antialiasing Filter, Input, Pin 30**

This pin needs a 1000 pF NPO capacitor connected to analog ground.

**FLTI, FLTO - 3D Filter, Input, Pin 33 and 34**

A 1000 pF capacitor must be connected between FLTI and FLTO if the 3D function is used.

**FLT3D - 3D Filter, Input, Pin 32**

A 0.01 µF capacitor must be connected from this pin to AGND if the 3D function is used.

**BCFG - Beep Configuration, Input, Pin 31**

This pin is the configuration control for the PC_BEEP bypass path. If this pin is grounded, the bypass path is disabled. If this pin is left floating, the PC_BEEP bypass path is enabled.

*Misc. Digital Interfaces*

**S/PDIF_OUT - Sony/Philips Digital Interface, Output, Pin 48**

This pin generates the S/PDIF digital output from the CS4299 when the SPEN bit in the *S/PDIF Control Register (Index 68h)* is 'set'. This output may be used to directly drive a resistive divider and coupling transformer to an RCA-type connector for use with consumer audio equipment.

**EAPD - External Amplifier Powerdown, Output, Pin 47**

This pin is used to control the powerdown state of an audio amplifier external to the CS4299. The output is controlled by the EAPD bit in the *Powerdown Ctrl/Stat Register (Index 26h)*. It is driven as a normal CMOS output and defaults low ('0') upon power-up.

*AC-Link*

**RESET# - AC '97 Chip Reset, Input, Pin 11**

This active low signal is the asynchronous Cold Reset input to the CS4299. The CS4299 must be reset before it can enter normal operating mode.

**SYNC - AC-Link Serial Port Sync pulse, Input, Pin 10**

This signal is the serial port timing signal for the AC-link. Its period is the reciprocal of the maximum sample rate, 48 kHz. The signal is generated by the controller, synchronous to BIT_CLK. SYNC is an asynchronous input when the CS4299 is configured as a primary audio codec and is in a PR4 powerdown state. A series terminating resistor of 47 Ω should be connected on the signal near the SYNC source.

**BIT_CLK - AC-Link Serial Port Master Clock, Input/Output, Pin 6**

This input/output signal controls the master clock timing for the AC-link. In primary mode, this signal is a 12.288 MHz output clock derived from a 24.576 MHz crystal on the XTL_IN input clock. When the CS4299 is in secondary mode, this signal is an input which controls the AC-link serial interface and generates all internal clocking including the AC-link serial interface timing and the analog sampling clocks. A series terminating resistor of 47 Ω should be connected on this signal close to the CS4299 in primary mode or close to the BIT_CLK source in secondary mode.

**SDATA_OUT - AC-Link Serial Data Input Stream to AC '97, Input, Pin 5**

This input signal receives the control information and digital audio output streams. The data is clocked into the CS4299 on the falling edge of BIT_CLK. A series terminating resistor of 47 Ω should be connected on this signal near the controller.

**SDATA_IN - AC-Link Serial Data Output Stream from AC '97, Output, Pin 8**

This output signal transmits the status information and digital audio input streams from the ADCs. The data is clocked out of the CS4299 on the rising edge of BIT_CLK. A series terminating resistor of 47 Ω should be connected on this signal as close to the CS4299 as possible.

*Power Supplies*

**DVdd1, DVdd2 - Digital Supply Voltage, Pins 1 and 9**

Digital supply voltage for the AC-link section of the CS4299. These pins can be tied to +5 V digital or to +3.3 V digital. The CS4299 and controller AC-link should share a common digital supply

**DVss1, DVss2 - Digital Ground, Pins 4 and 7**

Digital ground connection for the AC-link section of the CS4299. These pins should be isolated from analog ground currents.

**AVdd1, AVdd2 - Analog Supply Voltage, Pins 25 and 38**

Analog supply voltage for the analog and mixed signal sections of the CS4299. These pins must be tied to the analog +5 V power supply. It is strongly recommended that +5 V be generated from a voltage regulator to ensure proper supply currents and noise immunity from the rest of the system.

**AVss1, AVss2 - Analog Ground, Pins 26 and 42**

Ground connection for the analog, mixed signal, and substrate sections of the CS4299. These pins should be isolated from digital ground currents.

# 10 Parameter and Term Definitions

**AC '97 Specification**

Refers to the *Audio Codec '97 Component Specification Ver 2.1* published by the Intel® Corporation [6].

**AC '97 Controller or Controller**

Refers to the control chip which interfaces to the audio codec AC-link. This has been also called *DC '97* for Digital Controller '97 [6].

**AC '97 Registers or Codec Registers**

Refers to the 64-field register map defined in the AC '97 Specification.

**ADC**

Refers to a single Analog-to-Digital converter in the CS4299. "ADCs" refers to the stereo pair of Analog-to-Digital converters. The CS4299 ADCs have 18-bit resolution.

**Codec**

Refers to the chip containing the ADCs, DACs, and analog mixer. In this data sheet, the codec is the CS4299.

**DAC**

Refers to a single Digital-to-Analog converter in the CS4299. "DACs" refers to the stereo pair of Digital-to-Analog converters. The CS4299 DACs have 20-bit resolution.

**dB FS A**

dB FS is defined as dB relative to full-scale. The "A" indicates an A weighting filter was used.

**Differential Nonlinearity**

The worst case deviation from the ideal code width. Units in LSB.

**Dynamic Range (DR)**

DR is the ratio of the RMS full-scale signal level divided by the RMS sum of the noise floor, in the presence of a signal, available at any instant in time (no change in gain settings between measurements). Measured over a 20 Hz to 20 kHz bandwidth with units in dB FS A.

**FFT**

Fast Fourier Transform.

**Frequency Response (FR)**

FR is the deviation in signal level verses frequency. The 0 dB reference point is 1 kHz. The amplitude corner, Ac, lists the maximum deviation in amplitude above and below the 1 kHz reference point. The listed minimum and maximum frequencies are guaranteed to be within the Ac from minimum frequency to maximum frequency inclusive.

**Fs**

Sampling Frequency.

**Interchannel Gain Mismatch**

For the ADCs, the difference in input voltage to get an equal code on both channels. For the DACs, the difference in output voltages for each channel when both channels are fed the same code. Units are in dB.

**Interchannel Isolation**

The amount of 1 kHz signal present on the output of the grounded AC-coupled line input channel with 1 kHz, 0 dB, signal present on the other line input channel. Units are in dB.

**Line-level**

Refers to a consumer equipment compatible, voltage driven interface. The term implies a low driver impedance and a minimum 10 kΩ load impedance.

**Paths**

A-D: Analog in, through the ADCs, onto the serial link.

D-A: Serial interface inputs through the DACs to the analog output.

A-A: Analog in to Analog out (analog mixer).

**PC 99**

Refers to the *PC 99 System Design Guide* published by the Microsoft® Corporation [7].

**PLL**

Phase Lock Loop. Circuitry for generating a desired clock from an external clock source.

**Resolution**

The number of bits in the output words to the DACs, and in the input words to the ADCs.

**Signal to Noise Ratio (SNR)**

SNR, similar to DR, is the ratio of an arbitrary sinusoidal input signal to the RMS sum of the noise floor, in the presence of a signal. It is measured over a 20 Hz to 20 kHz bandwidth with units in dB.

**S/PDIF**

Sony/Phillips Digital Interface. This interface was established as a means of digitally interconnecting consumer audio equipment. The documentation for S/PDIF has been superseded by the IEC-958 consumer digital interface document.

**SRC**

Sample Rate Converter. Converts data derived at one sample rate to a differing sample rate. The CS4299 operates at a fixed sample frequency of 48 kHz. The internal sample rate converters are used to convert digital audio streams playing back at other frequencies to 48 kHz.

**Total Harmonic Distortion plus Noise (THD+N)**

THD+N is the ratio of the RMS sum of all non-fundamental frequency components, divided by the RMS full-scale signal level. It is tested using a -3 dB FS input signal and is measured over a 20 Hz to 20 kHz bandwidth with units in dB FS.

# 11 Reference Design

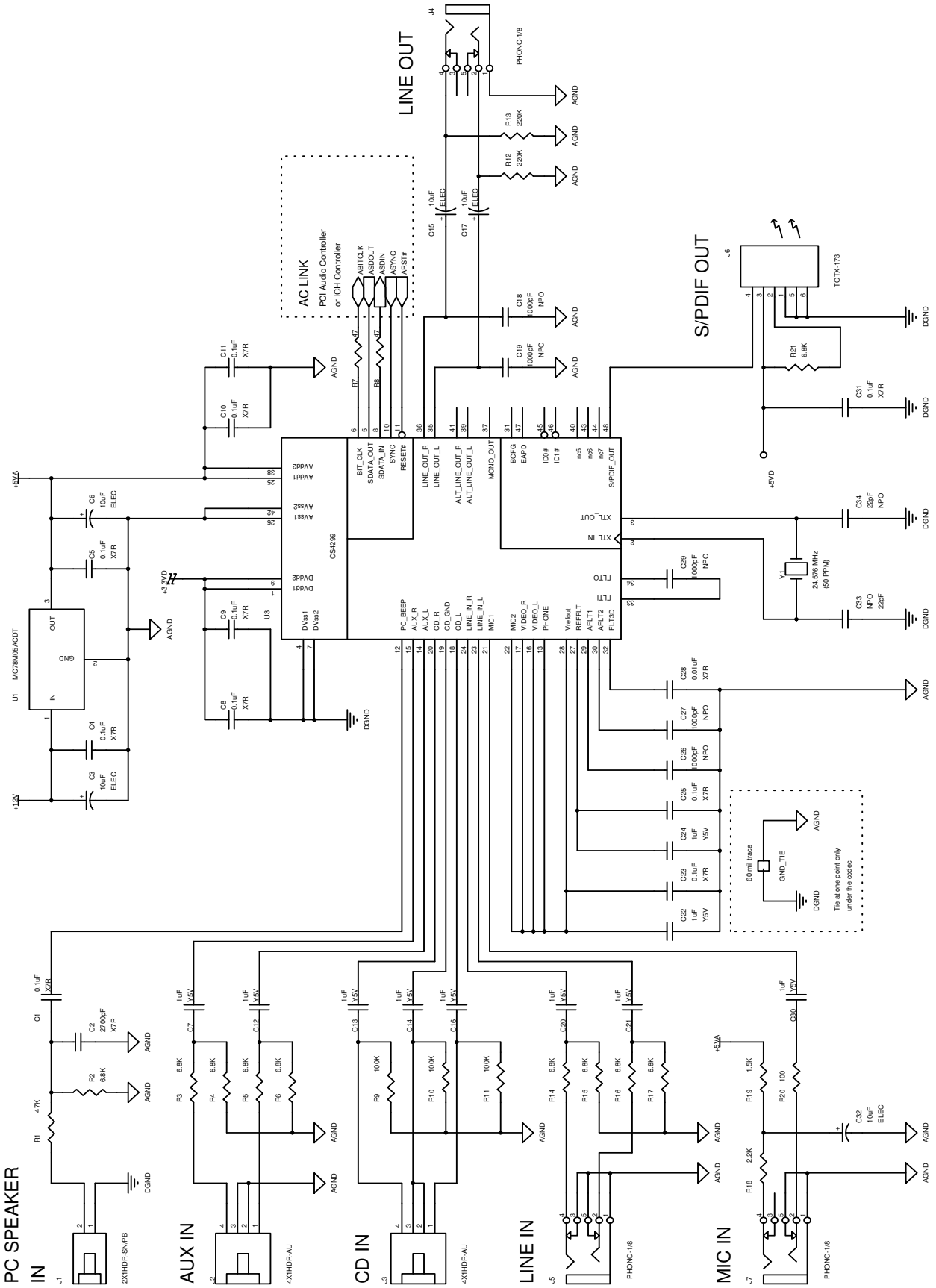



**Figure 11-1. CS4299 Reference Design**

# 12 References

1) Cirrus Logic, Audio Quality Measurement Specification, Version 1.0, 1997
*http://www.cirrus.com/en/pubs/whitePaper/meas100.pdf*

2) Cirrus Logic, AN18: Layout and Design Rules for Data Converters and Other Mixed Signal Devices, Version 6.0, February 1998

3) Cirrus Logic, AN22: Overview of Digital Audio Interface Data Structures, Version 2.0, February 1998

4) Cirrus Logic, AN134: AES and S/PDIF Recommended Transformers, Version 2, April 1999

5) Cirrus Logic, AN165: CS4297A/CS4299 EMI Reduction Techniques, Version 1.0, September 1999

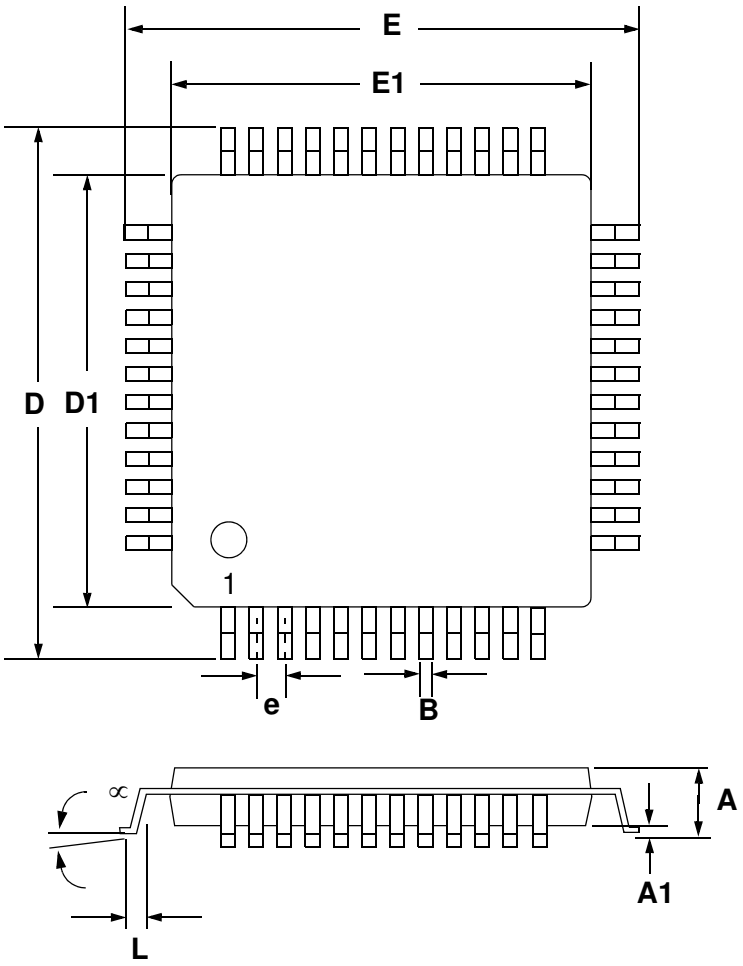
6) Intel®, Audio Codec ’97 Component Specification, Revision 2.1, May 1998

7) Microsoft®, PC 99 System Design Guide, Version 1.0, July 1999

8) Intel®, 82801AA (ICH) and 82801AB (ICH0) I/O Controller Hub, June 1999
*http://www.intel.com/design/chipsets/datashts/290655.htm*

# 13 Package Dimensions

## 48L LQFP PACKAGE DRAWING




| | INCHES | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|
| DIM | MIN | NOM | MAX | MIN | NOM | MAX |
| A | --- | 0.055 | 0.063 | --- | 1.40 | 1.60 |
| A1 | 0.002 | 0.004 | 0.006 | 0.05 | 0.10 | 0.15 |
| B | 0.007 | 0.009 | 0.011 | 0.17 | 0.22 | 0.27 |
| D | 0.343 | 0.354 | 0.366 | 8.70 | 9.0 BSC | 9.30 |
| D1 | 0.272 | 0.28 | 0.280 | 6.90 | 7.0 BSC | 7.10 |
| E | 0.343 | 0.354 | 0.366 | 8.70 | 9.0 BSC | 9.30 |
| E1 | 0.272 | 0.28 | 0.280 | 6.90 | 7.0 BSC | 7.10 |
| e* | 0.016 | 0.020 | 0.024 | 0.40 | 0.50 BSC | 0.60 |
| L | 0.018 | 0.24 | 0.030 | 0.45 | 0.60 | 0.75 |
| ∝ | 0.000° | 4° | 7.000° | 0.00° | 4° | 7.00° |

* Nominal pin pitch is 0.50 mm

Controlling dimension is mm.
JEDEC Designation: MS022

# 14 Revision History

| Revision | Date | Change |
|---|---|---|
| PP6 | March, 2006 | Updated suffixes of JQ/KQ to JQZ/KQZ. Added lead-free designator. |
| F1 | June, 2015 | De-featured -K variation. Added -B variations. |

**Important**: Please check www.Cirrus.com or with your Cirrus sales representative to confirm that you are using the latest revision of this document and to determine whether there are errata associated with this device.

## Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.

**IMPORTANT NOTICE**

The products and services of Cirrus Logic International (UK) Limited; Cirrus Logic, Inc.; and other companies in the Cirrus Logic group ("Cirrus") are sold subject to Cirrus's terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, indemnification, and limitation of liability. Software is provided pursuant to applicable license terms. Cirrus reserves the right to make changes to its products and specifications or to discontinue any product or service without notice. Customers should therefore obtain the latest version of relevant information from Cirrus to verify that the information is current and complete. Testing and other quality control techniques are utilized to the extent Cirrus deems necessary. Specific testing of all parameters of each device is not necessarily performed. In order to minimize risks associated with customer applications, the customer must use adequate design and operating safeguards to minimize inherent or procedural hazards. Cirrus is not liable for applications assistance or customer product design. The customer is solely responsible for its selection and use of Cirrus products.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). CIRRUS PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED FOR USE IN PRODUCTS SURGICALLY IMPLANTED INTO THE BODY, AUTOMOTIVE SAFETY OR SECURITY DEVICES, NUCLEAR SYSTEMS, LIFE SUPPORT PRODUCTS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF CIRRUS PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK AND CIRRUS DISCLAIMS AND MAKES NO WARRANTY, EXPRESS, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR PARTICULAR PURPOSE, WITH REGARD TO ANY CIRRUS PRODUCT THAT IS USED IN SUCH A MANNER. IF THE CUSTOMER OR CUSTOMER'S CUSTOMER USES OR PERMITS THE USE OF CIRRUS PRODUCTS IN CRITICAL APPLICATIONS, CUSTOMER AGREES, BY SUCH USE, TO FULLY INDEMNIFY CIRRUS, ITS OFFICERS, DIRECTORS, EMPLOYEES, DISTRIBUTORS AND OTHER AGENTS FROM ANY AND ALL LIABILITY, INCLUDING ATTORNEYS' FEES AND COSTS, THAT MAY RESULT FROM OR ARISE IN CONNECTION WITH THESE USES.

This document is the property of Cirrus and by furnishing this information, Cirrus grants no license, express or implied, under any patents, mask work rights, copyrights, trademarks, trade secrets or other intellectual property rights. Any provision or publication of any third party's products or services does not constitute Cirrus's approval, license, warranty or endorsement thereof. Cirrus gives consent for copies to be made of the information contained herein only for use within your organization with respect to Cirrus integrated circuits or other products of Cirrus, and only if the reproduction is without alteration and is accompanied by all associated copyright, proprietary and other notices and conditions (including this notice). This consent does not extend to other copying such as copying for general distribution, advertising or promotional purposes, or for creating any work for resale. This document and its information is provided "AS IS" without warranty of any kind (express or implied). All statutory warranties and conditions are excluded to the fullest extent possible. No responsibility is assumed by Cirrus for the use of information herein, including use of this information as the basis for manufacture or sale of any items, or for infringement of patents or other rights of third parties. Cirrus Logic, Cirrus, the Cirrus Logic logo design, CrystalClear, SoundFusion, and SoundClear are among the trademarks of Cirrus. Other brand and product names may be trademarks or service marks of their respective owners.

Copyright © 2001–2015 Cirrus Logic, Inc. All rights reserved.

Microsoft is a registered trademark of Microsoft Corporation in the United States and/or other countries.

Intel is a registered trademark of Intel Corporation.