CS5381

120 dB, 192 kHz, Multi-Bit Audio A/D Converter

Features

- Advanced Multi-bit Delta-Sigma Architecture
- 24-bit Conversion
- 120 dB Dynamic Range
- -110 dB THD+N
- Supports All Audio Sample Rates Including 192 kHz
- 260 mW Power Consumption
- High-Pass Filter or DC Offset Calibration
- Supports Logic Levels between 5 and 2.5 V
- Differential Analog Architecture
- Low-Latency Digital Filtering
- Overflow Detection
- Pin-Compatible with the CS5361

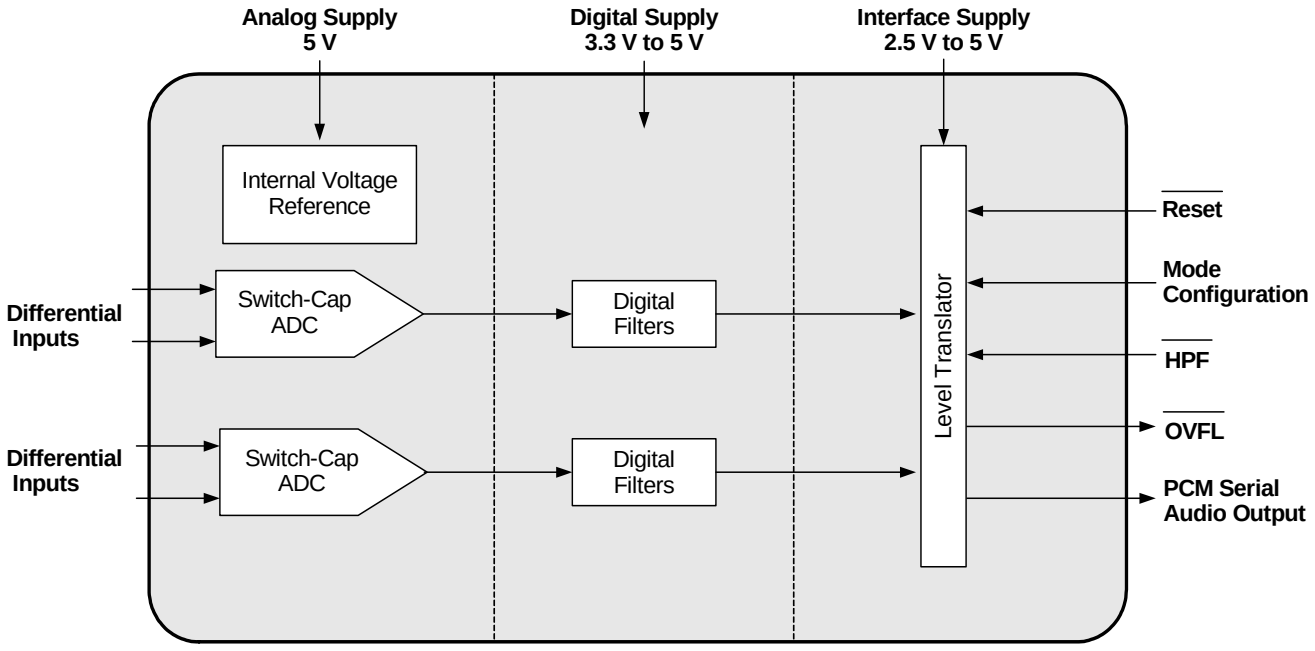
General Description

The CS5381 is a complete analog-to-digital converter for digital audio systems. It performs sampling, analog-to-digital conversion, and anti-alias filtering - generating 24-bit values for both left and right inputs in serial form at sample rates up to 216 kHz per channel.

The CS5381 uses a 5th-order, multi-bit delta-sigma modulator followed by digital filtering and decimation, which removes the need for an external anti-alias filter. The ADC uses a differential architecture which provides excellent noise rejection.

The CS5381 is available in 24-pin TSSOP and SOIC packages for Commercial grade (-10° to +70° C). The CDB5381 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please refer to the "Ordering Information" on page 22.

The CS5381 is ideal for audio systems requiring wide dynamic range, negligible distortion, and low noise - such as A/V receivers, DVD-R, CD-R, digital mixing consoles, and effects processors.



Copyright © Cirrus Logic, Inc. 2005
(All Rights Reserved)

TABLE OF CONTENTS

1. PIN DESCRIPTIONS 4
2. CHARACTERISTICS AND SPECIFICATIONS 5
SPECIFIED OPERATING CONDITIONS 5
ABSOLUTE MAXIMUM RATINGS 5
ANALOG CHARACTERISTICS (CS5381-KSZ/-KZZ) 6
DIGITAL FILTER CHARACTERISTICS 7
SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT 10
DC ELECTRICAL CHARACTERISTICS 13
DIGITAL CHARACTERISTICS 13
THERMAL CHARACTERISTICS 13
TYPICAL CONNECTION DIAGRAM 14
3. APPLICATIONS 15
3.1 Operational Mode/Sample Rate Range Select 15
3.2 System Clocking 15
3.2.1 Master Mode 15
3.2.2 Slave Mode 16
3.3 Power-Up Sequence 16
3.4 Analog Connections 16
3.5 High-Pass Filter and DC Offset Calibration 17
3.6 Overflow Detection 18
3.6.1 OVFL Configuration 18
3.6.2 OVFL Output Timing 18
3.7 Grounding and Power Supply Decoupling 18
3.8 Synchronization of Multiple Devices 18
3.9 Capacitor Size on the Reference Pin (FILT+) 19
4. PACKAGE DIMENSIONS 20
5. ORDERING INFORMATION 22
7. REVISION HISTORY 24

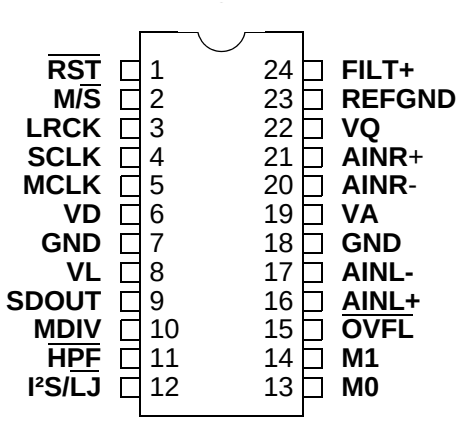
LIST OF FIGURES

Figure 1. Single-Speed Mode Stopband Rejection 8
Figure 2. Single-Speed Mode Transition Band 8
Figure 3. Single-Speed Mode Transition Band (Detail) 8
Figure 4. Single-Speed Mode Passband Ripple 8
Figure 5. Double-Speed Mode Stopband Rejection 8
Figure 6. Double-Speed Mode Transition Band 8
Figure 7. Double-Speed Mode Transition Band (Detail) 9
Figure 8. Double-Speed Mode Passband Ripple 9
Figure 9. Quad-Speed Mode Stopband Rejection 9
Figure 10. Quad-Speed Mode Transition Band 9
Figure 11. Quad-Speed Mode Transition Band (Detail) 9
Figure 12. Quad-Speed Mode Passband Ripple 9
Figure 13. Master Mode, Left-Justified SAI 11
Figure 14. Slave Mode, Left-Justified SAI 11
Figure 15. Master Mode, I²S SAI 11
Figure 16. Slave Mode, I²S SAI 11
Figure 17. OVFL Output Timing 11
Figure 18. Left-Justified Serial Audio Interface 12
Figure 19. I²S Serial Audio Interface 12
Figure 20. OVFL Output Timing, I²S Format 12
Figure 21. OVFL Output Timing, Left-Justified Format 12
Figure 22. Typical Connection Diagram 14
Figure 23. CS5381 Master Mode Clocking 15
Figure 24. Recommended Analog Input Buffer 17
Figure 25. CS5381 THD + N versus Frequency 19

LIST OF TABLES

Table 1. CS5381 Mode Control 15
Table 2. CS5381 Common Master Clock Frequencies 16
Table 3. CS5381 Slave Mode Clock Ratios 16

1. PIN DESCRIPTIONS



Pin Name	#	Pin Description
RST	1	**Reset** (*Input*) - The device enters a low power mode when low.
M/S	2	**Master/Slave Mode** *(Input)* - Selects operation as either clock master or slave.
LRCK	3	**Left Right Clock** (*Input*/*Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
SCLK	4	**Serial Clock** (*Input*/*Output*) - Serial clock for the serial audio interface.
MCLK	5	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
VD	6	**Digital Power** (*Input*) **-** Positive power supply for the digital section.
GND	7,18	**Ground** (*Input*) - Ground reference. Must be connected to analog ground.
VL	8	**Logic Power** (*Input*) **-** Positive power for the digital input/output.
SDOUT	9	**Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data.
MDIV	10	**MCLK Divider** *(Input*) **-** Enables a master clock divide by two function.
HPF	11	High-Pass Filter Enable *(Input*) - Enables the Digital High-Pass Filter.
I²S/LJ	12	**Serial Audio Interface Format Select** (*Input*) -Selects either the left-justified or I²S format for the SAI.
M0 M1	13,14	**Mode Selection** (*Input*) - Determines the operational mode of the device.
OVFL	15	**Overflow** *(Output, open drain)* **-** Detects an overflow condition on both left and right channels.
AINL+ AINL-	16, 17	**Differential Left Channel Analog Input** (*Input*) - Signals are presented differentially to the delta-sigma modulators via the AINL+/- pins.
VA	19	**Analog Power** (*Input*) **-** Positive power supply for the analog section.
AINR- AINR+	20, 21	**Differential Right Channel Analog Input** (*Input*) -Signals are presented differentially to the delta-sigma modulators via the AINR+/- pins.
VQ	22	**Quiescent Voltage** *(Output)* **-** Filter connection for the internal quiescent reference voltage.
REF_GND	23	**Reference Ground** (*Input*) - Ground reference for the internal sampling circuits.
FILT+	24	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.

2. CHARACTERISTICS AND SPECIFICATIONS

All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at VA = 5.0 V, VD = VL = 3.3 V, and TA = 25°C.

SPECIFIED OPERATING CONDITIONS

(GND = 0 V; all voltages with respect to 0 V.)

Parameters	Symbol	Min	Typ	Max	Units
DC Power Supply					
DC Power Supplies: Positive Analog	VA	4.75	5.0	5.25	V
Positive Digital	VD	3.1	-	5.25	V
Positive Logic	VL	2.37	-	5.25	V
Ambient Operating Temperature (Power Applied)	T_A	-10	-	+70	°C

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V, All voltages with respect to ground.) (Note 1)

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies: Analog	VA	-0.3	-	+6.0	V
Logic	VL	-0.3	-	+6.0	V
Digital	VD	-0.3	-	+6.0	V
Input Current (Note 2)	I_{in}	-10	-	+10	mA
Analog Input Voltage (Note 3)	V_{IN}	GND-0.7	-	VA+0.7	V
Digital Input Voltage (Note 3)	V_{IND}	-0.7	-	VL+0.7	V
Ambient Operating Temperature (Power Applied)	T_A	-50	-	+95	°C
Storage Temperature	T_{stg}	-65	-	+150	°C

Notes:

1. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.
2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SRC latch-up.
3. The maximum over/under voltage is limited by the input current.

ANALOG CHARACTERISTICS (CS5381-KSZ/-KZZ)

Test conditions (unless otherwise specified): Input test signal is a 1 kHz sine wave; measurement bandwidth is 10 Hz to 20 kHz.

Parameter		Symbol	Min	Typ	Max	Unit
Single-Speed Mode Fs = 48 kHz						
Dynamic Range	A-weighted		114	120	-	dB
	unweighted		111	117	-	dB
Total Harmonic Distortion + Noise	(Note 4)					
			-	-110	-104	dB
	-1 dB	THD+N	-	-97	-	dB
	-20 dB		-	-57	-	dB
	-60 dB					
Double-Speed Mode Fs = 96 kHz						
Dynamic Range	A-weighted		114	120	-	dB
	unweighted		111	117	-	dB
	40 kHz bandwidth unweighted		-	114	-	dB
Total Harmonic Distortion + Noise	(Note 4)					
			-	-110	-104	dB
	-1 dB	THD+N	-	-97	-	dB
	-20 dB		-	-57	-	dB
	-60 dB		-	-107	-	dB
	40 kHz bandwidth -1 dB					
Quad-Speed Mode Fs = 192 kHz						
Dynamic Range	A-weighted		114	120	-	dB
	unweighted		111	117	-	dB
	40 kHz bandwidth unweighted		-	114	-	dB
Total Harmonic Distortion + Noise	(Note 4)					
			-	-110	-104	dB
	-1 dB	THD+N	-	-97	-	dB
	-20 dB		-	-57	-	dB
	-60 dB		-	-107	-	dB
	40 kHz bandwidth -1 dB					
Dynamic Performance for All Modes						
Interchannel Isolation			-	110	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	-	dB
Gain Error			-5	-	5	%
Gain Drift			-	±100	-	ppm/°C
Offset Error	HPF enabled		-	0	-	LSB
	HPF disabled		-	100	-	LSB
Analog Input Characteristics						
Full-scale Input Voltage			1.07*VA	1.13*VA	1.18*VA	Vpp
Input Impedance (Differential)	(Note 5)		-	2.5	-	kΩ
Common Mode Rejection Ratio		CMRR	-	100	-	dB

4. Referred to the typical full-scale input voltage.
5. Measured between AIN+ and AIN-.

DIGITAL FILTER CHARACTERISTICS

Parameter			Symbol	Min	Typ	Max	Unit
Single-Speed Mode (2 kHz to 54 kHz sample rates)							
Passband	(-0.1 dB)	(Note 6)		0	-	0.47	Fs
Passband Ripple				-0.1	-	0.035	dB
Stopband		(Note 6)		0.58	-	-	Fs
Stopband Attenuation				-95	-	-	dB
Total Group Delay (Fs = Output Sample Rate)			t_{gd}	-	12/Fs	-	s
Double-Speed Mode (50 kHz to 108 kHz sample rates)							
Passband	(-0.1 dB)	(Note 6)		0	-	0.45	Fs
Passband Ripple				-0.1	-	0.035	dB
Stopband		(Note 6)		0.68	-	-	Fs
Stopband Attenuation				-92	-	-	dB
Total Group Delay (Fs = Output Sample Rate)			t_{gd}	-	9/Fs	-	s
Quad-Speed Mode (100 kHz to 216 kHz sample rates)							
Passband	(-0.1 dB)	(Note 6)		0	-	0.24	Fs
Passband Ripple				-0.1	-	0.035	dB
Stopband		(Note 6)		0.78	-	-	Fs
Stopband Attenuation				-97	-	-	dB
Total Group Delay (Fs = Output Sample Rate)			t_{gd}	-	5/Fs	-	s
High-Pass Filter Characteristics							
Frequency Response	-3.0 dB -0.13 dB	(Note 7)		-	1 20	- -	Hz Hz
Phase Deviation	@ 20 Hz	(Note 7)		-	10	-	Deg
Passband Ripple				-	-	0	dB
Filter Setting Time					10^5/Fs		s

6. The filter frequency response scales precisely with Fs.

7. Response shown is for Fs equal to 48 kHz. Filter characteristics scale with Fs.

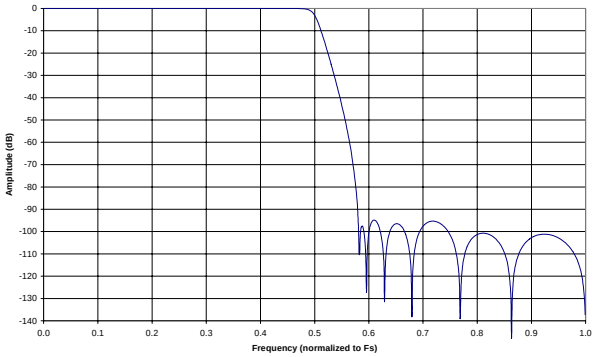


Figure 1. Single-Speed Mode Stopband Rejection

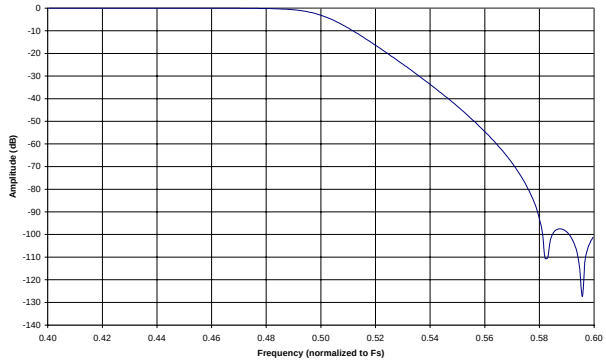


Figure 2. Single-Speed Mode Transition Band

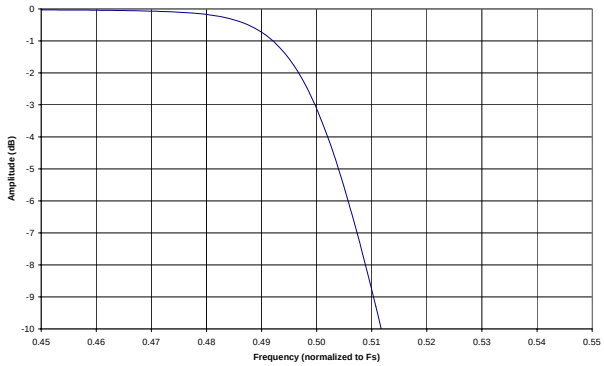


Figure 3. Single-Speed Mode Transition Band (Detail)

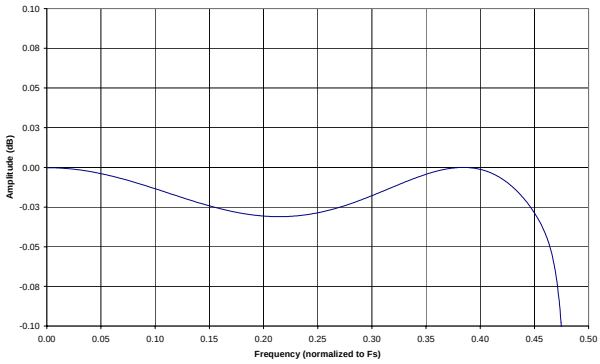


Figure 4. Single-Speed Mode Passband Ripple

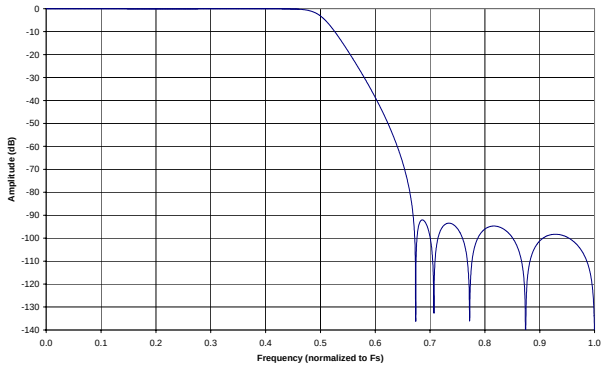


Figure 5. Double-Speed Mode Stopband Rejection

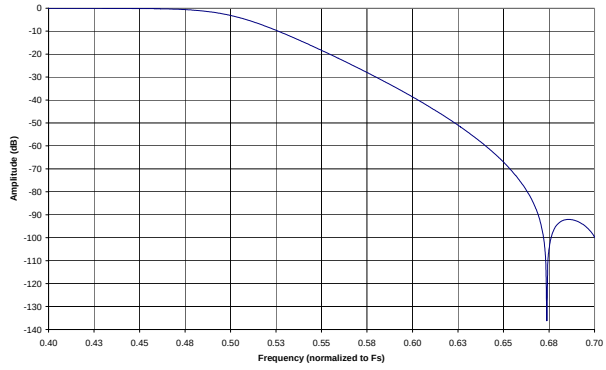


Figure 6. Double-Speed Mode Transition Band

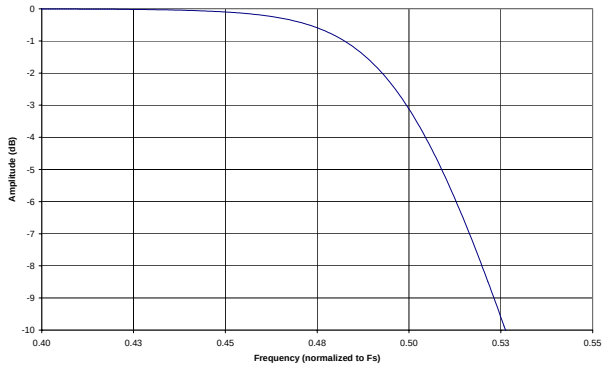


Figure 7. Double-Speed Mode Transition Band (Detail)

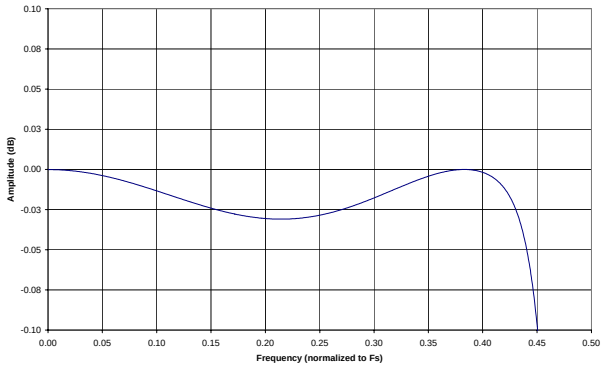


Figure 8. Double-Speed Mode Passband Ripple

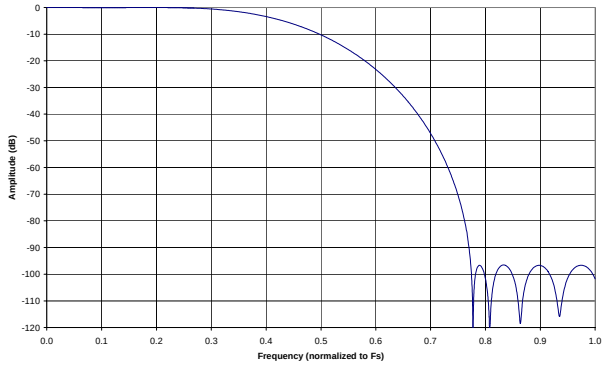


Figure 9. Quad-Speed Mode Stopband Rejection

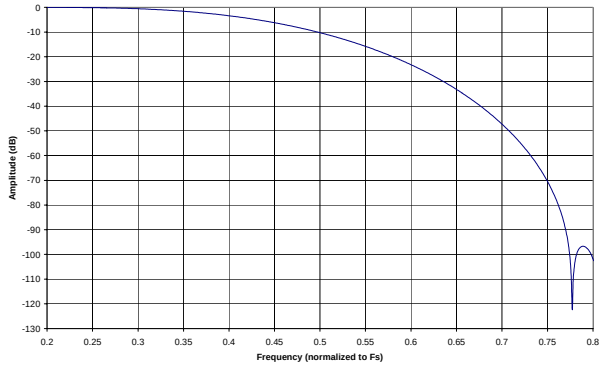


Figure 10. Quad-Speed Mode Transition Band

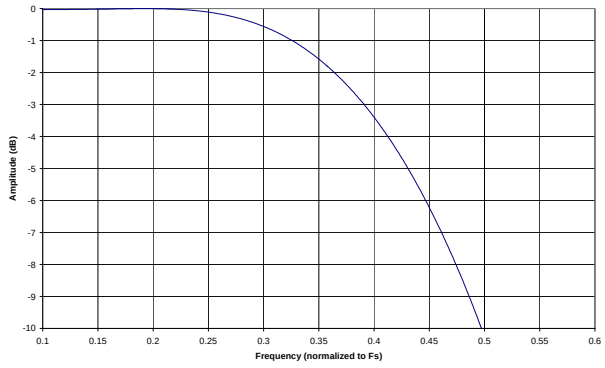


Figure 11. Quad-Speed Mode Transition Band (Detail)

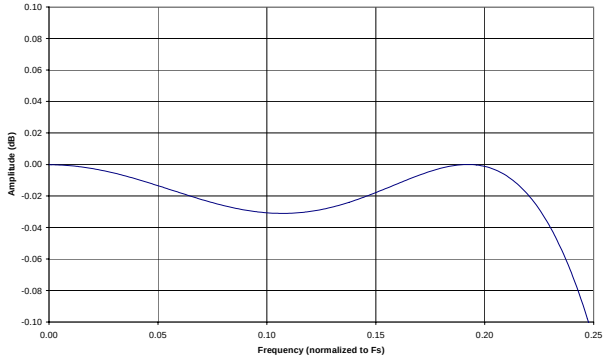


Figure 12. Quad-Speed Mode Passband Ripple

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT

(Logic “0” = GND = 0 V; Logic “1” = VL, C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Output Sample Rate Single-Speed Mode	Fs	2	-	54	kHz
Double-Speed Mode	Fs	50	-	108	kHz
Quad-Speed Mode	Fs	100	-	216	kHz
OVFL to LRCK Edge Setup Time	t_{setup}	$16/f_{sclk}$	-	-	s
OVFL to LRCK Edge Hold Time	t_{hold}	$1/f_{sclk}$	-	-	s
OVFL time-out on overrange condition					
Fs = 44.1, 88.2, 176.4 kHz		-	740	-	ms
Fs = 48, 96, 192 kHz		-	680	-	ms
MCLK Specifications					
MCLK Period	t_{clkw}	36	-	1953	ns
MCLK Duty Cycle		40	-	60	%
Master Mode					
SCLK falling to LRCK transition	t_{mslr}	-20	-	20	ns
SCLK falling to SDOUT valid	t_{sdo}	-	-	32	ns
SCLK Duty Cycle		-	50	-	%
Slave Mode					
Single-Speed					
Output Sample Rate	Fs	2	-	54	kHz
LRCK Duty Cycle		40	50	60	%
SCLK Period	t_{sclkw}	145	-	-	ns
SCLK Duty Cycle		45	50	55	%
SDOUT valid before SCLK rising	t_{stp}	10	-	-	ns
SDOUT valid after SCLK rising	t_{hld}	5	-	-	ns
SCLK falling to LRCK transition	t_{slrd}	-20	-	20	ns
Double-Speed					
Output Sample Rate	Fs	50	-	108	kHz
LRCK Duty Cycle		40	50	60	%
SCLK Period	t_{sclkw}	145	-	-	ns
SCLK Duty Cycle		45	50	55	%
SDOUT valid before SCLK rising	t_{stp}	10	-	-	ns
SDOUT valid after SCLK rising	t_{hld}	5	-	-	ns
SCLK falling to LRCK transition	t_{slrd}	-20	-	20	ns
Quad-Speed					
Output Sample Rate	Fs	100	-	216	kHz
LRCK Duty Cycle		40	50	60	%
SCLK Period	t_{sclkw}	72	-	-	ns
SCLK Duty Cycle		45	50	55	%
SDOUT valid before SCLK rising	t_{stp}	10	-	-	ns
SDOUT valid after SCLK rising	t_{hld}	5	-	-	ns
SCLK falling to LRCK transition	t_{slrd}	-8	-	8	ns

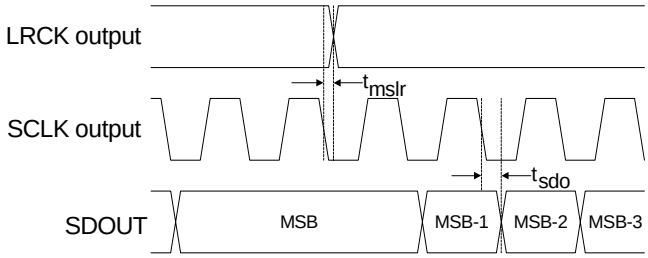


Figure 13. Master Mode, Left-Justified SAI

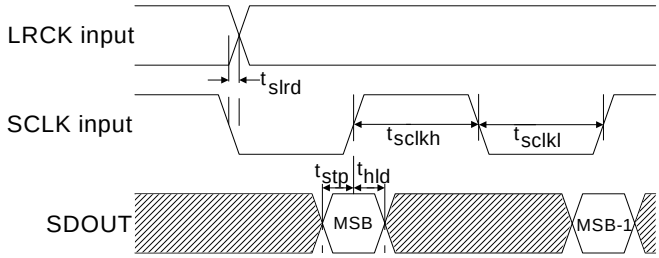


Figure 14. Slave Mode, Left-Justified SAI

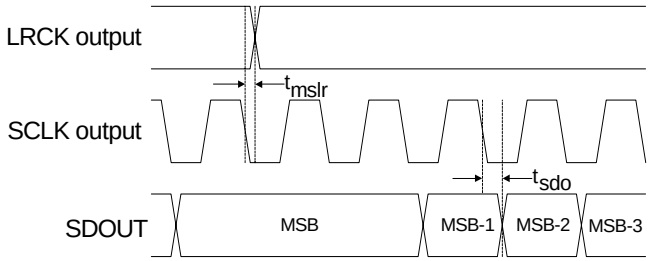


Figure 15. Master Mode, I²S SAI

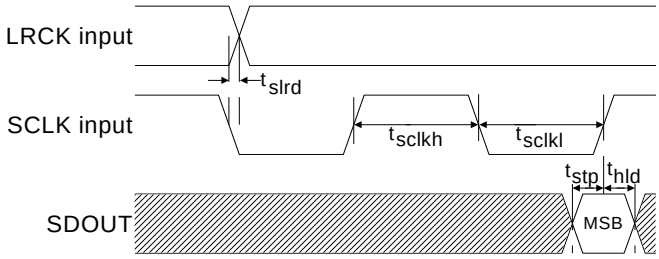


Figure 16. Slave Mode, I²S SAI

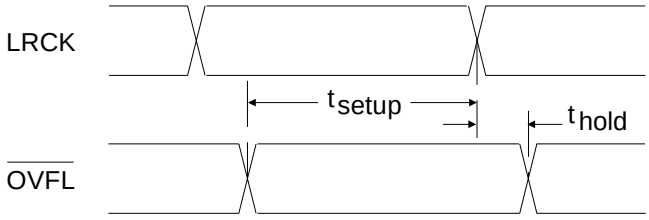


Figure 17. $\overline{\text{OVFL}}$ Output Timing

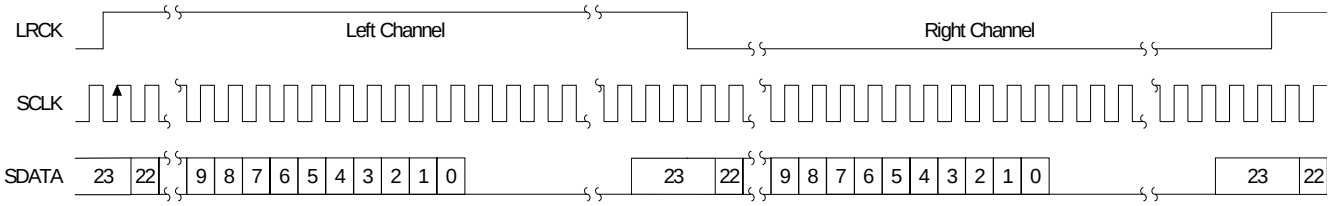


Figure 18. Left-Justified Serial Audio Interface

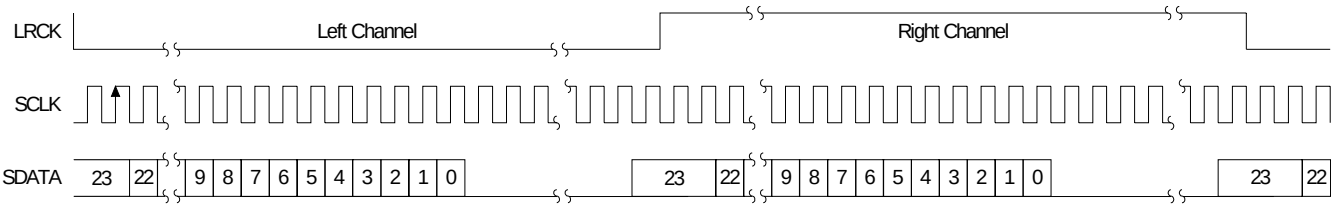


Figure 19. I²S Serial Audio Interface

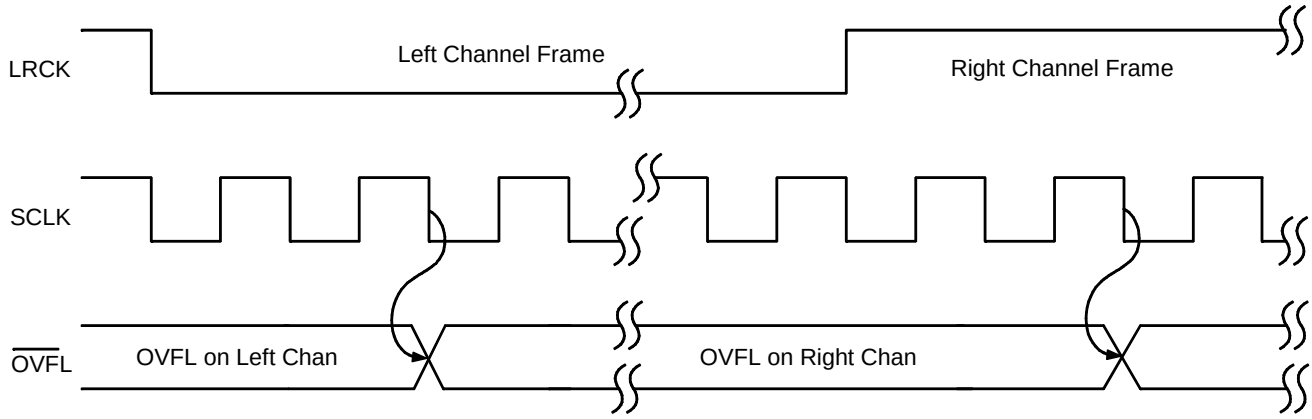


Figure 20. $\overline{\text{OVFL}}$ Output Timing, I²S Format

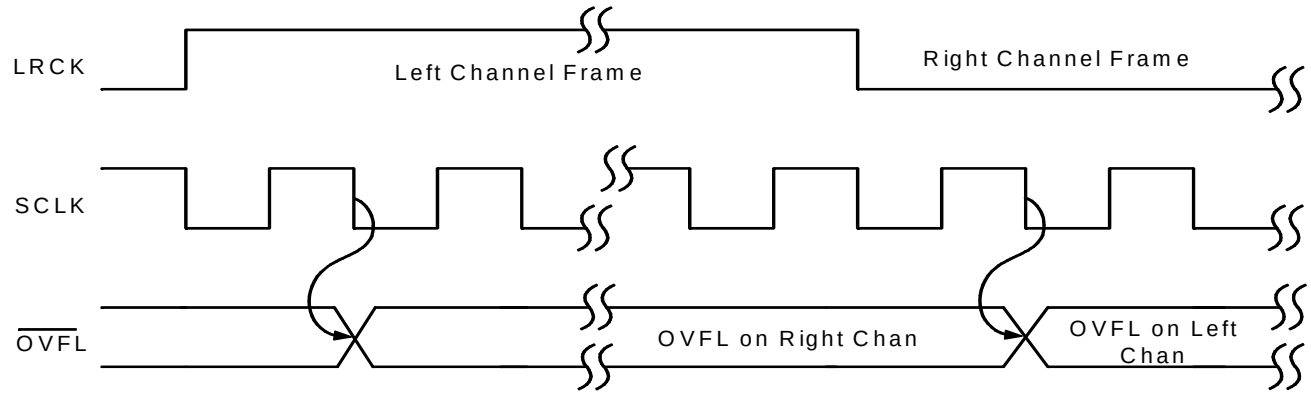


Figure 21. $\overline{\text{OVFL}}$ Output Timing, Left-Justified Format

DC ELECTRICAL CHARACTERISTICS

(GND = 0 V, all voltages with respect to ground. MCLK=12.288 MHz; Master Mode)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supply Current	VA = 5 V	I_A	-	36	43	mA
(Normal Operation)	VL,VD = 5 V	I_D	-	36	46	mA
	VL,VD = 3.3 V	I_D	-	24	28	mA
Power Supply Current	VA = 5 V	I_A	-	100	-	uA
(Power-Down Mode) (Note 8)	VL,VD = 5 V	I_D	-	100	-	uA
Power Consumption						
(Normal Operation)	VA, VL, VD = 5 V	-	-	360	445	mW
	VA = 5 V; VL, VD = 3.3 V	-	-	260	307	mW
	(Power-Down Mode)	-	-	1	-	mW
Power Supply Rejection Ratio (1 kHz)	(Note 9)	PSRR	-	65	-	dB
V_Q Nominal Voltage			-	2.5	-	V
Output Impedance			-	25	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA
Filt+ Nominal Voltage			-	5	-	V
Output Impedance			-	4.5	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA

8. Power-Down Mode is defined as $\overline{RST}$ = Low with all clocks and data lines held static.

9. Valid with the recommended capacitor values on FILT+ and VQ as shown in the Typical Connection Diagram.

DIGITAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	(% of VL)	V_{IH}	70%	-	-	V
Low-Level Input Voltage	(% of VL)	V_{IL}	-	-	30%	V
High-Level Output Voltage at I_o = 100 µA	(% of VL)	V_{OH}	70%	-	-	V
Low-Level Output Voltage at I_o = 100 µA	(% of VL)	V_{OL}	-	-	15%	V
$\overline{OVFL}$ Current Sink		I_{ovfl}	-	-	4.0	mA
Input Leakage Current		I_{in}	-10	-	10	µA

THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Allowable Junction Temperature		-	-	135	°C
Junction to Ambient Thermal Impedance					
(Multi-layer PCB) TSSOP	θ_{JA-TM}	-	70	-	°C/W
(Multi-layer PCB) SOIC	θ_{JA-SM}	-	60	-	°C/W
(Single-layer PCB) TSSOP	θ_{JA-TS}	-	105	-	°C/W
(Single-layer PCB) SOIC	θ_{JA-SS}	-	80	-	°C/W

TYPICAL CONNECTION DIAGRAM

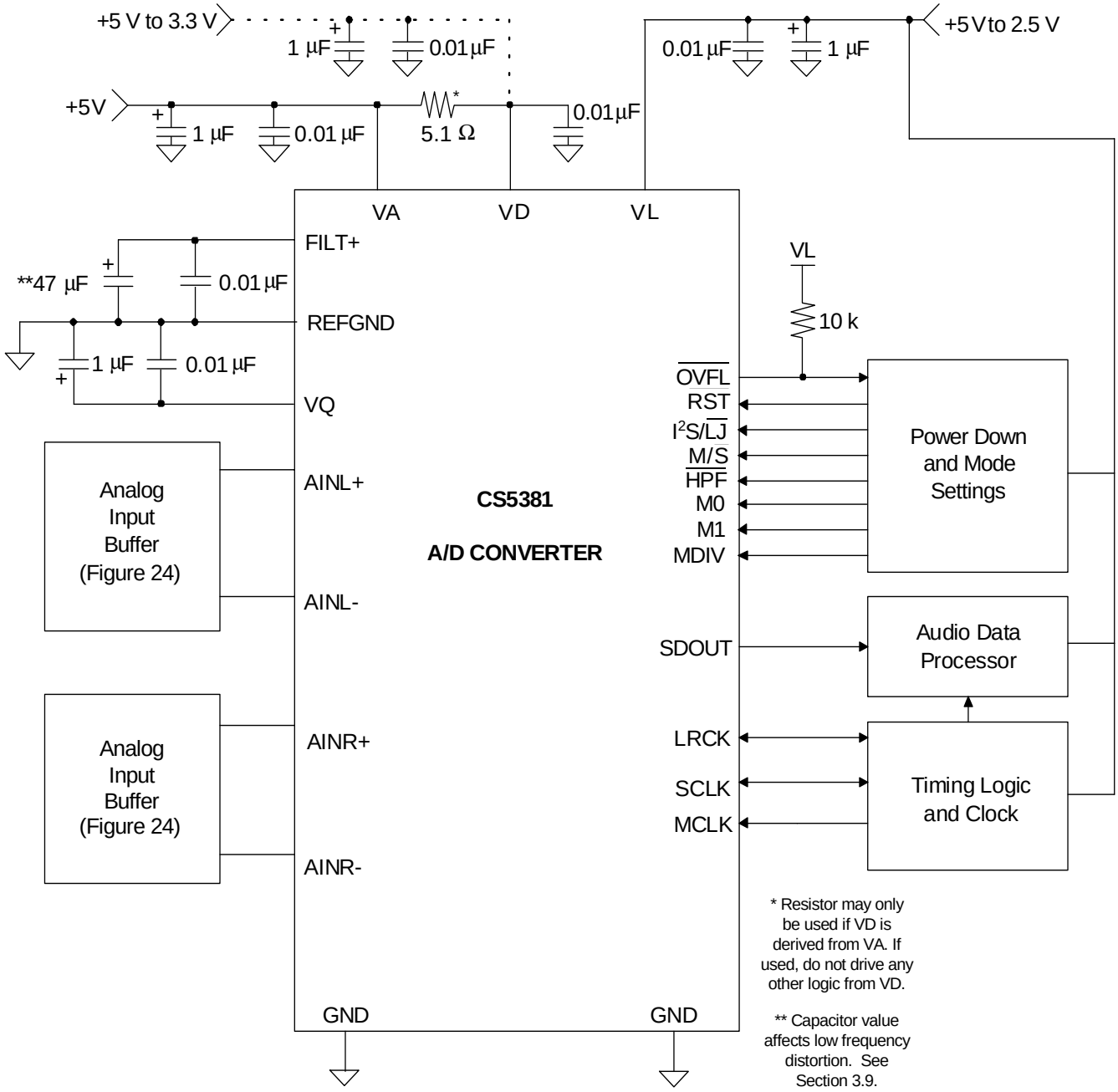


Figure 22. Typical Connection Diagram

3. APPLICATIONS

3.1 Operational Mode/Sample Rate Range Select

The output sample rate, Fs, can be adjusted from 2 kHz to 216 kHz. The CS5381 must be set to the proper speed mode via the mode pins, M1 and M0. Refer to Table 1.

M1 (Pin 14)	M0 (Pin 13)	MODE	Output Sample Rate (Fs)
0	0	Single-Speed Mode	2 kHz - 54 kHz
0	1	Double-Speed Mode	50 kHz - 108 kHz
1	0	Quad-Speed Mode	100 kHz - 216 kHz
1	1	Reserved	

Table 1. CS5381 Mode Control

3.2 System Clocking

The device supports operation in either Master Mode, where the left/right and serial clocks are synchronously generated on-chip, or Slave Mode, which requires external generation of the left/right and serial clocks. The device also includes a master clock divider in Master Mode where the master clock will be internally divided prior to any other internal circuitry when MDIV is enabled, set to logic 1. In Slave Mode, the MDIV pin needs to be disabled, set to logic 0.

3.2.1 Master Mode

In Master mode, LRCK and SCLK operate as outputs. The left/right and serial clocks are internally derived from the master clock with the left/right clock equal to Fs and the serial clock equal to 64x Fs, as shown in Figure 23. Refer to Table 2 for common master clock frequencies.

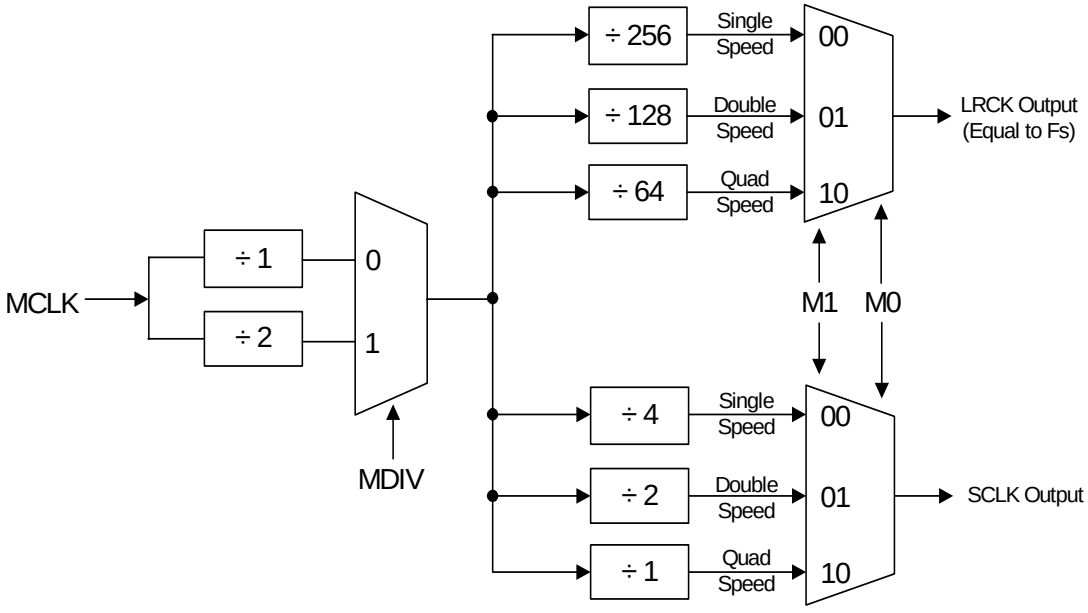


Figure 23. CS5381 Master Mode Clocking

SAMPLE RATE (kHz)	MDIV = 0 MCLK (MHz)	MDIV = 1 MCLK (MHz)
32	8.192	16.384
44.1	11.2896	22.5792
48	12.288	24.576
64	8.192	16.384
88.2	11.2896	22.5792
96	12.288	24.576
176.4	11.2896	22.5792
192	12.288	24.576

Table 2. CS5381 Common Master Clock Frequencies

3.2.2 Slave Mode

LRCK and SCLK operate as inputs in Slave mode. It is recommended that the left/right clock be synchronously derived from the master clock and must be equal to Fs. It is also recommended that the serial clock be synchronously derived from the master clock and be equal to 64x Fs to maximize system performance. Refer to Table 3 for required clock ratios.

	Single-Speed Mode Fs = 2 kHz to 54 kHz	Double-Speed Mode Fs = 50 kHz to 108 kHz	Quad-Speed Mode Fs = 100 kHz to 216 kHz
MCLK/LRCK Ratio	256x, 512x	128x, 256x	64x*, 128x
SCLK/LRCK Ratio	64x, 128x	64x	64x
* Only available in Master mode.			

Table 3. CS5381 Slave Mode Clock Ratios

3.3 Power-Up Sequence

Reliable power-up can be accomplished by keeping the device in reset until the power supplies, clocks and configuration pins are stable. It is also recommended that reset be enabled if the analog or digital supplies drop below the minimum specified operating voltages to prevent power glitch related issues.

The internal reference voltage must be stable for the device to produce valid data. Therefore, there is a delay between the release of reset and the generation of valid output, due to the finite output impedance of FILT+ and the presence of the external capacitance. This duration of this delay is less than 2500 LRCK cycles.

3.4 Analog Connections

The analog modulator samples the input at 6.144 MHz. The digital filter will reject signals within the stopband of the filter. However, there is no rejection for input signals which are (n × 6.144 MHz) the digital passband frequency, where n=0,1,2,... Refer to Figure 24, which shows the suggested filter that will attenuate any noise energy at 6.144 MHz in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) must be avoided since these can degrade signal linearity. C0G capacitors are recommended for this application.

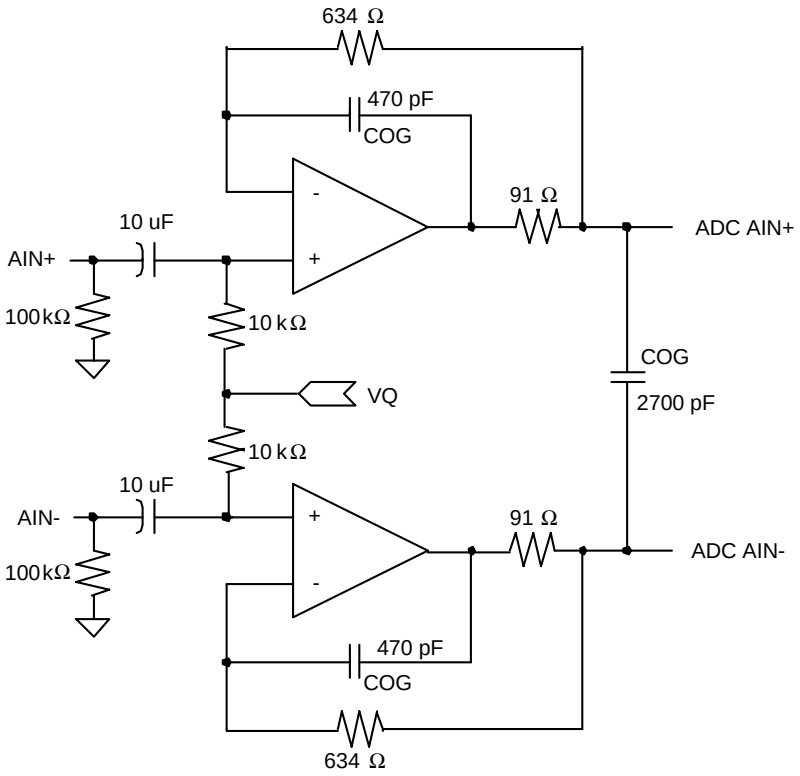


Figure 24. Recommended Analog Input Buffer

3.5 High-Pass Filter and DC Offset Calibration

The operational amplifiers in the input circuitry driving the CS5381 may generate a small DC offset into the A/D converter. The CS5381 includes a high-pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding “clicks” when switching between devices in a multi-channel system.

The high-pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. If the HPF pin is taken high during normal operation, the current value of the DC offset register is frozen and this DC offset will continue to be subtracted from the conversion result. This feature makes it possible to perform a system DC offset calibration by:

1. Running the CS5381 with the high-pass filter enabled until the filter settles. See the Digital Filter Characteristics for filter settling time.
2. Disabling the high-pass filter and freezing the stored DC offset.

A system calibration performed in this way will eliminate offsets anywhere in the signal path between the calibration point and the CS5381.

3.6 Overflow Detection

The CS5381 includes overflow detection on both the left and right channels. This time multiplexed information is presented as open drain, active low on pin 15, $\overline{\text{OVFL}}$. The OVFL_L and OVFL_R data will go to a logical low as soon as an overrange condition in the opposite channel is detected. The data will remain low as specified in the "Switching Characteristics - Serial Audio Port" section on page 10. This ensures sufficient time to detect an overrange condition regardless of the speed mode. After the timeout, the OVFL_L and OVFL_R data will return to a logical high if there has not been any other overrange condition detected. Please note that an overrange condition on either channel will restart the timeout period for both channels.

3.6.1 $\overline{\text{OVFL}}$ Configuration

If the system does not require overflow detection, the user may leave the $\overline{\text{OVFL}}$ pin disconnected. When using the overflow detection capability of the CS5381, a 10 kΩ pull-up resistor must be inserted between the $\overline{\text{OVFL}}$ pin and VL because the $\overline{\text{OVFL}}$ output is open drain, active low. This means that the $\overline{\text{OVFL}}$ pin is high impedance for the case of no overflow condition, but the pull-up resistor will pull the node to VL. When an overflow condition occurs, the $\overline{\text{OVFL}}$ pin can drive the node to GND thus indicating the presence of the overflow condition. In effect, the user can use the $\overline{\text{OVFL}}$ pin to illuminate an LED, or mute the channel with an external circuit or a DSP. Furthermore, because the $\overline{\text{OVFL}}$ output is open-drain, the $\overline{\text{OVFL}}$ pins of multiple CS5381 devices can be tied together such that an overflow condition on a single device will drive the line low. When connecting $\overline{\text{OVFL}}$ pins of multiple devices, only a single 10kΩ pull-up resistor is necessary.

3.6.2 $\overline{\text{OVFL}}$ Output Timing

In left-justified format, the $\overline{\text{OVFL}}$ pin is updated one SCLK period after an LRCK transition. In I²S format, the $\overline{\text{OVFL}}$ pin is updated two SCLK periods after an LRCK transition. Refer to Figures 20 and 21. In both cases, the $\overline{\text{OVFL}}$ data can be easily demultiplexed by using the LRCK to latch the data. In left-justified format, the rising edge of LRCK would latch the right channel overflow status, and the falling edge of LRCK would latch the left channel overflow status. In I²S format, the falling edge of LRCK would latch the right channel overflow status and the rising edge of LRCK would latch the left channel overflow status.

3.7 Grounding and Power Supply Decoupling

As with any high resolution converter, the CS5381 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 22 shows the recommended power arrangements, with VA and VL connected to clean supplies. VD, which powers the digital filter, may be run from the system logic supply or may be powered from the analog supply via a resistor. In this case, no additional devices should be powered from VD. Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest. All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The FILT+ and VQ decoupling capacitors, particularly the 0.01 µF, must be positioned to minimize the electrical path from FILT+ and REFGND. The CDB5381 evaluation board demonstrates the optimum layout and power supply arrangements. To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

3.8 Synchronization of Multiple Devices

In systems where multiple ADCs are required, care must be taken to achieve simultaneous sampling. To ensure synchronous sampling, the MCLK and LRCK must be the same for all of the CS5381's in the system. If only one master clock source is needed, one solution is to place one CS5381 in Master mode, and slave all of the other CS5381's to the one master. If multiple master clock sources are needed, a possible solution would be to supply all clocks from the same external source and time the CS5381 reset with the falling edge of MCLK. This will ensure that all converters begin sampling on the same clock edge.

3.9 Capacitor Size on the Reference Pin (FILT+)

The CS5381 requires an external capacitance on the internal reference voltage pin, FILT+. The size of this decoupling capacitor will affect the low frequency distortion performance as shown in Figure 25, with larger capacitor values used to optimize low frequency distortion performance. The THD+N curves in Figure 25 were measured with VA=VD=VL=5 V in Single-Speed Master Mode with a full-scale sinewave input.

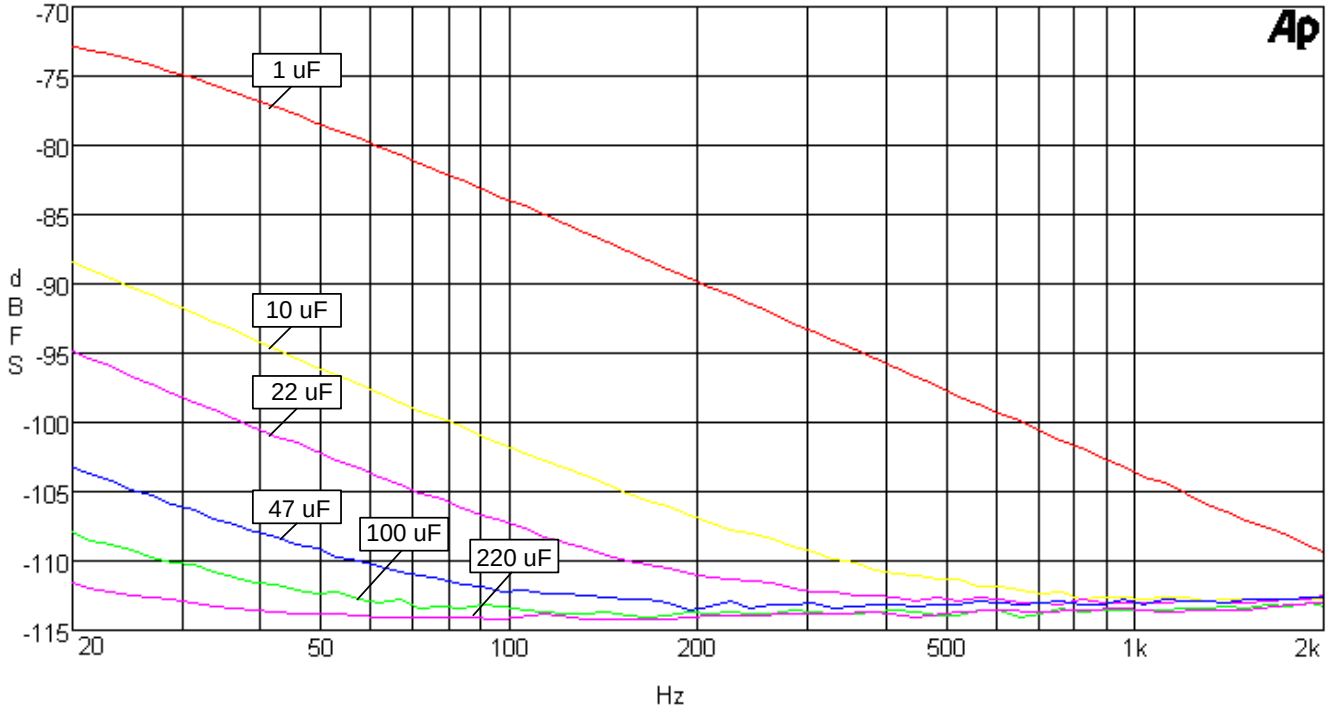
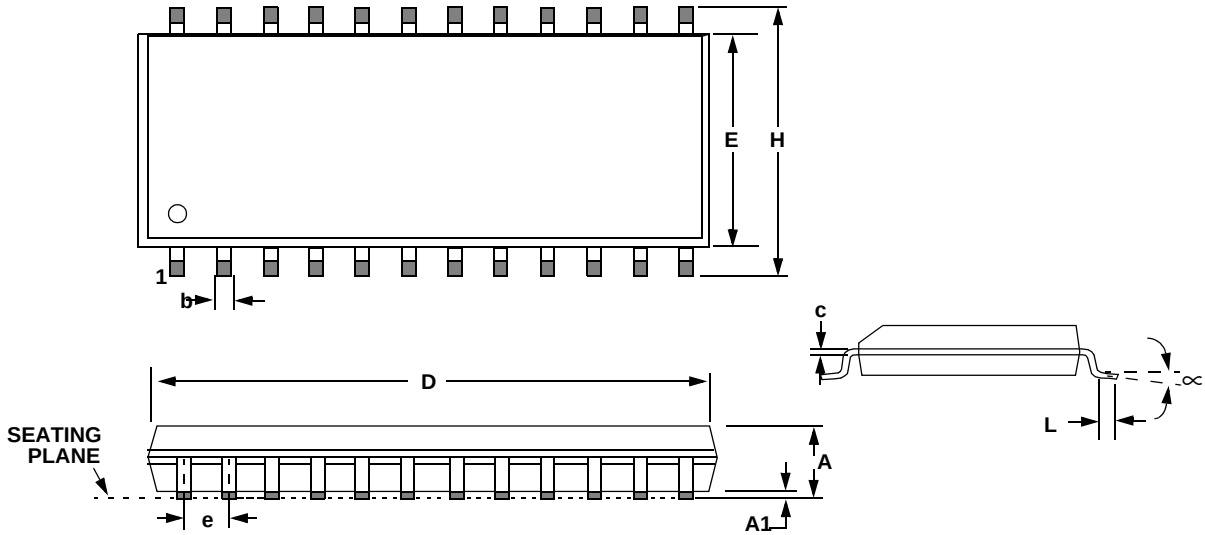


Figure 25. CS5381 THD + N versus Frequency

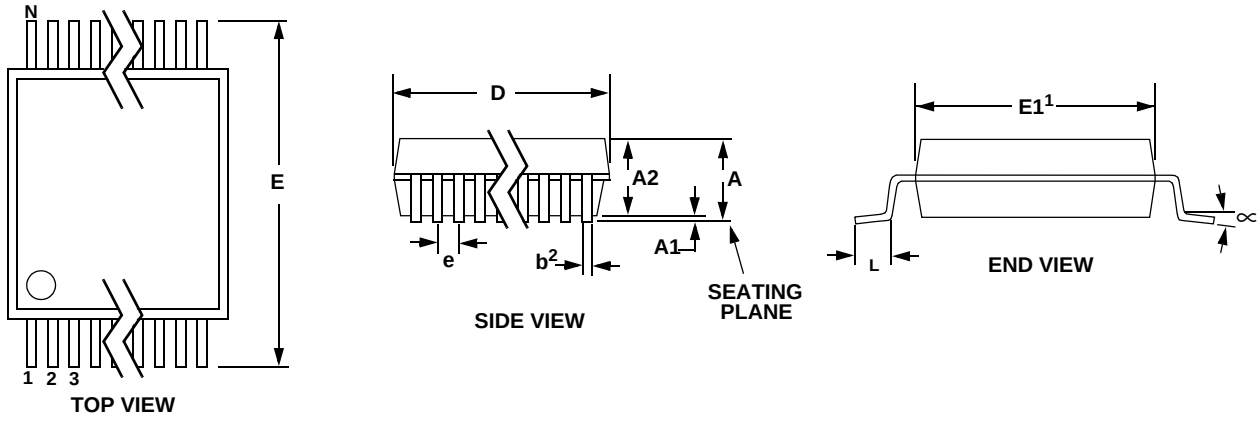
4. PACKAGE DIMENSIONS

24L SOIC (300 MIL BODY) PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.598	0.614	15.20	15.60
E	0.291	0.299	7.40	7.60
e	0.040	0.060	1.02	1.52
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
∝	0°	8°	0°	8°

24L TSSOP (4.4 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.043	--	--	1.10	
A1	0.002	0.004	0.006	0.05	--	0.15	
A2	0.03346	0.0354	0.037	0.85	0.90	0.95	
b	0.00748	0.0096	0.012	0.19	0.245	0.30	2,3
D	0.303	0.307	0.311	7.70	7.80	7.90	1
E	0.248	0.2519	0.256	6.30	6.40	6.50	
E1	0.169	0.1732	0.177	4.30	4.40	4.50	1
e	--	0.026 BSC	--	--	0.65 BSC	--	
L	0.020	0.024	0.028	0.50	0.60	0.70	
µ	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-153

Controlling Dimension is Millimeters.

Notes:

1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

5. ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS5381	120 dB, 192 kHz, Multi-Bit Audio A/D Converter	24-TSSOP	Yes	Commercial	-10° to +70° C	Bulk	CS5381-KZZ
						Tape & Reel	CS5381-KZZR
CS5381	120 dB, 192 kHz, Multi-Bit Audio A/D Converter	24-SOIC	Yes	Commercial	-10° to +70° C	Bulk	CS5381-KSZ
						Tape & Reel	CS5381-KSZR
CDB5381	CS5381 Evaluation Board	-	-	-	-	-	CDB5381

6 PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog input for a full-scale digital output.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

7. REVISION HISTORY

Release	Date	Changes
A1	December 2002	Initial Release
A2	October 2003	Changed front page description of digital filter Improved distortion specification from -105 dB to -110 dB Modified serial port timing specifications for slave mode operation Added pull-down resistors to recommended input buffer
A3	May 2004	Changed full-scale voltage specification to reflect VA supply voltage Added Applications section about capacitor value on FILT+ pin Changed input impedance specification from 37 to 2.5 kΩ Changed impedance specification on FILT+ from 35 to 4.5 kΩ
A4	August 2004	Add Lead free part number
F1	July 2005	Replaced diagrams showing $\overline{\text{OVFL}}$ functionality (see Figures 20 and 21) Replaced Figures 13, 15, 18 and 19 to demonstrate pre-emption of the MSB. Increased maximum digital current (I_D) specification at 5 V from 43 mA to 46 mA. .
F2	July 2005	Updated Ordering Information.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find the one nearest to you go to **www.cirrus.com**

IMPORTANT NOTICE

Cirrus Logic, Inc. and its subsidiaries ("Cirrus") believe that the information contained in this document is accurate and reliable. However, the information is subject to change without notice and is provided "AS IS" without warranty of any kind (express or implied). Customers are advised to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, indemnification, and limitation of liability. No responsibility is assumed by Cirrus for the use of this information, including use of this information as the basis for manufacture or sale of any items, or for infringement of patents or other rights of third parties. This document is the property of Cirrus and by furnishing this information, Cirrus grants no license, express or implied under any patents, mask work rights, copyrights, trademarks, trade secrets or other intellectual property rights. Cirrus owns the copyrights associated with the information contained herein and gives consent for copies to be made of the information only for use within your organization with respect to Cirrus integrated circuits or other products of Cirrus. This consent does not extend to other copying such as copying for general distribution, advertising or promotional purposes, or for creating any work for resale.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). CIRRUS PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED FOR USE IN AIRCRAFT SYSTEMS, MILITARY APPLICATIONS, PRODUCTS SURGICALLY IMPLANTED INTO THE BODY, AUTOMOTIVE SAFETY OR SECURITY DEVICES, LIFE SUPPORT PRODUCTS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF CIRRUS PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK AND CIRRUS DISCLAIMS AND MAKES NO WARRANTY, EXPRESS, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR PARTICULAR PURPOSE, WITH REGARD TO ANY CIRRUS PRODUCT THAT IS USED IN SUCH A MANNER. IF THE CUSTOMER OR CUSTOMER'S CUSTOMER USES OR PERMITS THE USE OF CIRRUS PRODUCTS IN CRITICAL APPLICATIONS, CUSTOMER AGREES, BY SUCH USE, TO FULLY INDEMNIFY CIRRUS, ITS OFFICERS, DIRECTORS, EMPLOYEES, DISTRIBUTORS AND OTHER AGENTS FROM ANY AND ALL LIABILITY, INCLUDING ATTORNEYS' FEES AND COSTS, THAT MAY RESULT FROM OR ARISE IN CONNECTION WITH THESE USES.

Cirrus Logic, Cirrus, and the Cirrus Logic logo designs are trademarks of Cirrus Logic, Inc. All other brand and product names in this document may be trademarks or service marks of their respective owners.