Data sheet acquired from Cypress Semiconductor Corporation.
Data sheet modified to remove devices not offered.

CY74FCT16543T
CY74FCT162543T
CY74FCT162H543T

SCCS059B - August 1994 - Revised September 2001

16-Bit Latched Transceivers

Features

- **I_{off} supports partial-power-down mode operation**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Industrial temperature range of −40˚C to +85˚C**
- **V_{CC} = 5V ± 10%**

CY74FCT16543T Features:

- **64 mA sink current, 32 mA source current**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25˚C**

CY74FCT162543T Features:

- **Balanced 24 mA output drivers**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A= 25˚C**

CY74FCT162H543T Features:

- **Bus hold retains last active state**
- **Eliminates the need for external pull-up or pull-down resistors**

Functional Description

The CY74FCT16543T and CY74FCT162543T are 16-bit, high-speed, low power latched transceivers that are organized as two independent 8-bit D-type latched transceivers containing two sets of eight D-type latches with separate Latch Enable ($\overline{LEAB}$, $\overline{LEAB}$) and Output Enable ($\overline{OEAB}$, $\overline{OEAB}$) controls for each set to permit independent control of inputting and outputting in either direction of data flow. For data flow from A to B, for example, the A-to-B input Enable ($\overline{CEAB}$) must be LOW in order to enter data from A or to take data from B as indicated in the truth table. With $\overline{CAEB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the three-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses $\overline{CEAB}$, $\overline{LEAB}$, and $\overline{OEAB}$ inputs flow-through pinout and small shrink packaging and in simplifying board design.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

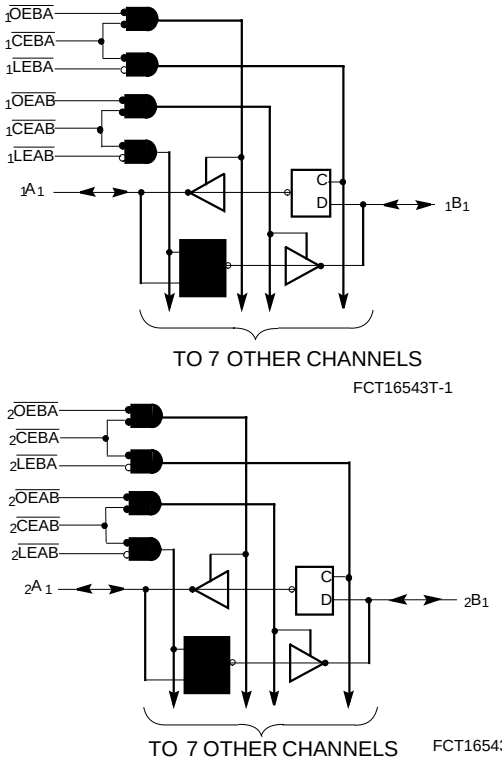
The CY74FCT16543T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162543T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162543T is ideal for driving transmission lines.

The CY74FCT162H543T is a 24-mA balanced output part that has “bus hold” on the data inputs. The device retains the input’s last state whenever the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.

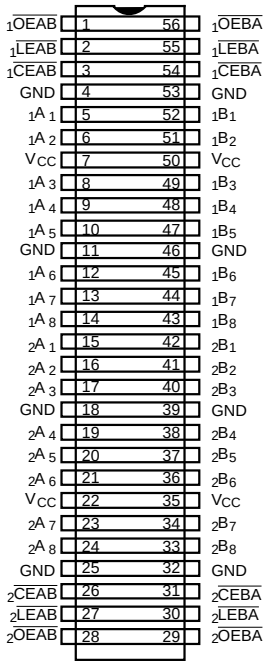
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Logic Block Diagrams



Pin Configuration

Top View
SSOP/TSSOP



FCT16543T-3

Pin Description

Name	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A	A-to-B Data Inputs or B-to-A Three-State Outputs[9]
B	B-to-A Data Inputs or A-to-B Three-State Outputs[9]

Function Table[1]

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A to B	B
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs[2]

Maximum Ratings[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....Com'l –55°C to +125°C

Ambient Temperature with Power Applied .....Com'l –55°C to +125°C

DC Input Voltage .....–0.5V to +7.0V

DC Output Voltage .....–0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .....–60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage.....>2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
V_H	Input Hysteresis[6]			100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=–18 mA		–0.7	–1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_I=V_{CC}			±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_I=GND			±1	µA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=2.7V			±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=0.5V			±1	µA
I_{OS}	Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=GND	–80	–140	–200	mA
I_O	Output Drive Current[7]	V_{CC}=Max., V_{OUT}=2.5V	–50		–180	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}≤4.5V[8]			±1	µA

Notes:

1. A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, LEBA, and $\overline{OEBA}$.
2. Data prior to LEAB LOW-to-HIGH Transition
   H = HIGH Voltage Level. L = LOW Voltage Level.
   X = Don't Care. Z = High Impedance.
3. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
4. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
5. Typical values are at V_{CC}= 5.0V, T_A= +25˚C ambient.
6. This parameter is specified but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
8. Tested at +25˚C.
9. On the 74FCT162H543T, these pins have bus hold.

Output Drive Characteristics for CY74FCT16543T

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=–3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=–15 mA	2.4	3.5		
		V_{CC}=Min., I_{OH}=–32 mA	2.0	3.0		
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162543T, CY74FCT162H543T

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit
I_{ODL}	Output LOW Current[7]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Current[7]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=–24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Capacitance[6] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions		Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	V_{IN}≤0.2V, V_{IN}≥V_{CC}–0.2V	5	500	µA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max.	V_{IN}=3.4V[10]	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[11]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND	V_{IN}=V_{CC} or V_{IN}=GND	60	100	µA/MHz
I_C	Total Power Supply Current[12]	V_{CC}=Max., f_1=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE}$=GND	V_{IN}=V_{CC} or V_{IN}=GND	0.6	1.5	mA
			V_{IN}=3.4V or V_{IN}=GND	0.9	2.3	mA
		V_{CC}=Max., f_1=2.5 MHz, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $\overline{OE}$=GND	V_{IN}=V_{CC} or V_{IN}=GND	2.4	4.5[13]	mA
			V_{IN}=3.4V or V_{IN}=GND	6.4	16.5[13]	mA

Notes:

10. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
    I_C = I_{CC}+$\Delta I_{CC} D_H N_T$+$I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
13. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range[14]

Parameter	Description	CY74FCT16543T CY74FCT162543T		CY74FCT16543AT CY74FCT162543AT		Unit	Fig. No.[15]
		Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A to B or B to A	1.5	8.5	1.5	6.5	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to A, $\overline{LEAB}$ to B	1.5	12.5	1.5	8.0	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A or B $\overline{CEBA}$ or $\overline{CEAB}$ to A or B	1.5	12.0	1.5	9.0	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A or B $\overline{CEBA}$ or $\overline{CEAB}$ to A or B	1.5	9.0	1.5	7.5	ns	1, 7, 8
t_{SU}	Set-up Time HIGH or LOW A or B to $\overline{LEAB}$ or $\overline{LEBA}$	2.0	—	2.0	—	ns	4
t_H	Hold Time HIGH or LOW A or B to $\overline{LEAB}$ or $\overline{LEBA}$	2.0	—	2.0	—	ns	4
t_W	$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW	4.0	—	4.0	—	ns	5
$t_{SK(O)}$	Output Skew[16]	—	0.5	—	0.5	ns	—

Parameter	Description	CY74FCT16543CT CY74FCT162543CT CY74FCT162H543CT		Unit	Fig. No.[15]
		Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A to B or B to A	1.5	5.1	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to A, $\overline{LEAB}$ to B	1.5	5.6	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A or B $\overline{CEBA}$ or $\overline{CEAB}$ to A or B	1.5	7.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A or B $\overline{CEBA}$ or $\overline{CEAB}$ to A or B	1.5	6.5	ns	1, 7, 8
t_{SU}	Set-up Time HIGH or LOW A or B to $\overline{LEAB}$ or $\overline{LEBA}$	2.0	—	ns	4
t_H	Hold Time HIGH or LOW A or B to $\overline{LEAB}$ or $\overline{LEBA}$	2.0	—	ns	4
t_W	$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW	4.0	—	ns	5
$t_{SK(O)}$	Output Skew[16]	—	0.5	ns	—

Notes:
14. Minimum limits are specified but not tested on Propagation Delays.
15. See “Parameter Measurement Information” in the General Information section.
16. Skew between any two outputs of the same package switching in the same directional. This parameter is ensured by design.

Ordering Information CY74FCT16543

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.1	CY74FCT16543CTPVC/PVCT	O56	56-Lead (300-Mil) SSOP	Industrial
6.5	CY74FCT16543ATPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
8.5	CY74FCT16543TPVC/PVCT	O56	56-Lead (300-Mil) SSOP	Industrial

Ordering Information CY74FCT162543

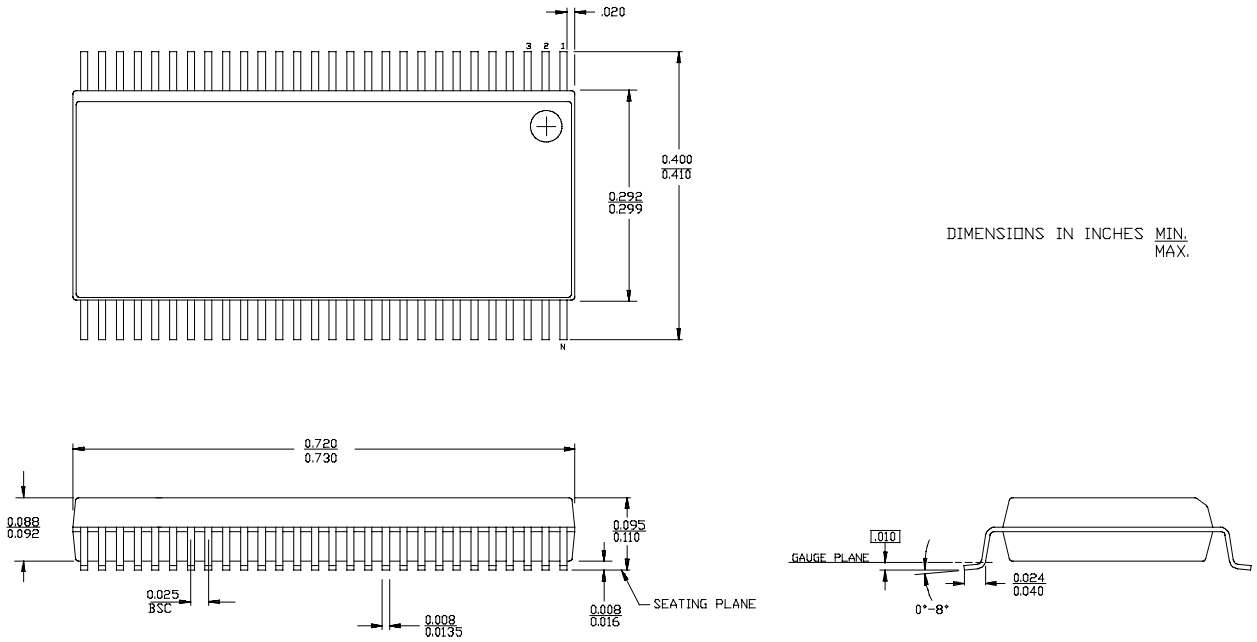
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.1	74FCT162543CTPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162543CTPVC	O56	56-Lead (300-Mil) SSOP	
	74FCT162543CTPVCT	O56	56-Lead (300-Mil) SSOP	
6.5	74FCT162543ATPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
8.5	CY74FCT162543TPVC/PVCT	O56	56-Lead (300-Mil) SSOP	Industrial

Ordering Information CY74FCT162H543T

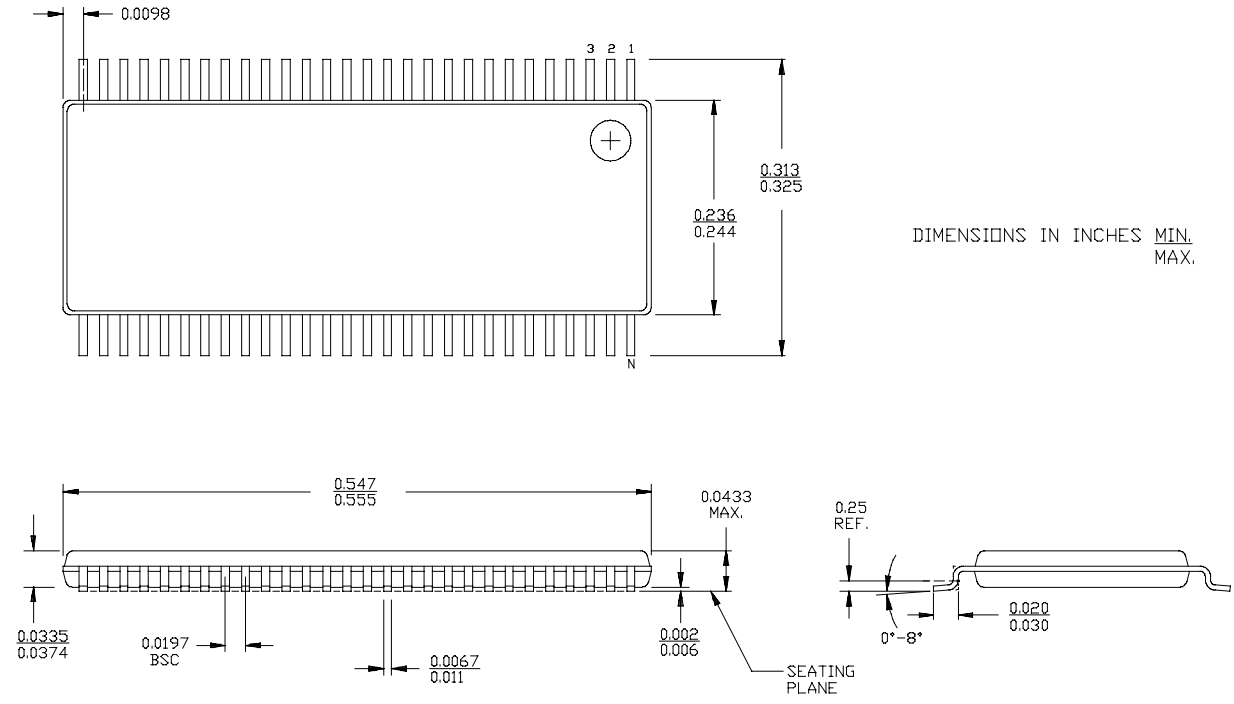
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.1	74FCT162H543CTPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial

Package Diagrams

56-Lead Shrunk Small Outline Package O56



56-Lead Thin Shrunk Small Outline Package Z56



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
74FCT162543ATPACT	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162543CTPACT	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162543CTPVCG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162543CTPVCT	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162543ETPACT	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI
74FCT162543ETPVCT	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
74FCT162543TPVCG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162543TPVCTG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162H543CTPACT	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT16543ATPACTE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT16543ATPACTG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT16543CTPVCG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT16543CTPVCTG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT16543TPVCG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT16543TPVCTG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT162543CTPVC	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT162543ETPAC	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI
CY74FCT162543ETPVC	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
CY74FCT162543TPVC	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT162543TPVCT	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT16543ATPACT	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT16543CTPVC	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT16543CTPVCT	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT16543ETPAC	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI
CY74FCT16543ETPACT	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI
CY74FCT16543ETPVC	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
CY74FCT16543ETPVCT	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
CY74FCT16543TPVC	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
CY74FCT16543TPVCT	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
FCT162543ATPACTE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
FCT162543ATPACTG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
FCT162543CTPACTE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
FCT162543CTPACTG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
FCT162543CTPVCTG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
FCT162H543CTPACTE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
FCT162H543CTPACTG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

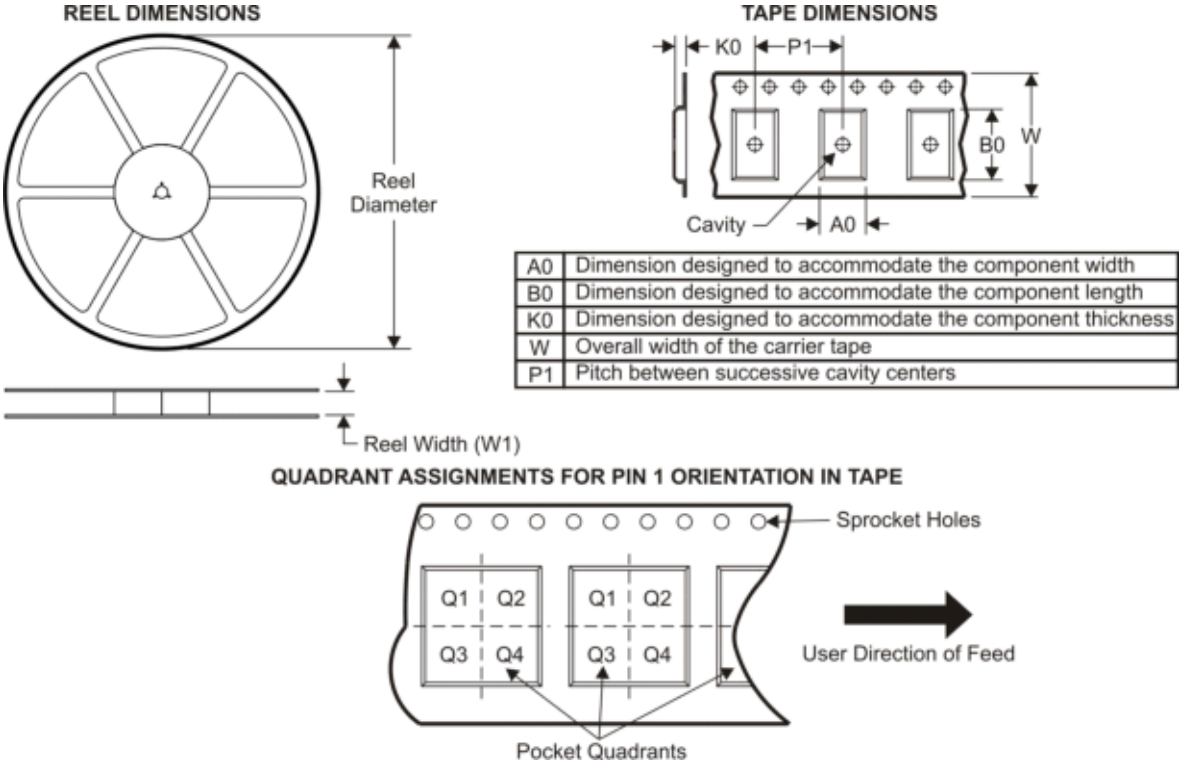
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

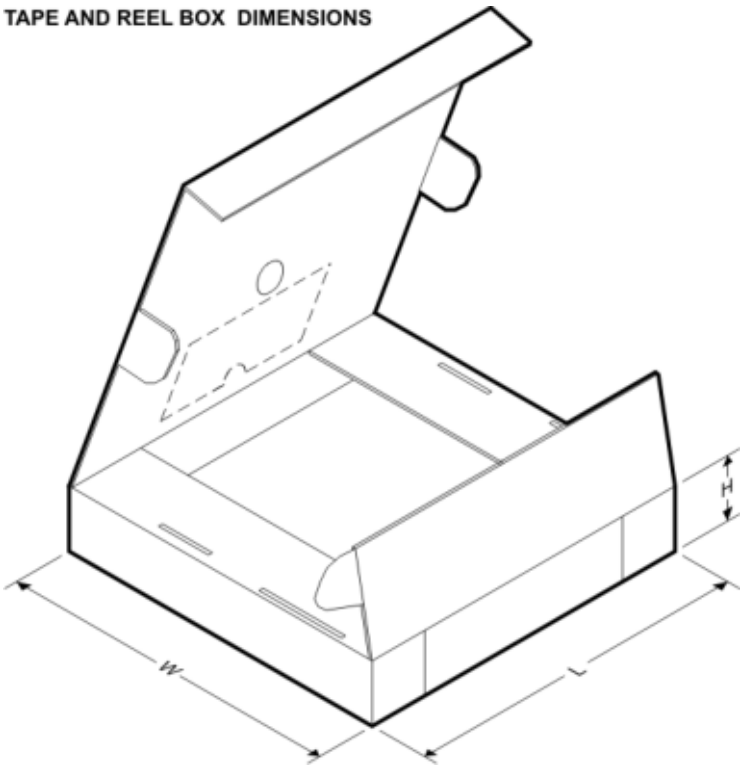


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74FCT162543ATPACT	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
74FCT162543CTPACT	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
74FCT162543CTPVCT	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
74FCT162H543CTPACT	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
CY74FCT162543TPVCT	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
CY74FCT16543ATPACT	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
CY74FCT16543CTPVCT	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
CY74FCT16543TPVCT	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



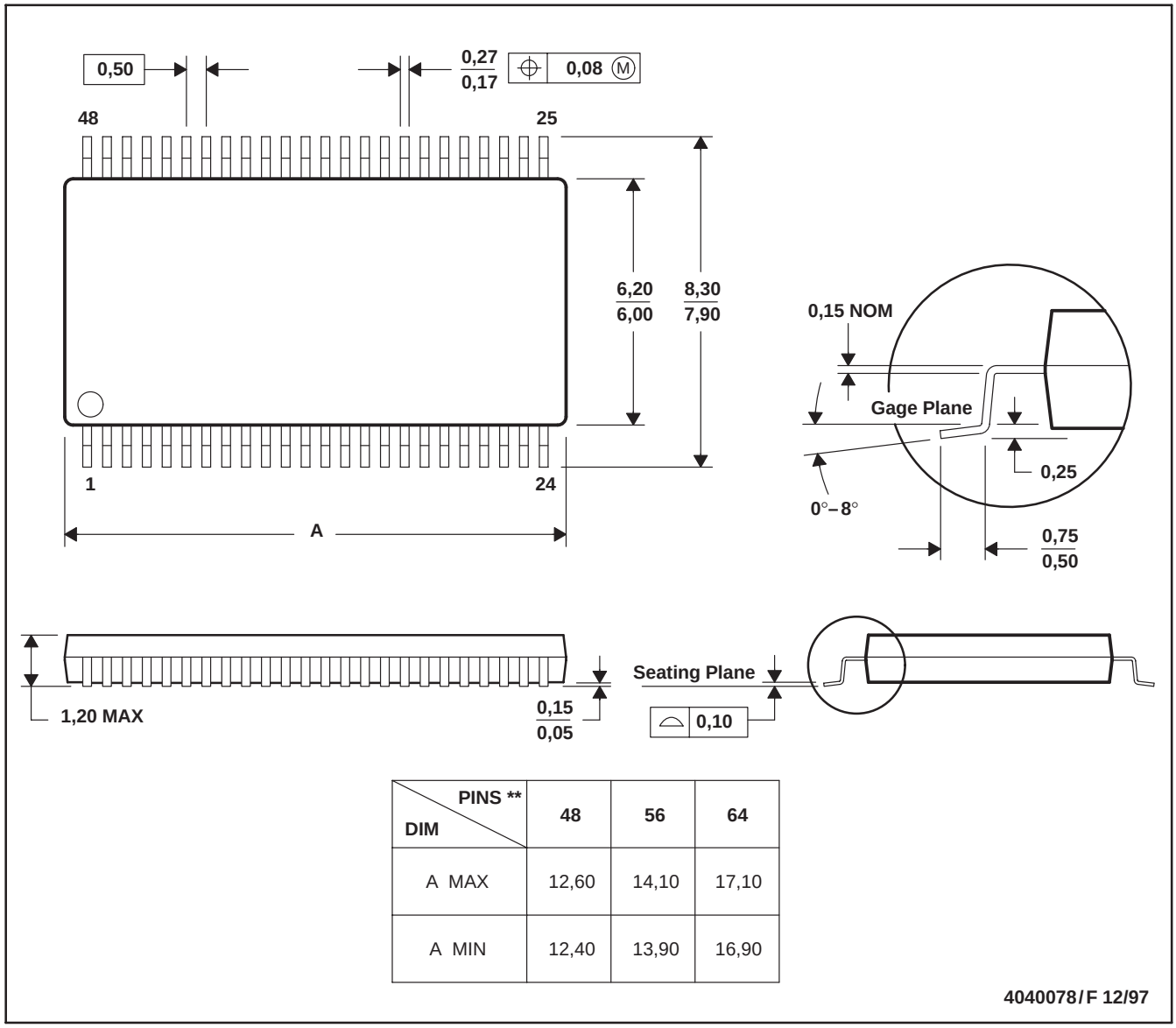
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74FCT162543ATPACT	TSSOP	DGG	56	2000	346.0	346.0	41.0
74FCT162543CTPACT	TSSOP	DGG	56	2000	346.0	346.0	41.0
74FCT162543CTPVCT	SSOP	DL	56	1000	346.0	346.0	49.0
74FCT162H543CTPACT	TSSOP	DGG	56	2000	346.0	346.0	41.0
CY74FCT162543TPVCT	SSOP	DL	56	1000	346.0	346.0	49.0
CY74FCT16543ATPACT	TSSOP	DGG	56	2000	346.0	346.0	41.0
CY74FCT16543CTPVCT	SSOP	DL	56	1000	346.0	346.0	49.0
CY74FCT16543TPVCT	SSOP	DL	56	1000	346.0	346.0	49.0

MTSS003D – JANUARY 1995 – REVISED JANUARY 1998

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



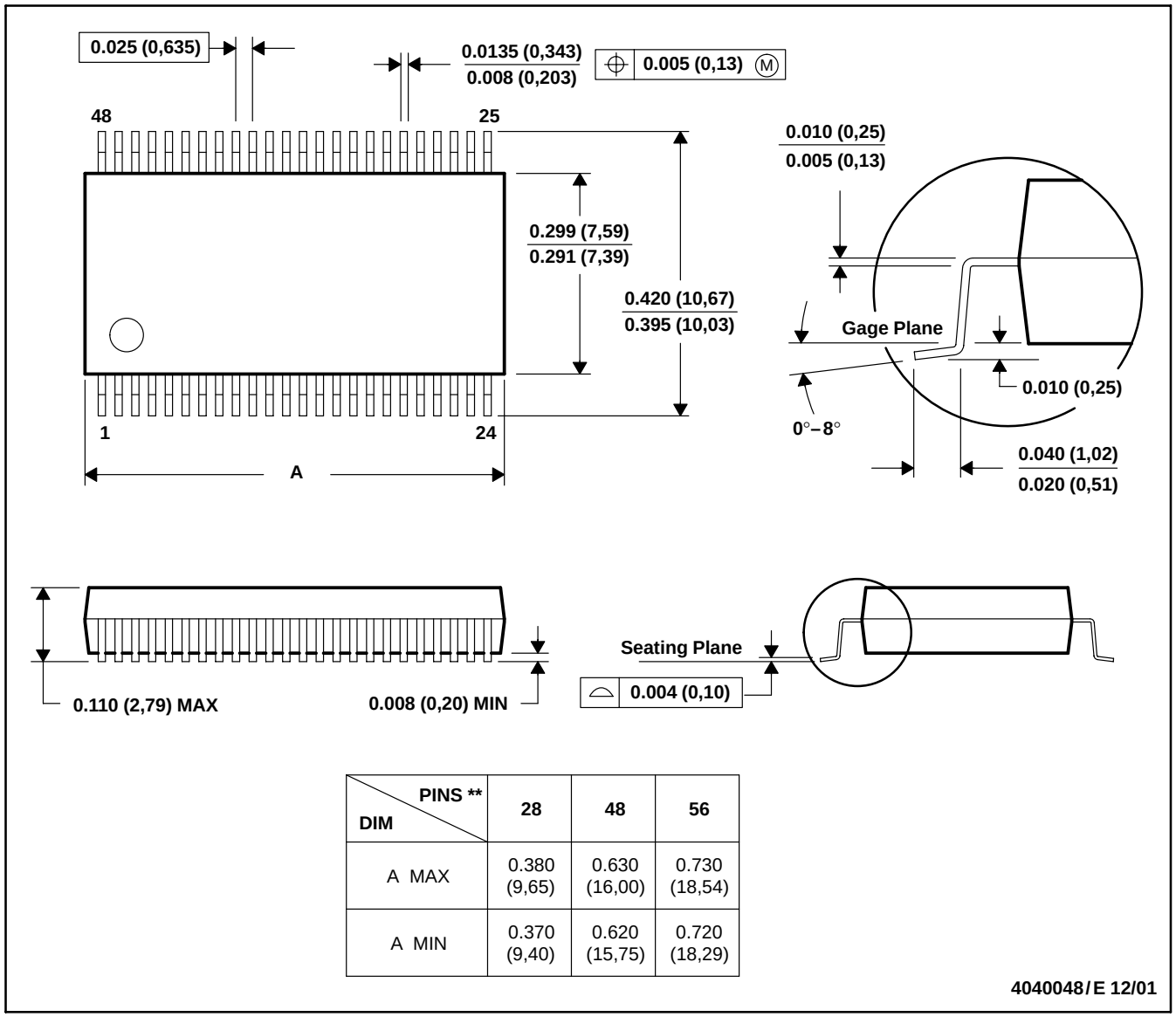
DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



DIM \ PINS **	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048/E 12/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74FCT162543ATPACT	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162543A	Samples
74FCT162543CTPACT	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162543C	Samples
74FCT162543CTPVCG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162543C	Samples
74FCT162543ETPACT	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI	-40 to 85		
74FCT162543ETPVCT	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85		
74FCT162543TPVCTG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162543	Samples
74FCT16543ATPACTG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16543A	Samples
74FCT16543TPVCTG4	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85		
CY74FCT162543CTPVC	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162543C	Samples
CY74FCT162543ETPAC	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI	-40 to 85		
CY74FCT162543ETPVC	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85		
CY74FCT162543TPVC	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162543	Samples
CY74FCT162543TPVCT	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162543	Samples
CY74FCT16543ATPACT	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16543A	Samples
CY74FCT16543CTPVC	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16543C	Samples
CY74FCT16543CTPVCT	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16543C	Samples
CY74FCT16543ETPAC	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI	-40 to 85		
CY74FCT16543ETPACT	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI	-40 to 85		
CY74FCT16543ETPVC	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85		
CY74FCT16543ETPVCT	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85		
CY74FCT16543TPVC	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16543	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CY74FCT16543TPVCT	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

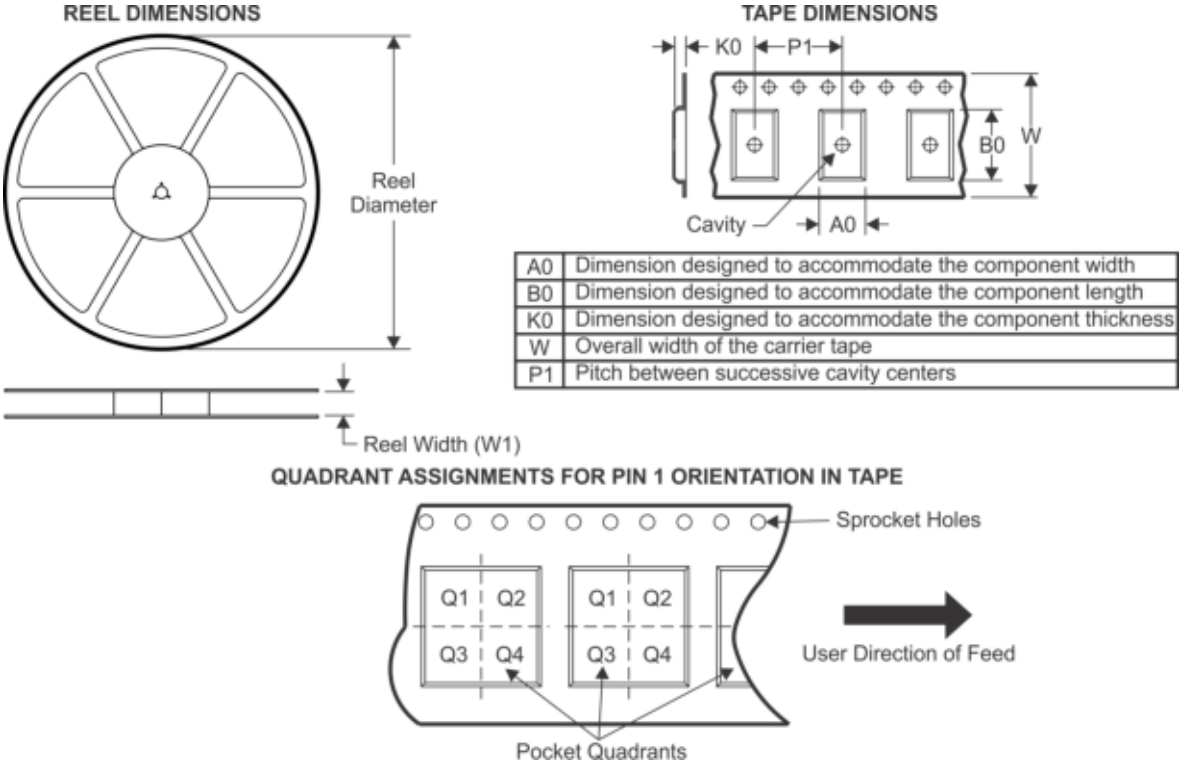
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

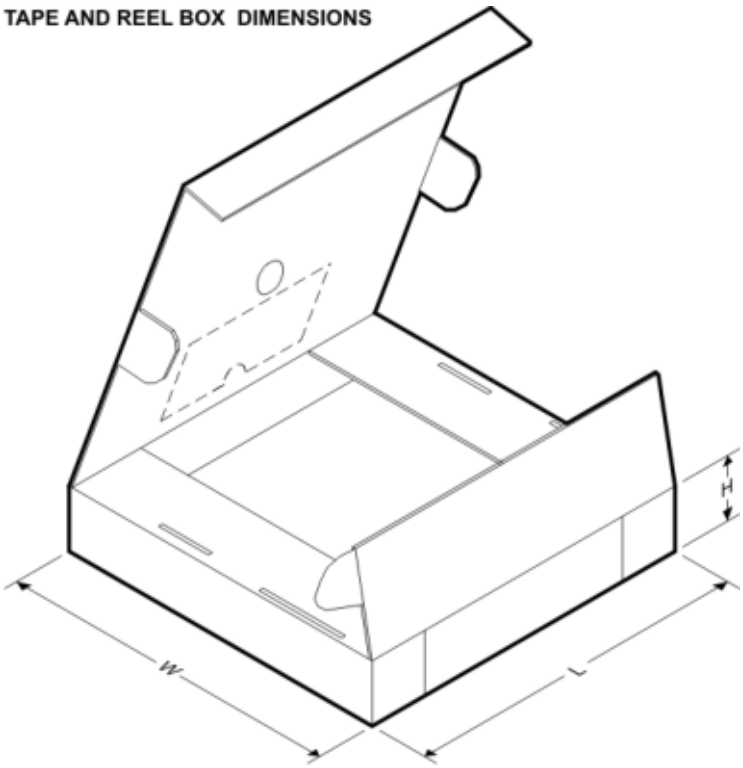


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74FCT162543ATPACT	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
74FCT162543CTPACT	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
CY74FCT162543TPVCT	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
CY74FCT16543ATPACT	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
CY74FCT16543CTPVCT	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

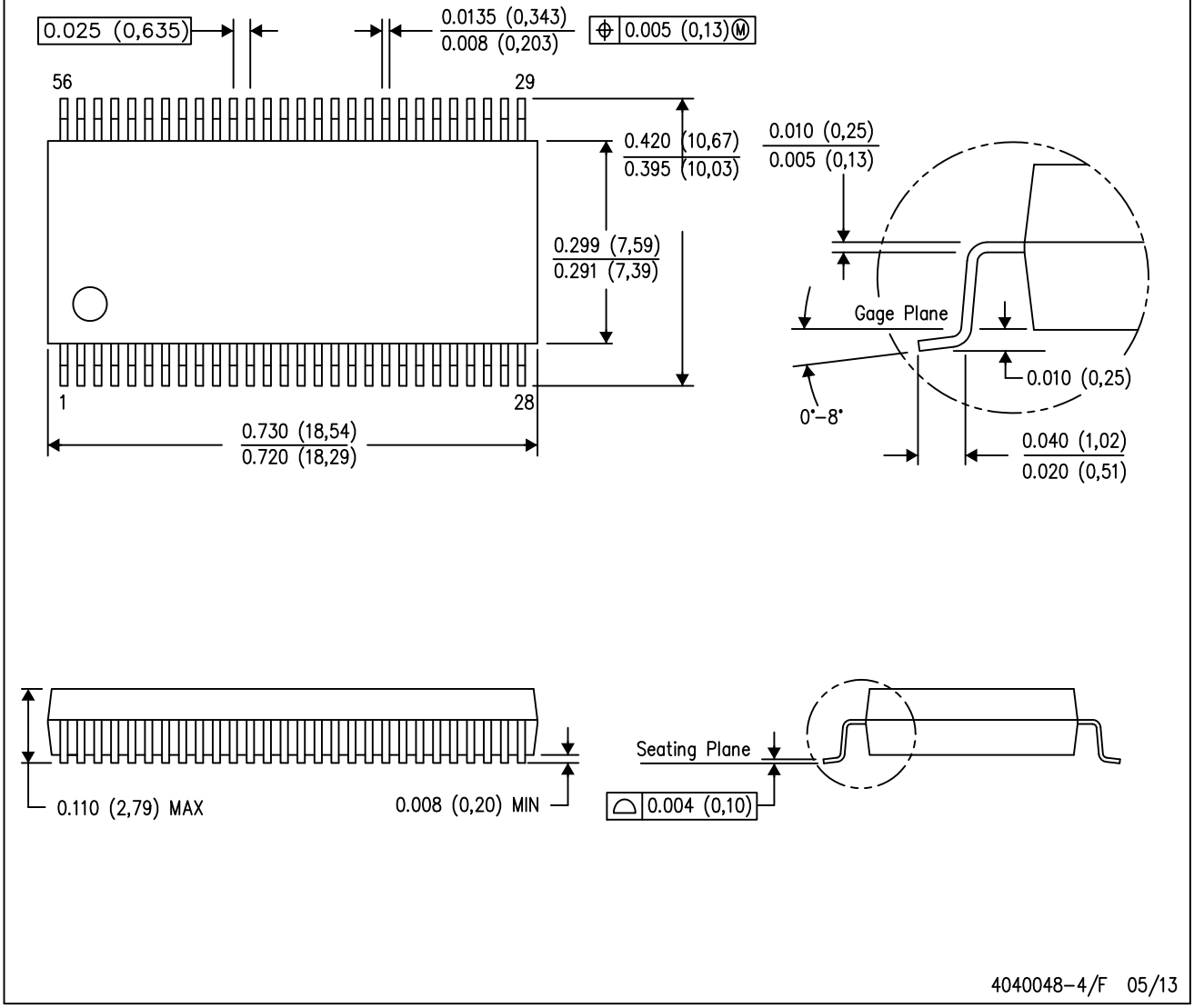
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74FCT162543ATPACT	TSSOP	DGG	56	2000	367.0	367.0	45.0
74FCT162543CTPACT	TSSOP	DGG	56	2000	367.0	367.0	45.0
CY74FCT162543TPVCT	SSOP	DL	56	1000	367.0	367.0	55.0
CY74FCT16543ATPACT	TSSOP	DGG	56	2000	367.0	367.0	45.0
CY74FCT16543CTPVCT	SSOP	DL	56	1000	367.0	367.0	55.0

DL (R–PDSO–G56) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

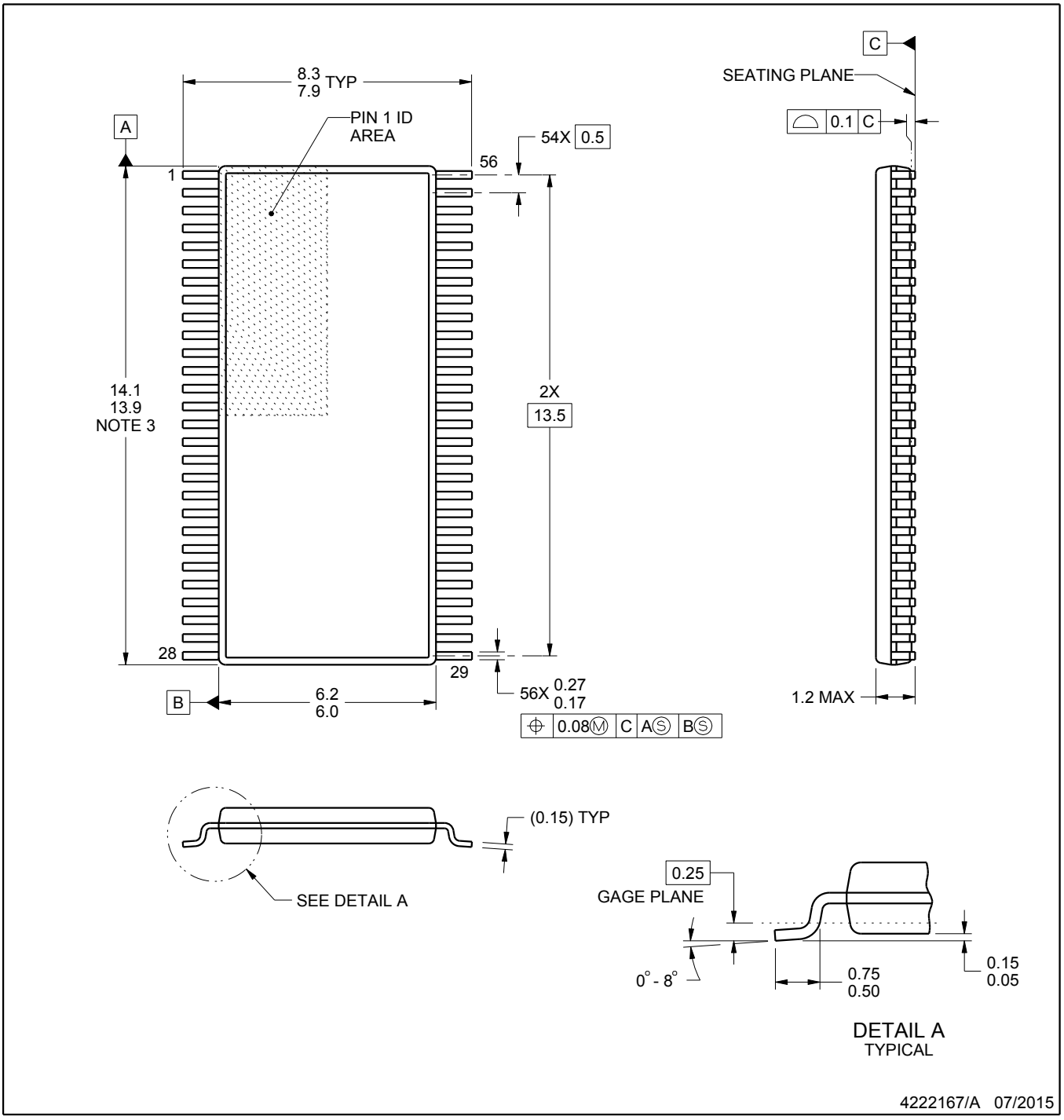
PowerPAD is a trademark of Texas Instruments.

PACKAGE OUTLINE

DGG0056A

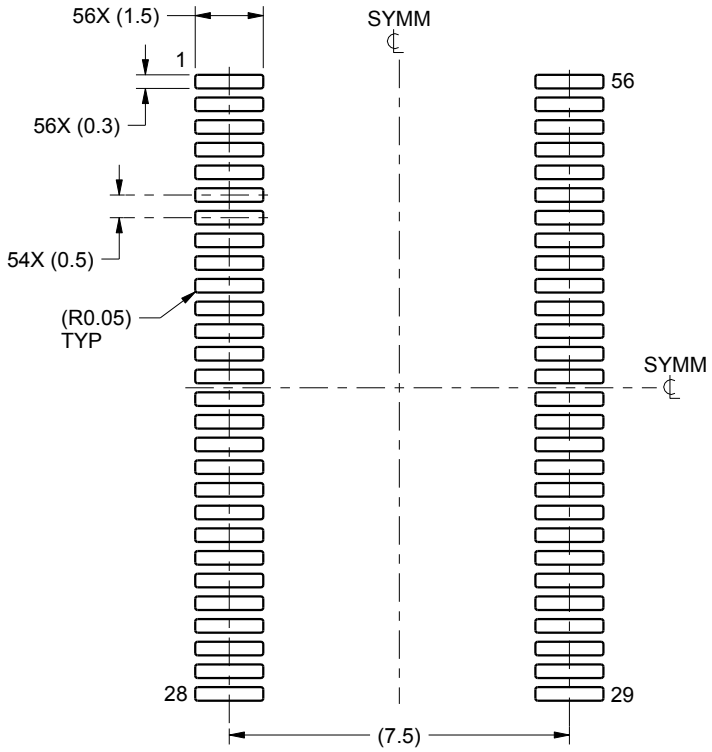
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

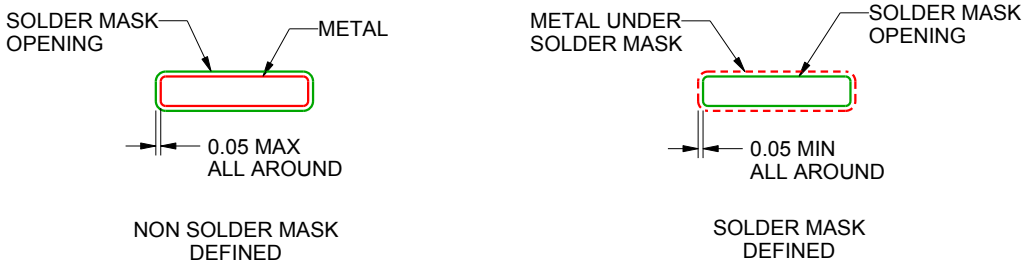


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

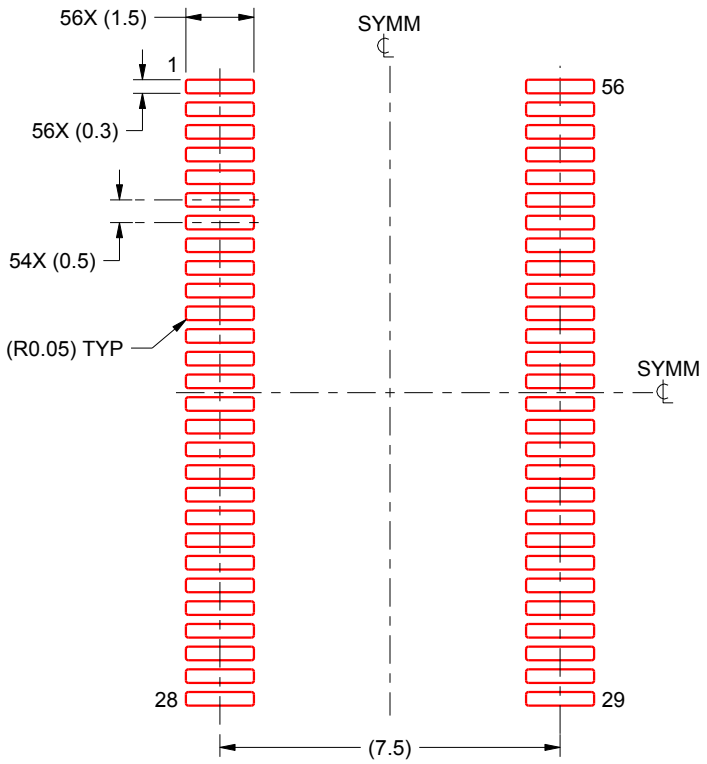


SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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