Data sheet acquired from Cypress Semiconductor Corporation.
Data sheet modified to remove devices not offered.

CY74FCT16823T
CY74FCT162823T

18-Bit Registers

SCCS062B - August 1994 - Revised September 2001

Features

- **I_{off} supports partial-power-down mode operation**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Industrial temperature range of −40˚C to +85˚C**
- **V_{CC} = 5V ± 10%**

CY74FCT16823T Features:

- **64 mA sink current, 32 mA source current**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25˚C**

CY74FCT162823T Features:

- **Balanced 24 mA output drivers**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, TA = 25˚C**

Functional Description

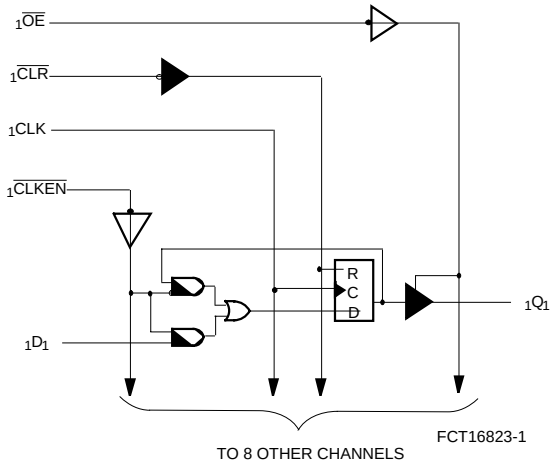
The CY74FCT16823T and the CY74FCT162823T 18-bit bus interface registers are designed for use in high-speed, low-power systems needing wide registers and parity. 18-bit operation is achieved by connecting the control lines of the two 9-bit registers. Flow-through pinout and small shrink packaging aids in simplifying board layout.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

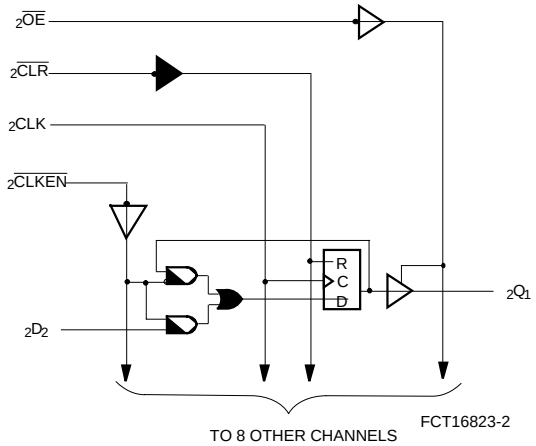
The CY74FCT16823T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162823T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162823T is ideal for driving transmission lines.

Logic Block Diagrams



FCT16823-1

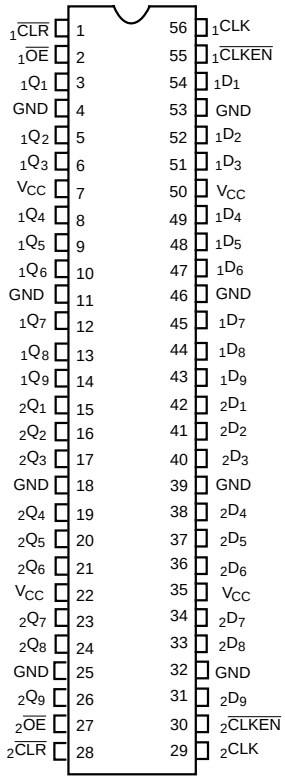


FCT16823-2

Pin Configuration

SSOP/TSSOP

Top View



FCT16823-3

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Pin Description

Name	Description
D	Data Inputs
CLK	Clock Inputs
$\overline{CLKEN}$	Clock Enable Inputs (Active LOW)
$\overline{CLR}$	Asynchronous Clear Inputs (Active LOW)
$\overline{OE}$	Output Enable Inputs (Active LOW)
Q	Three-State Outputs

Function Table[1]

Inputs						Outputs
$\overline{OE}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q	Function
H	X	X	X	X	Z	High Z
L	L	X	X	X	L	Clear
L	H	H	X	X	Q[2]	Hold
H	H	L	⌐	L	Z	Load
H	H	L	⌐	H	Z	
L	H	L	⌐	L	L	
L	H	L	⌐	H	H	

Maximum Ratings[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–55°C to +125°C

Ambient Temperature with Power Applied.....–55°C to +125°C

DC Input Voltage .....–0.5V to +7.0V

DC Output Voltage .....–0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .....–60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage.....>2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40°C to +85°C	5V ± 10%

Notes:

1. H = HIGH Voltage Level.
   L = LOW Voltage Level.
   X = Don't Care.
   Z = HIGH Impedance.
   ⌐=LOW-to-HIGH transition.
2. Output level before indicated steady-state input conditions were established.
3. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
4. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
V_H	Input Hysteresis[6]			100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=–18 mA		–0.7	–1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_I=V_{CC}			±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_I=GND			±1	µA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=2.7V			±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=0.5V			±1	µA
I_{OS}	Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=GND	–80	–140	–200	mA
I_O	Output Drive Current[7]	V_{CC}=Max., V_{OUT}=2.5V	–50		–180	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}≤4.5V[8]			1	µA

Output Drive Characteristics for CY74FCT16823T

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=–3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=–15 mA	2.4	3.5		
		V_{CC}=Min., I_{OH}=–32 mA	2.0	3.0		
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162823T

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit
I_{ODL}	Output LOW Voltage[7]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Voltage[7]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=–24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Capacitance[9] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Notes:

5. Typical values are at V_{CC}= 5.0V, T_A= +25°C ambient.
6. This input is specified but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
8. Tested at +25°C.
9. This parameter is specified but not tested.

Power Supply Characteristics

Parameter	Description	Test Conditions[10]		Min.	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	$V_{IN}\leq 0.2V$ $V_{IN}\geq V_{CC}-0.2V$	—	5	500	µA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max.	V_{IN}=3.4V[11]	—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[12]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=$\overline{CLKEN}$=GND	$V_{IN}=V_{CC}$ or V_{IN}=GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[13]	V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE}$=$\overline{CLKEN}$=GND at f_1=5 MHz	$V_{IN}=V_{CC}$ or V_{IN}=GND	—	0.8	1.7	mA
			V_{IN}=3.4V or V_{IN}=GND	—	1.3	3.2	
		V_{CC}=Max., at f_1=2.5 MHz, 50% Duty Cycle, Outputs Open, Eighteen Bits Toggling, $\overline{OE}$=$\overline{CLKEN}$=GND f_0=10 MHz	$V_{IN}=V_{CC}$ or V_{IN}=GND	—	4.2	7.1[14]	
			V_{IN}=3.4V or V_{IN}=GND	—	9.2	22.1[14]	

Notes:

10. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
11. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
12. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
13. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
14. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range[15]

Parameter	Description	Condition[16]	CY74FCT16823AT CY74FCT162823AT Min.	CY74FCT16823AT CY74FCT162823AT Max.	Unit	Fig.No.[16]
t_{PLH} t_{PHL}	Propagation Delay CLK to Q	C_L=50 pF R_L=500Ω	1.5	10.0	ns	1, 5
		C_L=300 pF[17] R_L=500Ω	1.5	20.0		
t_{PHL}	Propagation Delay $\overline{CLR}$ to Q	C_L=50 pF R_L=500Ω	1.5	14.0	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Q	C_L=50 pF R_L=500Ω	1.5	12.0	ns	1, 7, 8
		C_L=300 pF[17] R_L=500Ω	1.5	23.0		
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Q	C_L=5 pF[17] R_L=500Ω	1.5	7.0	ns	1, 7, 8
		C_L=50 pF R_L=500Ω	1.5	8.0		
t_{SU}	Set-Up Time HIGH or LOW, D to CLK	C_L=50 pF R_L=500Ω	3.0	—	ns	4
t_H	Hold Time HIGH or LOW, D to CLK		1.5	—	ns	4
t_{SU}	Set-Up Time HIGH or LOW, $\overline{CLKEN}$ to CLK		3.0	—	ns	9
t_H	Hold Time HIGH or LOW $\overline{CLKEN}$ to CLK		0.0	—	ns	9
t_W	CLK Pulse Width HIGH or LOW		6.0	—	ns	5
t_W	$\overline{CLR}$ Pulse Width LOW		6.0	—	ns	5
t_{REM}	Recovery Time $\overline{CLR}$ to CLK		6.0	—	ns	6
$t_{SK(O)}$	Output Skew[18]		—	0.5	ns	—

Switching Characteristics Over the Operating Range[15]

Parameter	Description	Condition[16]	CY74FCT16823CT CY74FCT162823CT Min.	CY74FCT16823CT CY74FCT162823CT Max.	Unit	Fig.No.[16]
t_{PLH} t_{PHL}	Propagation Delay CLK to Q	C_L=50 pF R_L=500Ω	1.5	6.0	ns	1, 5
		C_L=300 pF[17] R_L=500Ω	1.5	12.5		
t_{PHL}	Propagation Delay $\overline{CLR}$ to Q	C_L=50 pF R_L=500Ω	1.5	6.1	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Q	C_L=50 pF R_L=500Ω	1.5	5.5	ns	1, 7, 8
		C_L=300 pF[17] R_L=500Ω	1.5	12.5		
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Q	C_L=5 pF[17] R_L=500Ω	1.5	5.2	ns	1, 7, 8
		C_L=50 pF R_L=500Ω	1.5	6.5		

Switching Characteristics Over the Operating Range[15] (continued)

Parameter	Description	Condition[16]	CY74FCT16823CT CY74FCT162823CT		Unit	Fig.No.[16]
			Min.	Max.		
t_{SU}	Set-Up Time HIGH or LOW, D to CLK	C_L=50 pF R_L=500Ω	2.0	—	ns	4
t_H	Hold Time HIGH or LOW, D to CLK		1.5	—	ns	4
t_{SU}	Set-Up Time HIGH or LOW, $\overline{CLKEN}$ to CLK		3.0	—	ns	9
t_H	Hold Time HIGH or LOW $\overline{CLKEN}$ to CLK		0.0	—	ns	9
t_W	CLK Pulse Width HIGH or LOW		3.3	—	ns	5
t_W	$\overline{CLR}$ Pulse Width LOW		3.3	—	ns	5
t_{REM}	Recovery Time $\overline{CLR}$ to CLK		6.0	—	ns	6
$t_{SK(O)}$	Output Skew[18]		—	0.5	ns	—

Notes:
15. Minimum limits are specified but not tested on Propagation Delays.
16. See “Parameter Measurement Information” in the General Information section.
17. These limits are specified but not tested.
18. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.

Ordering Information CY74FCT16823

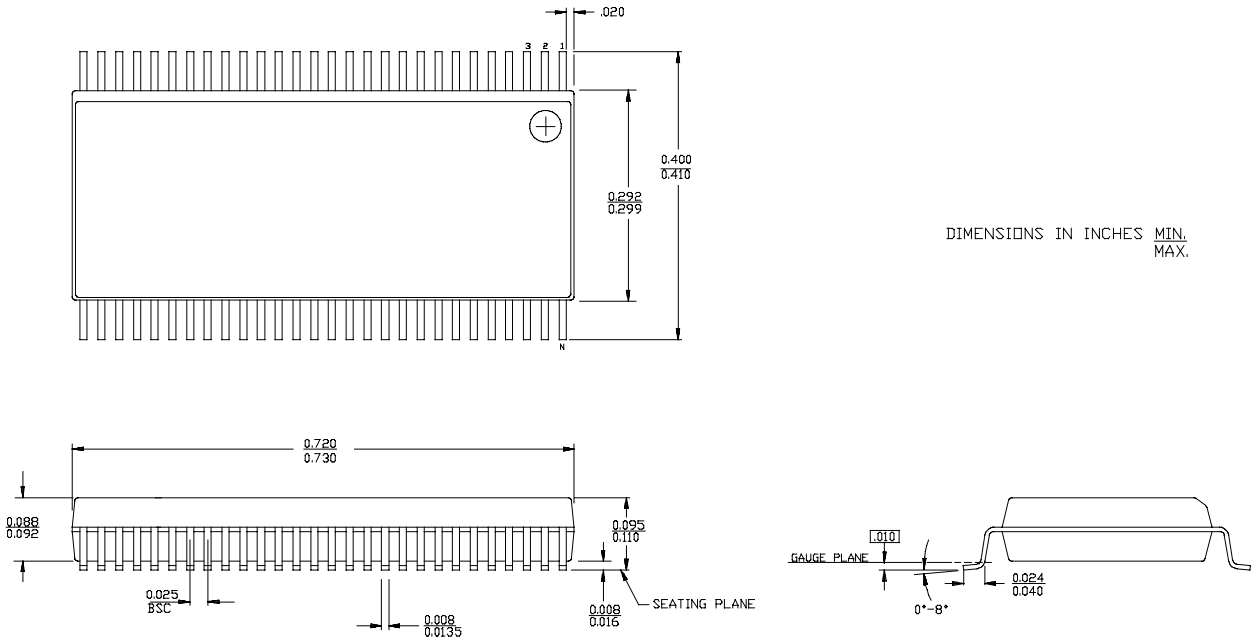
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.0	CY74FCT16823CTPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16823CTPVC/PVCT	O56	56-Lead (300-Mil) SSOP	
10.0	CY74FCT16823ATPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial

Ordering Information CY74FCT162823

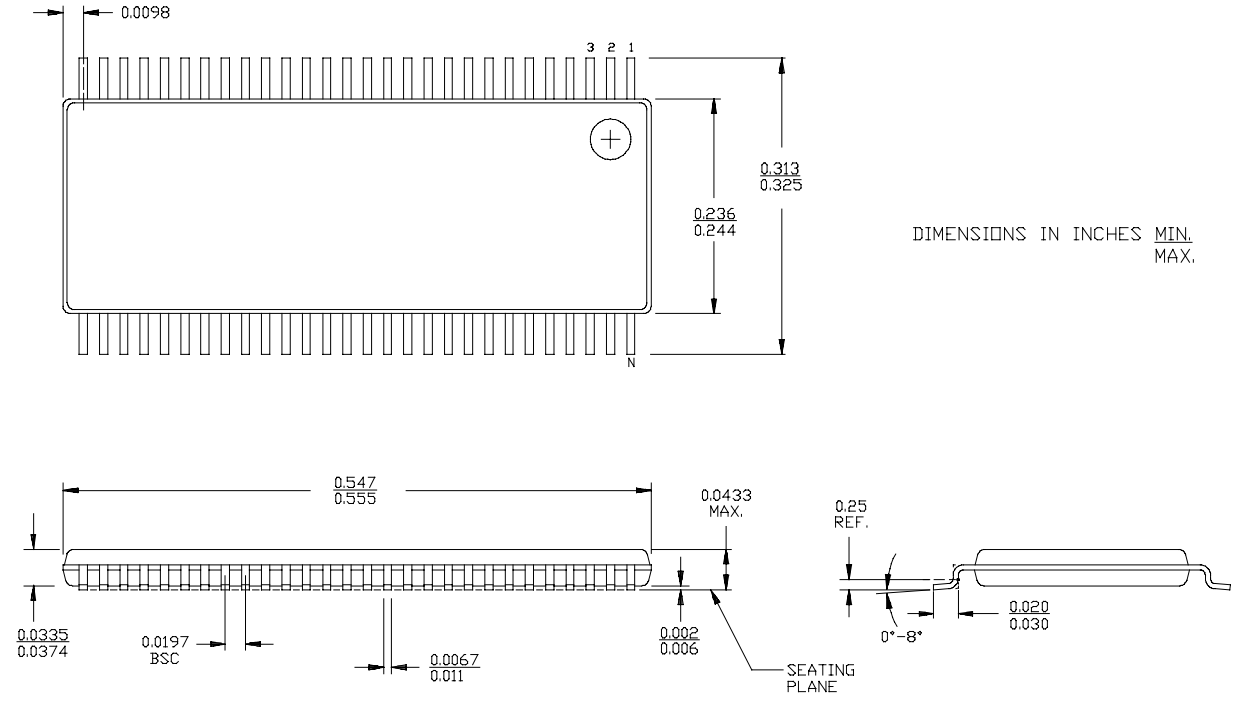
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.0	74FCT162823CTPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162823CTPVC	O56	56-Lead (300-Mil) SSOP	
	74FCT162823CTPVCT	O56	56-Lead (300-Mil) SSOP	
10.0	74FCT162823ATPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial

Package Diagrams

56-Lead Shrunk Small Outline Package O56



56-Lead Thin Shrunk Small Outline Package Z56



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CY74FCT16823ATPACT	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16823A	Samples
CY74FCT16823CTPVC	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16823C	Samples
CY74FCT16823CTPVCT	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16823C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

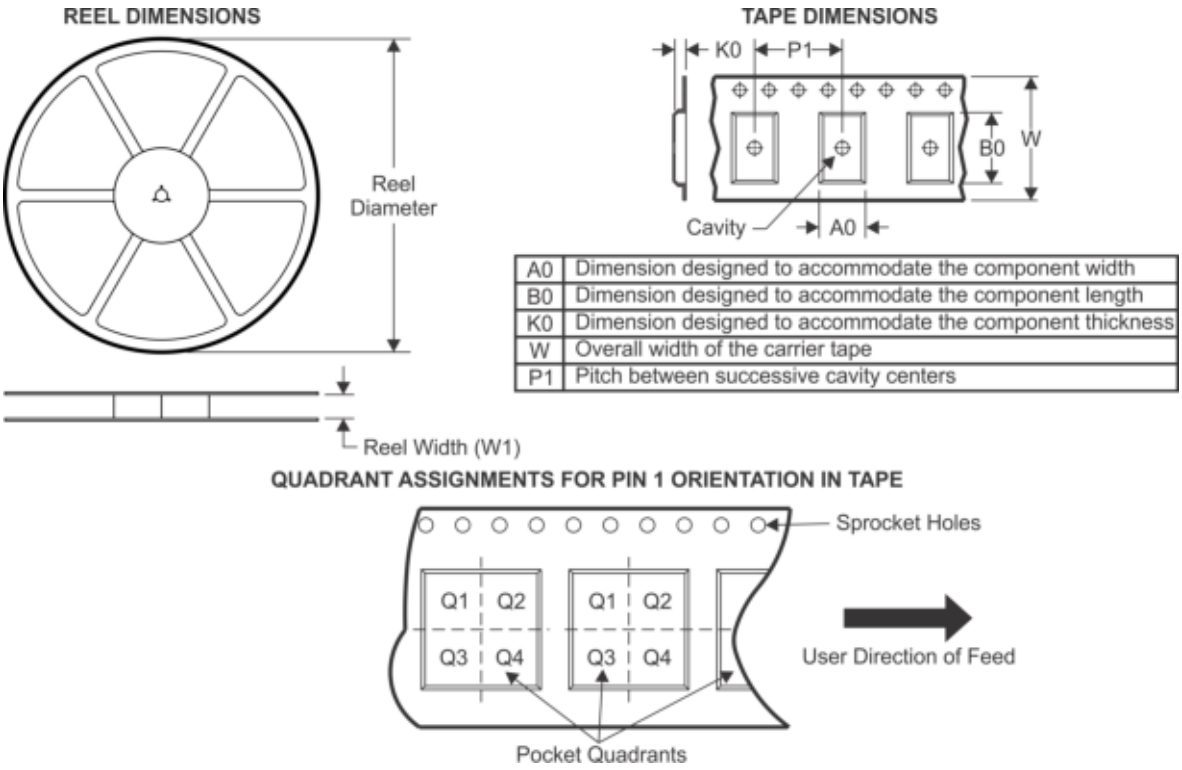
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

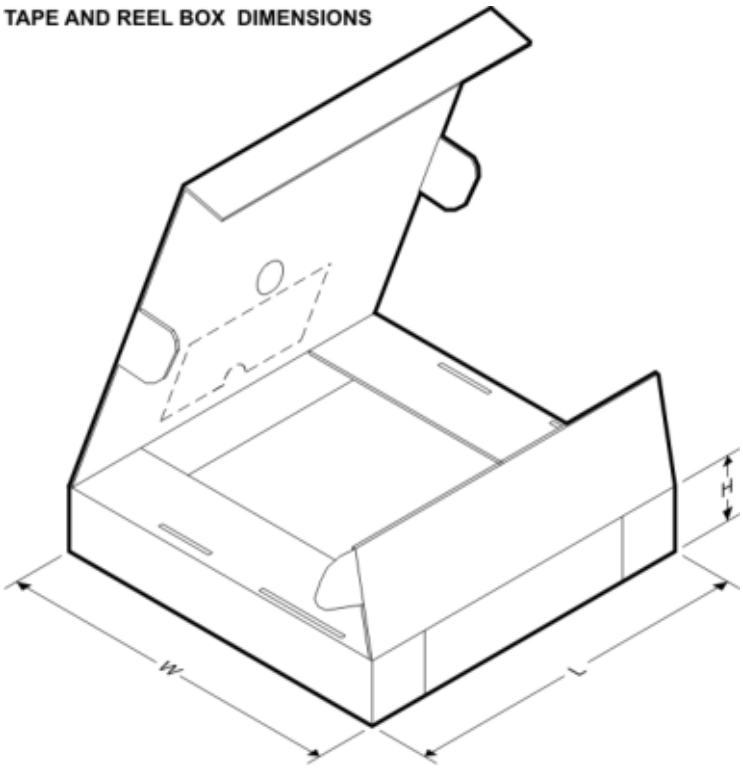


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT16823ATPACT	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
CY74FCT16823CTPVCT	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

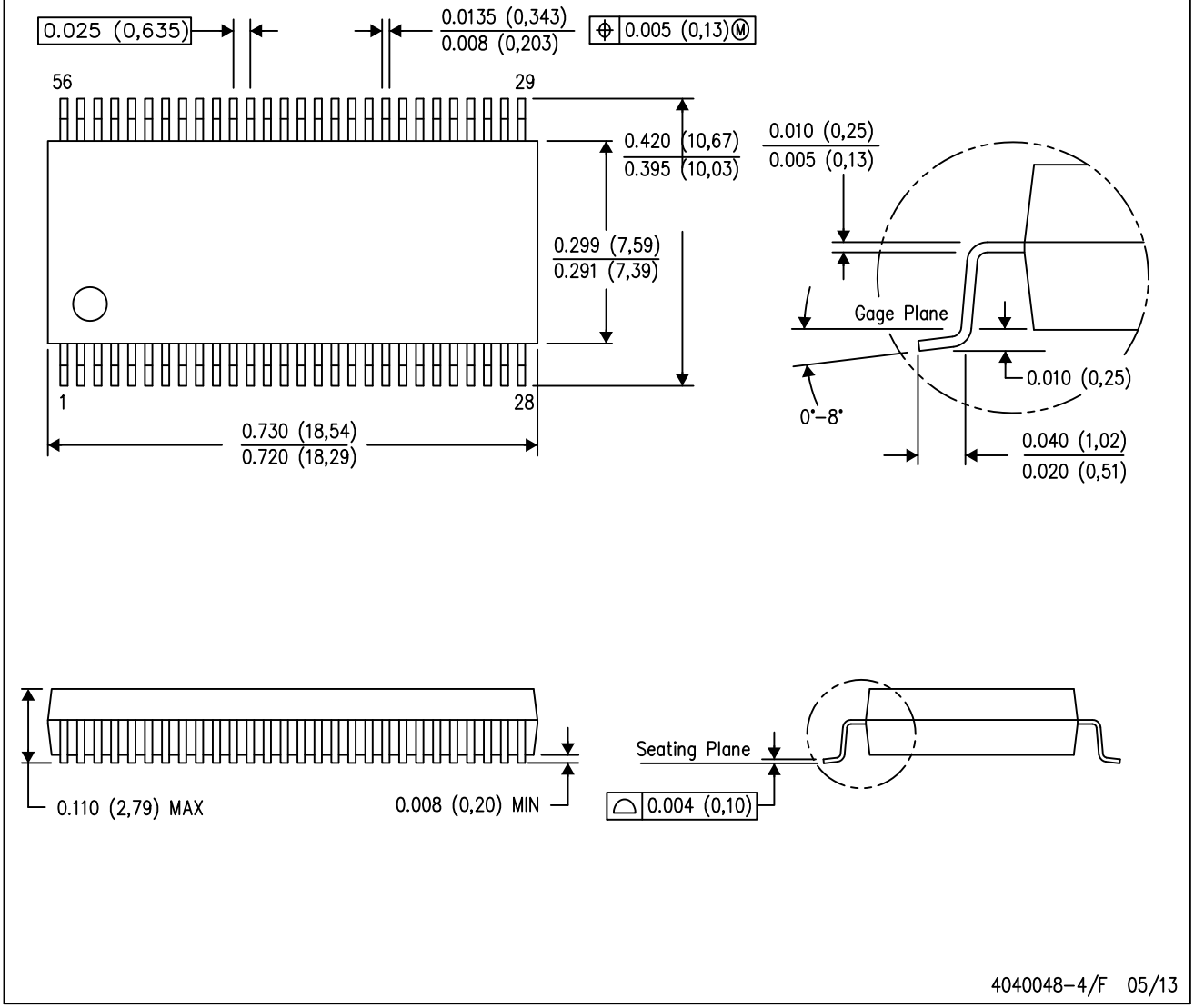
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT16823ATPACT	TSSOP	DGG	56	2000	367.0	367.0	45.0
CY74FCT16823CTPVCT	SSOP	DL	56	1000	367.0	367.0	55.0

DL (R–PDSO–G56) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

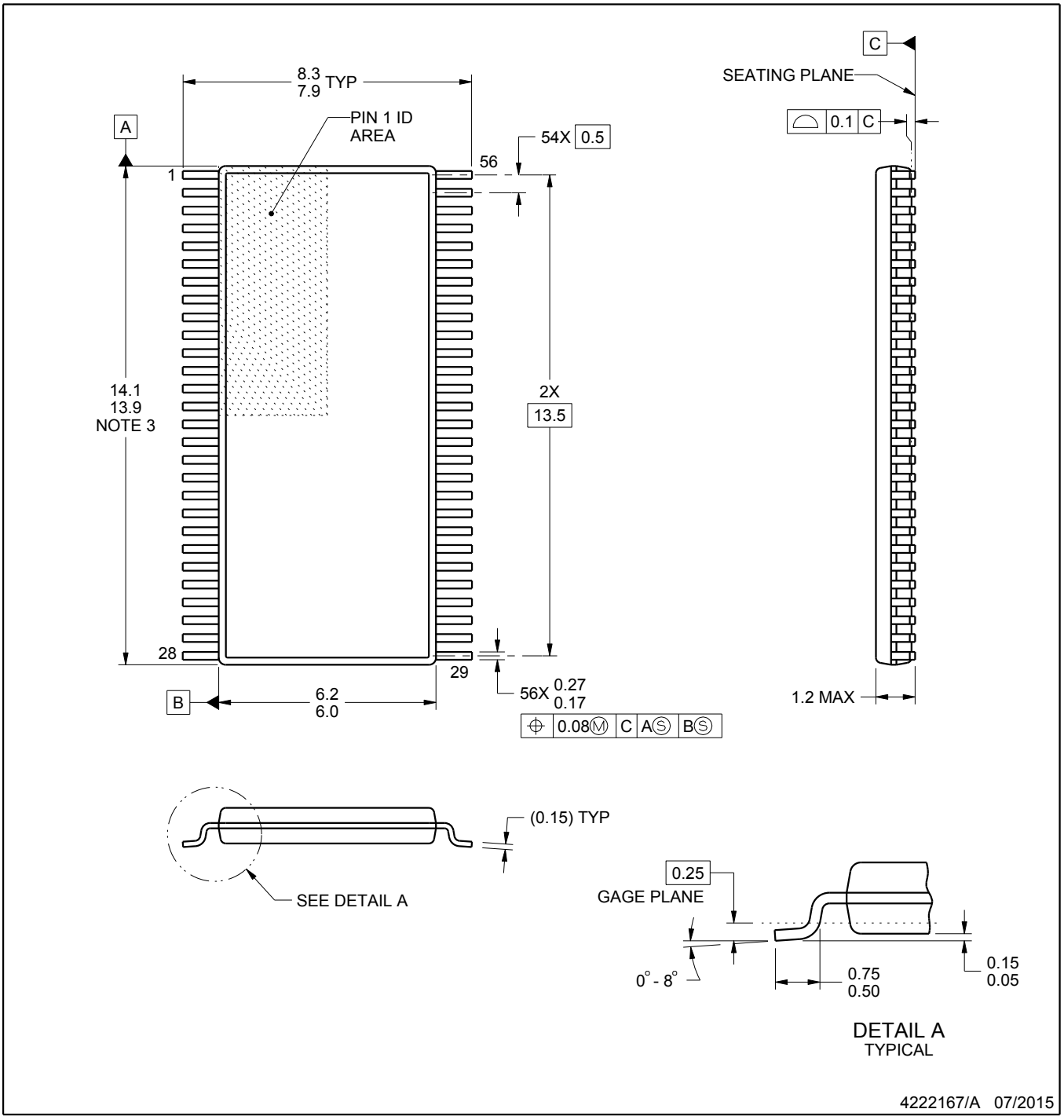
PowerPAD is a trademark of Texas Instruments.

PACKAGE OUTLINE

DGG0056A

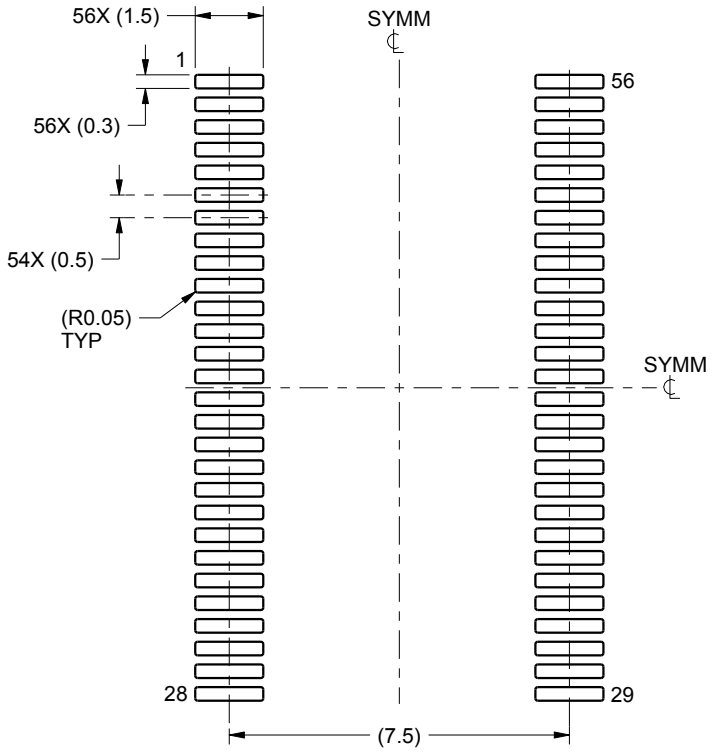
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

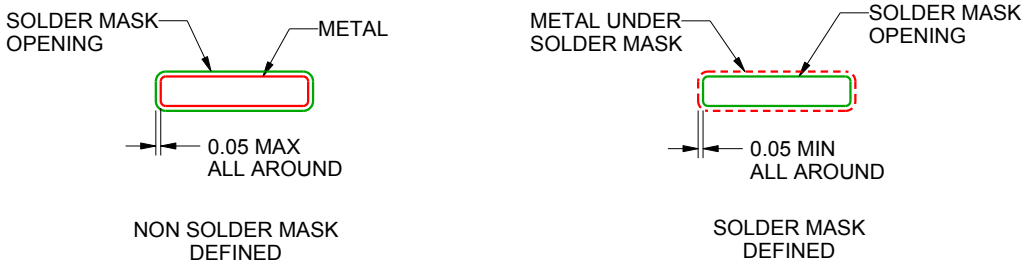


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

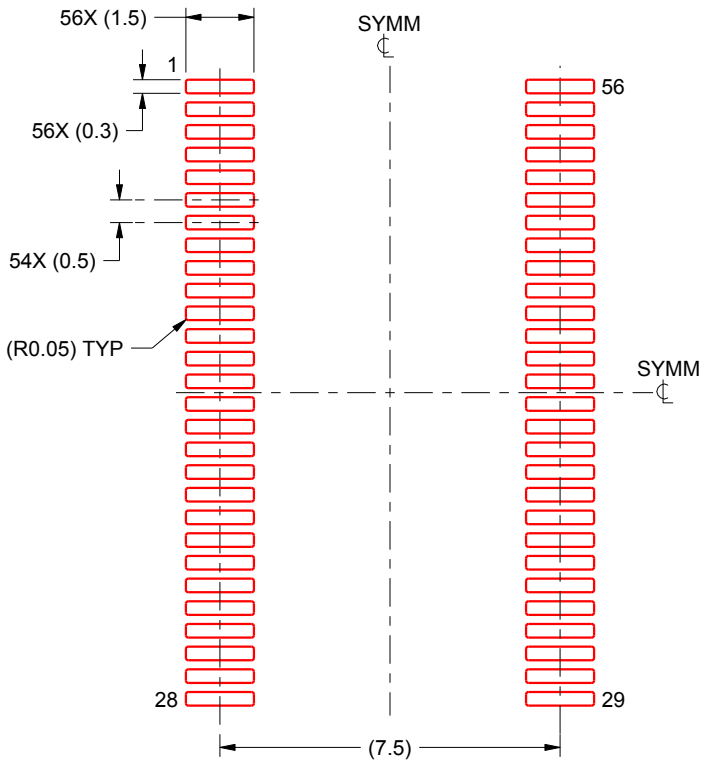


SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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