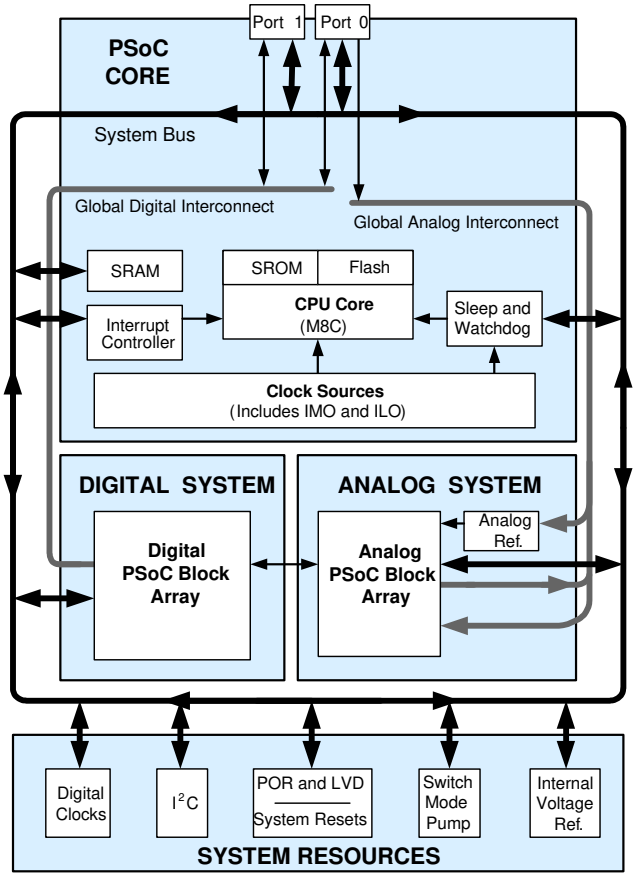
CY8CLED02

EZ-Color™ HB LED Controller

Features

- HB LED controller
  - Configurable dimmers support up to 2 independent LED channels
  - 8- to 32-bits of resolution per channel
  - Dynamic reconfiguration enables LED controller plus other features; Battery Charging, Motor Control
- Visual embedded design
  - LED-Based drivers
    - Binning compensation
    - Temperature feedback
    - Optical feedback
    - DMX512
- PrISM modulation technology
  - Reduces radiated EMI
  - Reduces low frequency blinking
- Powerful Harvard-architecture processor
  - M8C processor speeds up to 24 MHz
  - 3.0 V to 5.25 V operating voltage
  - Operating voltages down to 1.0 V using on-chip switch mode pump (SMP)
  - Industrial temperature range: –40 °C to +85 °C
- Flexible on-chip memory
  - 4 KB flash program storage 50,000 erase/write cycles
  - 256 Bytes static random access memory (SRAM) data storage
  - In-system serial programming (ISSP)
  - Partial flash updates
  - Flexible protection modes
  - EEPROM emulation in flash
- Advanced peripherals (PSoC® blocks)
  - Four digital PSoC blocks provide:
    - 8- to 32-bit timers, counters, and pulse-width modulator (PWMs)
    - Full-duplex universal asynchronous receiver transmitter (UART)
    - Multiple serial peripheral interface (SPI) masters or slaves
    - Connectable to all general purpose I/O (GPIO) pins
  - Four Rail-to-Rail analog PSoC blocks provide:
    - Up to 14-bit analog-to-digital (ADCs)
    - Up to 9-bit digital-to-analog (DACs)
    - Programmable gain amplifiers (PGAs)
    - Programmable filters and comparators
  - Complex peripherals by combining blocks
- Programmable pin configurations
  - 25 mA sink, 10 mA source on all GPIO
  - Pull-up, Pull-down, high Z, strong, or open drain drive modes on all GPIO
  - Up to 12 analog inputs on GPIO
  - Four 30 mA analog outputs on GPIO
  - Configurable interrupt on all GPIO
- Complete development tools
  - Free development software
    - PSoC® Designer™
  - Full-featured, in-circuit emulator (ICE) and Programmer
  - Full-speed emulation
  - Complex breakpoint structure
  - 128 KB trace memory

Logic Block Diagram



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EZ-Color™ Functional Overview

Cypress's EZ-Color family of devices offers the ideal control solution for High Brightness LED applications requiring intelligent dimming control. EZ-Color devices combine the power and flexibility of Programmable System-on-Chip (PSoC®); with Cypress' precise illumination signal modulation (PrISM™) drive technology providing lighting designers a fully customizable and integrated lighting solution platform.

The EZ-Color family supports a range of independent LED channels from 4 channels at 32 bits of resolution each, up to 16 channels at 8 bits of resolution each. This enables lighting designers the flexibility to choose the LED array size and color quality. PSoC Designer software, with lighting specific drivers, can significantly cut development time and simplify implementation of fixed color points through temperature, optical, and LED binning compensation. EZ-Color's virtually limitless analog and digital customization enables the simple integration of features in addition to intelligent lighting, such as Battery Charging, Image Stabilization, and Motor Control during the development process. These features, along with Cypress's best-in-class quality and design support, make EZ-Color the ideal choice for intelligent HB LED control applications.

Target Applications

- LCD Backlight
- Large Signs
- General Lighting
- Architectural Lighting
- Camera/Cell Phone Flash
- Flashlights

The PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and an internal main oscillator (IMO) and an internal low-speed oscillator (ILO). The CPU core, called the M8C, is a powerful, four-million instructions per second (MIPS), 8-bit Harvard-architecture microprocessor with speeds up to 24 MHz.

System resources provide additional capability, such as digital clocks to increase the flexibility of the PSoC; I^2C functionality for implementing an I^2C master, slave, or multi-master; an internal voltage reference that provides an absolute value of 1.3 V to a number of PSoC subsystems; a switch mode pump (SMP) that generates normal operating voltages off a single battery cell; and various system resets supported by the M8C.

The digital system is composed of an array of digital blocks, which can be configured into any number of digital peripherals. The digital blocks can be connected to the GPIO through a series of global busses that can route any signal to any pin, freeing designers from the constraints of a fixed peripheral controller.

The analog system consists of four analog blocks, supporting comparators, and analog-to-digital conversion up to 10 bits of precision.

The Digital System

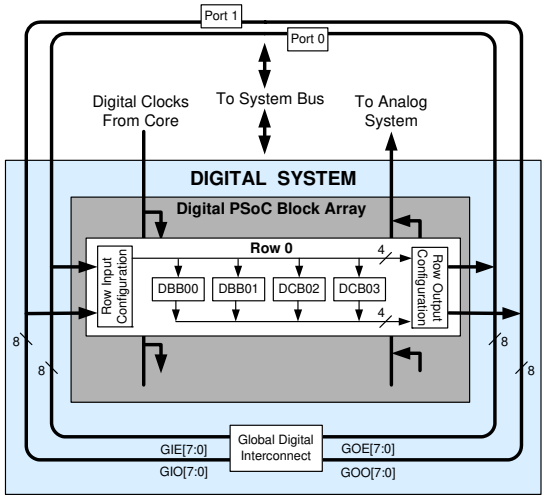
The digital system is composed of four digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8-, 16-, 24-, and 32-bit peripherals, which are called user modules. Digital peripheral configurations include those listed below.

- PrISM (8- to 32-bit)
- PWMs (8- to 32-bit)
- PWMs with dead band (8- to 32-bit)
- Counters (8- to 32-bit)
- Timers (8- to 32-bit)
- UART 8-bit with selectable parity
- SPI master and slave
- I^2C slave, master, multi-master (one available as a system resource)
- Cyclical redundancy checker (CRC)/generator (8- to 32-bit)
- IrDA (up to four)
- Generators (8- to 32-bit)

Connect the digital blocks to any GPIO through a series of global busses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by device family. This allows you the optimum choice of system resources for your application. Family resources are shown in the table titled EZ-Color Device Characteristics.

Figure 1. Digital System Block Diagram



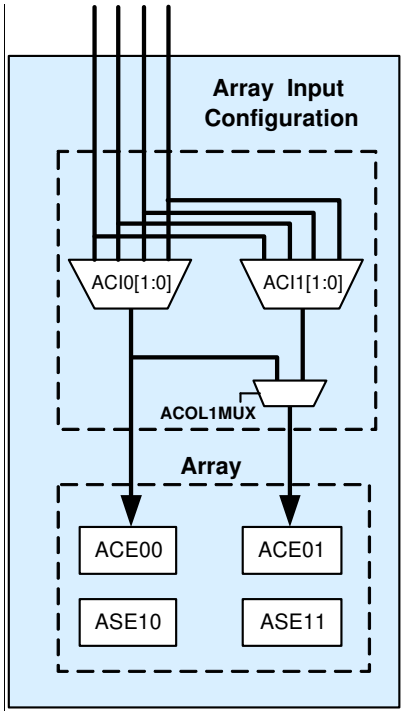
The Analog System

The analog system is composed of four configurable blocks that enable creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common EZ-Color analog functions (most available as user modules) are listed below.

- ADCs (single or dual, with 10-bit resolution)
- Pin-to-pin comparators (1)
- Single-ended comparators (up to two) with absolute (1.3-V) reference or 8-bit DAC reference
- 1.3-V reference (as a system resource)

In most PSoC based devices, analog blocks are provided in columns of three, which includes one continuous time (CT) and two switched capacitor (SC) blocks. This particular EZ-Color device provides limited functionality Type E analog blocks. Each column contains one CT block and one SC block.

Figure 2. Analog System Block Diagram



Additional System Resources

System resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital blocks as clock dividers.
- The I^2C module provides 100- and 400-kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low-voltage detect (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.
- An internal 1.3-V voltage reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch mode pump generates normal operating voltages from a single 1.2-V battery cell, providing a low cost boost converter.

EZ-Color Device Characteristics

Depending on your EZ-Color device characteristics, the digital, and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 4 analog blocks. The following table lists the resources available for specific EZ-Color device groups. The device covered by this data sheet is shown in the highlighted row of the table.

Table 1. EZ-Color Device Characteristics

Part Number	LED Channels	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size	CapSense®
CY8CLED02	2	16	1	4	8	0	2	4	256 Bytes	4K	No
CY8CLED04	4	56	1	4	48	2	2	6	1K	16K	Yes
CY8CLED08	8	44	2	8	12	4	4	12	256 Bytes	16K	No
CY8CLED16	16	44	4	16	12	4	4	12	2K	32K	No

Getting Started

The quickest path to understanding the EZ-Color silicon is by reading this datasheet and using the PSoC Designer integrated development environment (IDE). This datasheet is an overview of the EZ-Color integrated circuit and presents specific pin, register, and electrical specifications.

For up-to-date ordering, packaging, and electrical specification information, reference the latest device datasheets on the cypress website at http://www.cypress.com.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants website.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this lets you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also lets you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select user modules.
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

Pin Information

Pinouts

This section describes, lists, and illustrates the CY8CLED02 EZ-Color device pins and pinout configurations. The CY8CLED02 device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O. However, V_{SS}, V_{DD}, SMP, and XRES are not capable of Digital I/O.

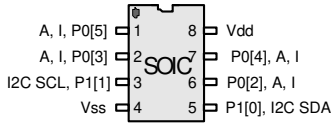
8-Pin Part Pinout

Table 2. 8-Pin Part Pinout (SOIC)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[5]	Analog column mux input.
2	I/O	I	P0[3]	Analog column mux input.
3	I/O	–	P1[1]	I^2C serial clock (SCL), ISSP-SCLK.
4	Power		V_{SS}	Ground connection.
5	I/O	–	P1[0]	I^2C serial data (SDA), ISSP-SDATA.
6	I/O	I	P0[2]	Analog column mux input.
7	I/O	I	P0[4]	Analog column mux input.
8	Power		V_{DD}	Supply voltage.

LEGEND: A = Analog, I = Input, and O = Output.

Figure 3. 8-Pin EZ-Color Device



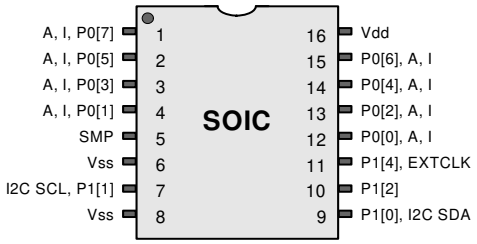
16-Pin Part Pinout

Table 3. 16-Pin Part Pinout (SOIC)

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input.
2	I/O	I	P0[5]	Analog column mux input.
3	I/O	I	P0[3]	Analog column mux input.
4	I/O	I	P0[1]	Analog column mux input.
5	Power		SMP	Switch mode pump (SMP) connection to required external components.
6	Power		V_{SS}	Ground connection.
7	I/O	–	P1[1]	I^2C SCL, ISSP-SCLK.
8	Power		V_{SS}	Ground connection.
9	I/O	–	P1[0]	I^2C SDA, ISSP-SDATA.
10	I/O	–	P1[2]	
11	I/O	–	P1[4]	Optional external clock input (EXTCLK).
12	I/O	I	P0[0]	Analog column mux input.
13	I/O	I	P0[2]	Analog column mux input.
14	I/O	I	P0[4]	Analog column mux input.
15	I/O	I	P0[6]	Analog column mux input.
16	Power		V_{DD}	Supply voltage.

LEGEND A = Analog, I = Input, and O = Output.

Figure 4. 16-Pin EZ-Color Device



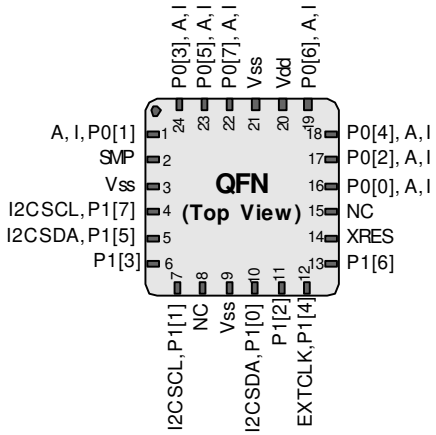
24-Pin Part Pinout

Table 4. 24-Pin Part Pinout (QFN)[2]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P0[1]	Analog column mux input.
2	Power		SMP	SMP connection to required external components.
3	Power		V_{SS}	Ground connection.
4	I/O	–	P1[7]	I^2C SCL.
5	I/O	–	P1[5]	I^2C SDA.
6	I/O	–	P1[3]	–
7	I/O	–	P1[1]	I^2C SCL, ISSP-SCLK[1].
8			NC	No connection.
9	Power		V_{SS}	Ground connection.
10	I/O	–	P1[0]	I^2C SDA, ISSP-SDATA[1].
11	I/O	–	P1[2]	–
12	I/O	–	P1[4]	Optional external clock input (EXTCLK).
13	I/O	–	P1[6]	
14	Input		XRES	Active high external reset with internal pull down.
15			NC	No connection.
16	I/O	I	P0[0]	Analog column mux input.
17	I/O	I	P0[2]	Analog column mux input.
18	I/O	I	P0[4]	Analog column mux input.
19	I/O	I	P0[6]	Analog column mux input.
20	Power		V_{DD}	Supply voltage.
21	Power		V_{SS}	Ground connection.
22	I/O	I	P0[7]	Analog column mux input.
23	I/O	I	P0[5]	Analog column mux input.
24	I/O	I	P0[3]	Analog column mux input.

LEGEND A = Analog, I = Input, and O = Output.

Figure 5. 24-Pin EZ-Color Device



Notes
1. These are the ISSP pins, which are not High Z at power-on reset (POR).
2. The center pad on the QFN package should be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.

Register Reference

Register Conventions

This section lists the registers of the CY8CLED02 EZ-Color device.

The register conventions specific to this section are listed in the following table.

Table 5. Register Conventions

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks, Bank 0 and Bank 1. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set to 1, the user is in Bank 1.

Note In the following register mapping tables, blank fields are Reserved and should not be accessed.

Table 6. Register Map Bank 0: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASE10CR0	80	RW		C0	
PRT0IE	01	RW		41			81			C1	
PRT0GS	02	RW		42			82			C2	
PRT0DM2	03	RW		43			83			C3	
PRT1DR	04	RW		44		ASE11CR0	84	RW		C4	
PRT1IE	05	RW		45			85			C5	
PRT1GS	06	RW		46			86			C6	
PRT1DM2	07	RW		47			87			C7	
	08			48			88			C8	
	09			49			89			C9	
	0A			4A			8A			CA	
	0B			4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50			90			D0	
	11			51			91			D1	
	12			52			92			D2	
	13			53			93			D3	
	14			54			94			D4	
	15			55			95			D5	
	16			56			96		I2C_CFG	D6	RW
	17			57			97		I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99		I2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW	PWM_CR	62	RW		A2		INT_VC	E2	RC
DBB00CR0	23	#		63			A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4			E4	
DBB01DR1	25	W		65			A5			E5	
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#	ADC0_CR	68	#		A8			E8	
DCB02DR1	29	W	ADC1_CR	69	#		A9			E9	
DCB02DR2	2A	RW		6A			AA			EA	
DCB02CR0	2B	#		6B			AB			EB	
DCB03DR0	2C	#	TMP_DR0	6C	RW		AC			EC	
DCB03DR1	2D	W	TMP_DR1	6D	RW		AD			ED	
DCB03DR2	2E	RW	TMP_DR2	6E	RW		AE			EE	
DCB03CR0	2F	#	TMP_DR3	6F	RW		AF			EF	
	30			70		RDI0RI	B0	RW		F0	
	31			71		RDI0SYN	B1	RW		F1	
	32		ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34			74		RDI0LT1	B4	RW		F4	
	35			75		RDI0RO0	B5	RW		F5	
	36		ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACE01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific.

Table 7. Register Map Bank 1: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASE10CR0	80	RW		C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43			83			C3	
PRT1DM0	04	RW		44		ASE11CR0	84	RW		C4	
PRT1DM1	05	RW		45			85			C5	
PRT1IC0	06	RW		46			86			C6	
PRT1IC1	07	RW		47			87			C7	
	08			48			88			C8	
	09			49			89			C9	
	0A			4A			8A			CA	
	0B			4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50			90		GDI_O_IN	D0	RW
	11			51			91		GDI_E_IN	D1	RW
	12			52			92		GDI_O_OU	D2	RW
	13			53			93		GDI_E_OU	D3	RW
	14			54			94			D4	
	15			55			95			D5	
	16			56			96			D6	
	17			57			97			D7	
	18			58			98			D8	
	19			59			99			D9	
	1A			5A			9A			DA	
	1B			5B			9B			DB	
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW	CMP_GO_EN	64	RW		A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5		ADC0_TR	E5	RW
DBB01OU	26	RW	AMD_CR1	66	RW		A6		ADC1_TR	E6	RW
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68			A8		IMO_TR	E8	W
DCB02IN	29	RW		69			A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B		CLK_CR3	6B	RW		AB		ECO_TR	EB	W
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30			70		RDI0RI	B0	RW		F0	
	31			71		RDI0SYN	B1	RW		F1	
	32		ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34			74		RDI0LT1	B4	RW		F4	
	35			75		RDI0RO0	B5	RW		F5	
	36		ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACE01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA		FLS_PR1	FA	RW
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific.

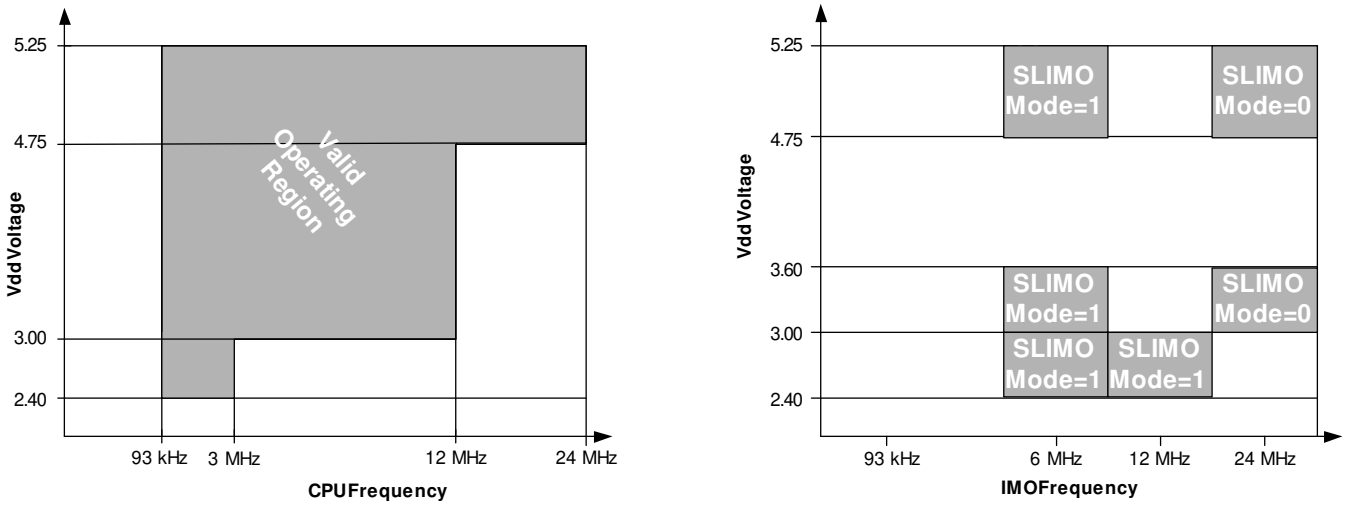
Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CLED02 EZ-Color device. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com.

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted.

Refer to Table 21 for the electrical specifications for the IMO using SLIMO mode.

Figure 6. Voltage versus CPU Frequency, and Voltage versus IMO Frequency



Absolute Maximum Ratings

Table 8. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	–55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 65 °C degrade reliability.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	°C	
$T_{BAKETIME}$	Bake Time	See package label	–	72	Hours	
T_A	Ambient temperature with power applied	–40	–	+85	°C	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} - 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tri-state	V_{SS} - 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	
ESD	Electrostatic discharge voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch up current	–	–	200	mA	

Operating Temperature

Table 9. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature	–40	–	+85	°C	
T_J	Junction temperature	–40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Thermal Impedances on page 34. You must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip-Level Specifications

Table 10 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 10. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	2.40	–	5.25	V	See DC POR and LVD specifications, Table 18 on page 20.
I_{DD}	Supply current, IMO = 24 MHz	–	3	4	mA	Conditions are V_{DD} = 5.0 V, 25 °C, CPU = 3 MHz, SYSCLK doubler disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz.
I_{DD3}	Supply current, IMO = 6 MHz	–	1.2	2	mA	Conditions are V_{DD} = 3.3 V, 25 °C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz, VC2 = 23.4 kHz, VC3 = 0.091 kHz.
I_{DD27}	Supply current, IMO = 6 MHz	–	1.1	1.5	mA	Conditions are V_{DD} = 2.55 V, 25 °C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz, VC2 = 23.4 kHz, VC3 = 0.091 kHz.
I_{SB27}	Sleep (mode) current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active. Mid temperature range.	–	2.6	4	µA	V_{DD} = 2.55 V, 0 °C to 40 °C.
I_{SB}	Sleep (mode) current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active.	–	2.8	5	µA	V_{DD} = 3.3 V, -40 °C ≤ T_A ≤ 85 °C.
V_{REF}	Reference voltage (Bandgap)	1.28	1.30	1.32	V	Trimmed for appropriate V_{DD}. V_{DD} = 3.0 V to 5.25 V.
V_{REF27}	Reference voltage (Bandgap)	1.16	1.30	1.330	V	Trimmed for appropriate V_{DD}. V_{DD} = 2.4 V to 3.0 V.
AGND	Analog ground	V_{REF} - 0.003	V_{REF}	V_{REF} + 0.003	V	

DC General Purpose I/O Specifications

Table 11 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 11. 5-V and 3.3-V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	
V_{OH}	High output level	V_{DD} - 1.0	–	–	V	I_{OH} = 10 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I_{OH} budget.
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 25 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined I_{OL} budget.
I_{OH}	High level source current	10	–	–	mA	V_{OH} = V_{DD}-1.0 V. See the limitations of the total current in the Note for V_{OH}.
I_{OL}	Low level sink current	25	–	–	mA	V_{OL} = 0.75 V. See the limitations of the total current in the Note for V_{OL}.
V_{IL}	Input low level	–	–	0.8	V	V_{DD} = 3.0 to 5.25.
V_{IH}	Input high level	2.1	–	–	V	V_{DD} = 3.0 to 5.25.
V_H	Input hysteresis	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.

Table 12 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C. Typical parameters are measured at 2.7 V at 25 °C and are for design guidance only.

Table 12. 2.7-V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	
V_{OH}	High output level	V_{DD} - 0.4	–	–	V	I_{OH} = 2.5 mA (6.25 typical), V_{DD} = 2.4 to 3.0 V (16 mA maximum, 50 mA typical combined I_{OH} budget).
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 10 mA, V_{DD} = 2.4 to 3.0 V (90 mA maximum combined I_{OL} budget).
I_{OH}	High level source current	2.5	–	–	mA	V_{OH} = V_{DD}-0.4 V. See the limitations of the total current in the Note for V_{OH}.
I_{OL}	Low Level Sink Current	10	–	–	mA	V_{OL} = 0.75 V. See the limitations of the total current in the Note for VOL.
V_{IL}	Input low level	–	–	0.75	V	V_{DD} = 2.4 to 3.0.
V_{IH}	Input high level	2.0	–	–	V	V_{DD} = 2.4 to 3.0.
V_H	Input hysteresis	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.

DC Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 13. 5-V DC Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average input offset voltage drift	–	10	–	μV/°C	
I_{EBOA}	Input leakage current (Port 0 analog pins)	–	200	–	pA	Gross tested to 1 μA.
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C.
V_{CMOA}	Common mode voltage range	0.0	–	V_{DD} - 1	V	
G_{OLOA}	Open loop gain	80	–	–	dB	
I_{SOA}	Amplifier supply current	–	10	30	μA	

Table 14. 3.3-V DC Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average input offset voltage drift	–	10	–	µV/°C	
I_{EBOA}	Input leakage current (Port 0 analog pins)	–	200	–	pA	Gross tested to 1 µA.
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C.
V_{CMOA}	Common mode voltage range	0	–	V_{DD} - 1	V	
G_{OLOA}	Open loop gain	80	–	–	dB	
I_{SOA}	Amplifier supply current	–	10	30	µA	

Table 15. 2.7-V DC Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average input offset voltage drift	–	10	–	µV/°C	
I_{EBOA}	Input leakage current (Port 0 analog pins)	–	200	–	pA	Gross tested to 1 µA.
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C.
V_{CMOA}	Common mode voltage range	0	–	V_{DD} - 1	V	
G_{OLOA}	Open loop gain	80	–	–	dB	
I_{SOA}	Amplifier supply current	–	10	30	µA	

DC Low Power Comparator Specifications

Table 16 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V at 25 °C and are for design guidance only.

Table 16. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	V_{DD} - 1	V	
I_{SLPC}	LPC supply current	–	10	40	µA	
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV	

DC Switch Mode Pump Specifications

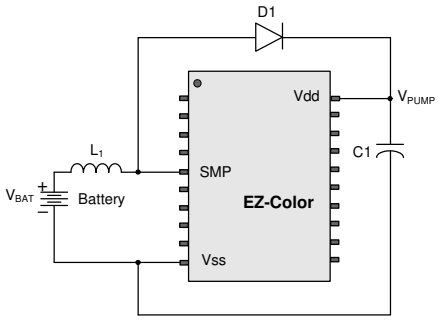
Table 17 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 17. DC Switch Mode Pump (SMP) Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PUMP5V}	5 V output voltage from pump	4.75	5.0	5.25	V	Configured as in Note 3. Average, neglecting ripple. SMP trip voltage is set to 5.0 V.
V_{PUMP3V}	3.3 V output voltage from pump	3.00	3.25	3.60	V	Configured as in Note 3. Average, neglecting ripple. SMP trip voltage is set to 3.25 V.
V_{PUMP2V}	2.6 V output voltage from pump	2.45	2.55	2.80	V	Configured as in Note 3. Average, neglecting ripple. SMP trip voltage is set to 2.55 V.
I_{PUMP}	Available output current V_{BAT} = 1.8 V, V_{PUMP} = 5.0 V V_{BAT} = 1.5 V, V_{PUMP} = 3.25 V V_{BAT} = 1.3 V, V_{PUMP} = 2.55 V	 5 8 8	 – – –	 – – –	 mA mA mA	Configured as in Note 3. SMP trip voltage is set to 5.0 V. SMP trip voltage is set to 3.25 V. SMP trip voltage is set to 2.55 V.
V_{BAT5V}	Input voltage range from battery	1.8	–	5.0	V	Configured as in Note 3. SMP trip voltage is set to 5.0 V.
V_{BAT3V}	Input voltage range from battery	1.0	–	3.3	V	Configured as in Note 3. SMP trip voltage is set to 3.25 V.
V_{BAT2V}	Input voltage range from battery	1.0	–	2.8	V	Configured as in Note 3. SMP trip voltage is set to 2.55 V.
$V_{BATSTART}$	Minimum input voltage from battery to start pump	1.2	–	–	V	Configured as in Note 3. 0 °C ≤ T_A ≤ 100. 1.25 V at T_A = –40 °C.
ΔV_{PUMP_Line}	Line regulation (over Vi range)	–	5	–	$\%V_O$	Configured as in Note 3. V_O is the "V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 18 on page 20.
ΔV_{PUMP_Load}	Load Regulation	–	5	–	$\%V_O$	Configured as in Note 3. V_O is the "V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 18 on page 20.
ΔV_{PUMP_Ripple}	Output voltage ripple (depends on cap/load)	–	100	–	mVpp	Configured as in Note 3. Load is 5 mA.
E_3	Efficiency	35	50	–	%	Configured as in Note 3. Load is 5 mA. SMP trip voltage is set to 3.25 V.
E_2	Efficiency	35	80	–	%	For I load = 1mA, V_{PUMP} = 2.55 V, V_{BAT} = 1.3 V, 10 µH inductor, 1 µF capacitor, and Schottky diode.
F_{PUMP}	Switching frequency	–	1.3	–	MHz	
DC_{PUMP}	Switching duty cycle	–	50	–	%	

Note
3. L_1 = 2 mH inductor, C_1 = 10 mF capacitor, D_1 = Schottky diode. See Figure 7 on page 20.

Figure 7. Basic Switch Mode Pump Circuit



DC POR and LVD Specifications

Table 18 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 18. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} value for PPOR trip					V_{DD} must be greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from Watchdog.
V_{PPOR0}	PORLEV[1:0] = 00b		2.36	2.40	V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	2.82	2.95	V	
V_{PPOR2}	PORLEV[1:0] = 10b		4.55	4.70	V	
	V_{DD} value for LVD trip					
V_{LVD0}	VM[2:0] = 000b	2.40	2.45	2.51[4]	V	
V_{LVD1}	VM[2:0] = 001b	2.85	2.92	2.99[5]	V	
V_{LVD2}	VM[2:0] = 010b	2.95	3.02	3.09	V	
V_{LVD3}	VM[2:0] = 011b	3.06	3.13	3.20	V	
V_{LVD4}	VM[2:0] = 100b	4.37	4.48	4.55	V	
V_{LVD5}	VM[2:0] = 101b	4.50	4.64	4.75	V	
V_{LVD6}	VM[2:0] = 110b	4.62	4.73	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.81	4.95	V	
	V_{DD} value for PUMP trip					
V_{PUMP0}	VM[2:0] = 000b	2.45	2.55	2.62[6]	V	
V_{PUMP1}	VM[2:0] = 001b	2.96	3.02	3.09	V	
V_{PUMP2}	VM[2:0] = 010b	3.03	3.10	3.16	V	
V_{PUMP3}	VM[2:0] = 011b	3.18	3.25	3.32[7]	V	
V_{PUMP4}	VM[2:0] = 100b	4.54	4.64	4.74	V	
V_{PUMP5}	VM[2:0] = 101b	4.62	4.73	4.83	V	
V_{PUMP6}	VM[2:0] = 110b	4.71	4.82	4.92	V	
V_{PUMP7}	VM[2:0] = 111b	4.89	5.00	5.12	V	

Notes
4. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
5. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.
6. Always greater than 50 mV above V_{LVD0}.
7. Always greater than 50 mV above V_{LVD3}.

DC Programming Specifications

Table 19 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 19. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5.0	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	3.0	3.1	3.2	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operations	3.0	–	5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	5	25	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.2	–	–	V	
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	V_{SS} + 0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} - 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block)	50,000[8]	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash endurance (total)[9]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention	10	–	–	Years	

DC I²C Specifications

Table 20 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 20. DC I²C Specifications[10]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}	Input low level	–	–	0.3 × V_{DD}	V	3.0 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}	Input high level	0.7 × V_{DD}	–	–	V	3.0 V ≤ V_{DD} ≤ 5.25 V

Notes

8. The 50,000 cycle flash endurance per block will only be guaranteed if the flash is operating within one voltage range. Voltage ranges are 2.4 V to 3.0 V, 3.0 V to 3.6 V, and 4.75 V to 5.25 V.
9. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
   For the full industrial range, you must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.
10. All GPIO meet the DC GPIO V_{IL} and V_{IH} specifications mentioned in section DC General Purpose I/O Specifications on page 16. The I²C GPIO pins also meet the mentioned specs.

AC Electrical Characteristics

AC Chip-Level Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and
–40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 21. 5-V and 3.3-V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24}	IMO frequency for 24 MHz	23.4	24	24.6[11,12]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. Refer to Figure 6 on page 13. SLIMO mode = 0.
F_{IMO6}	IMO frequency for 6 MHz	5.5	6	6.5[11,12]	MHz	Trimmed for 3.3 V operation using factory trim values. See Figure 6 on page 13. SLIMO mode = 1.
F_{CPU1}	CPU frequency (5 V nominal)	0.0937	24	24.6[11]	MHz	12 MHz only for SLIMO mode = 0.
F_{CPU2}	CPU frequency (3.3 V nominal)	0.0937	12	12.3[12]	MHz	SLIMO Mode = 0.
F_{BLK5}	Digital PSoC block frequency (5 V nominal)	0	48	49.2[11,13]	MHz	Refer to the section AC Digital Block Specifications on page 26.
F_{BLK33}	Digital PSoC block frequency (3.3 V nominal)	0	24	24.6[13]	MHz	
F_{32K1}	ILO frequency	15	32	64	kHz	
F_{32K_U}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the system resets section of the PSoC Technical Reference Manual for details on this timing.
t_{XRST}	External reset pulse width	10	–	–	µs	
DC24M	24 MHz duty cycle	40	50	60	%	
DC_{ILO}	ILO duty cycle	20	50	80	%	
Step24M	24 MHz trim step size	–	50	–	kHz	
Fout48M	48 MHz output frequency	46.8	48.0	49.2[11,12]	MHz	Trimmed. Using factory trim values.
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power-up.
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power up from 0 V. See the system resets section of the PSoC Technical Reference Manual.
t_{jit_IMO}	24-MHz IMO cycle-to-cycle jitter (RMS) [14]	–	200	700	ps	
	24-MHz IMO long term N cycle-to-cycle jitter (RMS) [14]	–	300	900	ps	N = 32
	24-MHz IMO period jitter (RMS) [14]	–	100	400	ps	

Notes
11. 4.75 V < V_{DD} < 5.25 V.
12. 3.0 V < V_{DD} < 3.6 V.
13. See the individual user module datasheets for information on maximum frequencies for user modules.
14. Refer to the application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information on jitter specifications.

Table 22. 2.7-V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO12}	IMO frequency for 12 MHz	11.5	12	12.7[15]	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 6 on page 13. SLIMO mode = 1.
F_{IMO6}	IMO frequency for 6 MHz	5.5	6	6.5[15]	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 6 on page 13. SLIMO mode = 1.
F_{CPU1}	CPU frequency (2.7 V nominal)	0.093	3	3.15[15]	MHz	24 MHz only for SLIMO mode = 0.
F_{BLK27}	Digital PSoC block frequency (2.7 V nominal)	0	12	12.5[15]	MHz	Refer to the section AC Digital Block Specifications on page 26.
F_{32K1}	ILO frequency	8	32	96	kHz	
F_{32K_U}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the system resets section of the PSoC Technical Reference Manual for details on this timing.
t_{XRST}	External reset pulse width	10	–	–	µs	
DC_{ILO}	ILO duty cycle	20	50	80	%	
F_{MAX}	Maximum frequency of signal on row input or row output	–	–	12.3	MHz	
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power up.
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power up from 0 V. See the system resets section of the PSoC Technical Reference Manual.
t_{jit_IMO}	12-MHz IMO cycle-to-cycle jitter (RMS)[16]	–	400	1000	ps	
	12-MHz IMO long term N cycle-to-cycle jitter (RMS)[16]	–	600	1300	ps	N = 32
	12-MHz IMO period jitter (RMS)[16]	–	100	500	ps	

Notes
15. 2.4 V < V_{DD} < 3.0 V.
16. Refer to the application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information on jitter specifications.

AC GPIO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

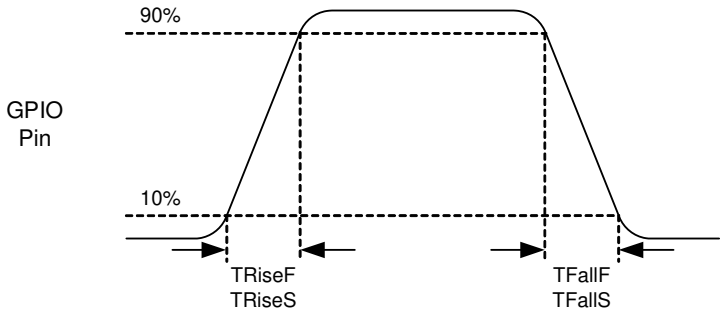
Table 23. 5-V and 3.3-V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	12	MHz	Normal strong mode
TRiseF	Rise time, normal strong mode, Cload = 50 pF	3	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10% - 90%
TFallF	Fall time, normal strong mode, Cload = 50 pF	2	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10% - 90%
TRiseS	Rise time, slow strong mode, Cload = 50 pF	10	27	–	ns	V_{DD} = 3 to 5.25 V, 10% - 90%
TFallS	Fall time, slow strong mode, Cload = 50 pF	10	22	–	ns	V_{DD} = 3 to 5.25 V, 10% - 90%

Table 24. 2.7-V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	3	MHz	Normal strong mode
TRiseF	Rise time, normal strong mode, Cload = 50 pF	6	–	50	ns	V_{DD} = 2.4 to 3.0 V, 10% - 90%
TFallF	Fall time, normal strong mode, Cload = 50 pF	6	–	50	ns	V_{DD} = 2.4 to 3.0 V, 10% - 90%
TRiseS	Rise time, slow strong mode, Cload = 50 pF	18	40	120	ns	V_{DD} = 2.4 to 3.0 V, 10% - 90%
TFallS	Fall time, slow strong mode, Cload = 50 pF	18	40	120	ns	V_{DD} = 2.4 to 3.0 V, 10% - 90%

Figure 8. GPIO Timing Diagram



AC Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Table 25. 5-V and 3.3-V AC Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{COMP1}	Comparator mode response time, 50 mVpp signal centered on reference	–	–	100	ns	
T_{COMP2}	Comparator mode response time, 2.5 V input, 0.5 V overdrive	–	–	300	ns	

Table 26. 2.7V AC Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{COMP1}	Comparator mode response Time, 50 mVpp signal centered on Ref	–	–	600	ns	
T_{COMP2}	Comparator mode response time, 1.5 V input, 0.5 V overdrive	–	–	300	ns	

AC Low Power Comparator Specifications

Table 27 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V at 25 °C and are for design guidance only.

Table 27. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RLPC}	LPC response time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}.

AC Digital Block Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 28. 5-V and 3.3-V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Unit	Notes
All functions	Block input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
Timer	Input clock frequency					
	No capture, V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	No capture, V_{DD} < 4.75 V	–	–	24.6	MHz	
	With capture	–	–	24.6	MHz	
	Capture pulse width	50[17]	–	–	ns	
Counter	Input clock frequency					
	No enable input, V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	No enable input, V_{DD} < 4.75 V	–	–	24.6	MHz	
	With enable input	–	–	24.6	MHz	
	Enable input pulse width	50[17]	–	–	ns	
Dead Band	Kill pulse width					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	50[17]	–	–	ns	
	Disable mode	50[17]	–	–	ns	
	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
CRCPRS (PRS Mode)	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	24.6	MHz	
SPIM	Input clock frequency	–	–	8.2	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock (SCLK) frequency	–	–	4.1	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_negated between transmissions	50[17]	–	–	ns	
Transmitter	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	49.2	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	24.6	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
Receiver	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	49.2	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	24.6	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	

Note
17. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

Table 29. 2.7-V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All Functions	Block input clock frequency			12.7	MHz	2.4 V < V_{DD} < 3.0 V.
Timer	Capture pulse width	100[18]	–	–	ns	
	Input clock frequency, with or without Capture	–	–	12.7	MHz	
Counter	Enable input pulse width	100	–	–	ns	
	Input clock frequency, no enable input	–	–	12.7	MHz	
	Input clock frequency, enable input	–	–	12.7	MHz	
Dead Band	Kill pulse width:					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	100	–	–	ns	
	Disable mode	100	–	–	ns	
	Input clock frequency	–	–	12.7	MHz	
CRCPRS (PRS Mode)	Input clock frequency	–	–	12.7	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	12.7	MHz	
SPIM	Input clock frequency	–	–	6.35	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input Clock (SCLK) Frequency	–	–	4.1	MHz	
	Width of SS_ Negated between transmissions	100	–	–	ns	
Transmitter	Input clock frequency	–	–	12.7	MHz	The baud rate is equal to the input clock frequency divided by 8.
Receiver	Input clock frequency	–	–	12.7	MHz	The baud rate is equal to the input clock frequency divided by 8.

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 30. 5-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz	
–	High period	20.6	–	5300	ns	
–	Low period	20.6	–	–	ns	
–	Power up IMO to switch	150	–	–	μs	

Note
18. 100 ns minimum input pulse width is based on the input synchronizers running at 12 MHz (84 ns nominal period).

Table 31. 3.3-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.093	–	12.3	MHz	Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.186	–	24.6	MHz	If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider will ensure that the fifty percent duty cycle requirement is met.
–	High period with CPU clock divide by 1	41.7	–	5300	ns	
–	Low period with CPU clock divide by 1	41.7	–	–	ns	
–	Power up IMO to switch	150	–	–	µs	

Table 32. 2.7-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.093	–	6.06	MHz	Maximum CPU frequency is 3 MHz at 2.7 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.186	–	12.12	MHz	If the frequency of the external clock is greater than 3 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider will ensure that the fifty percent duty cycle requirement is met.
–	High period with CPU clock divide by 1	83.4	–	5300	ns	
–	Low period with CPU clock divide by 1	83.4	–	–	ns	
–	Power up IMO to switch	150	–	–	µs	

AC Programming Specifications

Table 33 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 33. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall time of SCLK	1	–	20	ns	
T_{SSCLK}	Data setup time to falling edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data hold time from falling edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
T_{ERASEB}	Flash erase time (block)	–	10	–	ms	
T_{WRITE}	Flash block write time	–	80	–	ms	
T_{DSCLK3}	Data out delay from falling edge of SCLK	–	–	50	ns	3.0 ≤ V_{DD} ≤ 3.6
T_{DSCLK2}	Data out delay from falling edge of SCLK	–	–	70	ns	2.4 ≤ V_{DD} ≤ 3.0
$T_{ERASEALL}$	Flash erase time (Bulk)	–	20	–	ms	Erase all blocks and protection fields at once.
$T_{PROGRAM_HOT}$	Flash block erase + flash block write time	–	–	180[19]	ms	0 °C ≤ T_J ≤ 100 °C
$T_{PROGRAM_COLD}$	Flash block erase + flash block write time	–	–	360[19]	ms	–40 °C ≤ T_J ≤ 0 °C

AC I^2C Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 34. AC Characteristics of the I^2C SDA and SCL Pins for Vcc ≥ 3.0 V

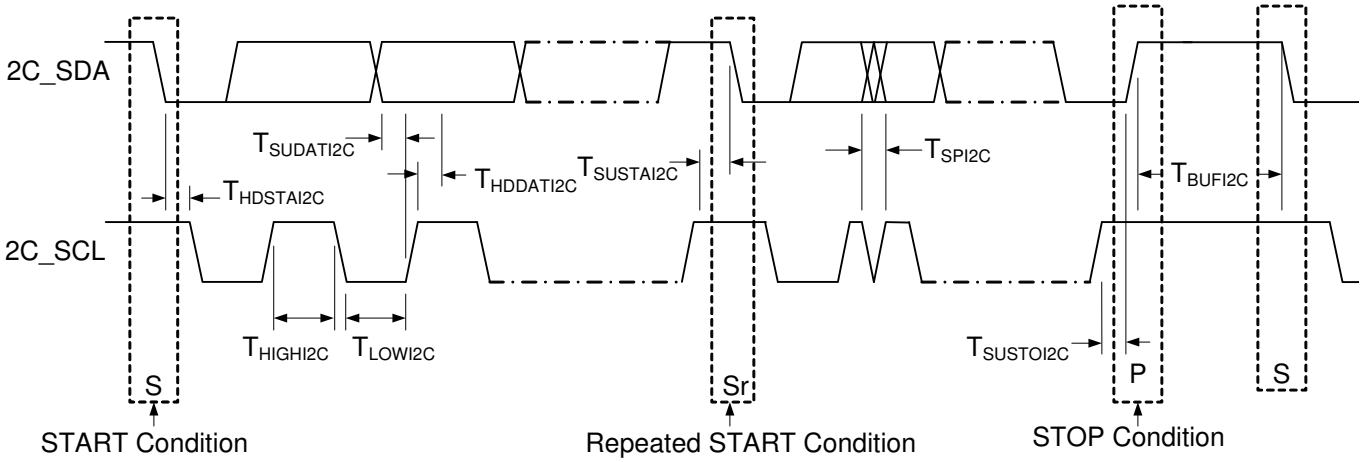
Symbol	Description	Standard-Mode		Fast-Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz	
$T_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	
T_{LOWI2C}	LOW period of the SCL Clock	4.7	–	1.3	–	µs	
$T_{HIGHI2C}$	HIGH period of the SCL Clock	4.0	–	0.6	–	µs	
$T_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs	
$T_{HDDATI2C}$	Data hold time	0	–	0	–	µs	
$T_{SUDATI2C}$	Data setup time	250	–	100[20]	–	ns	
$T_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	µs	
T_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs	
T_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	0	50	ns	

Note
19. For the full industrial range, you must employ a Temperature Sensor User Module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the flash APIs Application Note AN2015 - PSoC® 1 - Reading and Writing PSoC Flash.

Table 35. 2.7-V AC Characteristics of the I²C SDA and SCL Pins (Fast-Mode not Supported)

Symbol	Description	Standard-Mode		Fast-Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL clock frequency	0	100	–	–	kHz	
$T_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	–	–	µs	
T_{LOWI2C}	LOW period of the SCL Clock	4.7	–	–	–	µs	
$T_{HIGHI2C}$	HIGH period of the SCL Clock	4.0	–	–	–	µs	
$T_{SUSTAI2C}$	Setup Time for a repeated START condition	4.7	–	–	–	µs	
$T_{HDDATI2C}$	Data hold time	0	–	–	–	µs	
$T_{SUDATI2C}$	Data setup time	250	–	–	–	ns	
$T_{SUSTOI2C}$	Setup Time for STOP Condition	4.0	–	–	–	µs	
T_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	–	–	µs	
T_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	–	–	ns	

Figure 9. Definition for Timing for Fast-/Standard-Mode on the I²C Bus



Note

20. A Fast-Mode I²C-bus device can be used in a Standard-Mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

Packaging Information

This section illustrates the packaging specifications for the CY8CLED02 EZ-Color device, along with the thermal impedances for each package and minimum solder reflow peak temperature.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

Figure 10. 8-Pin (150-Mil) SOIC

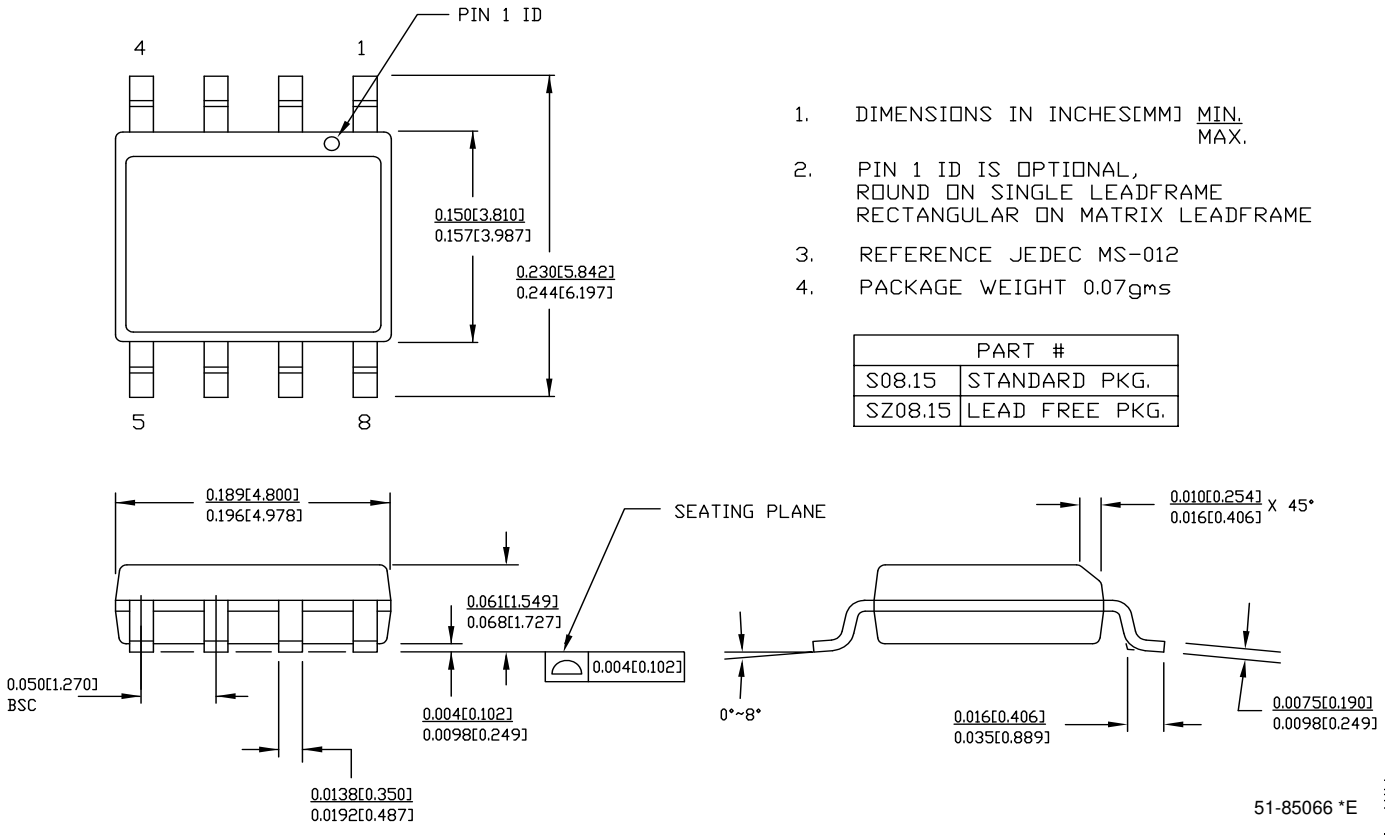


Figure 11. 16-Pin (150-Mil) SOIC

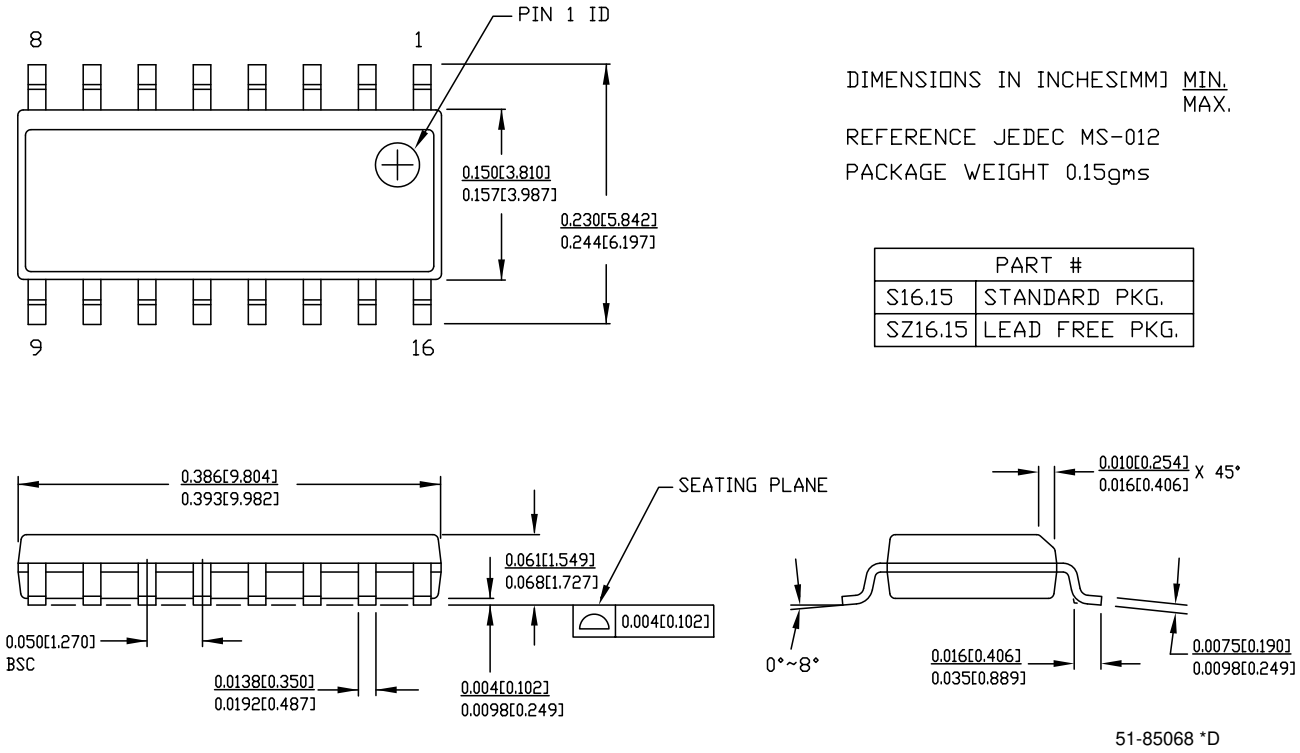
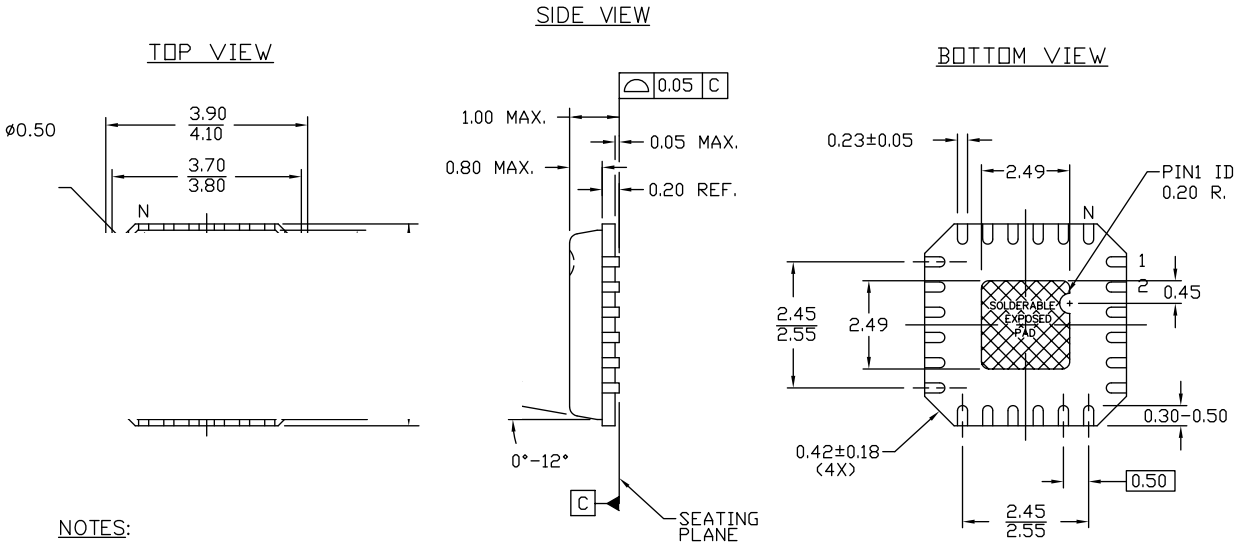


Figure 12. 24-Pin (4x4) QFN



NOTES:

1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.042g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LF24A	STANDARD
LY24A	LEAD FREE

51-85203 *C

Important Note

- For information on the preferred dimensions for mounting QFN packages, see the following Application Note at *Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages* available at http://www.amkor.com.
- Pinned vias for thermal conduction are not required for the low-power device.

Thermal Impedances

Table 36. Thermal Impedances per Package

Package	Typical θ_{JA}[21]
8-pin SOIC	186 °C/W
16-pin SOIC	125 °C/W
24-pin QFN[22]	40 °C/W

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 37. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Time at Maximum Temperature
8-pin SOIC	260 °C	30 s
16-pin SOIC	260 °C	30 s
24-pin QFN	260 °C	30 s

Notes
21. $T_J = T_A + POWER \times \theta_{JA}$
22. To achieve the thermal impedance specified for the QFN package, refer to *Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages* available at http://www.amkor.com.

Development Tool Selection

This section presents the development tools available for all current PSoC based devices including the CY8CLED02 EZ-Color family.

Software Tools

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of charge at http://www.cypress.com and includes a free C compiler.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube in-circuit emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com.

Hardware Tools

In-Circuit Emulator

A low cost, high functionality in-circuit emulator (ICE)) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of the USB port. The base unit is universal and will operate with all PSoC based devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the device on the target board and performs full speed (24 MHz) operation.

I^2C to USB Bridge

The I^2C to USB Bridge is a quick and easy link from any design or application's I^2C bus to a PC via USB for design testing, debugging and communication.

Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit allows you to program PSoC based devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg programming unit
- MiniEval socket programming and evaluation board
- 28-Pin CY8C29466-24PXI PDIP PSoC device sample
- 28-Pin CY8C27443-24PXI PDIP PSoC device sample
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation board with LCD module
- MiniProg programming unit
- 28-Pin CY8C29466-24PXI PDIP PSoC device sample (2)
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

Device Programmers

All device programmers are sold at the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular programmer base
- Three programming module cards
- MiniProg Programming Unit
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.
Note CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 programmer unit
- PSoC ISSP software CD
- 110 ~ 240 V power supply, Euro-Plug adapter
- USB 2.0 cable

Accessories (Emulation and Programming)

Table 38. Emulation and Programming Accessories

Part #	Pin Package	Flex-Pod Kit[23]	Foot Kit[24]	Adapter[25]
CY8CLED02-16SXI	16-pin SOIC	CY3250-LED02	CY3250-16SOIC-FK	Adapters can be found at http://www.emulation.com.
CY8CLED02-24LFXI	24-pin QFN	CY3250-LED02QFN	CY3250-24QFN-FK	

Ordering Information

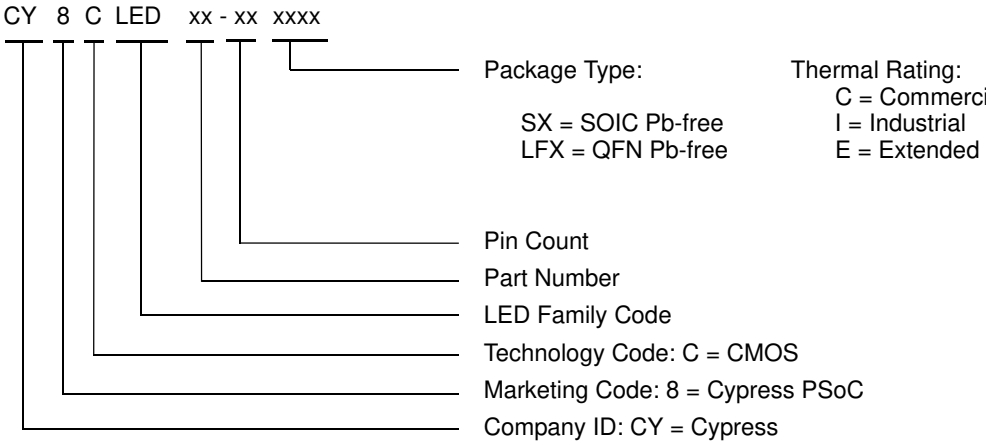
Key Device Features

The following table lists the CY8CLED02 EZ-Color devices' key package features and ordering codes.

Table 39. Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	RAM (Bytes)	Switch Mode Pump	Temperature Range	Digital Blocks	Analog Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
16-Pin (150-Mil) SOIC	CY8CLED02-16SXI	4 K	256	Yes	–40 °C to +85 °C	4	4	12	8	0	No
16-Pin (150-Mil) SOIC (Tape and Reel)	CY8CLED02-16SXIT	4 K	256	Yes	–40 °C to +85 °C	4	4	12	8	0	No
24-Pin (4x4) QFN	CY8CLED02-24LFXI	4 K	256	Yes	–40 °C to +85 °C	4	4	16	8	0	Yes
24-Pin (4x4) QFN (Tape and Reel)	CY8CLED02-24LFXIT	4 K	256	Yes	–40 °C to +85 °C	4	4	16	8	0	Yes

Ordering Code Definitions



Notes
23. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
24. Foot kit includes surface mount feet that can be soldered to the target PCB.
25. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com.

Acronyms

Table 40 lists the acronyms that are used in this document.

Table 40. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	LPC	low power comparator
ADC	analog-to-digital converter	MIPS	million instructions per second
API	application programming interface	PCB	printed circuit board
CMOS	complementary metal oxide semiconductor	PDIP	plastic dual-in-line package
CPU	central processing unit	POR	power-on reset
CRC	cyclic redundancy check	PPOR	precision power on reset
CT	continuous time	PRS	pseudo-random sequence
DAC	digital-to-analog converter	PSoC®	Programmable System-on-Chip
DC	direct current	PWM	pulse-width modulator
EEPROM	electrically erasable programmable read-only memory	QFN	quad flat no leads
GPIO	general purpose I/O	SC	switched capacitor
I/O	input/output	SRAM	static random access memory
ICE	in-circuit emulator	SLIMO	slow IMO
IDE	integrated development environment	SMP	switch mode pump
ILO	internal low speed oscillator	SOIC	small-outline integrated circuit
IMO	internal main oscillator	SPI™	serial peripheral interface
IrDA	infrared data association	SROM	supervisory read only memory
ISSP	in-system serial programming	UART	universal asynchronous receiver / transmitter
LCD	liquid crystal display	USB	universal serial bus
LED	light-emitting diode	XRES	external reset
LVD	low-voltage detect	WDT	watchdog timer

Reference Documents

Design Aids – Reading and Writing PSoC® Flash – AN2015 (001-40459)

Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 (001-14503)

Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages – available at http://www.amkor.com.

Document Conventions

Units of Measure

Table 41 lists the units of measure.

Table 41. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	µs	microsecond
dB	decibels	µH	micro henry
kHz	kilohertz	ps	picosecond
kΩ	kilo ohm	mV	millivolt
mA	milliampere	V	volt
mH	millihenry	%	percent
MHz	megahertz	µV	microvolt
nA	nano ampere	W	watt
pA	pico ampere	mm	millimeter
pF	picofarad	ns	nanosecond
µA	microampere	mVpp	millivolts peak-to-peak
µF	microfarad	ms	millisecond

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

Glossary

active high	1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are switched capacitor (SC) and continuous time (CT) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
Application programming interface (API)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.

Glossary (continued)

bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.
block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows you to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.

Glossary (continued)

digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.
duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.
External Reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
Flash	An electrically programmable and erasable, non-volatile technology that provides you the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is OFF.
Flash block	The smallest amount of flash ROM space that may be programmed at one time and the smallest amount of flash space that may be protected. A flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I^2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I^2C uses only two bi-directional pins, clock and data, both running at +5 V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows you to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls lower than a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the flash, SRAM, and register space.

Glossary (continued)

master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the *slave device*.
microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.
modulator	A device that imposes a signal on a carrier.
noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
Phase-locked loop (PLL)	An electronic circuit that controls an ***oscillator*** so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
Power-on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is lower than a pre-set level. This is one type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse-width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.

Glossary (continued)

serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.
shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform flash operations. The functions of the SROM may be accessed in normal user code, operating from flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level *API* for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning "voltage source." The most negative power supply signal.
Watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

Document History Page

Document Title: CY8CLED02 EZ-Color™ HB LED Controller Document Number: 001-13704				
Revision	**ECN #**	**Submission Date**	**Origin of Change**	**Description of Change**
**	1383443	See ECN	SFVTMP3/AESA	New document
*A	2732564	07/09/2009	CGX	Converted from Preliminary to Final
*B	2794355	10/28/2009	XBM	Added "Contents" on page 2 Updated "Development Tools" on page 6. Corrected FCPU1 and FCPU2 parameters in Table 21, "5-V and 3.3-V AC Chip-Level Specifications," on page 22 and Table 22, "2.7-V AC Chip-Level Specifications," on page 23
*C	2850593	01/14/2010	FRE	Updated DC GPIO, AC Chip-Level, and AC Programming Specifications as follows: Modified FIMO6 and TWRITE specifications. Replaced TRAMP (time) specification with SRPOWER_UP (slew rate) specification. Added note to Flash Endurance specification. Added IOH, IOL, DCILO, F32K_U, TPOWERUP, TERASEALL, TPROGRAM_HOT, and TPROGRAM_COLD specifications. Corrected the Pod Kit part numbers. Updated Development Tool Selection. Updated copyright and Sales, Solutions, and Legal Information URLs. Updated 24-Pin QFN package diagram.
*D	2903043	04/01/2010	NJF	Updated Cypress website links Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters Updated package diagrams Removed sections "Third Party Tools" and "Build a PSoC Emulator"
*E	3111554	12/15/10	NJF	Added DC I^2C Specifications table. Added F_{32K_U} max limit. Added Tjit_IMO specification, removed existing jitter specifications. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications. No specific changes were made to AC Digital Block Specifications table and I^2C Timing Diagram. They were updated for clearer understanding.
*F	3283843	07/13/11	DIVA	Updated Getting Started, Development Tools, and Designing with PSoC Designer. Removed obsolete kits. Removed reference to obsolete spec AN2012.
*G	3403622	10/12/11	MKKU	Removed the following pruned parts from the Ordering Information and Accessories (Emulation and Programming) sections. CY8CLED02-8SXI CY8CLED02-8SXIT

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