4 CHANNEL LOW CAPACITANCE TVS DIODE ARRAY

Product Summary

$V_{BR\ (MIN)}$	$I_{PP\ (MAX)}$	$C_{T\ (TYP)}$
5.5V	5	0.5pF

Description

The D3V3F4U10LP is a high-performance device suitable for protecting four high speed I/Os. These devices are assembled in U-DFN2510-10 packages and have high ESD surge capability, low ESD clamping voltage and Ultra-low capacitance.

Applications

Typically used at high-speed ports such as USB 3.0, USB 3.1, Serial ATA, Display port.

Features

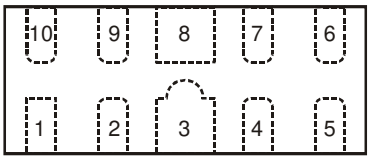
- Clamping Voltage: 5V at 16A IEC6100-4-2
- IEC61000-4-2 (ESD): Air — ±12kV, Contact — ±12kV
- IEC61000-4-5 (Lightning): 5A (8/20μs)
- 4 Channels of ESD Protection
- Ultra-Low Channel Input Capacitance of 0.5pF Typical
- TLP Dynamic Resistance: 0.25Ω
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Mechanical Data

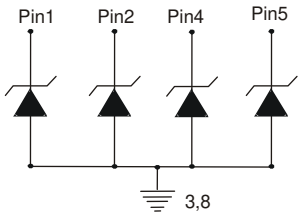
- Case: U-DFN2510-10
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: NiPdAu over Copper Leadframe (Lead Free Plating). Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.038 grams (Approximate)

U-DFN2510-10

Pin #	Description
1, 2, 4, 5	I/O
6, 7, 9, 10	No Connection
3, 8	Vss



Pin Description (Top View)



Device Schematic

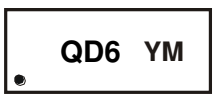
Ordering Information (Note 4)

Product	Compliance	Marking	Reel Size (inches)	Tape Width (mm)	Quantity per Reel
D3V3F4U10LP-7	Standard	QD6	7	8	3,000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information

U-DFN2510-10



QD6 = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: E = 2017)
M = Month (ex: 9 = September)

Date Code Key

Year	2015	2016	2017	2018	2019	2020
Code	C	D	E	F	G	H

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

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Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	Condition
Peak Pulse Current, per IEC61000-4-5	I_{PP}	5	A	I/O to V_{SS}, 8/20µs
Peak Pulse Power, per IEC61000-4-5	P_{PP}	30	W	I/O to V_{SS}, 8/20µs
ESD Protection – Contact Discharge, per IEC61000-4-2	$V_{ESD_CONTACT}$	±12	kV	I/O to V_{SS}
ESD Protection – Air Discharge, per IEC61000-4-2	V_{ESD_AIR}	±12	kV	I/O to V_{SS}

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation Typical (Note 5)	P_D	350	mW
Thermal Resistance, Junction to Ambient Typical (Note 5)	$R_{\theta JA}$	360	°C/W
Operating and Storage Temperature Range	T_J,T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	V_{RWM}	—	—	3.3	V	—
Reverse Current	I_R	—	—	1.0	µA	V_R = 3.3V, I/O to V_{SS}
Reverse Breakdown Voltage	V_{BR}	5.5	6.2	—	V	I_R = 1mA, I/O to V_{SS}
Forward Clamping Voltage	V_F	-1.0	-0.85	—	V	I_F = -15mA, I/O to V_{SS}
Holding Reverse Voltage	V_{HOLD}	—	1.3	—	V	I/O to V_{SS}
Reverse Clamping Voltage (Note 6)	V_C	—	3.5	—	V	I_{PP} = 5A, I/O to V_{SS}, 8/20µs
Clamping Voltage (Note 7)	V_C	—	5	—	V	TLP, 16A, t_P = 100ns, I/O to V_{SS}
Clamping Voltage (Note 7)	V_C	—	5	—	V	TLP, -16A, t_P = 100ns, I/O to V_{SS}
Dynamic Reverse Resistance	R_{DIF-R}	—	0.25	—	Ω	TLP, 10A, t_P = 100ns, I/O to V_{SS}
Dynamic Forward Resistance	R_{DIF-F}	—	0.2	—	Ω	TLP, 10A, t_P = 100ns, V_{SS} to I/O
Channel Input Capacitance	$C_{I/O}$	—	0.5	—	pF	$V_{I/O}$ = 0V, V_{SS} = 0V, f = 1MHz

Notes: 5. Device mounted on FR-4 PCB pad layout (2oz copper) as shown on Diodes Incorporated's suggested pad layout, which can be found on our website at http://www.diodes.com/package-outlines.html.

6. Clamping voltage value is based on an 8x20µs peak pulse current (I_{PP}) waveform.

7. Clamping voltage value is based on a TLP model. TLP conditions: Z_O=50Ω, t_P = 100ns, t_P = 1ns, averageing window; t1=70ns to t2=90ns.

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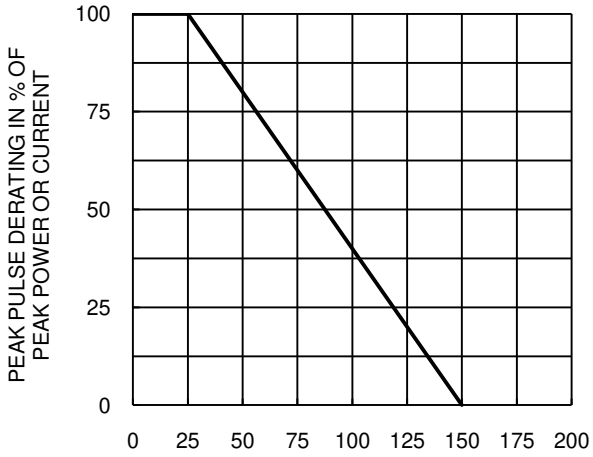


Figure 1. Pulse Derating Curve

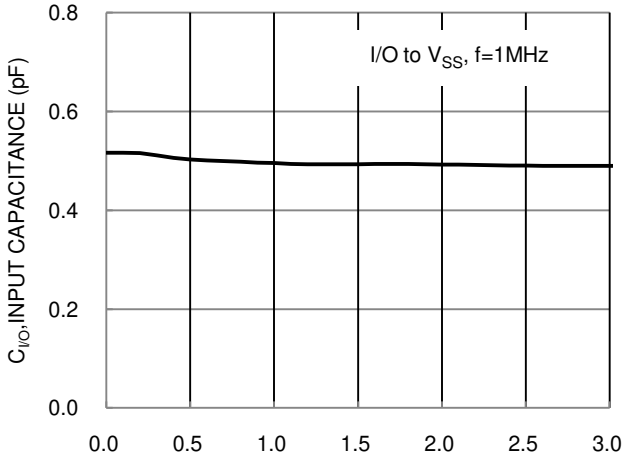


Figure 2. Input Capacitance vs. Input Voltage

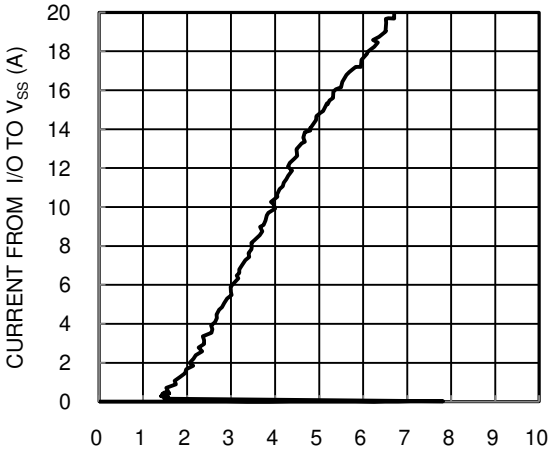


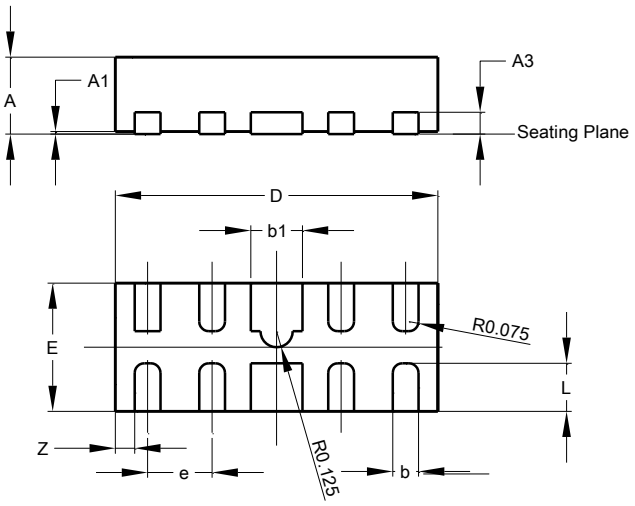
Figure 3. Current vs. Voltage

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Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

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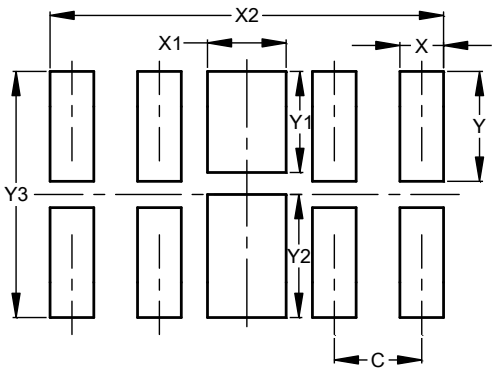


U-DFN2510-10			
Dim	**Min**	**Max**	**Typ**
A	0.545	0.605	0.575
A1	0.00	0.05	0.03
A3	-	-	0.13
b	0.15	0.25	0.20
b1	035	0.45	0.40
D	2.450	2.575	2.500
e	-	-	0.50
E	0.950	1.075	1.000
L	0.325	0.425	0.375
Z	-	-	0.150
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2510-10



Dimensions	Value (in mm)
C	0.500
X	0.250
X1	0.450
X2	2.250
Y	0.625
Y1	0.575
Y2	0.700
Y3	1.400

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