DAC1653D/DAC1658D

Dual 16-bit DAC: 10 Gbps JESD204B interface: x2, x4 and x8 interpolating

Datasheet
Revision 2.41

1. General description

DAC1653D and DAC1658D are high-speed, high-performance 16-bit dual channel Digital-to-Analog Converters (DACs). The devices provide sample rates up to 2 Gsps with selectable ×2, ×4 and ×8 interpolation filters optimized for multi-carrier and broadband wireless transmitters.

When both devices are referred to in this data sheet, the following convention will be used: DAC165xD.

The DAC165xD integrates a JEDEC JESD204B compatible high-speed serial input data interface running up to 10 Gbps allowing dual channel input sampling at up to 1 Gsps over four differential lanes. It offers numerous advantages over traditional parallel digital interfaces:

- Easier Printed-Circuit Board (PCB) layout
- Lower radiated noise
- Lower pin count
- Self-synchronous link
- Skew compensation
- Deterministic latency
- Multiple Device Synchronization (MDS); JESD204B subclass 1 compatible
- Harmonic clocking support
- Assured FPGA interoperability

There are two versions of the DAC165xD:

- Low common-mode output voltage (part identification DAC1653D)
- High common-mode output voltage (part identification DAC1658D)

An optional on-chip digital modulator converts the complex I/Q pattern from baseband to IF. The mixer frequency is set by writing to the Serial Peripheral Interface (SPI) control registers associated with the on-chip 40-bit Numerically Controlled Oscillator (NCO). This accurately places the IF carrier in the frequency domain. The 13-bit phase adjustment feature, the 12-bit digital gain and the 16-bit digital offset enable full control of the analog output signals.

The DAC165xD is fully compatible with device subclass 1 of the JEDEC JESD204B standard, guaranteeing deterministic and repeatable interface latency using the differential SYSREF signal. The device also supports harmonic clocking to reduce system-level clock synthesis and distribution challenges.

Multiple Device Synchronization (MDS) enables multiple DAC channels to be sample synchronous and phase coherent to within one DAC clock period. MDS is ideal for LTE and LTE-A MIMO transceiver applications.

The DAC165xD includes a ×2, ×4 or ×8 divider to achieve the best possible noise performance at the analog outputs, allowing harmonic clocking through the system. The internal regulator adjusts the full-scale output current between 10 mA and 30 mA.

The device is available in a VFQFP-N 56 package (8 mm × 8 mm).

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2. Features and benefits

- Dual channel 16-bit resolution
- 2.0 GSps maximum output update rate
- JEDEC JESD204B device subclass I compatible: SYSREF based deterministic and repeatable interface latency
- Multiple device synchronization enables multiple DAC channels to be sample synchronous and phase coherent to within one DAC clock period
- 1, 2 or 4 configurable JESD204B serial input lanes running up to 10 Gbps with embedded termination and programmable equalization gain (CTLE)
- 1 Gsps maximum baseband input data rate
- SPI interface (3-wire or 4-wire mode) for control setting and status monitoring
- Differential scalable output current from 10 mA to 30 mA
- Embedded NCO with 40-bit programmable frequency and 16-bit phase adjustment
- Embedded complex (IQ) digital modulator
- 1.2 V and 3.3 V power supplies (for DAC1653D series, the 3.3V supply voltage can be lowered to 2.7V for lower power consumption)
- Flexible SPI power supply (1.8 V or 1.2 V) ensuring compatibility with on-board SPI bus
- Flexible differential SYNC signals power supply (1.8 V or 1.2 V) ensuring compatibility with on-board devices
- Embedded Temperature Sensor
- Configurable IOs pins for monitoring, interrupt
- XBERT features (PRBS31, 23, 15, 7, JTSPAT, STLTP)
- $SFDR_{RBW}$ = 88 dBc typical (f_s = 1.50 Gsps; interpolation ×2; bandwidth = 250 MHz; f_{out} = 150 MHz)
- NSD = −167 dBc/Hz typical (f_o = 70 MHz)
- IMD3 = 85 dBc typical (f_s = 1.50 Gsps; interpolation ×2; f_{o1} = 152 MHz; f_{o2} = 155.1 MHz)
- Four carriers ACLR = 76 dB typical (f_s = 1.50 Gsps; f_{NCO} = 350 MHz)
- RF enable/disable pin and RF automatic mute
- Clock divider by 2, 4, 6 and 8 available at the input of the clock path
- Group delay compensation
- Analog offset control (10-bit auxiliary DACs)
- Power-down mode controls
- On-chip 0.7 V reference
- Industrial temperature range −40 °C to +85 °C
- Low (DAC1653D) or high (DAC1658D) common-mode output voltage
- VFQFP-N 56 package (8 mm × 8 mm)
- Embedded Power On Reset
- Lane swapping and polarity swapping
- Signal Power Detector, IQ-Range detector, Level detectors with Auto-Mute feature

3. Applications

- Wireless infrastructure radio base station transceivers, including: LTE-A, LTE, MC-GSM, W-CDMA, TD-SCDMA
- LMDS/MMDS, point-to-point microwave backhaul
- Direct Digital Synthesis (DDS) instruments
- High-definition video broadcast production equipment
- Automated Test Equipment (ATE)

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4. ORDERING INFORMATION

Table 1. Ordering information

Type number	Package			
	Name	Description	Shipping Packaging	Version
DAC1653D2G0NLGA8	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	Tape & Reel	PSC-4110
DAC1653D1G5NLGA8	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	Tape & Reel	PSC-4110
DAC1653D1G0NLGA8	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	Tape & Reel	PSC-4110
DAC1658D2G0NLGA8	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	Tape & Reel	PSC-4110
DAC1658D1G5NLGA8	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	Tape & Reel	PSC-4110
DAC1658D1G0NLGA8	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	Tape & Reel	PSC-4110
DAC1653D2G0NLGA	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	Tray	PSC-4110
DAC1653D1G5NLGA	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	Tray	PSC-4110
DAC1653D1G0NLGA	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	Tray	PSC-4110
DAC1658D2G0NLGA	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	Tray	PSC-4110
DAC1658D1G5NLGA	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	Tray	PSC-4110
DAC1658D1G0NLGA	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	Tray	PSC-4110

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5. BLOCK DIAGRAM

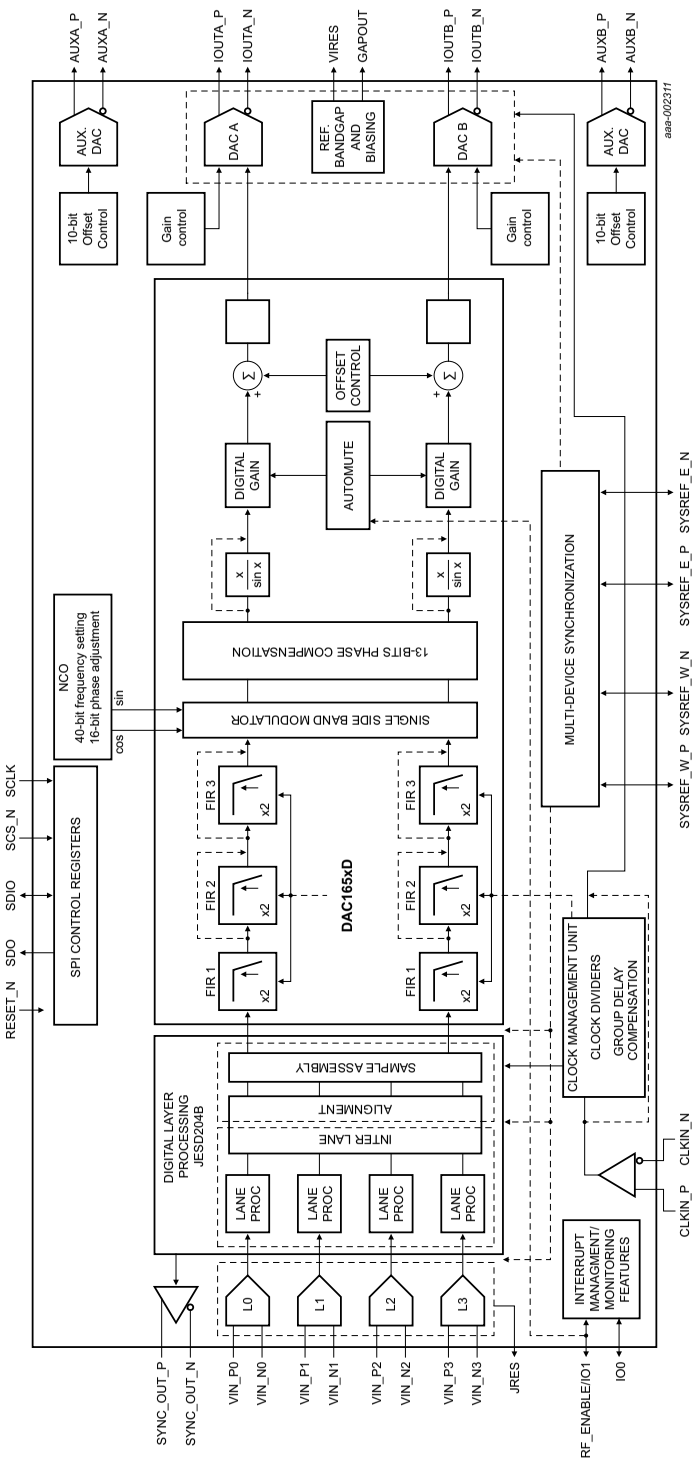


Fig 1. Block diagram

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6. PINNING INFORMATION

6.1 Pinning

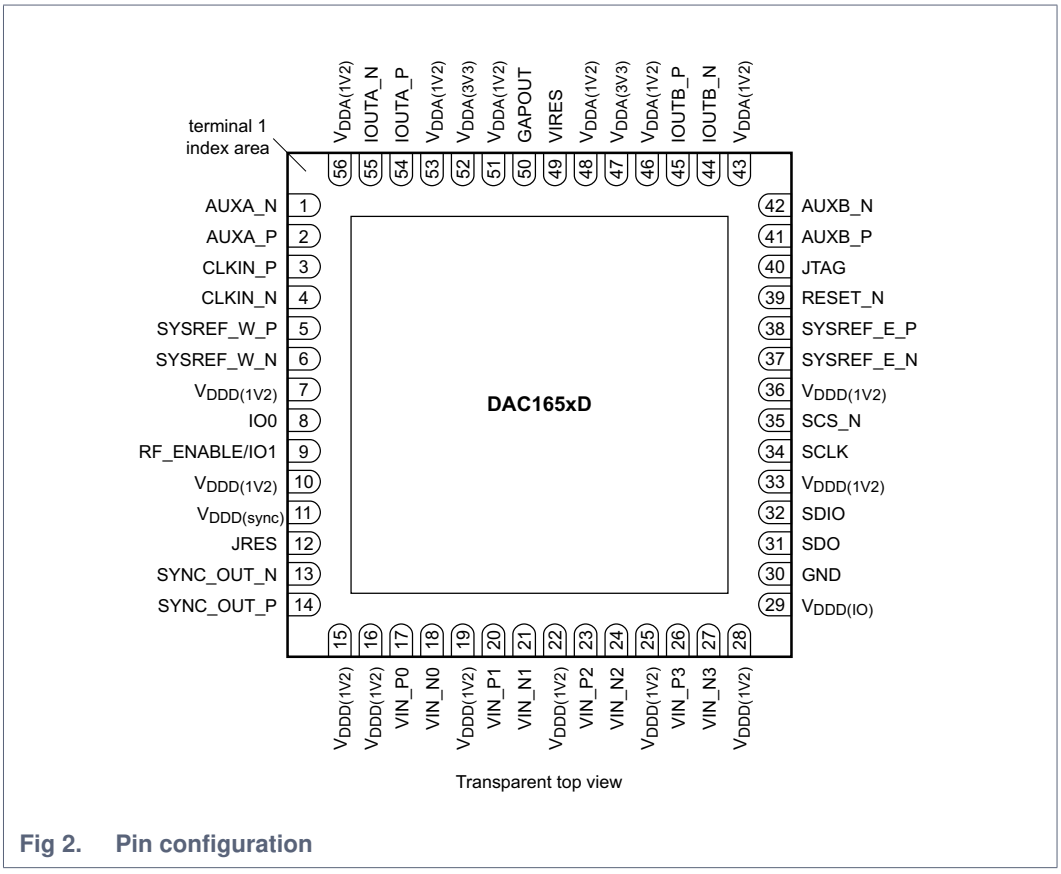


Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Description
AUXA_N	1	O	complementary auxiliary DAC A output current
AUXA_P	2	O	auxiliary DAC A output current
CLKIN_P	3	I	DAC clock positive input
CLKIN_N	4	I	DAC clock negative input
SYSREF_W_P	5	I/O	multiple device synchronization positive signal, west side (if not used, keep it floating)
SYSREF_W_N	6	I/O	multiple device synchronization negative signal, west side (if not used, keep it floating)
$V_{DDD(1V2)}$	7	P	1.2 V digital power supply
IO0	8	I/O	IO port bit 0
RF_ENABLE/IO1	9	I/O	IO port bit 1 or RF enable pin (see Section automute)
$V_{DDD(1V2)}$	10	P	1.2 V digital power supply
$V_{DDD(sync)}$	11	P	flexible power supply for SYNC differential signals (1.2 V to 1.8 V; see Section 11.2.1.1)
JRES	12	I/O	calibration resistor (6.98 kΩ 1%) for serial lanes termination
SYNC_OUT_N	13	O	synchronization request to transmitter, complementary output

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Table 2. Pin description *…continued*

Symbol	Pin	Type[1]	Description
SYNC_OUT_P	14	O	synchronization request to transmitter
$V_{DDD(1V2)}$	15	P	1.2 V digital power supply for JESD204B interface
$V_{DDD(1V2)}$	16	P	1.2 V digital power supply for JESD204B Lane 0
VIN_P0	17	I[2]	serial interface lane 0 positive input (AC coupling recommended)
VIN_N0	18	I[2]	serial interface lane 0 negative input (AC coupling recommended)
$V_{DDD(1V2)}$	19	P	1.2 V digital power supply for JESD204B Lane 0 and Lane 1
VIN_P1	20	I[2]	lane 1 serial interface positive input (AC coupling recommended)
VIN_N1	21	I[2]	serial interface lane 1 negative input (AC coupling recommended)
$V_{DDD(1V2)}$	22	P	1.2 V digital power supply for JESD204B Lane 1 and Lane 2
VIN_P2	23	I[2]	serial interface lane 2 positive input (AC coupling recommended)
VIN_N2	24	I[2]	serial interface lane 2 negative input (AC coupling recommended)
$V_{DDD(1V2)}$	25	P	1.2 V digital power supply for JESD204B Lane 2 and Lane 3
VIN_P3	26	I[2]	serial interface lane 3 positive input (AC coupling recommended)
VIN_N3	27	I[2]	serial interface lane 3 negative input (AC coupling recommended)
$V_{DDD(1V2)}$	28	P	1.2 V digital power supply for JESD204B Lane 3
$V_{DDD(IO)}$	29	P	flexible power supply for SPI IOs and IO0/IO1 signals (1.2 V to 1.8 V; see Section 11.2.1)
GND	30	G	connect to ground
SDO	31	O	SPI data output
SDIO	32	I/O	SPI data input/output
$V_{DDD(1V2)}$	33	P	1.2 V digital power supply
SCLK	34	I	SPI clock
SCS_N	35	I	SPI chip select (active LOW)
$V_{DDD(1V2)}$	36	P	1.2 V digital power supply
SYSREF_E_N	37	I/O	multiple device synchronization negative signal, east side (if unused, leave it floating)
SYSREF_E_P	38	I/O	multiple device synchronization positive signal, east side (if unused, leave it floating)
RESET_N	39	I	general reset (active LOW)
JTAG	40	G	JTAG connection (connect to ground)
AUXB_P	41	O	auxiliary DAC B output current
AUXB_N	42	O	complementary auxiliary DAC B output current
$V_{DDA(1V2)}$	43	P	1.2 V analog power supply
IOUTB_N	44	O	complementary DAC B output current
IOUTB_P	45	O	DAC B output current
$V_{DDA(1V2)}$	46	P	1.2 V analog power supply
$V_{DDA(3V3)}$	47	P	DAC1658D: 3.3 V analog power supply
			DAC1653D: 2.5 V to 3.3 V analog power supply
$V_{DDA(1V2)}$	48	P	1.2 V analog power supply
VIRES	49	I/O	DAC biasing resistor (562 Ω 1%)
GAPOUT	50	I/O	band gap input/output voltage
$V_{DDA(1V2)}$	51	P	1.2 V analog power supply
$V_{DDA(3V3)}$	52	P	DAC1658D: 3.3 V analog power supply
			DAC1653D: 2.5 V to 3.3 V analog power supply

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Table 2. Pin description *…continued*

Symbol	Pin	Type[1]	Description
$V_{DDA(1V2)}$	53	P	1.2 V analog power supply
IOUTA_P	54	O	DAC A output current
IOUTA_N	55	O	complementary DAC A output current
$V_{DDA(1V2)}$	56	P	1.2 V analog power supply

[1] P: power supply; G: ground; I: input; O: output.

[2] JESD204B input lanes can be swapped between P and N using dedicated registers. The order of lanes can be updated logically (see Section 11.8.5.3).

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7. LIMITING VALUES

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DDA(3V3)}$	analog supply voltage		–0.5	+4.6	V
$V_{DDD(1V2)}$	digital supply voltage		–0.5	+1.5	V
$V_{DDA(1V2)}$	analog supply voltage		–0.5	+1.5	V
V_I	input voltage	pins VIN_Px; VIN_Nx, VIRES, GAPOUT; referenced to 1V2	–0.5	+1.5	V
	input voltage for clocks and SYSREF pins	pins CLK_P,CLK_N, SYSREF_W_P; SYSREF_W_N, SYSREF_E_P;SYSREF_E_N;	–0.5	1.95	V
V_O	output voltage	pins IOUTA_P; IOUTA_N; IOUTB_P; IOUTB_N; AUXA_P; AUXA_N; AUXB_P and AUXB_N; referenced to GND	–0.5	+4.6	V
$V_{DDD(IO)}$	I/O digital supply voltage	pins SDO; SDIO; SCLK; SCS_N; RESET_N; JTAG; IO0; RF_ENABLE/IO1	–0.5	2.1	V
$V_{DDD(sync)}$	digital supply voltage for differential output buffers	pins SYNC_OUT_P; SYNC_OUT_N,	–0.5	2.1	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
T_j	junction temperature		–40	+125	°C

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8. THERMAL CHARACTERISTICS

Table 4. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
JEDEC 4L board					
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	23.6	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		[1]	13.7	K/W
$R_{th(j-b)}$	thermal resistance from junction to bottom case		[1]	0.9	K/W
JEDEC compliance board with additional layers count					
$R_{th(j-a)}$	thermal resistance from junction to ambient	6 layers	[2]	17.5	K/W
		8 layers	[2]	17.4	K/W
		12 layers	[2]	15.5	K/W

[1] In compliance with JEDEC test board; in free air with 64 thermal vias, class 5

[2] In free air with 64 thermal vias, class 5

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9. STATIC CHARACTERISTICS

9.1 Common characteristics

The DAC165xD requires supplies of both 3.3 V and 1.2 V or 1.3 V for DAC sample rate above 1.8 Gsps. The 1.2 V supply has separate digital and analog power supply pins. The SPI power supply is flexible. It can be set from1.2 V to1.8 V (see Section 11.2.1.1).

Table 5. Common characteristics

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; no inverse sin(x)/x; no output correction; output signal = 1 $V_{pp,diff}$; unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
Voltages							
$V_{DDA(3V3)}$	analog supply voltage	DAC1658D: high common mode output	C	3.15	3.3	3.45	V
		DAC1653D: low common mode output	C	2.7[2]	3.3	3.45	V
$V_{DDD(1V2)}$	digital supply voltage		C	1.14[3]	1.2	1.26	V
$V_{DDA(1V2)}$	analog supply voltage		C	1.14	1.2	1.26	V
$V_{DDD(IO)}$	I/O digital supply voltage		C	1.14	1.2	1.9	V
$V_{DDD(sync)}$	digital supply voltage for differential SYNC output buffers		C	1.14	1.2	1.9	V
Clock inputs (pins CLKIN_P, CLKIN_N)							
$V_{i(cm)}$	common-mode input voltage. Internal self-biased. AC-coupling recommended		D	-	800	-	mV
$V_{i(diff)}$	differential Peak-to-Peak voltage		D	400	1000	2000	mV
f_{in}	Input frequency compliance range	direct clocking	D			2000	MHz
		harmonic clocking (using clock divider)	D			3000	MHz
$R_{i(diff)}$	differential input resistor		D	-	100	-	Ω
C_i	input capacitance		D	-	2	-	pF
Digital inputs/outputs (SYSREF_W_P/SYSREF_W_N, SYSREF_E_P/SYSREF_E_N)							
$V_{i(cm)}$	common-mode input voltage	$V_{DDD(IO)}$=1.8V	D	800	1200	1400	mV
		$V_{DDD(IO)}$=1.2V	D	800	950	1100	mV
$V_{i(diff)}$	differential Peak-to-Peak voltage		D	400	800	1000	mV
$R_{i(diff)}$	differential input resistor (could be disconnected see Table 102)		D	-	100	-	Ω
C_i	input capacitance		D	-	0.7	-	pF
Digital inputs (pins SDO, SDIO, SCLK, SCS_N, RESET_N)							
V_{IL}	LOW-level input voltage		C	GND	-	$0.3V_{DDD(IO)}$	V
V_{IH}	HIGH-level input voltage		C	$0.7V_{DDD(IO)}$	-	$V_{DDD(IO)}$	V

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Table 5. Common characteristics *…continued*

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; no inverse sin(x)/x; no output correction; output signal = 1 $V_{pp,diff}$; unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
Digital inputs (VIN_Px/VIN_Nx) compliant with the LV-OIF-11G-SR; CML format							
V_{cm}	common-mode voltage	AC coupling is mandatory	D	0.580	-	1.126	V
$V_{pp-diff}$	differential peak-to-peak voltage	below 8 Gbps	D	80	-	-	mV
		above 8 Gbps	D	110	-	-	mV
Z_{diff}	differential impedance	controlled by SPI register	D	71	100	190	Ω
Hi-Z_{diff}	tri-state observed impendance		D	-	64	-	kΩ
DR	data rate		D	2	-	10	Gbps
Digital outputs (pins SYNC_OUT_P and SYNC_OUT_N)							
V_{cm}	common-mode voltage	controlled by SPI register			-		
		$V_{DDD(sync)}$ = 1.8 V	D	1.0	-	1.7	V
		$V_{DDD(sync)}$ = 1.2 V	I	0.4	-	1.1	V
$V_{O(diff)(swing)}$	swing differential output voltage		I	100	-	1200	mV
Digital outputs (pins SDO, SDIO)							
V_{OL}	LOW-level output voltage		I	-	-	$0.3V_{DDD(IO)}$	V
V_{OH}	HIGH-level output voltage		I	$0.7V_{DDD(IO)}$	-	-	V
Reference voltage output (pin GAPOUT)							
$V_{O(ref)}$	reference output voltage	T_{amb} = 25 °C	I	-	0.70	-	V
Analog auxiliary outputs (pins AUXA_P, AUXA_N, AUXB_P and AUXB_N)							
$I_{O(fs)}$	full-scale output current	normal resolution	I	-	2.3	-	mA
		high resolution	D	-	40	-	µA
$N_{DAC(aux)mono}$	auxiliary DAC monotonicity	guaranteed	D	-	10	-	bits
DAC output timing							
f_s	sampling rate	DAC165xD2G0	C	-[4]	-	2000	Msps
		DAC165xD1G5	C	-[4]	-	1500	Msps
		DAC165xD1G0	C	-[4]	-	1000	Msps
t_s	settling time	t_o = ±0.5LSB	D	-	20	-	ns

[1] D = guaranteed by design; C = guaranteed by characterization; I = industrially tested.

[2] Lower power supply value could be used but the overall DAC performances will be degraded.

[3] For frequencies higher than 1.7Gsps and when using all digital features (NCO, inv sin(x)/x, phase correction, ..) the minimum value is 1.165V

[4] Minimum value is linked to the JESD204B link configuration and lane rate

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9.2 Specific characteristics

Table 6. Currents characteristics

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; no inverse sin(x)/x; no output correction; output signal = 1 V(p-p),diff; unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	DAC165xD			Unit
				Min	Typ	Max	
Currents							
$I_{DDA(3V3)}$ [2]	analog supply current	DAC1658D High Common Mode: all use cases	I	-	64	68	mA
		DAC1653D Low Common Mode: all use cases	I	-	114	122	mA
$I_{DDD(IO)}$ [2]	digital supply current for IO pins	depends on SPI IO0/IO1 activity	I	-	0.5	1	mA
$I_{DDD(sync)}$ [2]	digital supply current for SYNC pins	all use cases	I	-	5	7	mA
$I_{DDD(1V2)}$	digital supply current	NCO off;×2 interpolation; MDS off; invsinc off, phase correction off					
		f_s = 983.04 Msps	C	-	250	285	mA
		f_s = 1474.56 Msps	C	-	330	365	mA
		f_s = 1966.80 Msps	C	-	400	445	mA
$I_{DDA(1V2)}$ [2]	analog supply current	$V_{DDA(1V2)}$ = 1.2 V	I	-	203	220	mA

[1] D = guaranteed by design; C = guaranteed by characterization; I = industrially tested.

[2] Power supply independent of the DAC sampling frequency.

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Table 7. Specific characteristics

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; no inverse sin(x)/x; no output correction; output signal = 1 V(p-p),diff; unless otherwise specified.

Symbol	Parameter	Conditions	Test	DAC1658D: High common-mode			DAC1653D: Low common-mode			Unit
				Min	Typ	Max	Min	Typ	Max	
Power										
P_{tot}	total power dissipation	NCO off;×2 interpolation; MDS off; invsinc off, phase correction off								
		V_{DDA} = 3.3 V; all V_{DDD} = 1.2 V								
		f_s = 983.04 Msps; four JESD204B lanes at 4.9152 Gbps	C	-	761	873	-	932	1059	mW
		f_s = 1474.56 Msps; four JESD204B lanes at 7.3728 Gbps	C	-	857	974	-	1028	1160	mW
		f_s = 1966.80 Msps; four JESD204B lanes at 9.8304 Gbps	C	-	941	1075	-	1112	1261	mW
		NCO on;×2 interpolation; MDS off; invsinc off, phase correction off								
		f_s = 983.04 Msps; four JESD204B lanes at 4.9152 Gbps	C		833	955	-	1004	1141	mW
		f_s = 1474.56 Msps; four JESD204B lanes at 7.3728 Gbps	C		953	1088	-	1124	1273	mW
		f_s = 1966.80 Msps; four JESD204B lanes at 9.8304 Gbps	C		1085	1233	-	1256	1418	mW
		full power-down[2]	C	-	-	5	-	-	5	mW
Analog outputs (pins IOUTA_P, IOUTA_N, IOUTB_P, IOUTB_N)										
$I_{O(fs)}$	full-scale output current		D	10	20	30	10	20	30	mA
$I_{O(cm_offset)}$	additional common current	this additional common current is to be taken into account into filter design and component connection	D	-	1.6	-	-	1.6	-	mA
V_{O_comp}	output voltage compliance range	$V_{DDA(3V3)}$ =3.3 V	D	$V_{DDA(3V3)}$ -1.0	-	$V_{DDA(3V3)}$	0	-	1.0	V
		$V_{DDA(3V3)}$ =2.5 V	D	n.a.	n.a.	n.a.	0	-	0.6	V
R_o	internal output resistance		D	-	250	-	-	250	-	kΩ

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Table 7. Specific characteristics …continued

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; no inverse sin(x)/x; no output correction; output signal = 1 V(p-p),diff; unless otherwise specified.

Symbol	Parameter	Conditions	Test	DAC1658D: High common-mode			DAC1653D: Low common-mode			Unit
				Min	Typ	Max	Min	Typ	Max	
C_{PN}	differential output capacitance		D	-	0.5	-	-	0.5	-	pF
C_P	positive output capacitance		D	-	5.5	-	-	5.5	-	pF
C_N	negative output capacitance		D	-	5.5	-	-	5.5	-	pF

[1] D = guaranteed by design; C = guaranteed by characterization; I = industrially tested.

[2] Full power-down mode is done by setting the following registers: x0043=x01; x0040=xF3 and x0020=x00.

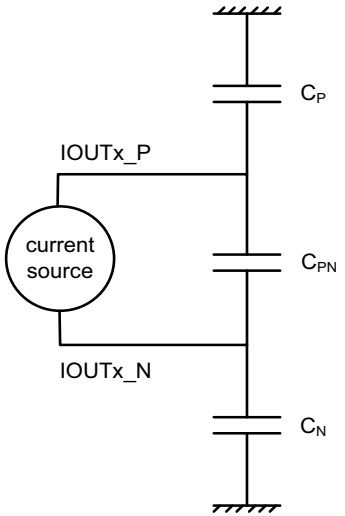


Fig 3. DAC output simplified model

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10. Dynamic characteristics

Table 8. Dynamic characteristics DAC165xD

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; no auxiliary DAC used; no inverse sin(x)/x; no output correction; output signal = 1 V(p-p),diff; output common mode voltage = 2.7 V (DAC1658D) or 0.5 V (DAC1653D); unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	DAC1658D High common-mode			DAC1653D Low common-mode			Unit
			f_s	1 Gsps	1.5 Gsps	2 Gsps	1 Gsps	1.5 Gsps	2 Gsps	
SFDR	spurious-free dynamic range	interpolation x2 BW = f_s / 2 V_{DDA} = 3.3 V; f_o = 20 MHz								
		at −1 dBFS	C	92	91	90	92	91	90	dBc
		at −7 dBFS	C	86	86	87	86	85	85	dBc
		at −14 dBFS	C	80	80	79	80	80	79	dBc
		V_{DDA} = 3.3 V; f_o = 150 MHz								
		at −1 dBFS	I	85	84	83	82	83	81	dBc
		at −7 dBFS	C	83	81	79	80	79	77	dBc
		at −14 dBFS	C	77	76	72	77	75	73	dBc
		V_{DDA} = 3.3 V; f_o = 350 MHz								
		at −1 dBFS	C	67	76	75	66	76	73	dBc
		at −7 dBFS	C	70	76	75	68	75	73	dBc
		at −14 dBFS	C	70	72	70	70	72	70	dBc
IMD3	third-order intermodulation distortion	V_{DDA} = 3.3 V; f_{o1} = 20 MHz; f_{o2} = 21 MHz; −7 dBFS per tone	C	92	92	95	92	92	95	dBc
		V_{DDA} = 3.3 V; f_{o1} = 230 MHz; f_{o2} = 231 MHz; −7 dBFS per tone	C	80	83	87	80	83	87	dBc
ACPR	adjacent channel power ratio	f_o = 40 MHz								
		1 WCDMA carrier; BW = 5 MHz	C	80	80	80	80	80	80	dBc
		4 WCDMA carriers; BW = 20 MHz	C	77	78	77	77	78	77	dBc
		f_o = 350 MHz								
		1 WCDMA carrier; BW = 5 MHz	C	80	80	80	78	79	79	dBc
		4 WCDMA carriers; BW = 20 MHz	C	75	76	75.5	75	76	75	dBc
NSD	noise spectral density	f_o = 70 MHz at −1 dBFS	C		-167			−165		dBc/Hz

[1] D = guaranteed by design; C = guaranteed by characterization; I = industrially tested.

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$V_{DDA(3V3)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; no inverse sin(x)/x; no output correction; input level = -1/-7/-14 dBFS; output signal = 1 V(p-p),diff; output common mode voltage = 2.7 V (DAC1658D) or 0.5 V (DAC1653D); unless otherwise specified.

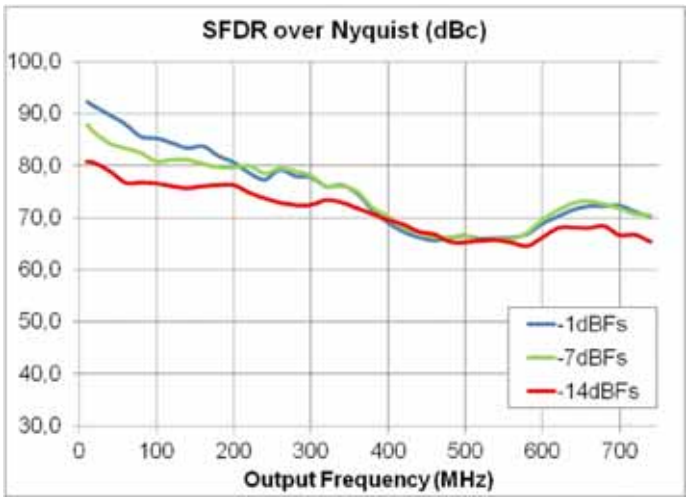


Fig 4. SFDR(dBc) over Nyquist depending of fout (MHz) and input level (dBFS)

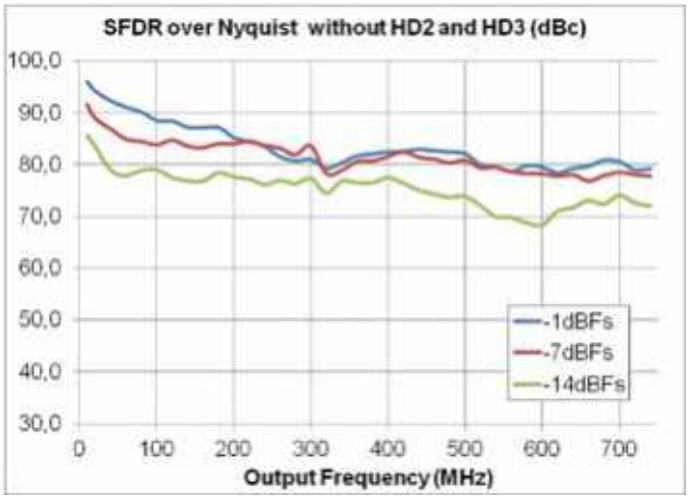


Fig 5. SFDR without HD2 and HD3 (dBc) over Nyquist depending of fout (MHz) and input level (dBFS)

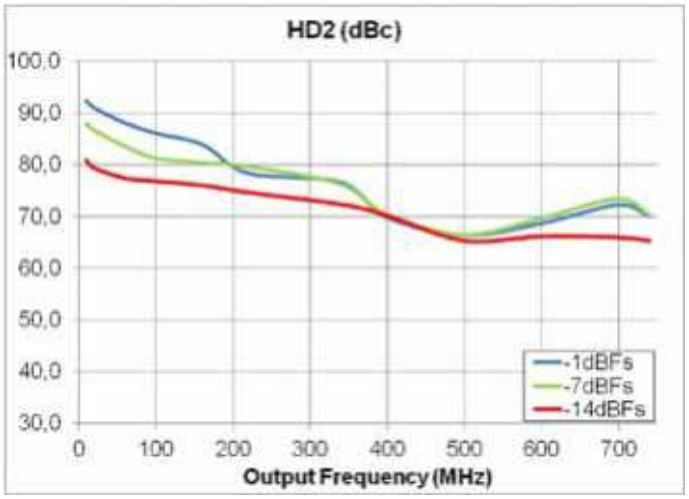


Fig 6. HD2(dBm) over Nyquist depending of fout (MHz) and input level (dBFS)

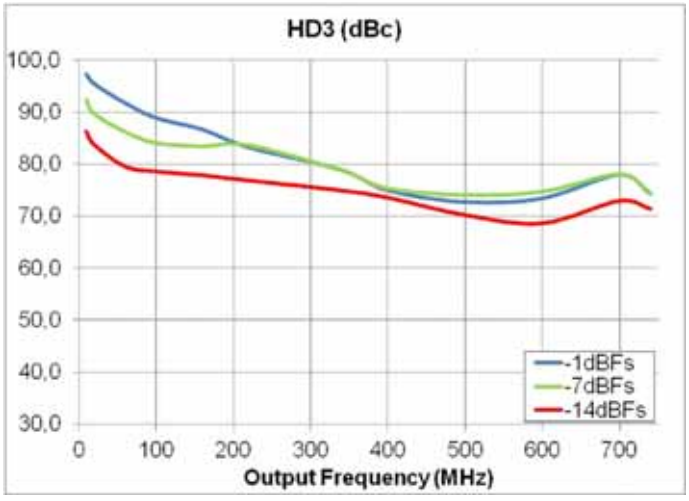


Fig 7. HD3 (dBm) over Nyquist depending of fout (MHz) and input level (dBFS)

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$V_{DDA(3V3)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; no inverse sin(x)/x; no output correction; input level = -7/ -14 / -19 dBFS per tone, 1 MHz spacing; output signal = 1 V(p-p),diff; output common mode voltage = 2.7 V (DAC1658D) or 0.5 V (DAC1653D); unless otherwise specified.

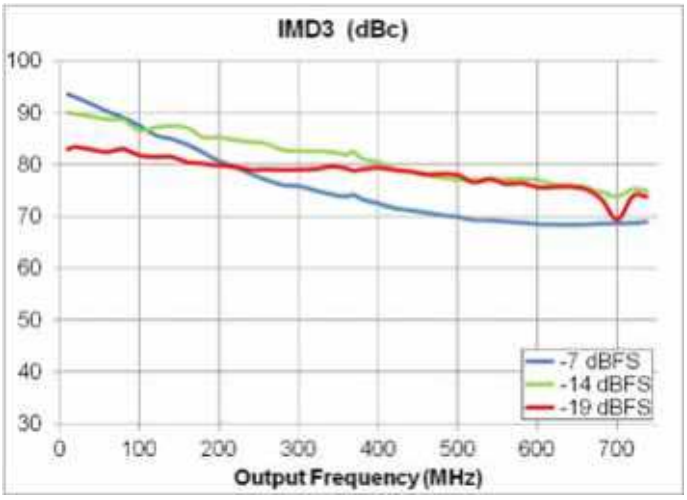


Fig 8. IMD3 (dBc) depending of fout (MHz) and input level per tone (dBFS)

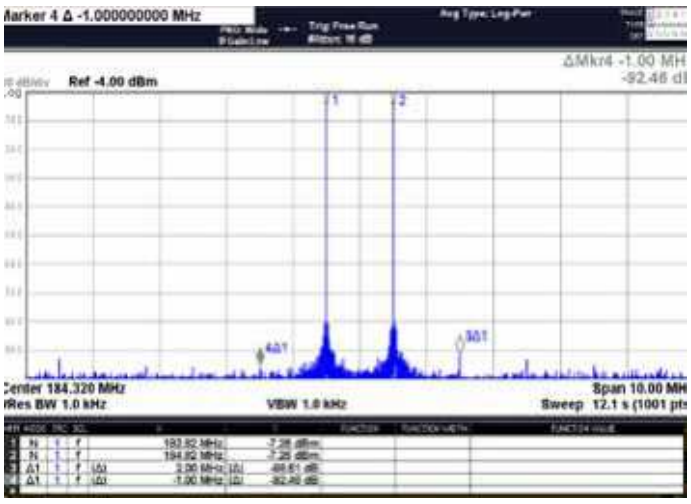


Fig 9. IMD3 (dBc) for two tones (spacing 1 MHz) centered at 184.32 MHz

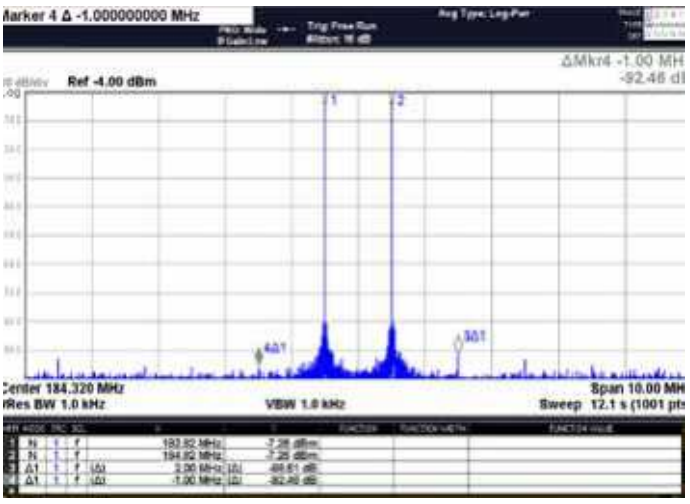


Fig 10. IMD3 (dBc) for two tones (spacing 10 MHz) centered at 184.32 MHz

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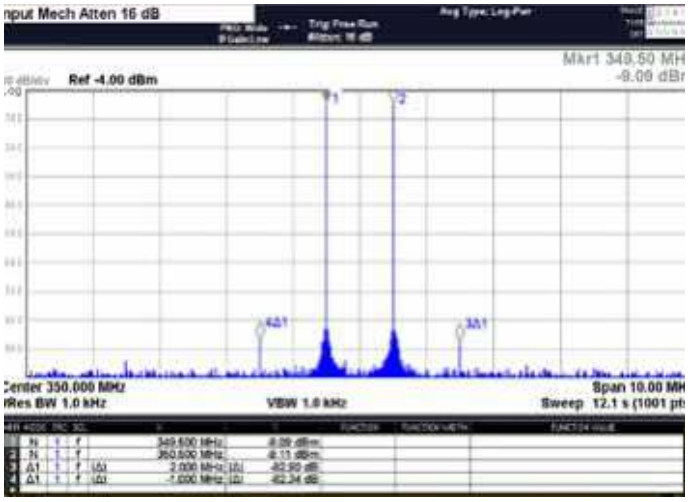


Fig 11. IMD3 (dBc) for two tones (spacing 1 MHz) centered at 350 MHz

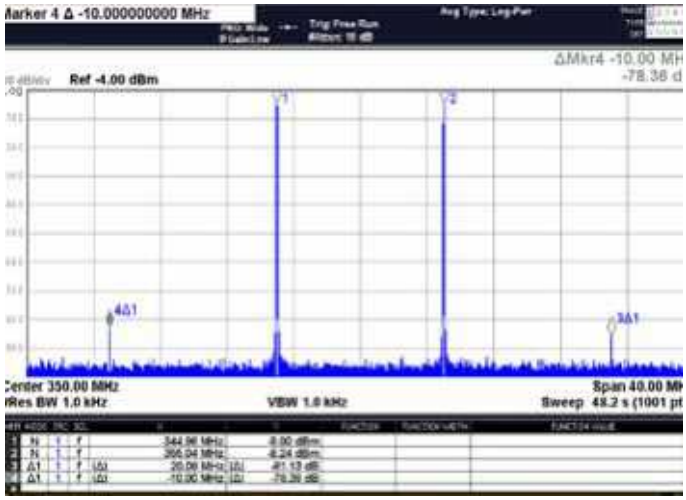


Fig 12. IMD3 (dBc) for two tones (spacing 10 MHz) centered at 350 MHz

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$V_{DDA(3V3)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1 Gsps, 1.5 Gsps and 2 Gsps sample rates used; no auxiliary DAC used; no inverse sin(x)/x; no output correction; input level = -1 dBFS; output signal = 1 V(p-p),diff; output common mode voltage = 2.7 V (DAC1658D) or 0.5 V (DAC1653D); unless otherwise specified.

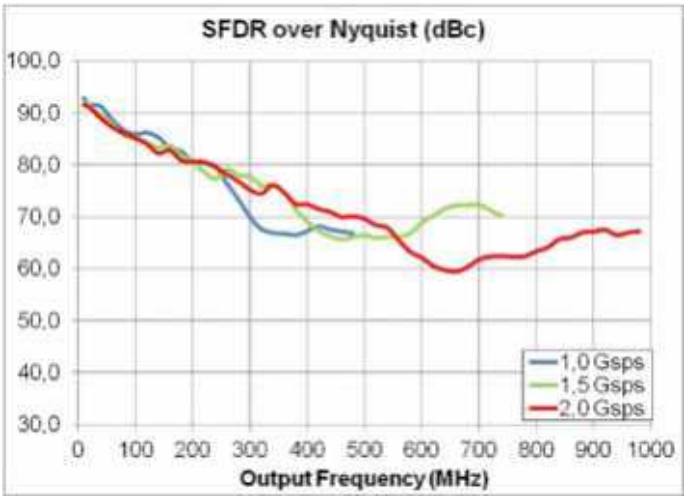


Fig 13. SFDR (dBc) over Nyquist depending of fout (MHz) and sampling frequency (Gsps)

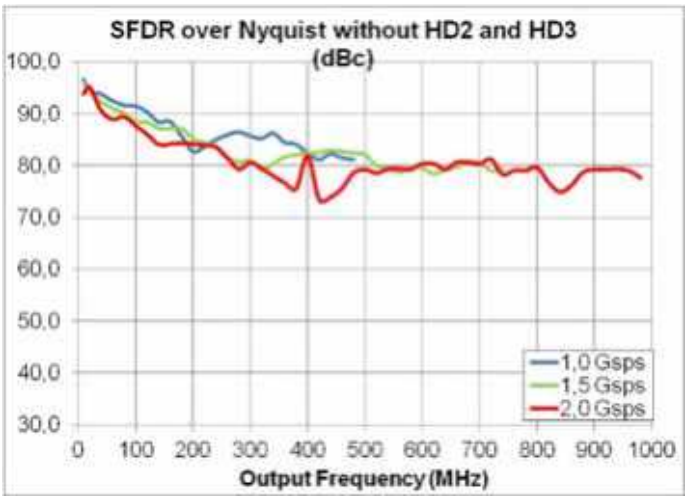


Fig 14. SFDR without HD2 and HD3 (dBc) over Nyquist depending of fout (MHz) and sampling frequency (Gsps)

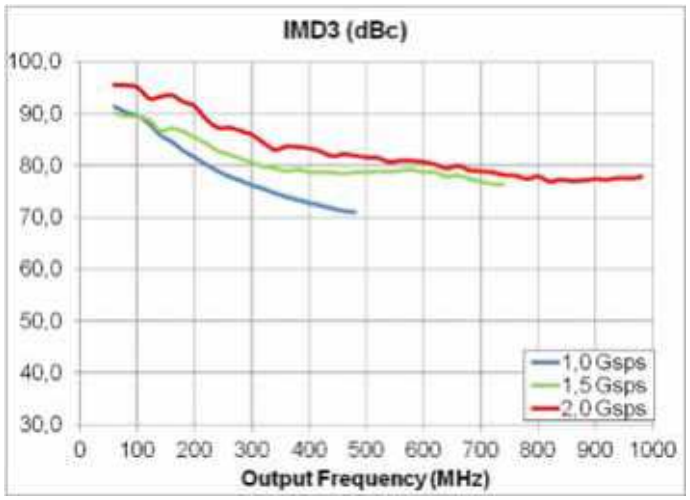


Fig 15. IMD3 (dBc) depending of fout (MHz) and sampling frequency (Gsps)

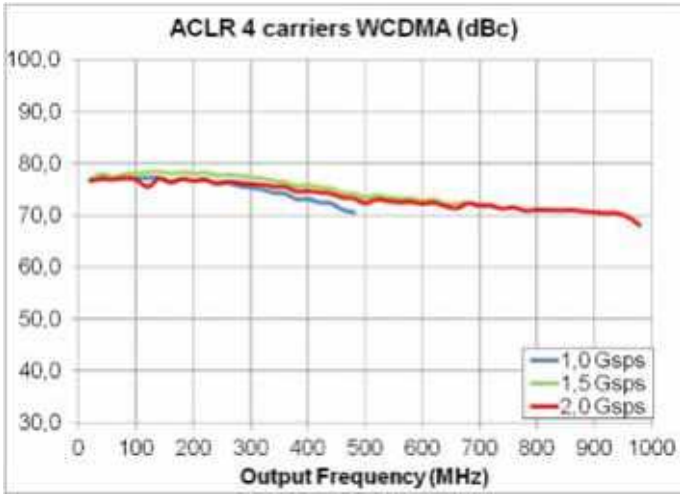


Fig 16. ACLR WCDMA 4 carriers depending of fout (MHz) and sampling frequency (Gsps)

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$V_{DDA(3V3)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1 Gsps, 1.5 Gsps and 2 Gsps sample rates used; no auxiliary DAC used; no inverse sin(x)/x; no output correction; input level = -1 dBFS; output signal = 1 V(p-p),diff; output common mode voltage = 2.7 V (DAC1658D) or 0.5 V (DAC1653D); unless otherwise specified.

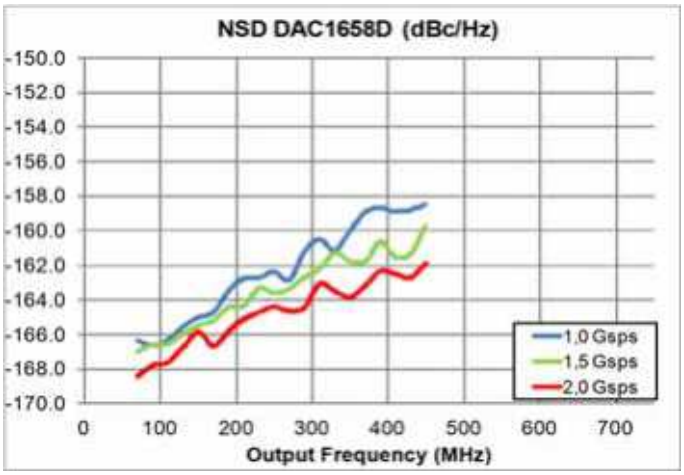


Fig 17. DAC1658D NSD (dBc/Hz) depending of output frequency (MHz)

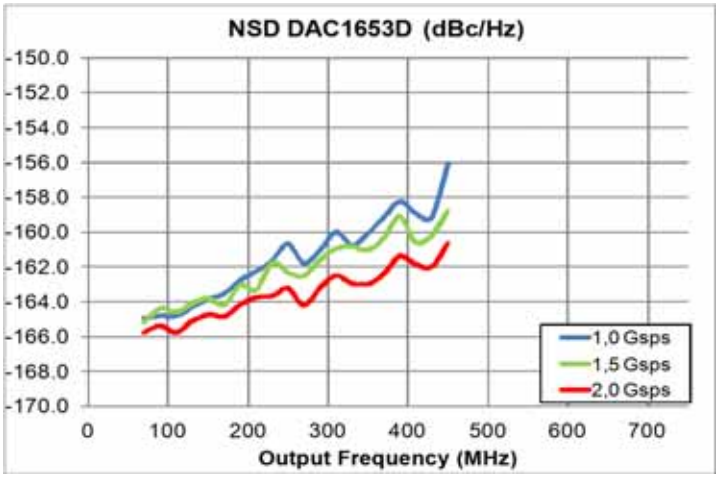


Fig 18. DAC1653D NSD (dBc/Hz) depending of output frequency (MHz)

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$V_{DDA(3V3)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; no inverse sin(x)/x; no output correction; output signal = 1 V(p-p),diff; output common mode voltage = 2.7 V (DAC1658D) or 0.5 V (DAC1653D); unless otherwise specified.



Fig 19. ACLR of 1 carrier LTE (BW=20 MHz) centered at 184.32 MHz



Fig 20. ACLR of 2 carriers LTE (BW=2 x 20 MHz) centered at 184.32 MHz



Fig 21. ACLR of 1 carrier LTE (BW=20 MHz) centered at 350 MHz



Fig 22. ACLR of 2 carriers LTE (BW=2 x 20 MHz) centered at 350 MHz

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Other parameters are specified as follow: $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; no inverse sin(x)/x; no output correction; output signal = 1 V(p-p),diff, output signal frequency = 100 MHz; unless otherwise specified.

Reducing the $V_{DDA(3V3)}$ power supply allows to decrease the total power consumption for the DAC1653D. However, specific correctives factors needs to be apply to the dynamic performances for DAC1653D. These correctives factors depend of the value of analog power supply $V_{DDA(3V3)}$ and the value of the output common mode voltage V_{cm}.

Second harmonic distortion HD2 is only dependent of the $V_{DDA(3V3)}$ power supply value.

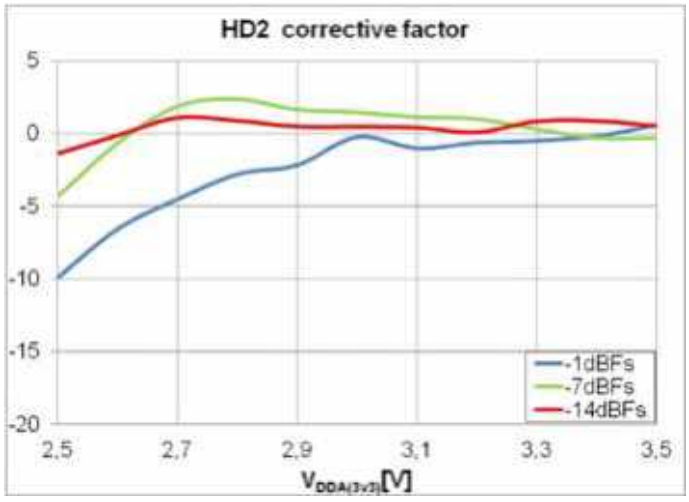


Fig 23. HD2 corrective factor (dB) depending of $V_{DDA(3V3)}$ (V) and input level per tone (dBFS)

Third harmonic distortion HD3 and Intermodulation product IMD3 are dependents of the difference voltage between $V_{DDA(3V3)}$ power supply and V_{cm} common mode output voltage.

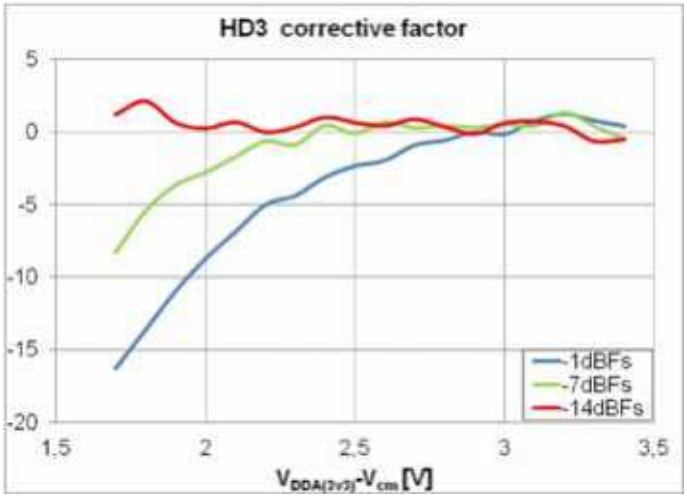


Fig 24. HD3 corrective factor (dB) depending of ($V_{DDA(3V3)}$- V_{cm}) (V) and input level per tone (dBFS)

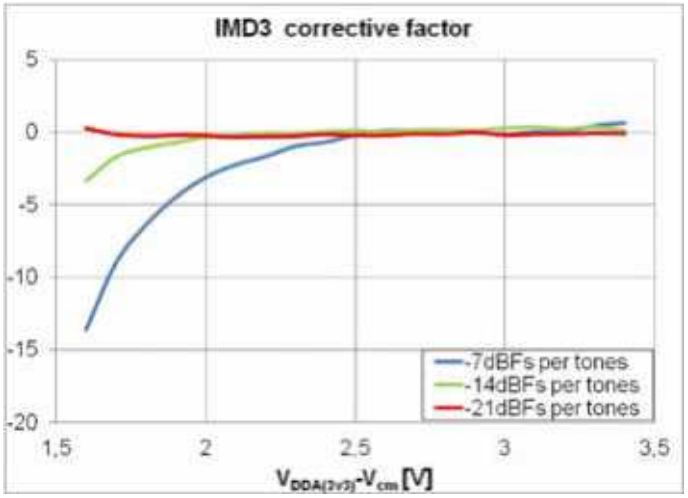


Fig 25. IMD3 corrective factor (dB) depending of ($V_{DDA(3V3)}$- V_{cm}) (V) and input level per tone (dBFS)

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$V_{DDA(3V3)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; no inverse sin(x)/x; no output correction; input level = -1 dBFS; output signal = 1 V(p-p),diff; output common mode voltage = 2.7 V (DAC1658D) or 0.5 V (DAC1653D); unless otherwise specified.

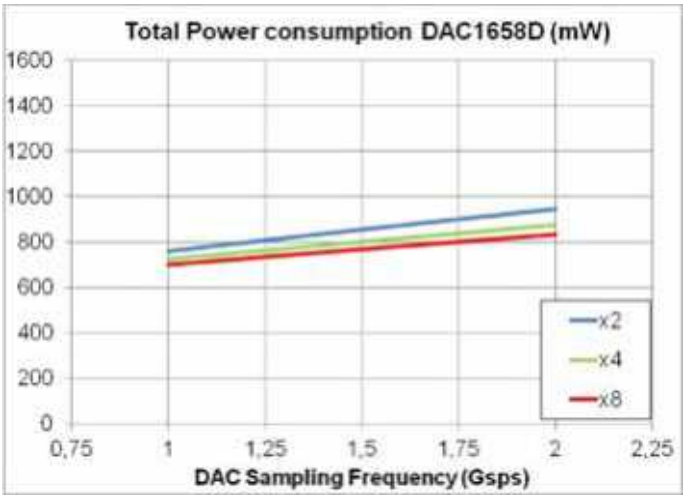


Fig 26. Total Power consumption DAC1658D (mW) depending of the DAC sampling frequency and the interpolation factor (all digital features off)

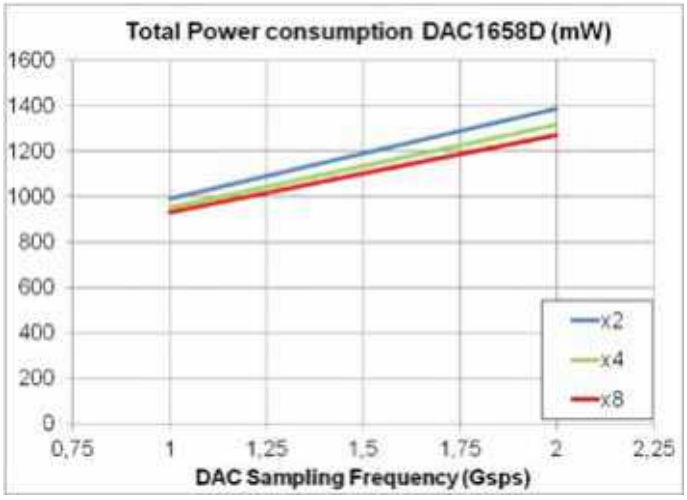


Fig 27. Total Power consumption DAC1658D (mW) depending of the DAC sampling frequency and the interpolation factor (all digital features on)

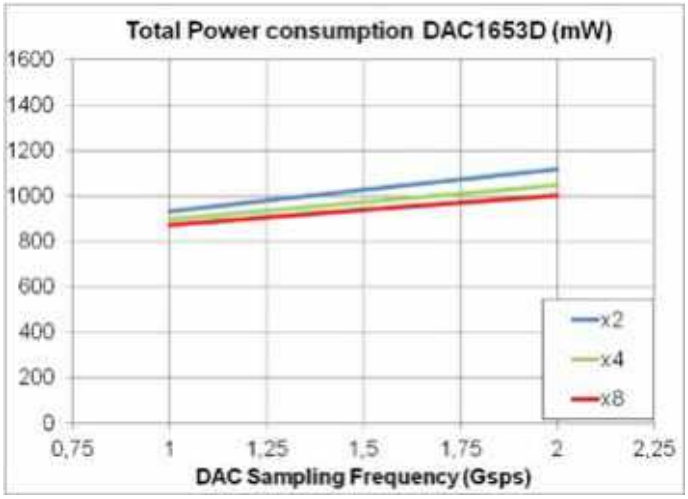


Fig 28. Total Power consumption DAC1653D (mW) depending of the DAC sampling frequency and the interpolation factor (all digital features off)

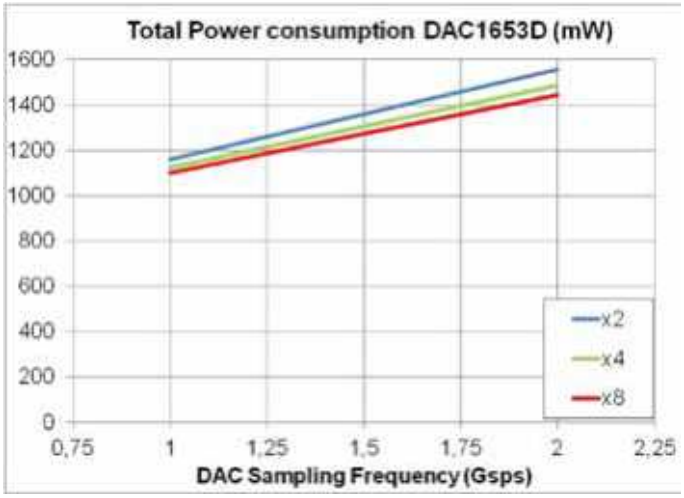


Fig 29. Total Power consumption DAC1653D (mW) depending of the DAC sampling frequency and the interpolation factor (all digital features on)

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Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; ; no auxiliary DAC used; no inverse sin(x)/x; no output correction; output signal = 1 V(p-p),diff; output common mode voltage = 2.7 V (DAC1658D) or 0.5 V (DAC1653D); unless otherwise specified.

Power supplies consumption for $V_{DDA(3V3)}$ = 3.3 V and $V_{DDA(1V2)}$ = 1.2 V are not dependents of the DAC sampling rate or the interpolation factor.

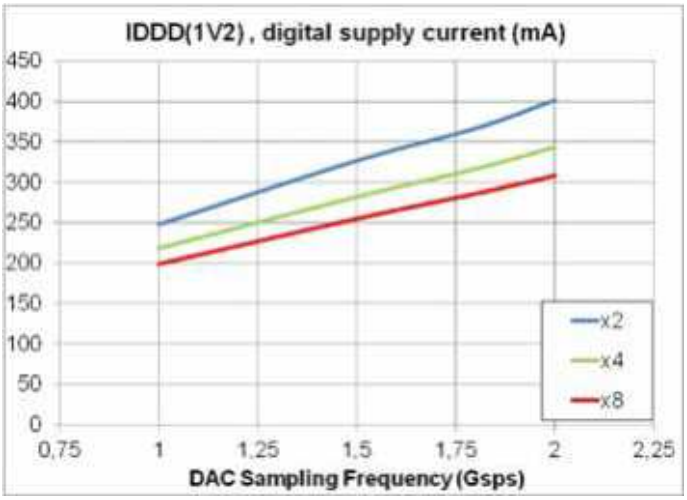


Fig 30. Digital supply current (IDDD(1v2) depending of the DAC sampling frequency and the interpolation factor (all digital features off)

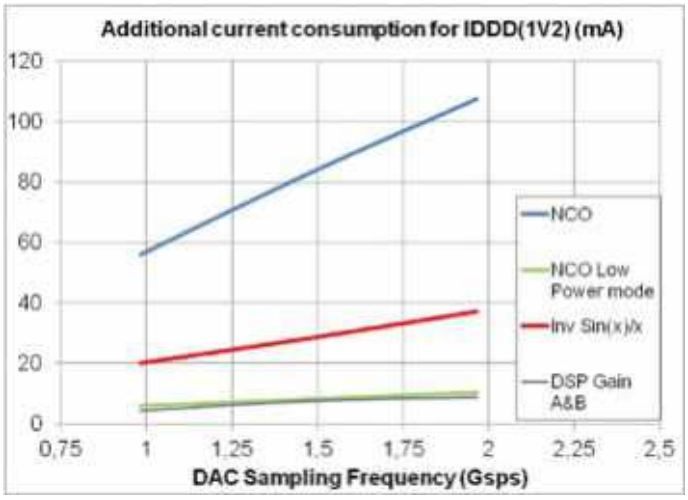


Fig 31. Additional digital supply current for IDDD(1v2) depending of the DAC sampling frequency and digital features

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11. Application information

11.1 General description

The DAC165xD is a dual 16-bit DAC operating up to 2.0 Gsps. A maximum input data rate up to 1000 Msps is supported to enable more capability for wideband and multicarrier systems. The incorporated quadrature modulator and 40-bit Numerically Controlled Oscillator (NCO) simplifies the frequency selection of the system. This is also possible because of the ×2, ×4 or ×8 interpolation filters which remove undesired images.

The DAC165xD supports the following JESD204B key features:

- 10-bit/8-bit decoding
- Code group synchronization
- Initial Lane Alignment (ILA)
- $1 + x^{14} + x^{15}$ scrambling polynomial
- Character replacement
- TX/RX synchronization management via SYNC synchronization signals
- Multiple Converter Device Alignment-Multiple Lanes (MCDA-ML) device (subclass 1 compatible)
- Independent Link Synchronization support
- Deterministic latency
- Multiple Device Synchronization (MDS); JESD204B subclass 1 compatible
- Harmonic clocking support
- Number L of serial lanes: 1, 2, 4 (see LMF-S configuration)
- Number M of data converters: 1 or 2 (see LMF-S configuration)
- Number F of octets per frame: 1, 2, 4 (see LMF-S configuration)
- Number S of samples per frame: 1, 2 (see LMF-S configuration)
- Embedded test pattern (PRBS31, PRBS23, PRBS15, PRBS7, JTSPAT, STLTP)

The DAC165xD can be interfaced with any logic device that features high-speed SERializer/DESerializer (SERDES) functionality. This macro is now widely available in Field-Programmable Gate Array (FPGA) of different vendors. Standalone SERDES ICs can also be used.

The DAC165xD includes polarity swapping for each of the lanes and additionally offers lane swapping to enhance the intrinsic board layout simplification of the JESD204B standard. Each physical lane can be configured logically as lane 0, lane 1, lane 2 or lane 3.

This device is MCDA-ML compatible, offering inter lane alignment between several devices. An IDT proprietary mechanism in combination with the JESD204B subclass I clause enables maintenance of sample alignment between devices up to the final analog output stage. Output samples are automatically aligned to the SYSREF signal generated by a dedicated IC or by the FPGA itself. A system with several DAC165xDs can produce data with a guaranteed alignment of less than +/-1 DAC output clock period. The DAC165xD incorporates two differential SYSREF ports (located on opposite sides of the IC) to simplify the PCB layout design. The device also enables independent link reinitialization.

The DAC165xD generates two complementary current outputs on pins IOUTA_P/IOUTA_N and IOUTB_P/IOUTB_N, corresponding to channel 'A' and 'B', respectively, providing a nominal full-scale output current of 20 mA. An internal reference is available for the reference current which is externally adjustable using pin VIRES.

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The DAC165xD requires configuration before operating. It features an SPI slave interface to access the internal registers. Some of these registers also provide information about the JESD204B interface status. Optionally, an interrupt capability can be programmed using those registers to ensure ease of use of the device.

Because of the JESD204B standardization, the DAC165xD does not require any adjustment from the Transmit Logic Device (TLD) to capture the input data streams. Some autolock features can be monitored using the SPI registers.

The DAC165xD supports the following LMF configuration as described in the JESD204B standard (register LMF_CTRL; see Table 124):

Table 9. LMF configuration

L-M-F	S[1]	HD[2]
1-2-4	1	0
2-2-2	1	0
4-2-2	2	0
4-2-1	1	1

[1] S is the number of samples per frame.

[2] HD is the high-density bit as described in the JESD204B specification.

A new IDT auto-mute feature enables switching off of the RF output signal as a result of various internal events occurring.

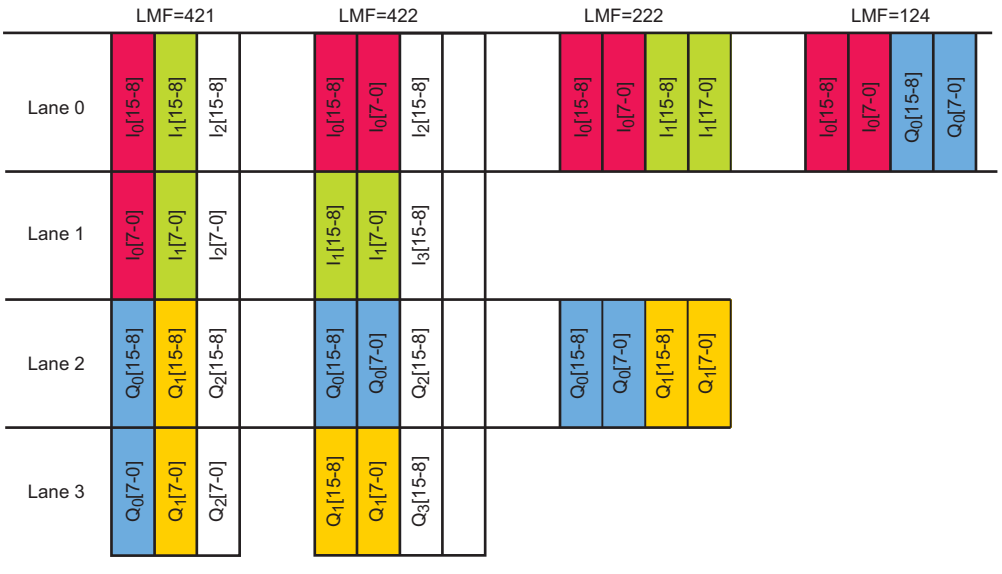


Fig 32. Frame assembly byte representation

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11.2 Device operation

The DAC165xD provides a lot of flexibility in its way of working through its SPI registers. The SPI registers are divided in blocks of registers. Each block is associated with some global functions which are described below. Section 11.12 shows an overview of all register blocks, including the register descriptions.

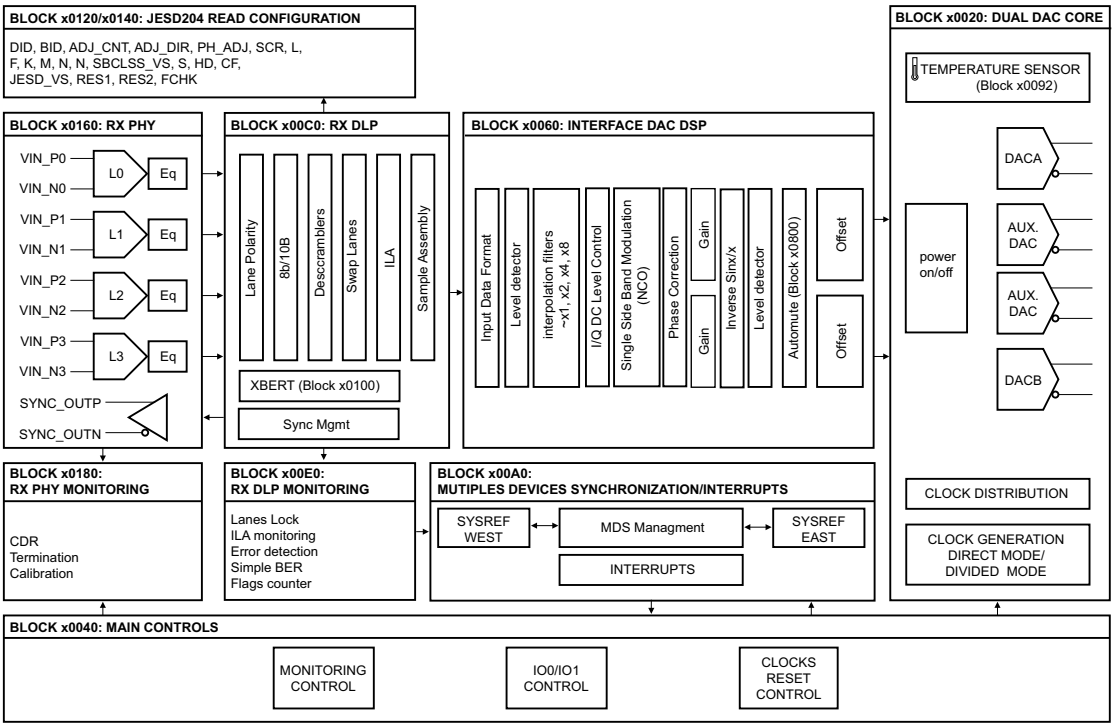


Fig 33. SPI register blocks partition

11.2.1 SPI configuration block

This block of registers specifies how the SPI controller and the identification of the chip work.

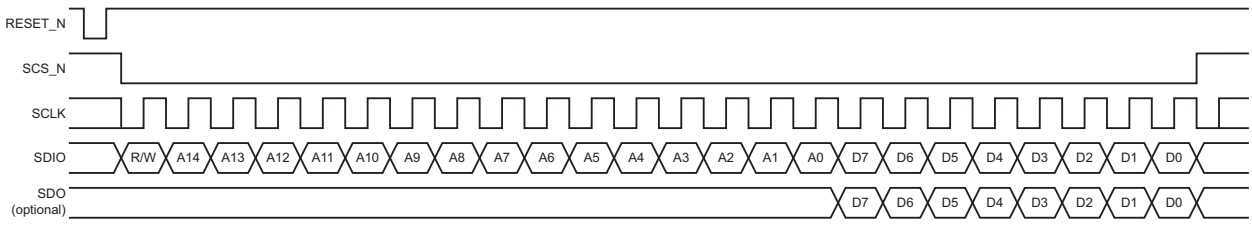
11.2.1.1 Protocol description

The DAC165xD serial interface is a synchronous serial communication port allowing easy interfacing with many industry microprocessors. It provides access to the registers that define the operating modes of the chip in both Write mode and Read mode. The reference voltage of the interface is $V_{DDD(IO)}$. Depending on the power supply level of the SPI master device, it can be set from1.2 V to1.8 V.

This interface can be configured as a 3-wire type (SDIO as bidirectional pin) or a 4-wire type (SDIO and SDO as unidirectional pins, input and output ports, respectively). In both configurations, SCLK acts as the serial clock and SCS_N acts as the serial chip select.

The DAC165xD SPI-interface is a slave-device. Multiple slave-device can be attached to the same master interface as long as each device has its own serial chip select signal (SCS_N).

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R/W indicates the mode access.

The RESET_N signal is not linked to the SPI interface but enable the reset of the registers to the default values.

Fig 34. SPI protocol

Table 10. Read mode or Write mode access description

R/W	Description
0	Write mode operation
1	Read mode operation

A[14:0] indicates which register is being addressed. If a multiple transfer occurs, this address points to the first register to be accessed.

11.2.1.2 SPI controller configuration

The 3-wire or 4-wire mode is set by bit SPI_4W of register SPI_CFG_A (see Table 48). The default mode is 3-wire mode.

A software SPI reset can be called via bit SPI_RST of register SPI_CFG_A (see Table 48). This reset reinitializes all SPI registers, except register SPI_CFG_A and SPI_CFG_B, to their default settings. Only a hardware reset on pin RESET_N can reset to their default values. Reset the device to its default value at start-up time to avoid any uncontrolled states.

The SPI streaming mode is enabled by default. In this mode, the Read or Write process carries on as long as the SCS_N signal is low. The streaming mode requires a first address 'n' to be set at the beginning of the SPI sequence. The following data are associated from this address in an ascending (auto-increment) or descending (auto-decrement) mode. This ascending/descending mode is specified by bit SPI_ASC of register SPI_CFG_A. Figures below represent the readback of 2 bytes data in a 3 wires mode for the ascendant and descendant mode.

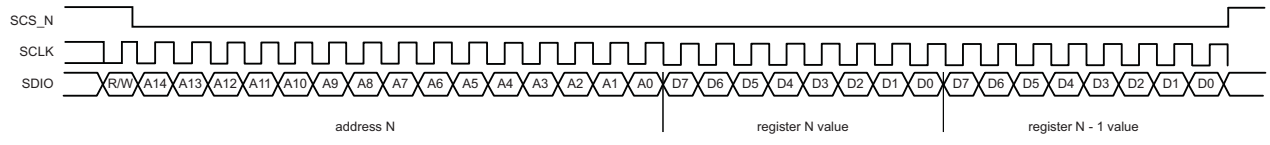


Fig 35. Consecutive 2-byte data readback under descending address

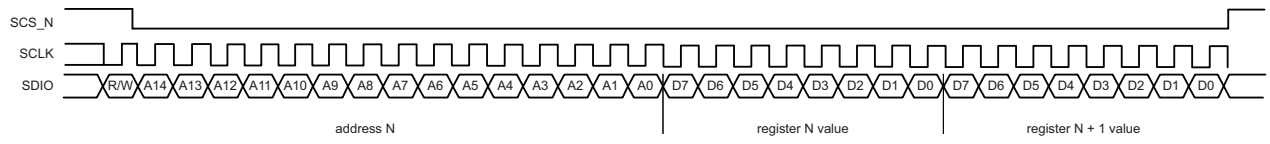


Fig 36. Consecutive 2-byte data readback under ascending address

The streaming mode can be disabled by setting bit SPI_SNGL of register SPI_CFG_B (see Table 48). In this single-byte mode, only 1 byte of data can be written or read, whatever the state of the SCS_N signal.

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11.2.1.3 Double buffering and Transfer mode

Some register functions (like the NCO frequency value) are split over multiple registers. If this is the case, the first address consists of the LSB byte and the highest address in the MSB byte. When programming these registers sequentially, some unexpected behavior can occur at the DAC output. It is preferable to program this set of registers simultaneously. A double buffering feature is available on some registers allowing sequential programming of the first buffers and transferring the values to the final register simultaneously.

The transfer request is done by setting the TRANSFER_BIT bit of register SPI_CFG_C register (see Table 53). The device clears this bit (autoclear) indicating to the SPI master device that the transfer is complete.

The SPI_RBACK_BUFF bit of register SPI_CFG_B (see Table 48) allows the reading back of the first stage of buffers (in case the register is double buffered).

The following registers are double buffered:

Table 11. Double buffered registers
See *Table 71*

Address	Register
0062h	NCO_PH_OFFSET_LSB
0063h	NCO_PH_OFFSET_MSB
0064h	NCO_FREQ_B0
0065h	NCO_FREQ_B1
0066h	NCO_FREQ_B2
0067h	NCO_FREQ_B3
0068h	NCO_FREQ_B4
0069h	PH_CORR_CTRL_0
006Ah	PH_CORR_CTRL_1
006Bh	DAC_A_DGAIN_LSB
006Ch	DAC_A_DGAIN_MSB
006Dh	DAC_B_DGAIN_LSB
006Eh	DAC_B_DGAIN_MSB
006Fh	DAC_OUT_CTRL
0070h	DAC_LVL_DET
0071h	DAC_A_OFFSET_LSB
0072h	DAC_A_OFFSET_MSB
0073h	DAC_B_OFFSET_LSB
0074h	DAC_B_OFFSET_MSB
0075h	IQ_LVL_CTRL
0076h	I_DC_LVL_LSB
0077h	I_DC_LVL_MSB
0078h	Q_DC_LVL_LSB
0079h	Q_DC_LVL_MSB
007Ah	SPD_CTL
007Bh	SPD_THRESHOLD_LSB
007Ch	SPD_THRESHOLD_MSB

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11.2.1.4 Device description

Registers CHIP_TYPE, CHIP_ID_0, CHIP_ID_1 and CHIP_VS (see Table 51) represent the ID card of the device.

Registers VEND_ID_LSB and VEND_ID_MSB (see Table 52) represent the IDT manufacturer identifier.

11.2.1.5 SPI RESET_N wait duration requirement

After a Power On Reset or a RESET_N request, a wait duration is needed before sending the first SPI command. Please refer to the following table to apply the expected wait duration.

Table 12. Wait duration after hard reset

FDAC	wait duration before first SPI command
1.0 Gsps	40 µs
1.5 GSps	30 µs
2.0 Gsps	20 µs

11.2.1.6 SPI timing description - 4 wires mode

The SPI interface can operate at a frequency of up to 25 MHz. Figure 37 and Figure 38 show the SPI timing in 4 wires mode.

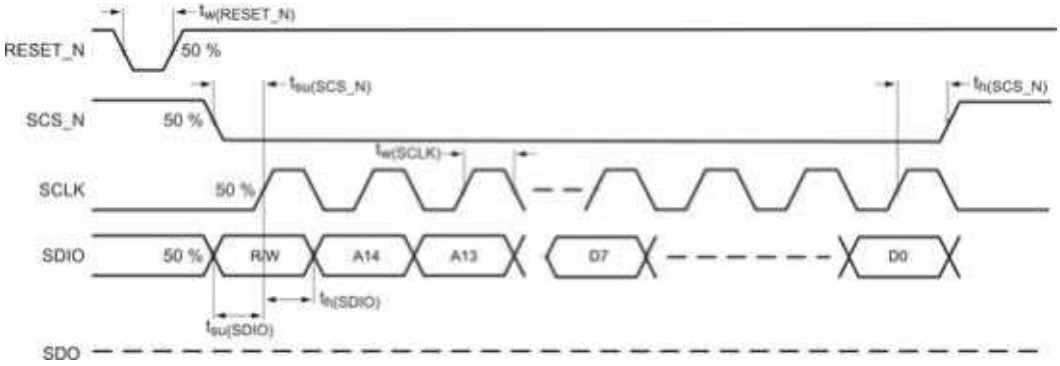


Fig 37. SPI timing diagram - 4 wires - write mode

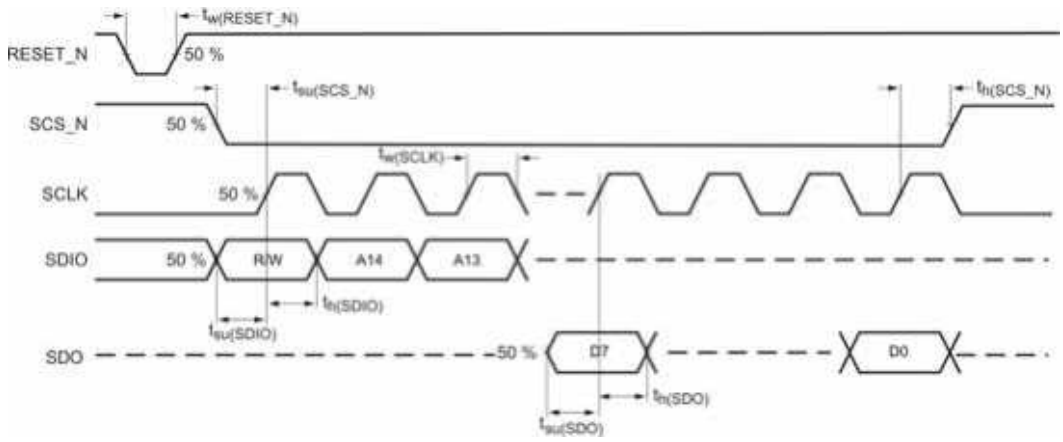


Fig 38. SPI timing diagram - 4 wires - read mode

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The SPI timing characteristics are given in Table 13.

Table 13. SPI timing characteristics - 4 wires

Symbol	Parameter		Min	Typ	Max	Unit
f_{SCLK}	SCLK frequency					
	$V_{DDD(IO)}$=1.8V		-	-	25	MHz
	$V_{DDD(IO)}$=1.2V		-	-	20	MHz
$t_{w(SCLK)}$	SCLK pulse width (high)		20	-	-	ns
	SCLK pulse width (low)		depends of propagation time and master timing requirements			
$t_{su(SCS_N)}$	SCS_N set-up time		5	-	-	ns
$t_{h(SCS_N)}$	SCS_N hold time		20	-	-	ns
$t_{su(SDIO)}$	SDIO set-up time		5	-	-	ns
$t_{h(SDIO)}$	SDIO hold time		5	-	-	ns
$t_{su(SDO)}$	SDO set-up time		5	-	-	ns
$t_{h(SDO)}$	SDO hold time		5	-	-	ns
$t_{w(RESET_N)}$	RESET_N pulse width	[1]	30	-	-	ns

[1] The RESET_N signal is asynchronous to the SPI interface, but enables the reset of the registers to the default values.

11.2.1.7 SPI timing description - 3 wires mode

The SPI interface can operate at a frequency of up to 15 MHz. Figure 39 and Figure 40 show the SPI timing in 3 wires mode.

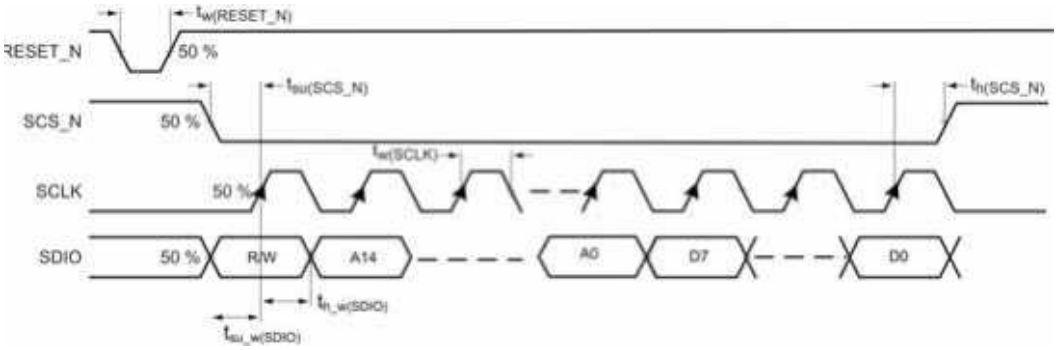


Fig 39. SPI timing diagram - 3 wires - write mode

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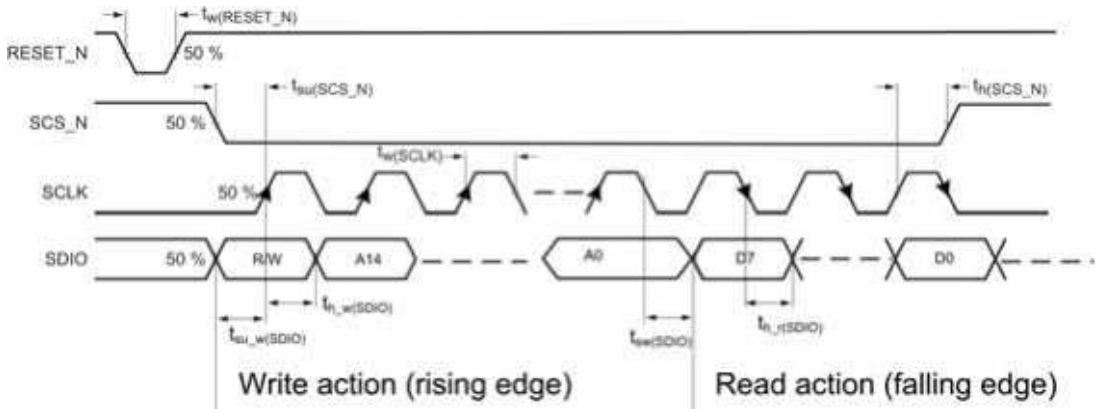


Fig 40. SPI timing diagram - 3 wires - read mode

The SPI timing characteristics are given in Table 14.

Table 14. SPI timing characteristics - 3 wires

Symbol	Parameter		Min	Typ	Max	Unit
f_{SCLK}	SCLK frequency		-	-	15	MHz
$t_{w(SCLK)}$	SCLK pulse width (high)		30	-	-	ns
	SCLK pulse width (low)		depends of propagation time and master timing requirements			
$t_{su(SCS_N)}$	SCS_N set-up time		5	-	-	ns
$t_{h(SCS_N)}$	SCS_N hold time		20	-	-	ns
$t_{su_w(SDIO)}$	SDIO set-up time		5	-	-	ns
$t_{h_w(SDIO)}$	SDIO hold time		5	-	-	ns
$t_{sw(SDIO)}$	SDIO switch time (write to read mode)					
	$V_{DDD(IO)}$=1.8V		9	-	20	ns
	$V_{DDD(IO)}$=1.2V		9	-	25	ns
$t_{h_r(SDIO)}$	SDO hold time (read mode)					
	$V_{DDD(IO)}$=1.8V		6	-	20	ns
	$V_{DDD(IO)}$=1.2V		6	-	25	ns
$t_{w(RESET_N)}$	RESET_N pulse width	[1]	30	-	-	ns

[1] The RESET_N signal is asynchronous to the SPI interface, but enables the reset of the registers to the default values.

11.2.1.8 SPI IOs strength

The SPI interface can operate at a voltage $V_{DDD(IO)}$ in the 1.2V to 1.8V range. The current strength of the IOs could also been programmed regarding the amount of switching noise and minimum working frequency of the serial bus. Refer to Table 67 to program the appropriate bits.

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Table 15. EHS modes
Programmable current drive strength.

xx_EHS		
Value	**Output mode**	**Comment**
00	very low noise / low speed	
01	medium noise / fast speed	recommended mode
10	low noise / medium speed	default mode
11	high noise / high speed	

11.2.2 Main device configuration and Start-up Sequence

The registers of block MAIN are used for the main configuration of the DAC165xD.

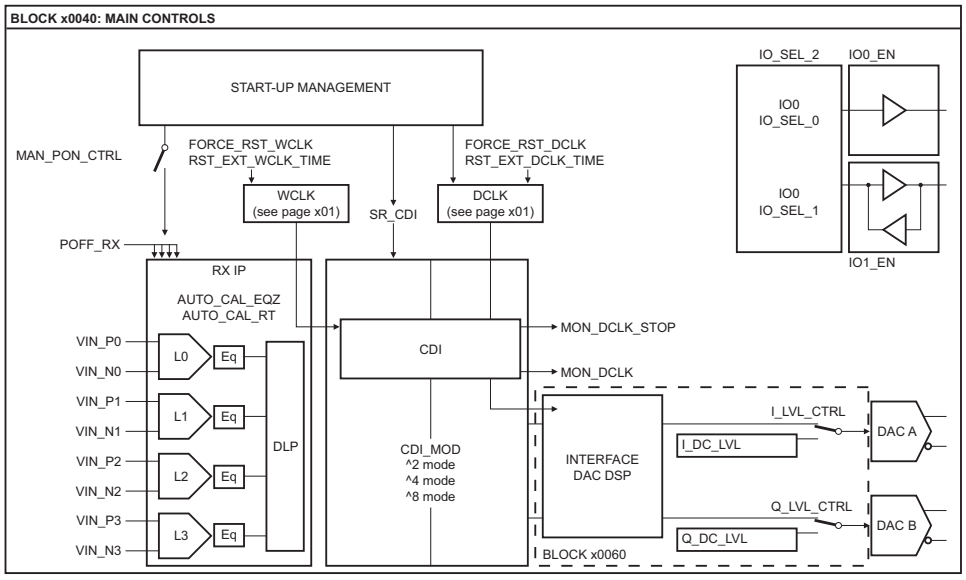


Fig 41. Main controls

Once power supplies are established (no specific requirement neither on slope nor on sequence), reset the device by asserting the RESET_N pin and provide the clock on the DAC_CLK_P/N pins. After this reset, a wait time is needed before sending the first SPI command. Refer to the SPI section to specify the duration (ex: 40µs at 1GHz).

At start-up, the two clocks WCLK and DCLK are forced to reset states to avoid that the DAC outputs any dummy signal through bits FORCE_RST_DCLK and FORCE_RST_WCLK of the MAIN_CTRL register (see Table 64). The device configuration has to be done before releasing these two clocks.

Here are some guidelines to ensure basic correct SPI programming. As DCLK and WCLK are kept to reset, the programming sequence of the registers is not important after the reset:

1. Proceed to a software reset of all SPI registers (see Section 11.2.1.2)
2. Disable the Power Down mode
3. Specify the Interpolation mode (see Table 16) and/or SSBM mode (see Table 18)
4. Specify the Clocks configuration (see Section 11.2.6.1):
   a. Divider bypass or Divider mode
   b. WCLK division ratio

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5. Specify the Clock Domain Interface (CDI) mode (Section 11.2.6.1 and Table 25)
6. Specify the JESD204B LMF configuration (see Section 11.8.5.11)
7. Specify the JESD204B logical lanes order (see Section 11.8.5.3) and polarity
8. Specify which JESD204B physical lanes have to be turned off using the POFF_RX bits of register MAIN_CTRL (see Table 64)
9. Set the SYNCB output common mode level and swing (see Section 11.8.5.5)
10. Provide the K28.5 (Code Group Synchronization) to all used JESD204B lanes.
11. Release the WCLK and DCLK reset by de-asserting the bits FORCE_RST_DCLK and FORCE_RST_WCLK of the MAIN_CTRL register (see Table 64)

Other SPI configurations can be added using these basic settings.

SPI configuration example:

1. Register x0000 write x99 : Mandatory: configure SPI in 3 or 4 wires and proceed to soft reset
2. Register x0043 write x00 : Mandatory: disable the power down mode
3. Register x0060 write x02 : Mandatory: specify NCO usage and Interpolation mode
4. Specify internal clocks for RX-PHY
   a. Register x0022 write x22 : Mandatory: specify and reset internal clocks for RX-PHY
   b. Register x0022 write x44 : Mandatory: specify and reset internal clocks for RX-PHY
5. Register x004B write x01 : Mandatory: specify the CDI mode
6. Register x00DE write x92 : Mandatory: specify the JESD204B LMF configuration
7. Register x00CE write x1B : Optional: specify the JESD204B logical lanes order
8. Register x00CD write x0F : Optional: specify the JESD204B physical lanes polarity
9. Register x00C7 write x63 : Optional: specify the scrambler option
10. Register x0075 write x85 : Optional: specify that the DAC will output DC value when RX-PHY is not synchronized
11. Register x0080 write x90 : Optional: specify the MUTE options
12. Register x017D write xC4 : Recommended: Set the SYNCB output common mode level and swing
13. Provide the K28.5 (Code Group Synchronization) to all used JESD204B lanes.
14. Register x0040 write x00 :Mandatory: Specify which JESD204B physical lanes have to be turned off using the POFF_RX bits and release the WCLK and DCLK resets

Remark: All the Double Buffering registers programmed before the DCLK reset release are transfered automatically after the DCLK reset release. After this reset release, these registers need the TRANSFER_BIT to be active.

11.2.2.1 Power Down mode

The latest version of DAC165xD starts in Power Down mode at startup time. By default it uses the level on the multi purpose RF_ENABLE pin to wake up the device. This feature can be disabled by writing value x00 in register PD_ANA_CTRL (see Table 66).

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11.2.3 Interface DAC DSP block

This module is the interface between the data processing in the high-speed serial receiver and the dual DAC core. The controls of the Digital Signal Processing (DSP) of the DAC are specified to set up the interpolation filter, and enable or disable the various gains and offsets of the data digital path. The data signals have already been processed by the Digital Lane Processing (DLP, see Section 11.12.7). They are provided to this module through the Clock Domain Interface (Section 11.2.6.1). This module is clocked by the digital clock DCLK.

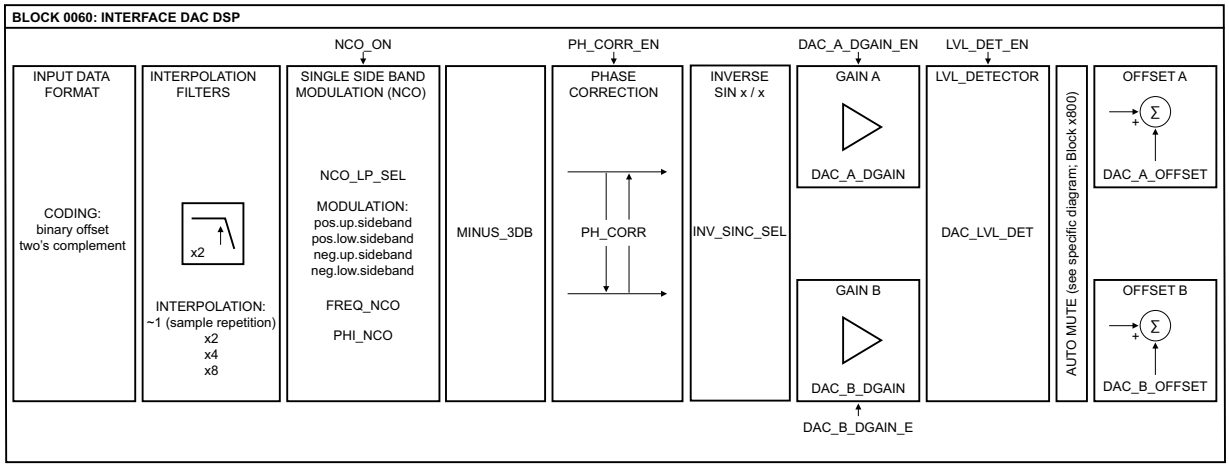


Fig 42. Interface DAC DSP overview

11.2.3.1 Input data format

After decoding in the high-speed serial receiver, the data representation can be specified as binary offset coding or as two's complement coding using register CODING_IQ (see Table 80).

11.2.3.2 Finite Impulse Response (FIR) filters

The DAC165xD provides three interpolation filters described by their coefficients in Table 17. The three interpolation FIR filters have a stop band attenuation of at least 80 dBc and a pass band ripple of less than 0.0005 dB.

The interpolation ratio can be set through register TX_CFG (see Table 72).

Table 16. Interpolation

Symbol	Access	Value	Description
INTERPOLATION[1:0]	R/W		interpolation
		00	no interpolation/~×1 interpolation
		01	×2 interpolation
		10	×4 interpolation
		11	×8 interpolation

The 'no interpolation' or '~×1' (quasi ×1) mode is in fact a degenerated ×2 interpolation mode where the samples are repeated twice.

Remark: The INTERPOLATION setting must be coupled with the DCLK and WCLK clock configurations and with CDI mode (see Section 11.2.6.1).

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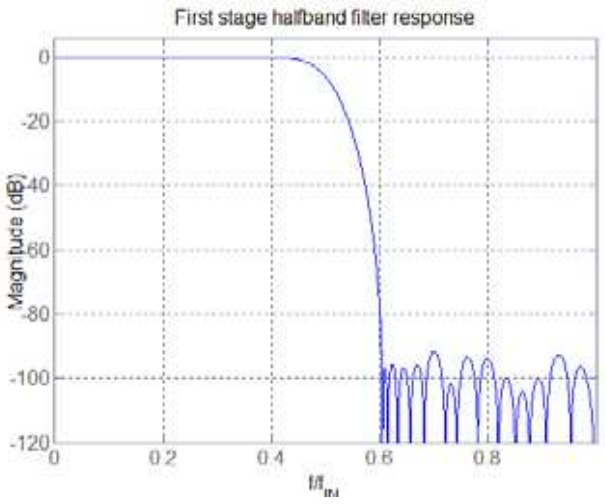


Fig 43. First stage half-band filter response (used in ×2, ×4, and ×8 interpolation)

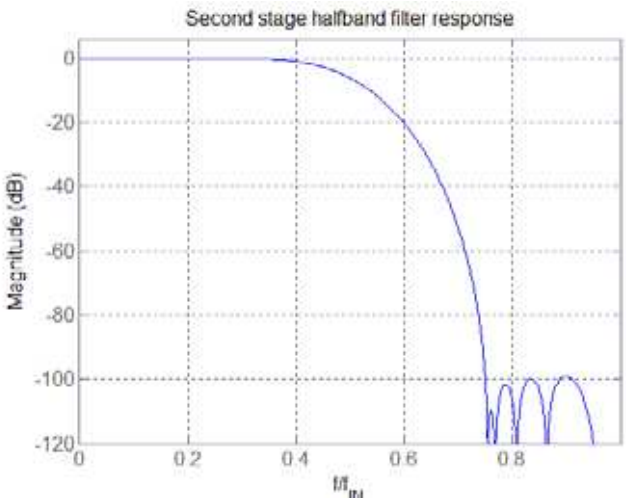


Fig 44. Second stage half-band filter response (used in ×2, ×4, and ×8 interpolation)

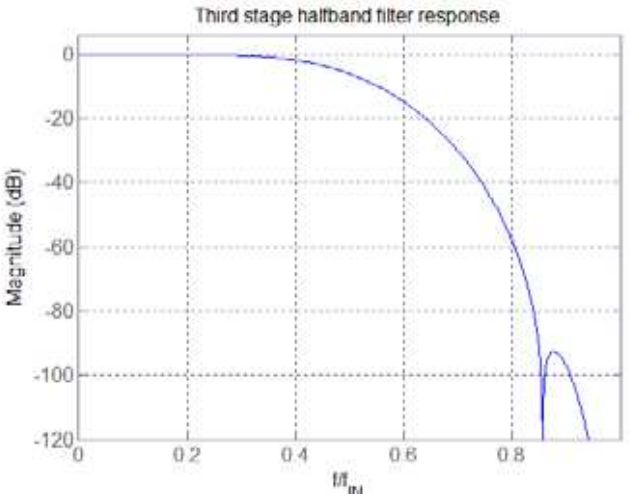


Fig 45. Third stage half-band filter response (used in ×8 interpolation)

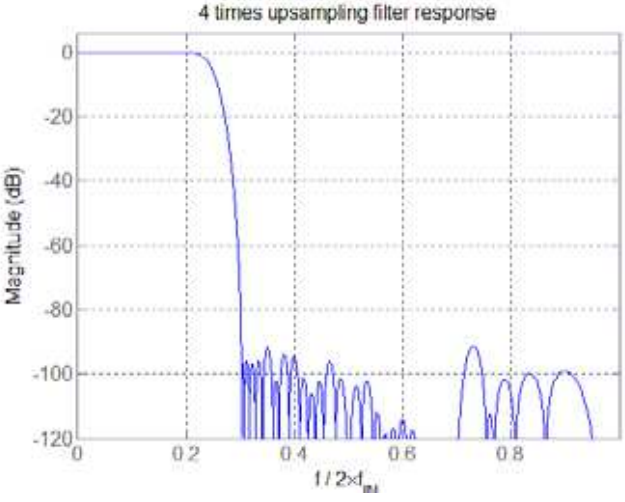


Fig 46. ×4 interpolation cumulated filter response

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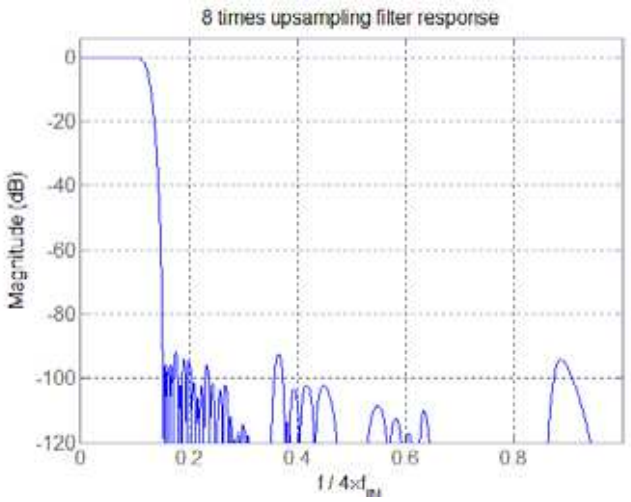


Fig 47. ×8 interpolation cumulated filter response

Table 17: Interpolation filter coefficients

First interpolation filter			Second interpolation filter			Third interpolation filter		
Lower	Upper	Value	Lower	Upper	Value	Lower	Upper	Value
-	H(27)	+65536	H(11)	-	+32768	H(7)	-	+1024
H(26)	H(28)	+41501	H(10)	H(12)	+20272	H(6)	H(8)	+615
H(25)	H(29)	0	H(9)	H(13)	0	H(5)	H(9)	0
H(24)	H(30)	−13258	H(8)	H(14)	−5358	H(4)	H(10)	−127
H(23)	H(31)	0	H(7)	H(15)	0	H(3)	H(11)	0
H(22)	H(32)	+7302	H(6)	H(16)	+1986	H(2)	H(12)	+27
H(21)	H(33)	0	H(5)	H(17)	0	H(1)	H(13)	0
H(20)	H(34)	−4580	H(4)	H(18)	−654	H(0)	H(14)	−3
H(19)	H(35)	0	H(3)	H(19)	0	-	-	-
H(18)	H(36)	+2987	H(2)	H(20)	+159	-	-	-
H(17)	H(37)	0	H(1)	H(21)	0	-	-	-
H(16)	H(38)	−1951	H(0)	H(22)	−21	-	-	-
H(15)	H(39)	0	-	-	-	-	-	-
H(14)	H(40)	+1250	-	-	-	-	-	-
H(13)	H(41)	0	-	-	-	-	-	-
H(12)	H(42)	-773	-	-	-	-	-	-
H(11)	H(43)	0	-	-	-	-	-	-
H(10)	H(44)	+456	-	-	-	-	-	-
H(9)	H(45)	0	-	-	-	-	-	-
H(8)	H(46)	−252	-	-	-	-	-	-
H(7)	H(47)	0	-	-	-	-	-	-
H(6)	H(48)	+128	-	-	-	-	-	-
H(5)	H(49)	0	-	-	-	-	-	-
H(4)	H(50)	−58	-	-	-	-	-	-
H(3)	H(51)	0	-	-	-	-	-	-
H(2)	H(52)	+22	-	-	-	-	-	-
H(1)	H(53)	0	-	-	-	-	-	-
H(0)	H(54)	−6	-	-	-	-	-	-

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11.2.3.3 Single Side Band Modulator (SSBM)

The single side band modulator is a quadrature modulator that enables the mixing of the I data and Q data with the sine and cosine signals generated by the NCO to generate path A and B as described in Figure 48.

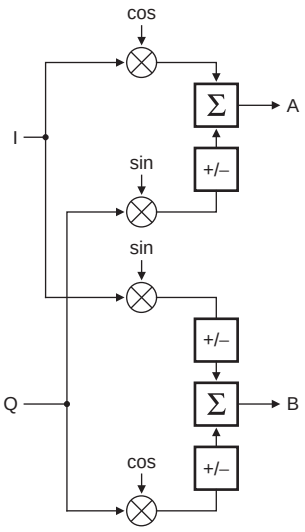


Fig 48. Single sideband modulator principle

Table 18 shows the various possibilities set by register MODULATION (see Table 72).

Table 18. Complex modulator operation mode

MODULATION[2:0]	Mode	Path A	Path B
000	bypass	$I(t)$	$Q(t)$
001	positive upper sideband	$I(t) \times cos(\omega_{NCO} \times t) - Q(t) \times sin(\omega_{NCO} \times t)$	$I(t) \times sin(\omega_{NCO} \times t) + Q(t) \times cos(\omega_{NCO} \times t)$
010	positive lower sideband	$I(t) \times cos(\omega_{NCO} \times t) + Q(t) \times sin(\omega_{NCO} \times t)$	$I(t) \times sin(\omega_{NCO} \times t) - Q(t) \times cos(\omega_{NCO} \times t)$
011	negative upper sideband	$I(t) \times cos(\omega_{NCO} \times t) - Q(t) \times sin(\omega_{NCO} \times t)$	$-I(t) \times sin(\omega_{NCO} \times t) - Q(t) \times cos(\omega_{NCO} \times t)$
100	negative lower sideband	$I(t) \times cos(\omega_{NCO} \times t) + Q(t) \times sin(\omega_{NCO} \times t)$	$-I(t) \times sin(\omega_{NCO} \times t) + Q(t) \times cos(\omega_{NCO} \times t)$
others	not defined	-	-

The effect of the MODULATION parameter is better viewed after mixing the A and B signal with a LO frequency through an IQ modulator.

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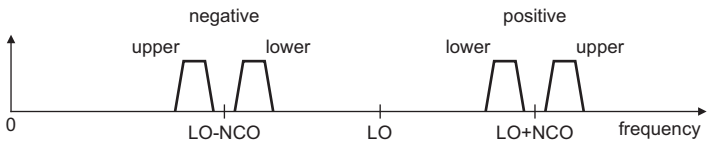


Fig 49. Complex modulation after LO mixing

11.2.3.4 40-bit NCO

The SSBM used the complex signals coming from the NCO (Numerically Controlled Oscillator) to mix the I and Q signals. The 5 registers NCO_FREQ_B0 to NCO_FREQ_B4 over 40 bits (see Table 74) can set the frequency.

The frequency is calculated with Equation 1:

$$f_{NCO} = \frac{NCO_FREQ \times f_s}{2^{40}} \quad (1)$$

Where:

- NCO_FREQ is the value set in the bits NCO_FREQ[39:0] of the NCO frequency registers (see Table 74).
- f_s is the final DAC output clock sampling frequency

The registers NCO_PH_OFFSET_LSB and NCO_PH_OFFSET_MSB over 16 bits from 0° to 360° (see Table 73) can set the phase of the NCO.

11.2.3.5 NCO low power

When using NCO low power (bit NCO_LP_SEL; see Table 72), the five most significant bits of register NCO_FREQ_B4 (bits NCO_FREQ[39:32]; bits [31:0] are masked by zero; see Table 74) can set the frequency.

The frequency is calculated with Equation 2:

$$f_{NCO} = \frac{NCO_FREQ \times f_s}{2^{40}} \quad (2)$$

Where:

- NCO_FREQ is the value set in the masked bits NCO_FREQ[39:0] of the NCO frequency registers (see Table 74).
- f_s is the DAC output clock sampling frequency

11.2.3.6 Minus 3dB

During normal operation, a full-scale pattern is also full-scale at the DAC output. When the I data and the Q data approach full-scale simultaneously, saturation can occur. The Minus 3dB function (bit MINUS_3DB of register DAC_OUT_CTRL; see Table 77) can be used to reduce the 3 dB gain in the modulator. It retains a full-scale range at the DAC output without added interferers.

11.2.3.7 Phase correction

The IQ modulator which follows the DACs can have a phase imbalance resulting in undesired sidebands. By adjusting the phase between the I and Q channels, the unwanted sidebands can be reduced.

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Without compensation the I and Q channels have a phase difference of π / 2 (90°). The registers PH_CORR_CTRL_0 and PH_CORR_CTRL_1(see Table 75) ensure a phase variation from 75.7° to 104.3° by steps 0.0035°. The two registers define a signed value that ranges from –4096 to +4095. The equation: PH_CORR[12:0] / 16384 gives the resulting phase compensation (in radians). The phase correction can be enabled by register PH_CORR_EN (see Table 75).

11.2.3.8 Inverse sin(x) / x

A selectable FIR filter is incorporated to compensate the sin(x) / x effect caused by the roll-off effect of the DAC. The coefficients are represented in Table 19. This feature is controlled by register INV_SINC_SEL (see Table 72).

Table 19. Inversion filter coefficients

Inversion filter		
Lower	**Upper**	**Value**
H(1)	H(9)	+1
H(2)	H(8)	–4
H(3)	H(7)	+13
H(4)	H(6)	–51
H(5)	-	+610

Remark: The transfer function of this features adds some gain to the signals and some saturation can occur with a level of distortion in the output spectrum as result. Update the digital gain accordingly to avoid this saturation.

11.2.3.9 Digital gain

The full-scale output current for each DAC is the sum of the two complementary current outputs:

- $I_{OA(fs)} = I_{IOUTA_P} + I_{IOUTA_N}$
- $I_{OB(fs)} = I_{IOUTB_P} + I_{IOUTB_N}$

The IQ-modulator can have an amplitude imbalance which results in undesired sidebands. The unwanted sideband can be reduced by adjusting the amplitude of signals A and B. The two gains are purely digital and could be enabled by registers DAC_A_GAIN_EN and DAC_B_GAIN_EN (see Table 77).

The output current of DAC A depends on the digital input data and the gain factor defined by bits DAC_A_DGAIN[11:0] of register DAC_A_DGAIN_MSB and register DAC_A_DGAIN_LSB (see Table 76).

$$I_{IOUTA_P} = I_{OA(fs)} \times \frac{(DAC_A_DGAIN[11{:}0])}{4096} \times \left(\frac{DATAA}{65535}\right) \quad (3)$$

$$I_{IOUTA_N} = I_{OA(fs)} \times \left(1 - \frac{(DAC_A_DGAIN[11{:}0])}{4096} \times \left(\frac{DATAA}{65535}\right)\right) \quad (4)$$

The output current of DAC B depends on the digital input data and the gain factor defined by bits DAC_B_DGAIN[11:0] of register DAC_B_DGAIN_MSB and DAC_B_DGAIN_LSB (see Table 76).

$$I_{IOUTB_P} = I_{OB(fs)} \times \frac{(DAC_B_DGAIN[11{:}0])}{4096} \times \left(\frac{DATAB}{65535}\right) \quad (5)$$

$$I_{IOUTB_N} = I_{OB(fs)} \times \left(1 - \frac{(DAC_B_DGAIN[11{:}0])}{4096} \times \left(\frac{DATAB}{65535}\right)\right) \quad (6)$$

Table 20 shows the output current as a function of the input data, when $I_{OA(fs)} = I_{OB(fs)} = 20$ mA.

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Table 20. DAC transfer function

Data	I15 to I0/Q15 to Q0 (binary coding)	I15 to I0/Q15 to Q0 (two's complement coding)	IOUTA_P/ IOUTB_P	IOUTA_N/ IOUTB_N
0	0000 0000 0000 0000	1000 0000 0000 0000	0 mA	20 mA
...	...	...	...	....
32768	1000 0000 0000 0000	0000 0000 0000 0000	10 mA	10 mA
...	...	...	...	...
65535	1111 1111 1111 1111	0111 1111 1111 1111	20 mA	0 mA

11.2.3.10 Auto-mute

The DAC165xD provides a new Auto-mute feature allowing muting the DAC analog output if a conditional event occurs. The Auto-mute feature is based on a state machine as described in Figure 51 and on the control of the digital gains.

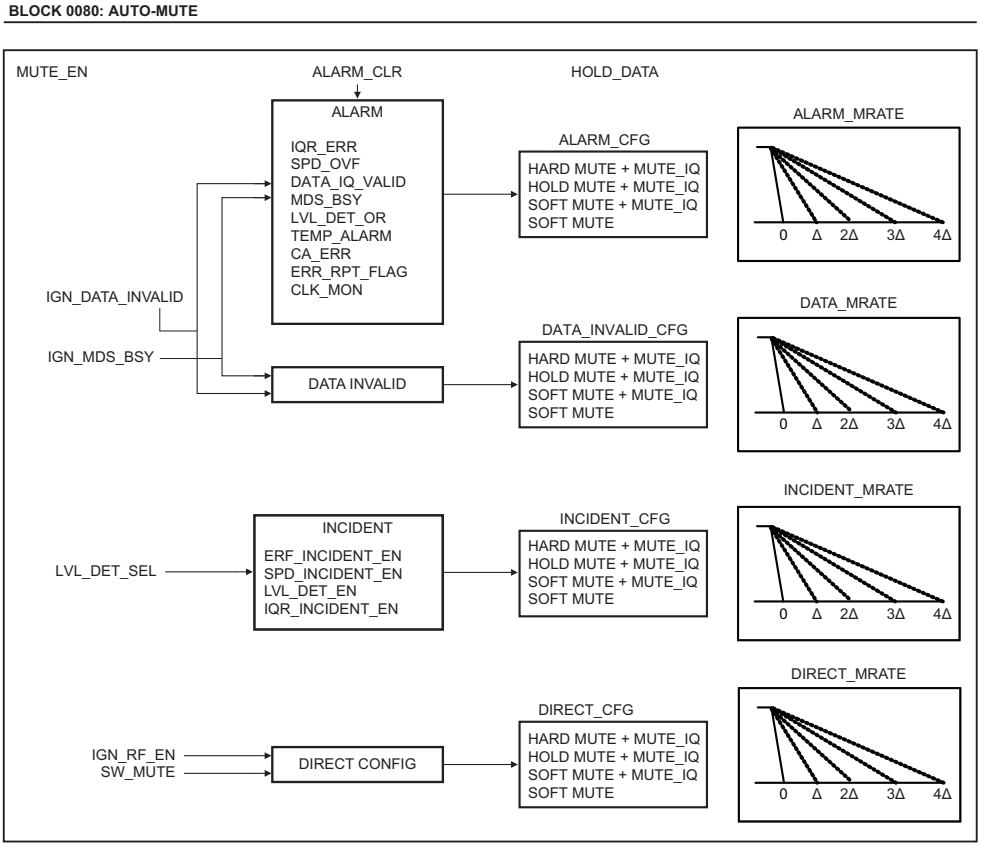


Fig 50. Auto-mute overview

In normal operating mode, the state machine is in IDLE state. The digital gains are specified by the user.

Various mute events can be detected in the DAC. These trigger the MUTE state. Once the MUTE state is entered, the DAC automatically sets the digital gains to zero using several mute actions. The SOFT mute and HOLD mute drops to zero gradually. The HARD mute drop to zero instantly (see Figure 52).

When the digital gains have been set to zero, the state machine enters the WAIT state. In this state, the gains are kept at zero. The state machine stays in this mode until the end of the wait period and the mute event is not de-asserted.

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When the mute event is cleared and the wait period has elapsed, the state machine enters the DEMUTE state. In this state, the digital gains are set again to the initial values. This is done relatively to the mute rate setting. If during this state, a new mute event is triggered, the state machine enters the MUTE state again. The gain decreases from the current gains values, not from the initial ones.

When the digital gains reach the initial values, the state machine enters the IDLE state again.

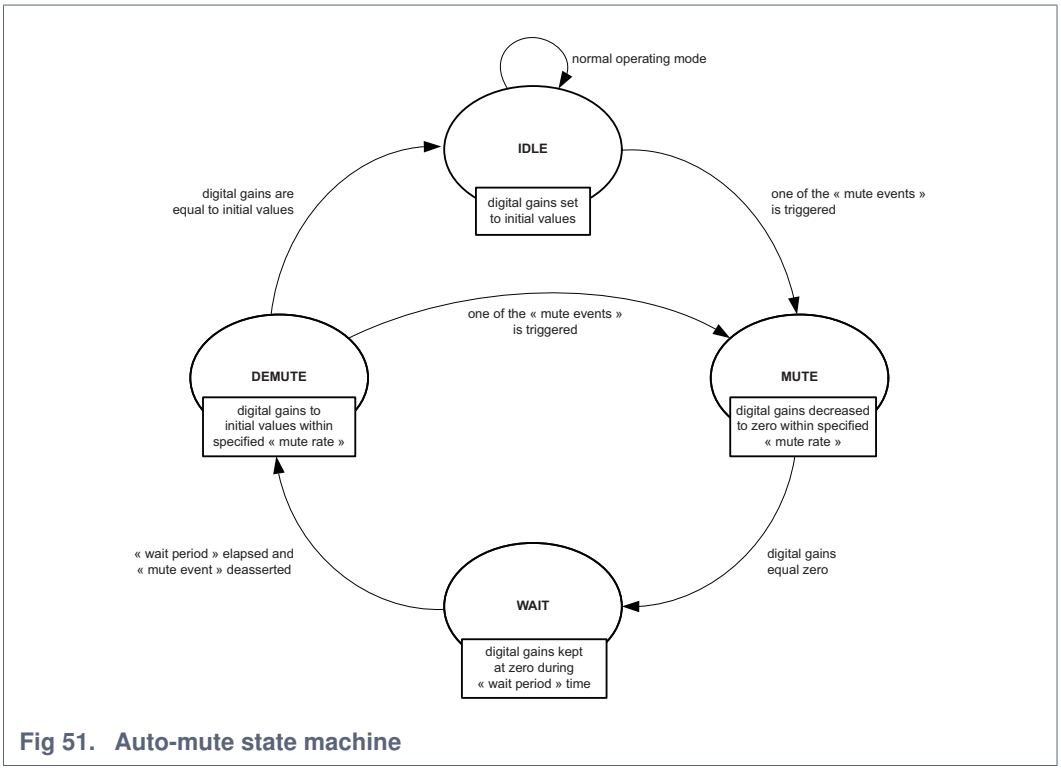


Fig 51. Auto-mute state machine

The mute feature is set by enabling bit MUTE_ENA in register MUTE_CTRL_0 (see Table 85).

Mute events

The MUTE action is triggered by one of the following mute events. Each of them is linked to either an error detection, a status change or signal power monitoring:

- SPI_SW_MUTE:

  Software event that can be requested by the host interface through the SPI bus.
- RF_EN:

  Hardware event that can be requested by the host interface through pin RFTX_ENABLE/IO1
- CLK_MON:

  Event linked to the monitoring of the clocks in the receiver physical layer control block.
- MON_DCLK_ERR:

  Event triggered when a clock error occurs in the CDI (see Section 11.2.6.1).
- CA_ERR:

  Event triggered when a clock error occurs in the DLP (see Section 11.8.3).
- TEMP_ALARM:

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Event triggered when the temperature sensor measures a temperature that exceeds the threshold value. TEMP_SEL_MAN must be specified first (see Table 94).

- ERR_RPT_FLAG:

  Event triggered when DATA_INVALID is detected by the DLP (see Section 11.8.3).

- LVL_DET_OR:

  Event triggered when the signal levels exceed the LVL_DET (see Table 77) on channel X or Y. LVL_DET_EN and LVL_DET must be set first (see Table 77 and Table 78).

- MDS_BSY:

  Event triggered while the MDS process is busy capturing the SYSREF (see Section 11.7.3).

- DATA_IQ_VALID:

  Event is triggered when DATA_INVALID is detected by the DLP (see Section 11.8.3)

- SPD_OVF:

  Event triggered when the Signal Power Detector (SPD) average value is exceeding the threshold value (Section 11.2.4.2).

- IQR_ERR:

  Event triggered when the IQ signal is out of range (see Section 11.2.4.3).

The monitoring of these events can also be done using the interrupt process available in the DAC165xD (see Section 11.8). Once the interrupt is detected, the host controller (e.g. an FPGA) can read back the events flags in registers INTR_FLAGS_0 and INTR_FLAGS_1 (see Table 92) and determine the actions to be taken.

Ignore events option

Set bits IGN_RT_EN, IGN_MDS_BSY, and IGN_DATA_V_IQ of the mute control register (see Table 85) for the mute controller to ignore certain events.

Mute event categories

The MUTE state is entered when one of the mute events is asserted. Four categories of mute events can be distinguished: ALARM, DATA, INCIDENT, and DIRECT (see Table 21).

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Table 21. Mute event categories

Mute event	ALARM[1]		DATA		INCIDENT		DIRECT	
	Enable	Disable	Enable	Disable	Enable	Disable	Enable	Disable
SPI_SW_MUTE							default[2]	
RF_EN							default	IGN_RF_EN
CLK_MON	ALARM_EN [0][3]							
MON_DCLK_ERR	ALARM_EN [1][3]							
CA_ERR	ALARM_EN [2][3]							
TEMP_ALARM	ALARM_EN [3][3]							
ERR_RPT_FLAG	ALARM_EN [4][3]		default		ERF_INCIDENT_EN			
LVL_DET_OR	ALARM_EN [5][3]							
MDS_BSY	ALARM_EN [6][3]		default	IGN_MDS_BSY				
DATA_IQ_VALID	ALARM_EN [7][3]		default	IGN_DATA_V_IQ				
SPD_OVF	ALARM_EN [8][3]				SPD_INCIDENT_EN			
IQR_ERR	ALARM_EN [9][3]				IQR_INCIDENT_EN			

[1] All ALARM mute events can be disabled using bit IGN_ALARM. However, their detection can still be monitored using the INTERRUPT module.

[2] This bit is not auto-clear.

[3] The ALARM mute events must be cleared with bit ALARM_CLR to move from the WAIT state to the DEMUTE state.

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Priority between categories

The priority in which the Auto-mute module evaluates its inputs is:

- Priority 1: DIRECT: controlled via software (SW_MUTE) or hardware (pin IO[1] used as RF_ENABLE)
- Priority 2: ALARM: selectable set of triggers
- Priority 3: DATA: controlled by data path module (DLP, MDS, JESD204B state machine)
- Priority 4: INCIDENT: selectable set of incidents (Signal Power Detector, IQ-Range, Level Detector)

Mute actions

Four mute actions can be selected for each of the four previous mute event categories.

mute IQ: The digital data is reset to its default value (bits I_DC_LVL and Q_DC_LVL; see Table 80) to avoid disturbances in the FIR filters.

Register MUTE_CTRL_1 (see Table 85):

- Hard_mute + mute IQ:

  The digital gains of the DACs are set to zero immediately (within 1 DAC clock period). The digital path is filled with the default I and Q levels.
- Hold_mute + mute IQ:

  The outputs of the DACs are kept to the latest good value (within 1 DAC clock period). The digital path is filled with the default I and Q levels.

  Remark: Bit HOLD_DATA (see Table 85) must be enabled for this action. If this bit is not set, the overall Hold_mute + mute IQ actions are not taken into account.
- Soft_mute + mute IQ:

  The digital gains of the DACs are swept down to zero at the x_MUTE_RATE value (see Table 87). The digital path is filled with the default I and Q levels.
- Soft_mute:

  The outputs of the DACs are swept down to zero at the x_MUTE_RATE value (see Table 87). The digital path is kept with the received values.

Remark: As the DC offsets are applied after the digital gain, the outputs are still impacted by their values, even if a mute action event occurs.

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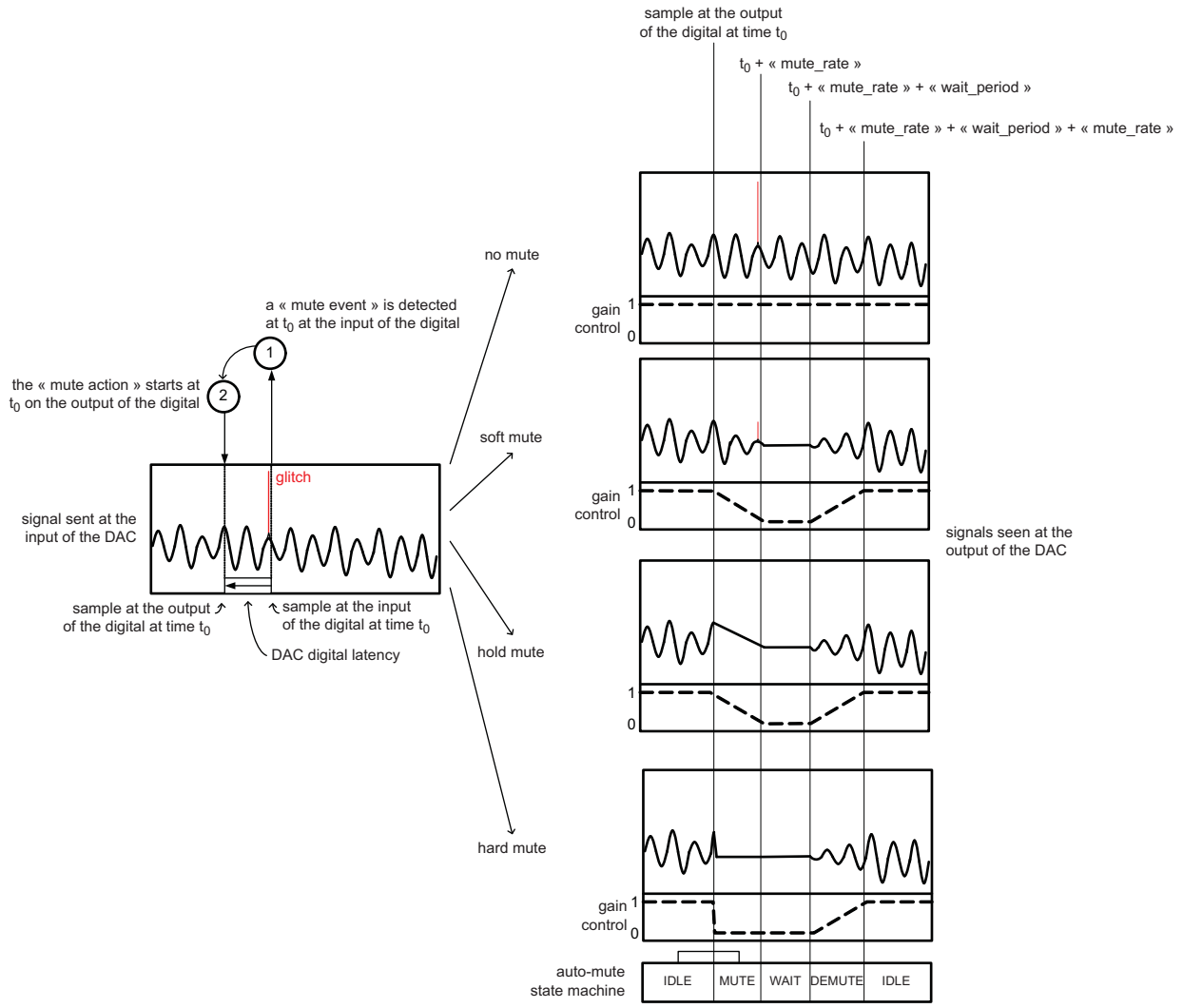


Fig 52. Mute actions representation

Mute rate

The time period used to decrease or increase the gains during a MUTE or DEMUTE state is called mute rate. Each mute action category has its own mute rate available through the registers ALARM_MRATE, DATA_MRATE, INCIDENT_MRATE and DIRECT_MRATE.

Table 22. Mute rate availability
Through ALARM_MRATE, DATA_MRATE, INCIDENT_MRATE, and DIRECT_MRATE.

DAC clock	750 MHz	1 GHz	1.5 GHz	1.76 GHz
Period ×8 (ns)	10.67	8.00	5.33	4.54
Value	Mute rate (ns)	Mute rate (ns)	Mute rate (ns)	Mute rate (ns)
0000	10.67	8.00	5.33	4.54
0001	21.34	16.00	10.66	9.09
0010	42.68	32.00	21.32	18.18

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Table 22. Mute rate availability *...continued*
Through ALARM_MRATE, DATA_MRATE, INCIDENT_MRATE, and DIRECT_MRATE.

DAC clock	750 MHz	1 GHz	1.5 GHz	1.76 GHz
Period ×8 (ns)	10.67	8.00	5.33	4.54
Value	Mute rate (ns)	Mute rate (ns)	Mute rate (ns)	Mute rate (ns)
0011	85.36	64.00	42.64	36.36
0100	170.72	128.00	85.28	72.72
0101	341.44	256.00	170.56	145.45
0110	682.88	512.00	341.12	290.90
0111	1,365.76	1,024.00	682.24	581.81
1000	2,731.52	2,048.00	1,364.48	1163.63
1001	3,642.47	2,731.00	1,819.53	1551.71
1010	5,463.04	4 096.00	2,728.96	2327.27
1011	7,283.61	5,461.00	3,638.39	3102.84
1100	10,926.08	8,192.00	5,457.92	4654.54
1101	14,557.88	10,915.00	7,272.12	6201.71
1110	21,852.16	16,384.00	10,915.84	9309.09
1111	43,704.32	32,768.00	21,831.68	18618.18

Mute wait period

The wait period time can be calculated with Equation 7:

$$wait\ period = (MUTE_WAIT_PERIOD + 1) \times 8 \times DAC_CLK_PERIOD \quad (7)$$

At 1 Gsps, this gives a wait period between 8 ns and 527 μs.

DEMUTE triggering

When the mute action is either a DIRECT, an INCIDENT or a DATA mute action, the WAIT state is enabled as long as the wait period is not elapsed and the event is not released.

When the mute action is an ALARM mute action, the WAIT state is enabled as long as the alarm controller is not reset using bit ALARM_CLR (see Table 85).

11.2.3.11 Digital offset adjustment

When the DAC165xD analog output is DC connected to the next stage, the digital offset correction (bits DAC_A_OFFSET[15:0] and DAC_B_OFFSET[15:0]; see Table 79) can be used to adjust the common-mode level at the output of each DAC. Table 23 shows the variation range of the digital offset.

Table 23. Digital offset adjustment

DAC_A_OFFSET[15:0] DAC_B_OFFSET[15:0] (two's complement)	Offset applied
1000 0000 0000 0000	–32768
1000 0000 0000 0001	–32767
...	...
1111 1111 1111 1111	–1

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Table 23. Digital offset adjustment …continued

DAC_A_OFFSET[15:0] DAC_B_OFFSET[15:0] (two's complement)	Offset applied
0000 0000 0000 0000	0
0000 0000 0000 0001	+1
...	...
0111 1111 1111 1110	+32766
0111 1111 1111 1111	+32767

Care should be taken when adding DC offset to large signal.The resulting signal might exceeds the 16 bits dynamic of the DAC.

11.2.4 Signal detectors

11.2.4.1 Level detector

A level detector feature is available at the end of the digital path. It can be enabled using bit LVL_DET_EN (see Table 77). This feature specifies a signal output range limited (or clipped) to −128 × LVL_DET to +128 × LVL_DET around the half Full-Scale (FS) (see Table 78). If the signal value enters the upper or lower clipping area, it is clipped to +128 × LVL_DET or −128 × LVL_DET, respectively). Figure 53 shows this behavior.

Use this feature in combination with the auto-mute feature to avoid unexpected spectral spurs after the clipping of the signal (see Section 11.2.3.10).

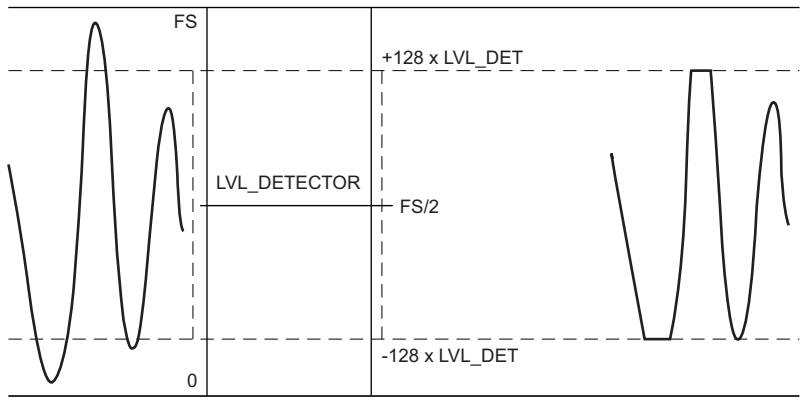


Fig 53. Level detector operation

Table 24. Level detector values

LVL_DET[7:0]	Peak excursion from full-scale / 2	Code output range (binary offset)	dBFS value 10log(peak excursion x 2 / 65536)
00h	0	32768	NaN
...		...	...
19h	3200	32568 to 35968	−10.1 dBFS
...		...	...
80h	16384	16384 to 49152	−3 dBFS
...		...	...

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Table 24. Level detector values …continued

LVL_DET[7:0]	Peak excursion from full-scale / 2	Code output range (binary offset)	dBFS value 10log(peak excursion x 2 / 65536)
CBh	25984	6784 to 58752	-1 dBFS
...		...	...
FFh	32767	0 to 65535	0 dBFS

11.2.4.2 Signal Power Detector (SPD)

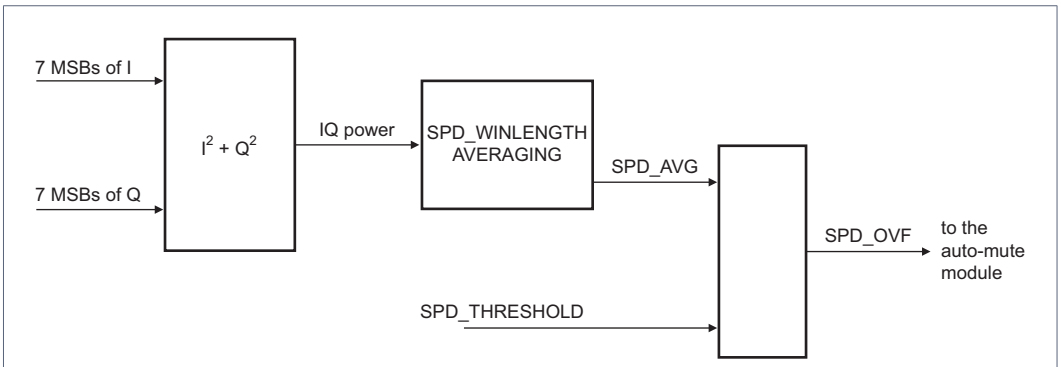


Fig 54. Signal power detector

The Signal Power Detector (SPD) takes the 7 MSBs of the I and Q signal to determine the IQ power of an IQ-pair. Averaging is done over the programmable number (2^6, 2^7 to 2^{21}) of IQ-pairs using the SPD_WINLENGTH register (see Table 82). If the SPD_AVG bit (see Table 83) exceeds the 16-bits threshold value, the SPD overflow (SPD_OVF) flag becomes active and can invoke a mute action depending on the mute control settings.

The SPD can have a large response time because of the samples average based algorithm. This must be taken into account at system level.

11.2.4.3 IQ Range (IQR)

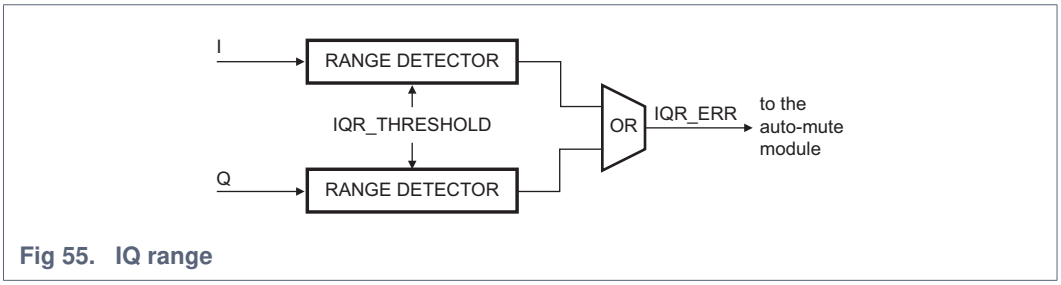


Fig 55. IQ range

The IQ range detector checks if the I and Q signal values are within the range specified by register IQR_THRESHOLD (see Table 89) compared to the center value (= 0 if the data are in 2 complement's representation or 32768 if the data are in binary offset representation):

–IQR_THRESHOLD < I – center value < +IQR_THRESHOLD

–IQR_THRESHOLD < Q – center value < +IQR_THRESHOLD

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11.2.5 Pin RF_ENABLE

A RF_ENABLE pin is available to shutdown the analog output of the DACs. The shutdown consists in a MUTE request on the MUTE controller. This trigger is active low and is part of the DIRECT_CFG mute events container (see Section 11.2.3.10). This means that to enable the DACs output, a signal high needs to be applied on the pin. When applying a signal low, the MUTE controller will mute the DACs output.

Pin 9 is a multipurpose pin and needs to be properly configured to act as the RF_ENABLE feature. Because the RF_ENABLE feature is using the MUTE controller, it needs to be configured too.

The following registers must be set to configure pin 9 in RF_ENABLE mode (these are the default values at start-up time):

- IO_DIR[1] must be set to '0' to set the pin to input mode (see Table 67)
- IGN_RF_EN (see Table 85) must be disabled to allow the triggering of the event
- MUTE_ENA (see Table 85) must be enabled

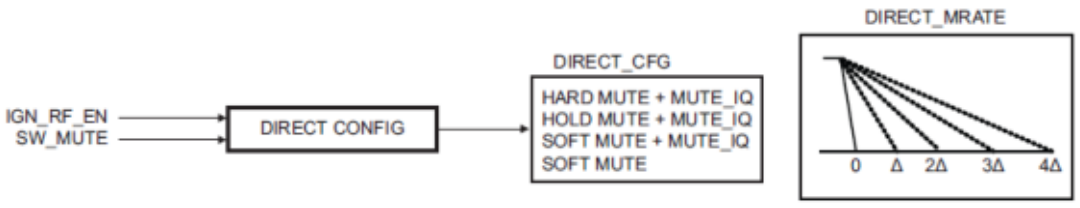


Fig 56. RF_ENABLE trigger in MUTE controller

11.2.6 Analog core of the dual DAC

This section refers to the analog configuration required to set up the dual DAC core. The clock and output stages are described as well as the internal registers (Block x0020; see Figure 57 and Table 54) used to configure the clock tree inside the chip.

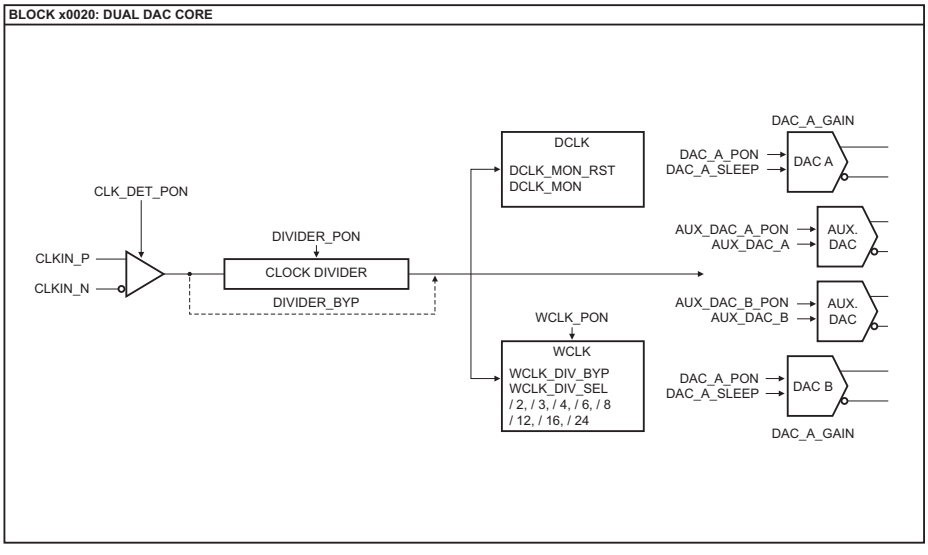


Fig 57. Dual DAC core overview

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11.2.6.1 Clocks

The DAC165xD requires one single differential clock (CLKIN_P, CLKIN_N) for the whole device (including the digital data path, the dual DAC core and the JESD204B interface).

During the reset phase (RESET_N asserted), the input clock must be stable and running, ensuring a proper reset of the complete device.

Clock input external configuration

The DAC165xD incorporates one differential clock input, CLKIN_N/CLKIN_P, with embedded 100 Ω differential resistor. The clock input can be LVDS but it can also be interfaced with CML.

The clock input buffer is self biased, so an AC coupling circuit could be used and this is the recommended usage. The minimum requested differential voltage is about 500mVpp,diff but a higher voltage swing of 1000mVpp,diff will give better results. In case of AC coupling, the DAC165xD self-biased clock common mode voltage is typically 800mV. When using DC coupling the common mode level has to be set around this 800mV level. It is recommended to use AC coupling for LVDS.

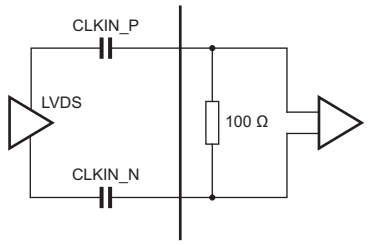


Fig 58. LVDS clock configuration

Clock frequency input range

The DAC165xD can only operate in two modes:

- Direct clocking mode:

  The input clock frequency is limited to 2 GHz
- Divided clocking mode:

  The input clock is internally divided by 2, 4, 6, or 8. The maximum input frequency is 3 GHz. This mode allows the programming of the group delay feature.

Clocks internal configuration

The following registers must be specified to configure the DAC165xD clocking mode:

- WCLK_GENCFG to specify the WCLK configuration (see Table 56)
- DCKDIV_CFG to specify the DCLK configuration and the divider / group delay feature (see Table 60)
- PON_DCKDIV_CFG to power on the clock divider (required only for divided clock) (see Table 58)

The final clock is referred to as the "DAC clock". This is the clock that is going directly to the dual DAC core and is running at maximum speed. From this DAC clock two digital clocks are derived: DCLK and WCLK.

DCLK is the digital clock used for all logic related to the Digital Signal Processing (DSP) of the DAC. DCLK is automatically generated from the registers PON_DAC_CORE_CFG_0, INTERPOLATION (see Table 72) and CDI_MOD (see Table 69). Registers MON_DCLK (see Table 70) and CLK_MON_RST (see Table 56) can be used to monitor this automatic generation. This flag can also raise the interrupt feature (see Interrupt section).

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WCLK is the digital clock used for all logic related to the Digital Lane Processing (DLP) of the input interface. The divider ratio WCLK_DIV_SEL (see Table 56) must be specified using the following equation:

$$\frac{WCLK}{DAC_Clock} = \frac{M}{(L \times INTERPOLATION)} \quad (8)$$

Where:

- M stands for the number of DACs used inside the DAC165xD (M = 2)

  Remark: DAC165xD is a dual core device therefore M = 2. It is possible to use the device in a single core manner, but the configuration must still be set to M = 2 and the related lanes and DAC core must be powered off.
- L stands for the number of serial input lanes used (L = 1, L = 2, or L = 4)
- INTERPOLATION stands for the interpolation factor specified in register INTERPOLATION (see Table 72).

Table 25 shows the results for nominal use cases

Table 25. WCLK_DIV selection

LMF configuration	Interpolation ratio	WCLK/DAC clock	WCLK_DIV_BYP	WCLK_DIV_SEL
421 / 422	2	1/4	0	010
	4	1/8	0	100
	8	1/16	0	110
222	2	1/2	0	000
	4	1/4	0	010
	8	1/8	0	100
124	2	1	1	xxx
	4	1/2	0	000
	8	1/4	0	010
211	2	1/2	0	000
	4	1/4	0	010
	8	1/8	0	100

Clock divider and Group Delay configuration

To enable the Clock division, the dividers biasing should be powered on using PON_DCKDIV_1 and PON_DCKDIV_2 (see Table 58). Then the division ratio CLKDIV_SEL_DIV needs to be configured and the default bypass mode must be disabled (CLKDIV_CLK_BYP) see Table 60. In this mode, the CLKDIV_SEL_PHASE bits are used to specify the group delay phase. The CLKDIV_SEL_DIV must be set during the DAC initialization phase only (see Table 60).

When changing the DAC clock phase during nominal usage, the DAC output will be kept at the previous value while the new phase is set. For instance, setting the DAC clock phase from setting 0 to setting 1 will imply a 1.5 DAC clock constant value. No glitches are expected during this phase.

Table 26. CLKDIV_SEL_PHASE selection

CLKDIV_SEL_PHASE	
000	DAC clock phase = 0
001	DAC clock phase = 1 x (CLK IN period) /2
010	DAC clock phase = 2 x (CLK IN period) /2
011	DAC clock phase = 3 x (CLK IN period) /2
100	DAC clock phase = 4 x (CLK IN period) /2

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Table 26. CLKDIV_SEL_PHASE selection *...continued*

CLKDIV_SEL_PHASE	
101	DAC clock phase = 5 x (CLK IN period) /2
110	DAC clock phase = 6 x (CLK IN period) /2
111	DAC clock phase = 7 x (CLK IN period) / 2

Clock Domain Interface (CDI)

A CDI logic handles the error-free data transition from the WCLK clock domain to the DCLK domain. It consists of 12 buffers that absorb the phase variation between the two clocks. The reliability of the data transmission depends on the clock-frequency ratios and therefore on the interpolation mode. The CDI must be set in the same mode as the interpolation ratio to be properly configured. This mode is configured with register CDI_CTRL (see Table 69).

Table 27. Interpolation and CDI modes

Interpolation	CDI mode	Maximum input data rate (Msps)
		DAC165xD2G0 / DAC165xD1G5 / DAC165xD1G0
~1	Mode 0 (^2)	1000
×2	Mode 0 (^2)	1000
×4	Mode 1 (^4)	500
×8	Mode 2 (^8)	250

Ideally, buffer number 11 is selected as the reference. If jitter of +/- 1 clock cycle is injected between the clocks occurs, the pointer can oscillate between buffers 10 and 0. If more jitter is injected, the range increases to buffers 9 and 1, etc.

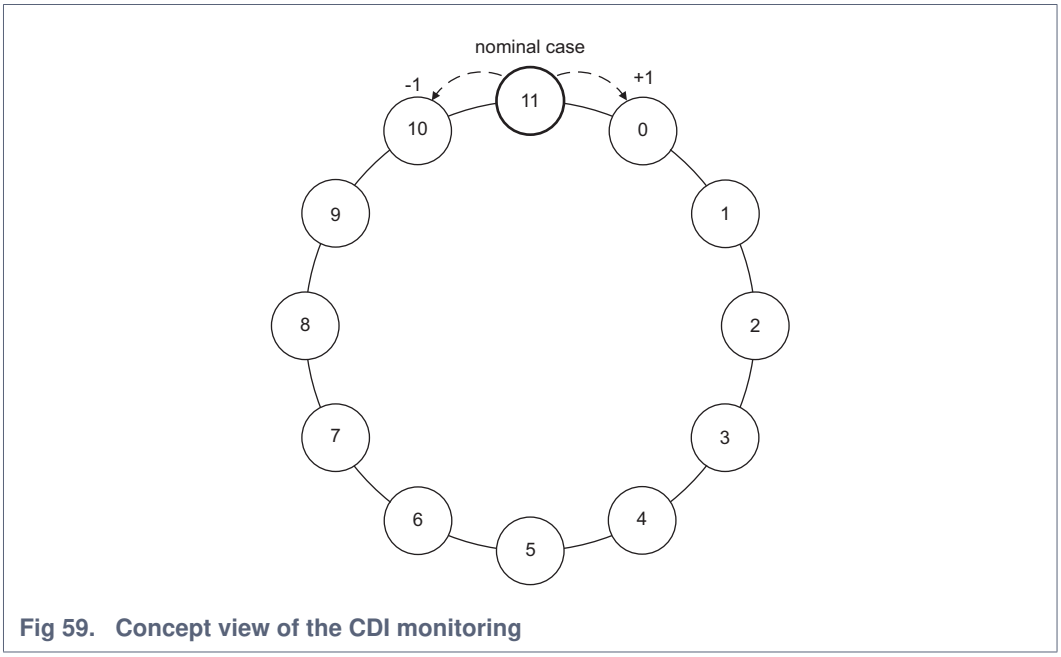


Fig 59. Concept view of the CDI monitoring

This buffer position can be monitored using register MON_DCLK (see Table 70).

The variation of the buffer location could also raise an interrupt (see Section 11.8).

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11.3 Overall Latency

The implementation of the different features of the DAC165xD imply a different latency regarding the mode used. This latency is dependent of the following features:

1. the LMF-S configuration
2. the Interpolation mode
3. the Phase Correction usage
4. the SSBM/NCO usage
5. the InvSin(x)/x usage

The total latency is expressed in DAC clock cycles and could therefore be scaled regarding the DAC clock frequency used. Moreover, the values of the table are showing the uncertainties due to the internal design implementation. There are two buffers/fifo that are used to compensate the skew between the lanes (ILA_MON_L_LN_xx see Table 126) and to delay the data path (MDS_MAN_ADJ_DLY see Table 106). The values of the table are provided for the case when all the lanes are aligned (ILA_MON_LN_xx = 8 by default) and the MDS_MAN_ADJ_DLY is set to 0 (minimal delay). See Table 29 for additional delays.

Remark: The overall latency values are given when the MDS feature is not used.

Table 28. Latency for LMF-S (without MDS, Phase correction, SSBM, and InvSin x/x)

LMF-S	Interpolation	Total latency DAC clk		
		min	avg	max
421-1 or 422-2	x2	250	254	266
	x4	420	424	444
	x8	740	744	780
222-1	x2	216	220	228
	x4	352	356	368
	x8	588	592	612
124-1	x2	195	199	205
	x4	310	314	322
	x8	504	508	520

Table 29. Additional latency

Digital feature	Additional latency
Lanes skew compensation	+/- 7 wclk (see Table 25 for the DAC clock ratio)
MDS_MAN_ADJ_DLY	0 to 256 DAC clk
Phase Correction	+16 DAC clk
SSBM/NCO	+16 DAC clk
InvSin(x)/x	+4 DAC clk

11.4 Analog dual DAC core

The DAC165xD core consists of two DACs. Each of them can be independently set to Power-down mode if using the DAC in single channel mode is preferred (DAC_A_PON, DAC_B_PON; see Table 55).

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11.4.1 Regulation

The DAC165xD reference circuitry integrates an internal band gap reference voltage which delivers a 0.7 V reference on the GAPOUT pin. Decouple pin GAPOUT using a 100 nF capacitor.

The reference current is generated via an external resistor of 562 Ω (1 %) connected to VIRES.

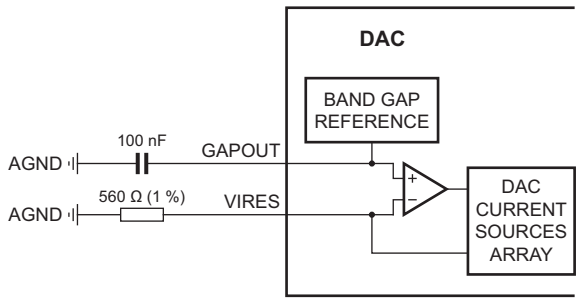


Fig 60. Internal reference configuration

Figure 60 shows the optimal configuration for temperature drift compensation because the band gap reference voltage can be matched to the voltage across the feedback resistor.

The DAC current can also be adjusted by applying an external reference voltage to the non-inverting input pin GAPOUT and disabling the internal band gap reference voltage (bit BGAP_PON; see Table 55).

11.4.2 Full-scale current adjustment

The default full-scale current ($I_{O(fs)}$) is 20 mA. However, further adjustments, ranging from 10 mA to 30 mA, can be made to both DACs independently using the SPI interface. The registers values allowed to reach lower and higher current values but those values are out the range that maintains the typical dynamics performances.

The settings applied to DAC_A_AGAIN[9:0] (see Table 61) define the full-scale current of DAC A:

$$I_{O(fs)}\ \mu A = DAC_A_AGAIN_X2 \times DAC_A_AGAIN[9{:}0] \times 25 \quad (9)$$

The DAC_B_AGAIN[9:0] (see Table 61) define the full-scale current of DAC B:

$$I_{O(fs)}\ \mu A = DAC_B_AGAIN_X2 \times DAC_B_AGAIN[9{:}0] \times 25 \quad (10)$$

11.5 Analog output

11.5.1 DAC1658D: High common-mode output voltage

The device has two output channels, each producing two complementary current outputs, which enable the reduction of even-order harmonics and noise. The pins are IOUTA_P/IOUTA_N and IOUTB_P/IOUTB_N. Connect these pins using a load resistor R_L to the 3.3 V analog power supply ($V_{DDA(3V3)}$).

Figure 61 shows the equivalent analog output circuit of one DAC. This circuit includes a parallel combination of NMOS current sources and associated switches for each segment.

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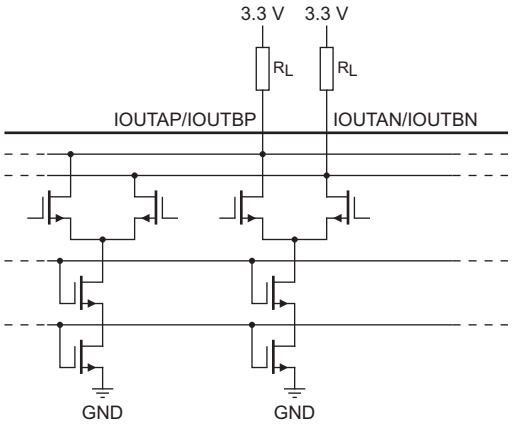


Fig 61. Equivalent analog output circuit

The cascode source configuration increases the output impedance of the source, which improves the dynamic performance of the DAC because there is less distortion.

Depending on the application, the various stages and the targeted performances, the device can be used for an output level of up to 2 V (p-p) with degraded performances. To reach optimal performances a value of 1 V (p-p) differential is strongly advised.

11.5.2 DAC1653D: Low common-mode output voltage

The device has two output channels, each producing two complementary current outputs, which enable the reduction of even-order harmonics and noise. The pins are IOUTA_P/IOUTA_N and IOUTB_P/IOUTB_N. Connect these pins using a load resistor R_L to the analog ground (GND).

Figure 62 shows the equivalent analog output circuit of one DAC. This circuit includes a parallel combination of PMOS current sources and associated switches for each segment.

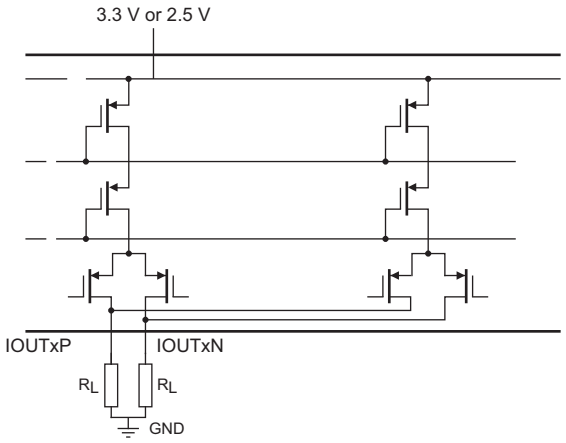


Fig 62. Equivalent analog output circuit

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11.5.2.1 Auxiliary DACs

The DAC165xD integrates two auxiliary DACs, which are used to compensate any offset between the DACs and the next stage in the transmission path. Both auxiliary DACs have a 10-bit resolution and are current sources (referenced to ground). Both of them can be disabled using bits DAC_A_AUX_PON and DAC_B_AUX_PON of the Auxiliary DACs registers (see Table 62).

The full-scale output current for each DAC is the sum of the two complementary current outputs:

$$I_{OAUXA(fs)} = I_{AUXA_P} + I_{AUXA_N}$$

$$I_{OAUXB(fs)} = I_{AUXB_P} + I_{AUXB_N}$$

The output current depends on the digital input data set by SPI registers DAC_A_AUX_MSB (bits DAC_A_AUX[9:8]), DAC_A_AUX_LSB (bits DAC_A_AUX[7:0]), DAC_B_AUX_MSB (bits DAC_B_AUX[9:8]) and DAC_B_AUX_LSB (bits DAC_B_AUX[7:0]; see Table 62).

$$I_{AUXA_P} = I_{OAUXA(fs)} \times \left(\frac{\text{DAC_A_AUX[9:0]}}{1023}\right) \quad (11)$$

$$I_{AUXA_N} = I_{OAUXA(fs)} \times \left(\frac{1023 - \text{DAC_A_AUX[9:0]}}{1023}\right) \quad (12)$$

$$I_{AUXB_P} = I_{OAUXB(fs)} \times \left(\frac{\text{DAC_B_AUX[9:0]}}{1023}\right) \quad (13)$$

$$I_{AUXB_N} = I_{OAUXB(fs)} \times \left(\frac{1023 - \text{DAC_B_AUX[9:0]}}{1023}\right) \quad (14)$$

Table 30 shows the output current as a function of the auxiliary DACs data DATAA and DATAB Equation 11 to Equation 14.

Table 30. Auxiliary DAC transfer function

DATAA / DATAB	DAC_A_AUX[9:0]/DAC_B_AUX[9:0] (binary coding)	I_{AUXA_P} / I_{AUXB_P} (mA)	I_{AUXA_N} / I_{AUXB_N} (mA)
0	00 0000 0000	0	2.3
...	...	...	...
512	10 0000 0000	1.15	1.15
...	...	...	...
1023	11 1111 1111	2.3	0

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11.6 Temperature sensor

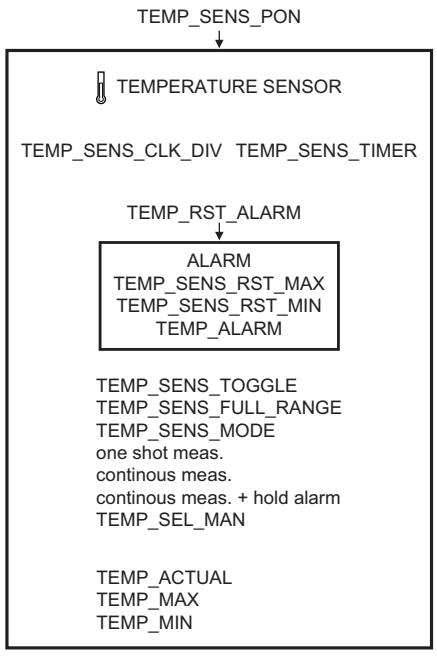


Fig 63. Temperature sensor

The DAC165xD embeds a temperature sensor to monitor the temperature inside the chip. This module is based on a 6-bit resolution ADC clocked at DAC_CLK / (8 × TEMP_CLK_DIV). The mode of measurements is configurable as a one shot measurement, continuous measurements or continuous measurements with alarm flag held in case of temperature exceeding a preset threshold. In continuous mode, the measurement is done every TEMP_SENS_TIMER cycles. The TEMPS_LVL specifies the threshold level that is compared with the measured value. If the measured value exceeds the threshold, the TEMP_ALARM flag is set and triggers a mute action (see Section 11.2.3.10). The maximum and minimum temperatures measured are stored in registers TEMP_MAX (see Table 98) and TEMP_MIN (see Table 99). The current temperature is stored in register TEMP_ACTUAL (see Table 97). Once the TEMP_ALARM flag is set, it must be reset using the TEMP_SENS_RST_ALARM bit of the temperature sensor control register (see Table 93). The maximum and minimum temperature can also be reset using bits TEMP_SENS_RST_MAX and TEMP_SENS_RST_MIN of the temperature sensor control register (see Table 93).

The value stored in the maximum, current, and minimum registers represents the output value of the ADC. This value must be matched to the real temperature.

$$T\ (°C) = \alpha \times ADC_value - offset \quad (15)$$

Where:

- α = 4.64 °C
- ADC_value is either TEMP_MAX, TEMP_MIN or TEMP_ACTUAL
- offset = 50.34 °C

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11.7 Multiple Device Synchronization (MDS); JESD204B subclass I

The MDS feature enables multiple DAC channels to be sampled synchronously and phase coherently to within one DAC clock period. This feature is part of the JESD204B standard but the implementation adds some unique features that simplify the PCB design. The alignment of the data is certified within one DAC clock cycle, however, the kick-off of the NCO is not synchronous to the SYSREF and will create a NCO carrier phase difference up to eight DAC clock cycles. Refers to the “MDS guidelines” application note to have more information on this topic.

11.7.1 Non-deterministic latency of a system

In a system using multiple DAC devices, there are numerous sources of timing uncertainties. Figure 64 gives an overview of these uncertainties.

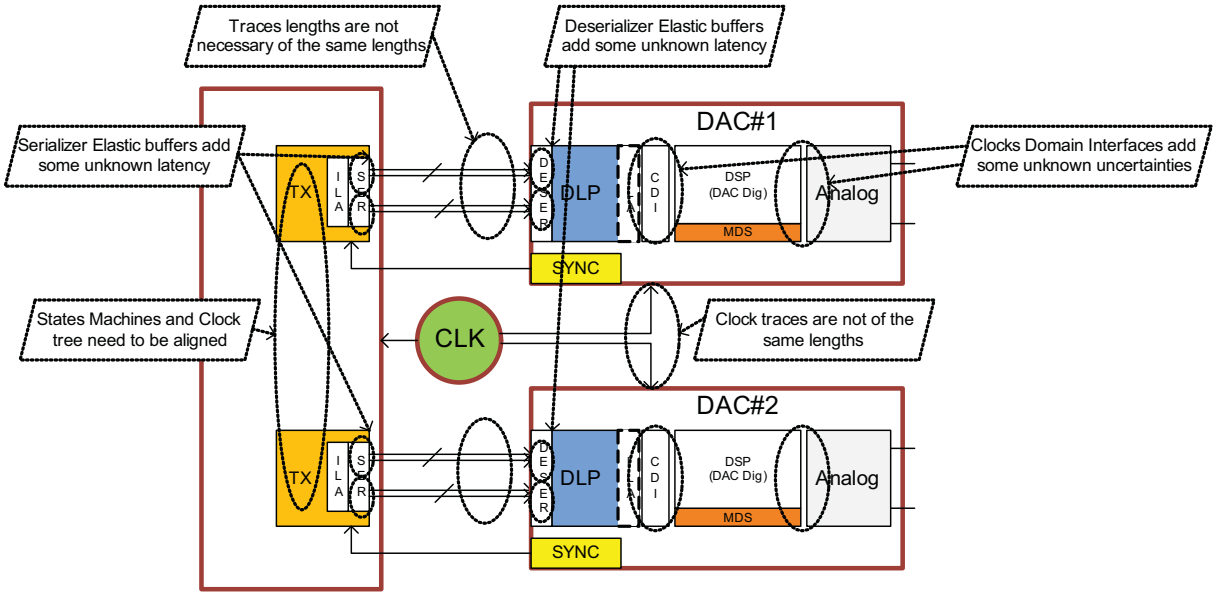


Fig 64. Timing uncertainties when using multiple DAC devices

The sources of uncertainties are shared between the Transmitter devices (TX), the Receiver devices (RX), the PCB layout and the architectures of the JESD204B system clocks. A single device can detect timing drift and uncertainties, but not at system level. Therefore a synchronization process is required to enable the system to output the analog signals of all the RX devices in a coherent way. Moreover, the system becomes predictable if from one start-up to another one, the overall latency is deterministic.

The MDS feature of the DAC165xD has been implemented in accordance with the JESD204B subclass 1 specification to fulfill these requirements.

11.7.2 JESD204B system clocks and SYSREF clock

There are various system 'clocks' that are used in the JESD204B specification. However, only one of them is seen at system level, the device clock, which is provided to the device. The other clocks are related to the JESD204B standard and are used to assemble/deassemble the data in octets and then in 10B words (see JESD204B standard). Figure 65 and Table 31 show the relationship between them.

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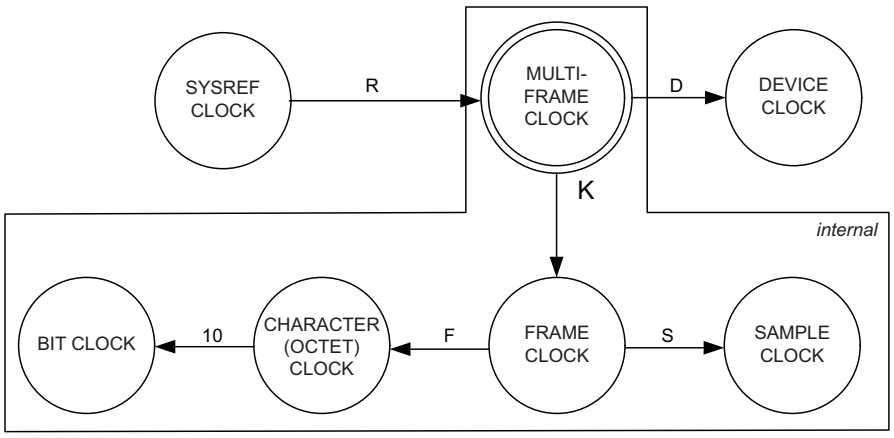


Fig 65. JESD204B system clocks

Table 31. Relationship between various clocks

Clock name	Ratio with respect to multi-frame clock	Comments regarding JESD204B specification
multi-frame clock	1	-
frame clock	× K	Ceil(17 / F) ≤ K ≤ min(32, floor(1024 / F))
character clock	× F × K	F = 1 to 256
bit clock	× 10 × F × K	8b/10b encoding
sample clock	× S × K	S = 1 to 32
device clock	× D	D is integer
sysref clock	/ R	R is integer

As all clocks can be derived from the Multi-Frame Clock (MFC), this clock becomes the reference for a JESD204B system. Each device used in the system has its own local version of the MFC. These local version are called Local Multi-Frame Clock (LMFC). Due to the timing uncertainties the phase relationships between all the device LMFCs are unknown. The goal of MDS is to be able to realign all LMFCs in a deterministic and accurate way.

To align all the LMFCs within the system, a new clock named SYSREF (SYStem REFerence) is used. This clock is linked to the multi-frame clock by a divided ratio R, therefore it is a low frequency signal.

The SYSREF signals must be propagated to all the devices of the system. They are used as a timing reference to align the internal LMFC of each devices. To ensure that all phases of the signals are aligned at the source, the SYSREF signals and the device clocks must be generated from the same clock IC (see Figure 66). The appropriate clock device could be found within the IDT Timing Division unit portfolio.

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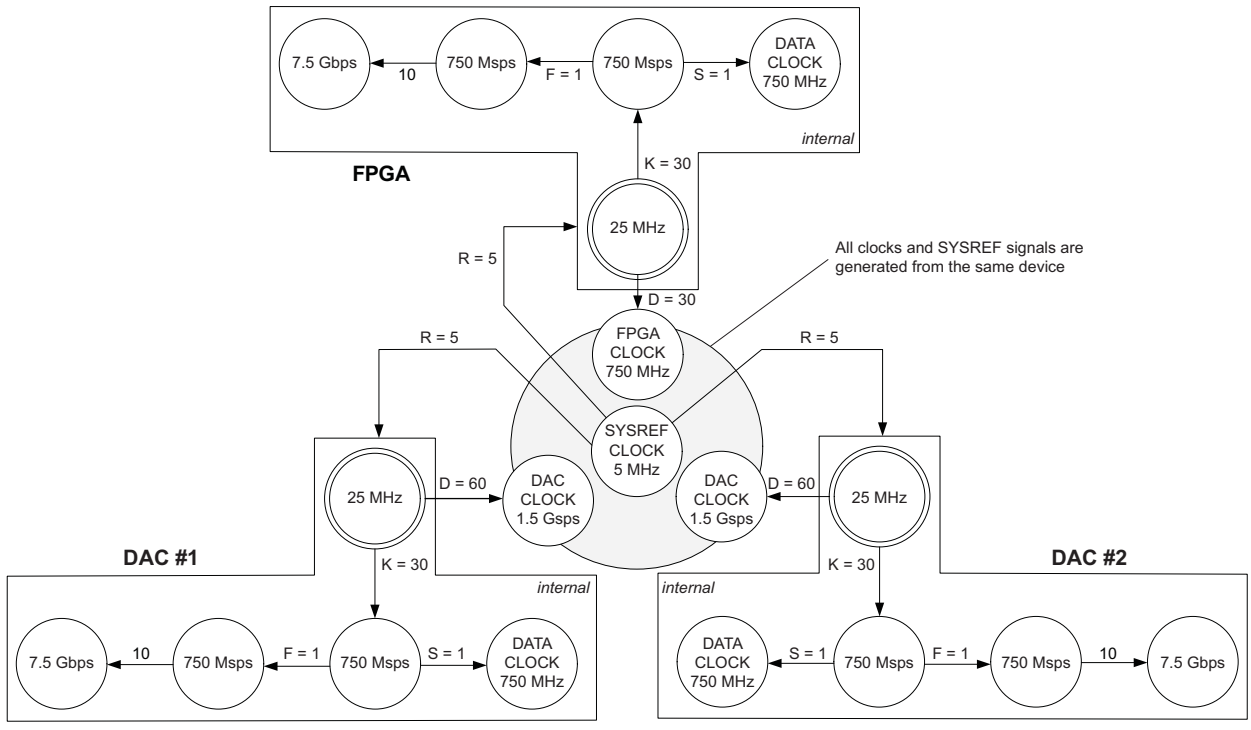


Fig 66. System overview

All the JESD204B devices will capture their SYSREF signal and use it to align their datastream/LMFC. The edge detection of the SYSREF signal is used as a system timing reference and the device align their LMFCs phase to the closest edge of the SYSREF. To ensure an accurate alignment within all devices, the SYSREF signal must show the same phase at the input port of all the devices to synchronize. Therefore, the trace lengths of the SYSREF signals must be equal for all the DAC devices.

The DAC165xD embeds updated SYSREF buffers. Both West and East side are using the incoming SYSREF signal asynchronously to remove the uncertainties due to the sampling moment inside each devices. There is no more setup and hold constraint on the SYSREF signal.

The following figure shows the virtual LMFCs before and after alignment to the SYSREF clock.

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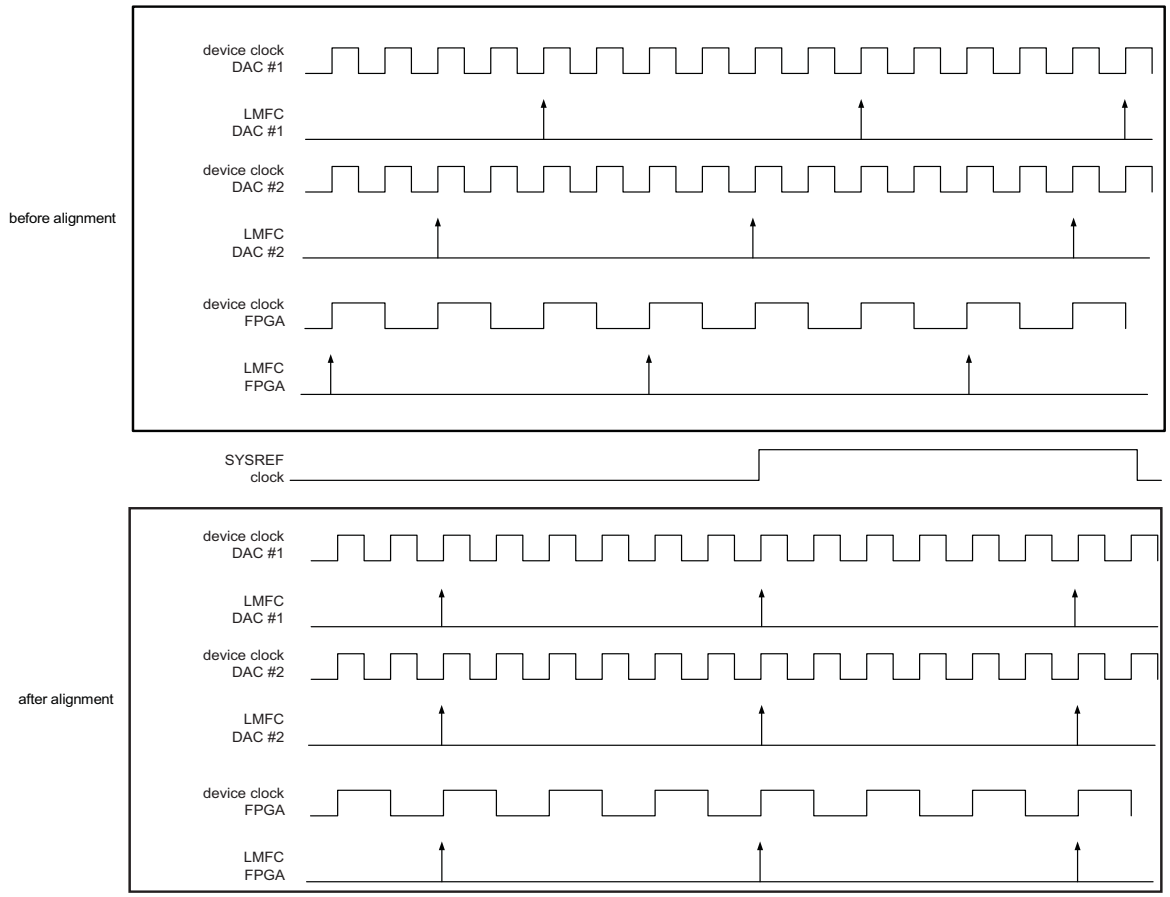


Fig 67. LMFCs before and after alignment to the SYSREF clock

11.7.3 MDS implementation

The DAC165xD MDS implementation is based on two modules as described in Figure 68:

- **M1**:

  This module contains the SYSREF detector and the control loop used to create a $LMFC_{DAC}$ signal. The control loop is clocked with the digital clock. The digital clock equals DAC clock / 8.

- **M2**:

  This module compares the phase of the $LMFC_{RCV}$ received from the JESD204B digital lane processing to the phase of the $LMFC_{DAC}$ and shifts the position of the buffer to align the data path to the $LMFC_{DAC}$.

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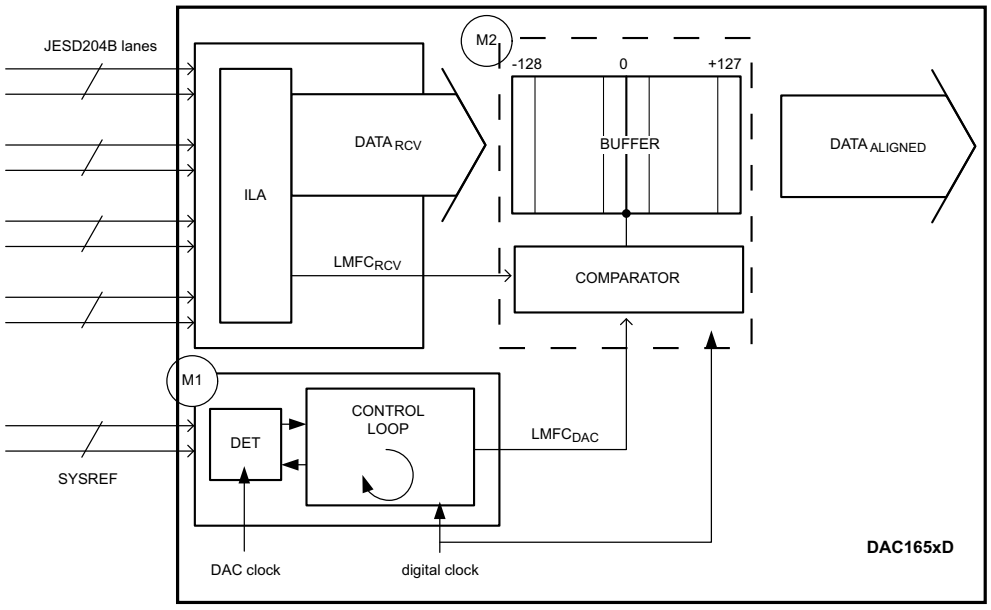


Fig 68. Modules of MDS implementation

11.7.3.1 SYSREF signal

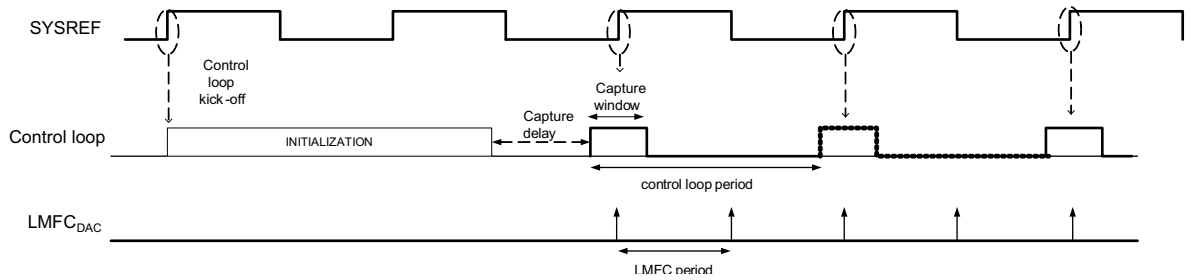
SYSREF can be either a periodic, or a “gapped” periodic signal. The one shot (strobe pulse) is not supported.. It is an active high signal which is sampled by the DAC clock. The sampling of the SYSREF signal could be done either one the DAC clock rising edge, either on the DAC clock falling edge.

The period of the SYSREF signal is an integer multiple of the LMFC period. The LMFC and frame clock within a device shall be phase aligned to the DAC clock sampling edge upon which the sampled SYSREF value has transitioned from 0 to 1.

11.7.3.2 Capturing the SYSREF signal

Module M1 ensures the capture of the SYSREF signal at DAC clock accuracy. This is done by an early-late detector and a control-loop. The control-loop must capture several SYSREF edges to deliver an accurate $LMFC_{DAC}$ signal to the M2 module. The Initialization of the control-loop is triggered by the edge detection of the SYSREF signal (see Figure 69). The capture is done during the capture window and is repeated at the end of every control loop period until the signal is locked. The SYSREF edge must occur within the capture window.

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In this example the SYSREF period is twice the LMFC period (R=2)

Fig 69. Capturing the SYSREF signal

Figure 70 shows an example on how to set up the M1 module.

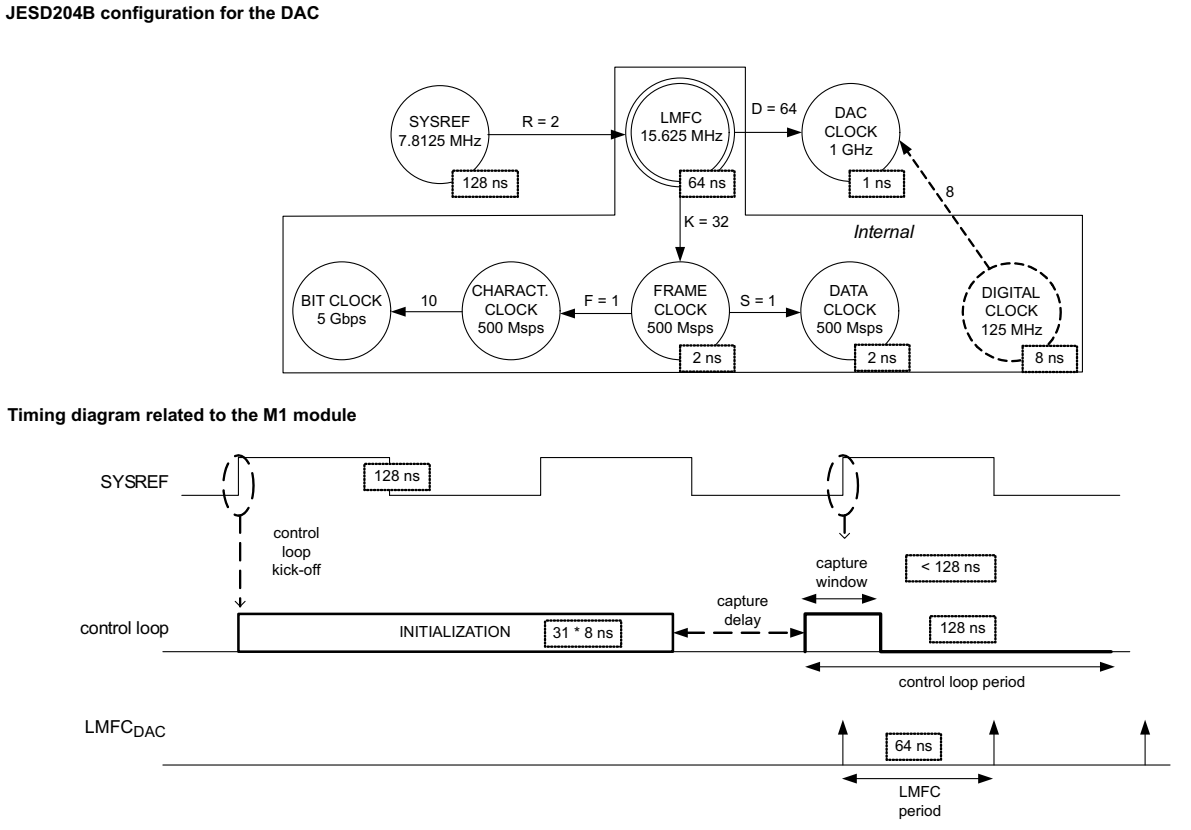


Fig 70. Example of how to set up the M1 module

The DAC165xD requires the following parameters:

- **LMFC_PERIOD (register x0AA)**:
  Period of the LMFC in digital clock cycles (e.g. 8 × 8 ns)
- **Capture window and control loop period**:

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These are specified using MDS_WIN_HIGH and MDS_WIN_LOW registers (respectively x0A9 and x0A8; see Table 109). They are expressed in digital clock cycles and must be set using the following equations:

$$capture\ window = 2 \times (MDS_WIN_HIGH + 1)$$

$$control\ loop\ period = capture\ window + MDS_WIN_LOW + 1$$

Remark: The capture window must be smaller than the SYSREF period.

At the end of the capture process, the $LMFC_{MDS}$ signal is provided to the M2 module and the MDS_LOCK bit of the MDS status register (see Table 113) is set to 1. If the M1 module cannot lock, the MDS_BSY flag is kept high and a mute action can be held (see Section 11.2.3.10, Table 85, and Table 86).

11.7.3.3 Aligning the LMFCs and the data

Module M2 ensures the phase alignment of the $LMFC_{RCV}$ to the closest $LMFC_{DAC}$ edge. The $LMFC_{RCV}$ is issued from the digital lane processing by analyzing the ILA sequence using the multi-frames /A/ symbols present. The transmitter (TX) is expected to have its self-synchronization process to the global MFC_{SYSTEM}. It generates the ILA sequence based on the aligned $LMFC_{TX}$. The total latency of the link is compounded of a fixed value (due to PCB traces, devices internal fixed delays, etc.) and a random value (due to elastic buffers, clocks domains interface, etc.). By buffering the data and the $LMFC_{RCV}$ after the initial-lane alignment process, the M2 module is capable to adjust the position of the buffer delay to match the recovered $LMFC_{DAC}$.

Figure 71 shows the alignment process for two links. The two links have two different total latencies but due to the $LMFC_{TX}$ and $LMFC_{DAC}$ phase synchronization to the MFC_{SYSTEM}, the various devices are capable to align to the same MFC_{SYSTEM} edge in a fixed and deterministic way.

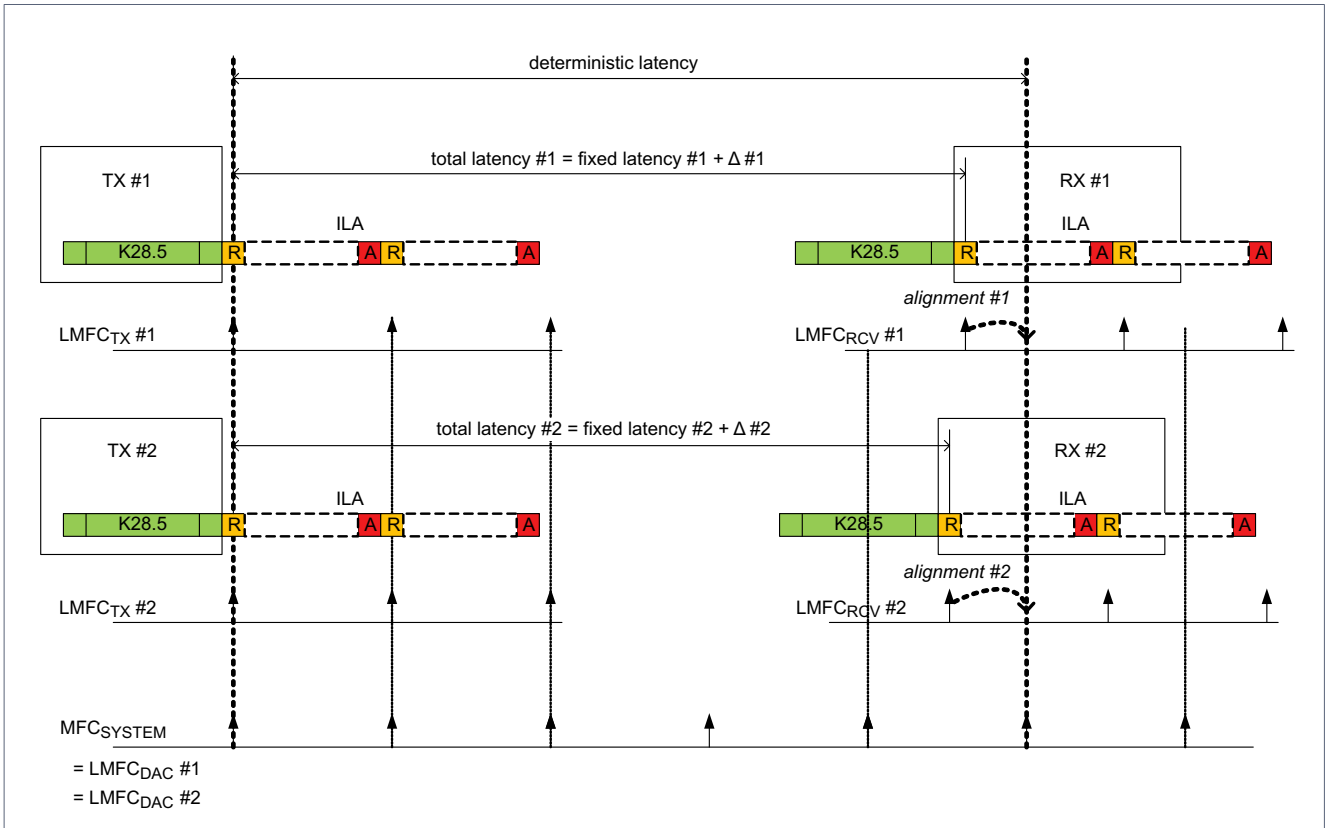


Fig 71. Multiple devices alignment process

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Take special care when selecting the MFC_{SYSTEM} period. A longer period is better than a short one. In general, the MFC_{SYSTEM} period must be at least two times the maximum latency between devices to avoid a wrong edge selection as shown in Figure 72.

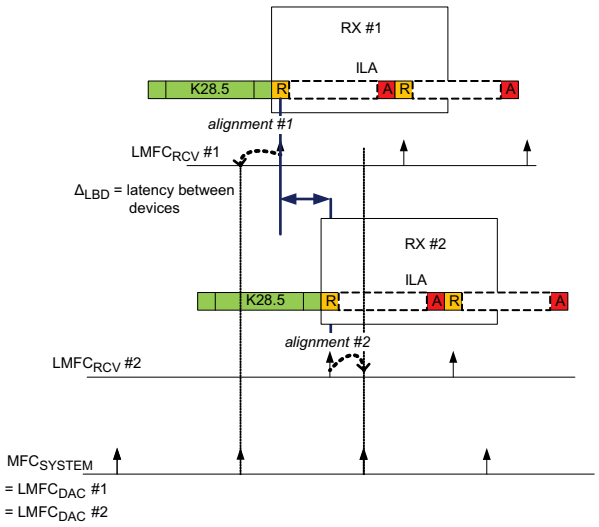


Fig 72. Wrong edge selection

11.7.3.4 Monitoring the MDS process

The buffer adjustment performed using the M1 and M2 modules can be read back using the MDS_ADJ_DLY register (see Table 112). Bits 7 to 3 of this register represent the coarse delay expressed in digital clock cycles whereas bits 2 to 0 represent the fine adjustment in DAC clock cycles. The buffer adjustment has a default value of 80h.

MDS_LOCK bit is set to 1 when the MDS process is completed. You can use this bit to check if the device is aligned to the SYSREF.

11.7.3.5 MDS registers signification

There is many registers linked to the monitoring of the MDS process. The following diagram is showing the way their signification in terms of timing relationships. The global reference is the SYSREF signal at the input of the DAC pins. In order to achieve a reliable alignment through multiples devices, it is necessary to tune LMFC_PRESET register in all DAC devices in order to have a read value of register I_ENA_SAMPLE that is about the LMFC_PERIOD/2 (in DCLK). This programation will make sure that all the DAC devices are aligned to the same SYSREF edge. The LMFC_PRESET value should be the same in all DACs.

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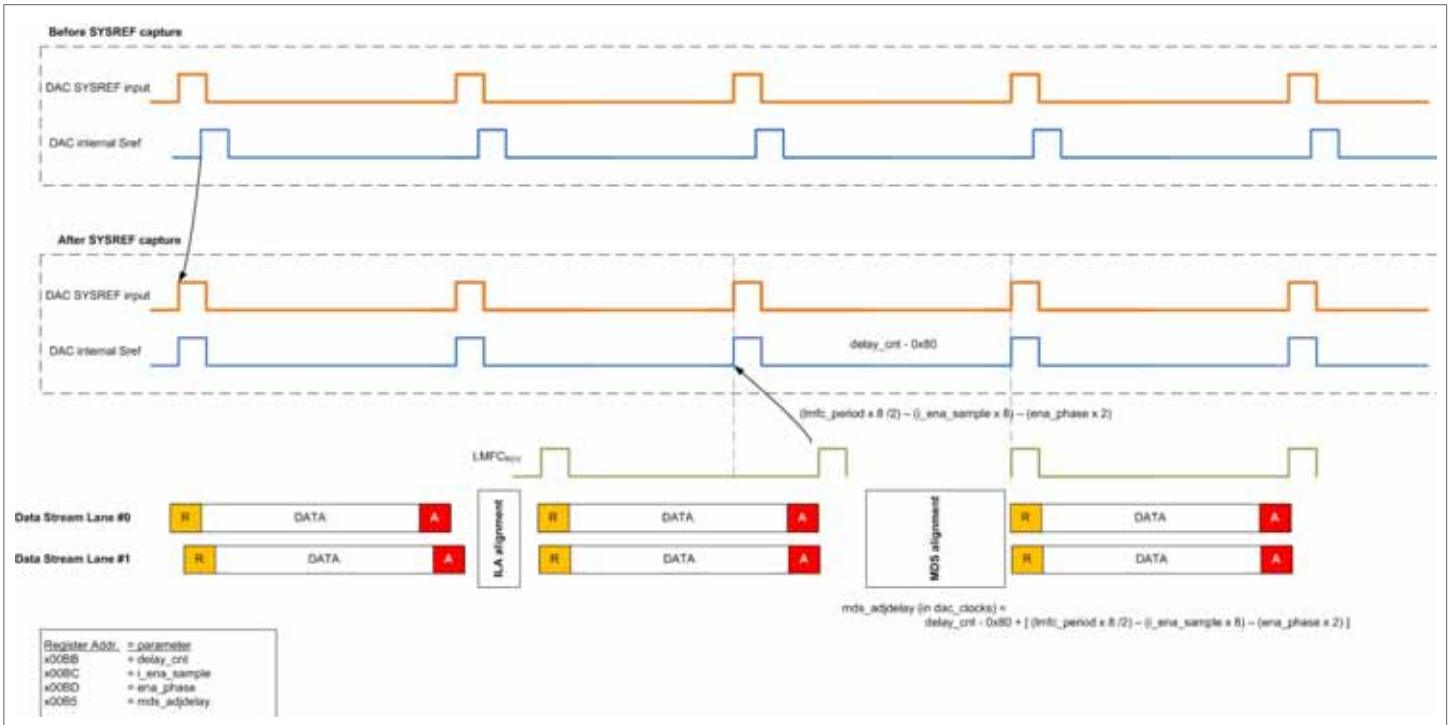


Fig 73. MDS timing overview

11.7.3.6 Adding adjustment offset

The DAC165xD allows adding an offset on top of the automatic adjustment. This is available via register MDS_OFFSET_DLY (see Table 108). The offset range is from −16 to 15 digital clock cycles. This offset value can be set at the start-up time as well as in at later period. This enables compensating a layout error or adding a specific phase to one DAC device.

Another adjustment delay can be set but only after a first automatic alignment using the manual adjustment delay register MDS_MAN_ADJ_DLY (see Table 106) with a resolution of DAC clk.

11.7.3.7 Selecting the SYSREF input port

The DAC165xD incorporates two SYSREF differential ports: SYSREF_E_P/N (East side of the device) and SYSREF_W_P/N (West side of the device). One of these ports can be selected as the input for the SYSREF signal and will be capture in an asynchronous way.

Remark: *SYSREF signal is only needed during SYNC_Request periods. The signal should/could be switched off later to avoid analog disturbances.*

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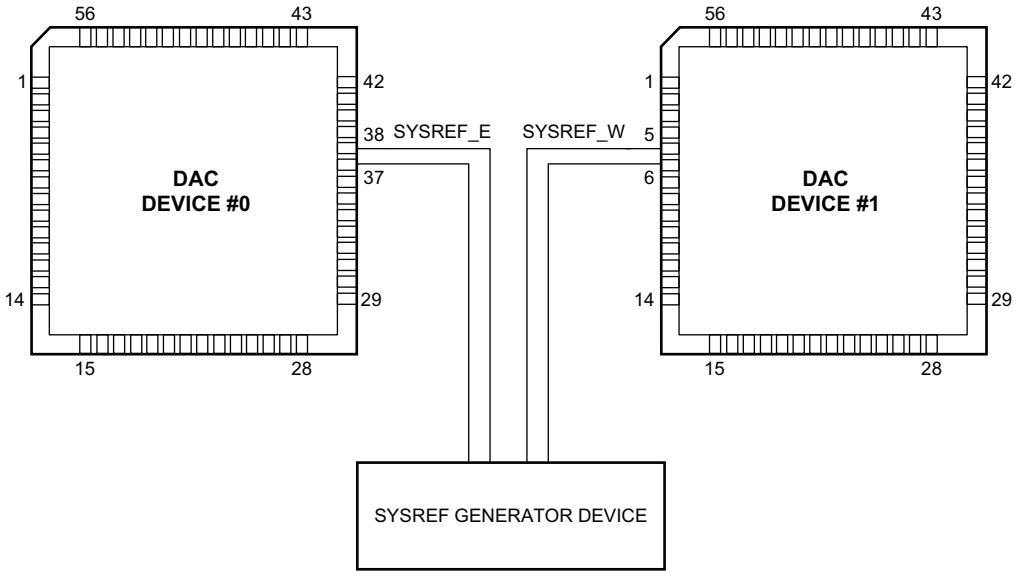


Fig 74. SYSREF differential ports

Register MDS_EAST_WEST (see Table 103) is used to select between the East port or the West port. Each SYSREF input buffer has an optional internal differential resistor termination of about 100 Ω. This resistor can be enabled with registers MDS_SEL_EAST_RT and MDS_SEL_WEST_RT (see Table 104). Polarity could also been switched using MDS_SYSREF_POL_W and MDS_SYSREF_POL_E bits.

11.7.3.8 MDS script example

Here are some guidelines to ensure basic correct MDS SPI programming (based on default register settings). This sequence must be applied before DCLK and WCLK resets are released (step 11 in Section 11.2.2):

1. Specify the asynchronous mode and the polarity expected for East and West input by asserting the bits of register MDS_MISC_CFG (see Table 59)
2. Specify the input to use (MDS_EAST_WEST bit) by asserting MDS_MAIN (see Table 103)
3. Power on the expected SYSREF buffer by setting PON_SYSREF_W or PON_SYSREF_E (see Table 104)
4. Specify optional offset delay by programming register MDS_OFFSET_DLY (see Table 108)
5. Specify the MDS_WIN_LOW and MDS_WIN_HIGH registers (see Table 109)
6. Specify the LMFC_PERIOD (see Table 110)

Other advanced settings could be added, refer to the IDT application note about MDS.
Once the device started (after WCLK and DCLK clocks release), the MDS_LOCK bit could be checked to verify that MDS process has worked (see Table 113)

SPI configuration example:

1. Register x002B write x08: Mandatory: use asynchronous mode
2. Register x00A0 write xCD: Mandatory: specify the correct option and input selection (here East)
3. Register x00A2 write x24: Mandatory: power on the East SYSREF buffer and activate the internal resistor
4. Register x00A7 write a value if needed: Optional: use this register to compensate a PCB layout issue
5. Register x00A8 write x0B: Mandatory: specify the MDS_WIN_HIGH

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6. Register x00A9 write x01: Mandatory: specify the MDS_WIN_LOW
7. Register x00AA write x10: Mandatory: specify the LMFC_PERIOD

11.8 Interrupts

In some cases it may be useful if the host-controller is notified that a certain internal event has taken place by means of an interrupt . The DAC165xD includes a simple interrupt (INTR) controller for this purpose.

The INTR-signal can be made available on one of the I/O pins. The polarity is programmable (see section Section 11.8.7).

11.8.1 Events monitored

The DAC165xD monitors various internal events and indicates their occurrence in the INTR_FLAGS registers (see Table 92). The following event can be observed:

- INTR_DLP:

  Digital Lane Processing (DLP) has its own interrupt controller. The result of this slave controller is provided to the main interrupt controller through the INTR_DLP bit (see Section 11.8.3).
- MDS_BSY and $\overline{\text{MDS_BSY}}$:

  Refer to the activity of the MDS controller. During the SYSREF capture phase, the MDS_BUSY signal is high, and becomes low once finished.
  - MDS_BSY reflects the start of the activity of the MDS controller
  - $\overline{\text{MDS_BSY}}$ reflects the end of the activity of the MDS controller
- TEMP_ALARM:

  Indicates that the temperature measured by the on-chip temperature sensor exceeds the threshold temperature (see Section 11.6).
- LVL_DET_OR:

  Indicates that one of the level detectors is enabled.
- CA_ERR:

  Indicates a DLP clock error.
- CLK_MON:

  Indicates a CDI clock error.
- DCLK_ERR_MON:

  Indicates a drift on the DCLK as specified by register INTR_MON_DCLK_RANGE (see Table 90).
- ERR_RPT_FLAG:

  Indicates the transmission of error reporting via the SYNCB interface.
- ALARM_STATE:

  Indicates when an auto-mute event occurs (see Section 11.2.3.10).

11.8.2 Enabling interrupts

An indication of an 0→1 transition of the corresponding monitor- or error indicator activates the INTR-signal can be given using the INTR_EN_0 and INTR_EN_1 registers (see Table 91). The INTR_FLAGS (see Table 92) registers indicate which of the selected events has invoked the interrupt. When bit INTR_RST (see Table 90) is set to 1 the flags and the INTR-signal are reinitialized.

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11.8.3 Digital Lane Processing (DLP) interrupt controller

The DLP has its own interrupt controller that reports to the main interrupt controller. This DLP interrupt controller is managed from the SPI registers of block x00E0 (see Figure 75).

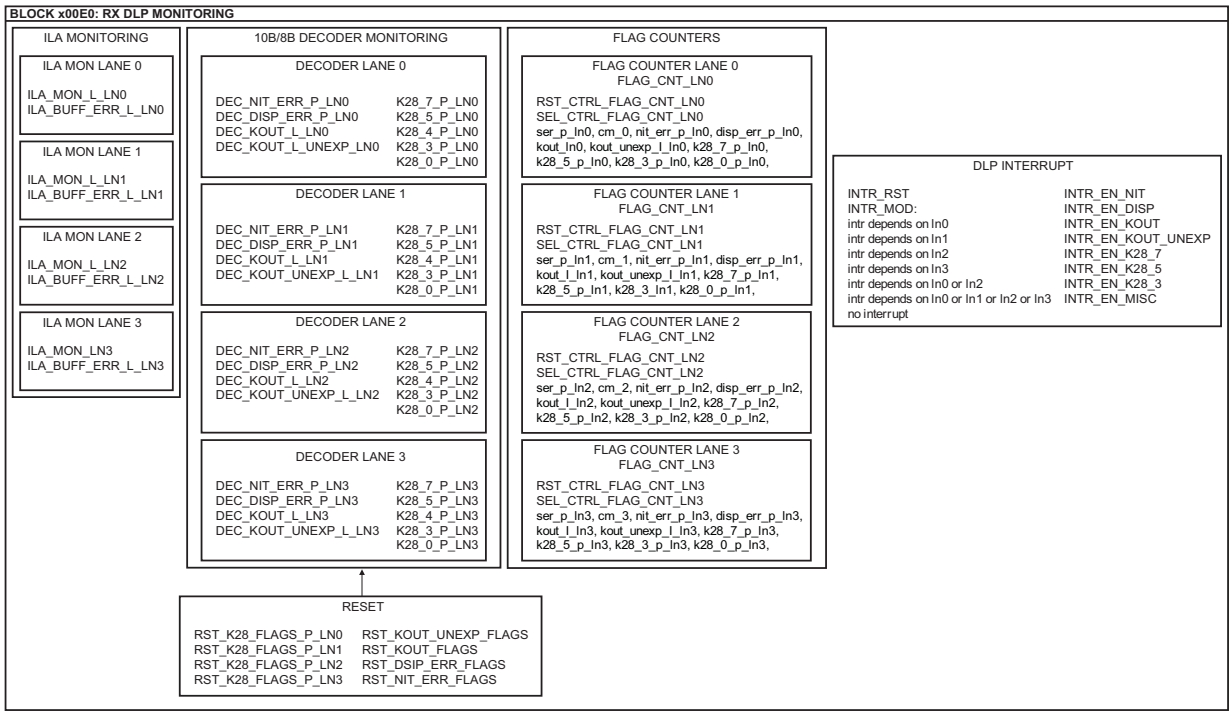


Fig 75. Digital lane processing monitoring

As this interrupt controller is dedicated to the JESD204B serial interface the INTR_MODE bits (see Table 142) must be specified according to the LMF configuration used in the system.

Table 32. INTR_MOD settings

INTR_MOD	Interrupt setting[1]	Nominal LMF use[2]
000	DLP interrupt depends on lane 0	124
001	DLP interrupt depends on lane 1	124
010	DLP interrupt depends on lane 2	124
011	DLP interrupt depends on lane 3	124
100	DLP interrupt depends on lane 0 or lane 2	222
101	DLP interrupt depends on lane 0 or lane 1 or lane 2 or lane 3	421 / 422
110	Hold_flagcnt[3]	-
111	no interrupt	-

[1]The lane numbering refers to the logical lanes (see Section 11.8.4).

[2]Any mode can also be used for debug purposes.

[3]The "HOLD_FLAG_CNT" feature is explained in Section 11.8.6.1.

Register INTR_DLP is reinitialized when the bit INTR_RST control is set to logic 1 (see Table 90).

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The DLP events that can be monitored with the interrupt controller are programmable via register INTR_EN (see Table 91). Those events are related to the lanes specified by the INTR_MOD bits in register INTR_SER_CTRL (see Table 142). They can be enabled by the following bits:

- INTR_EN_NIT: A Not-In-Table (NIT) error has occurred on one of the lanes
- INTR_EN_DISP: A disparity error has occurred on one of the lanes
- INTR_EN_KOUT: K control characters have been detetected on one of the lanes
- INTR_EN_KOUT_UNEXP: An unexpected K control character has been detected on one of the lanes
- INTR_EN_K28_7: A K28.7 symbol has been detected on one of the lanes
- INTR_EN_K28_5: A K28.5 symbol has been detected on one of the lanes
- INTR_EN_K28_3: A K28.3 symbol has been detected on one of the lanes
- INTR_EN_MISC: An event related to the INTR_MISC_EN register (see Table 135) has occurred

  Register INTR_MISC_EN (see Table 135) refers to two kinds of events, mainly for debug purposes:
  - Lane x has reached the CS_INIT state (see Table 35)
  - An error has occurred in the ILA alignment process on lane x

When register INTR_DLP is invoked, the “FLAGS” registers must be read to determine which event has occurred:

- An INTR_EN_NIT event is related to the DEC_NIT_ERR_LNx bits of register DEC_FLAGS (see Table 128)
- An INTR_EN_DISP event is related to the DEC_DISP_ERR_LNx bits of register DEC_FLAGS (see Table 128)
- An INTR_EN_KOUT event is related to the DEC_KOUT_LNx bits of register KOUT_FLAGS (see Table 129)
- An INTR_EN_KOUT_UNEXP event is related to the DEC_KOUT_UNEXP_LNx bits of register KOUT_UNEXP_FLAGS (see Table 131)
- An INTR_ENA_K28_7 event is related to the K28_7_LNx bits of register K28_FLAG (see Table 130)
- An INTR_EN_K28_5 event is related to the K28_5_LNx bits of register K28_FLAG (see Table 130)
- An INTR_EN_K28_3 event is related to the K28_3_LNx bits of register K28_FLAG (see Table 130)
- An INTR_EN_MISC event is related to the CS_STATE_LNx bits of register CS_STATE_LNX (see Table 133) and the ILA_BUFF_ERR_LNx bits of register ILA_BUFF_ERR register (see Table 127)

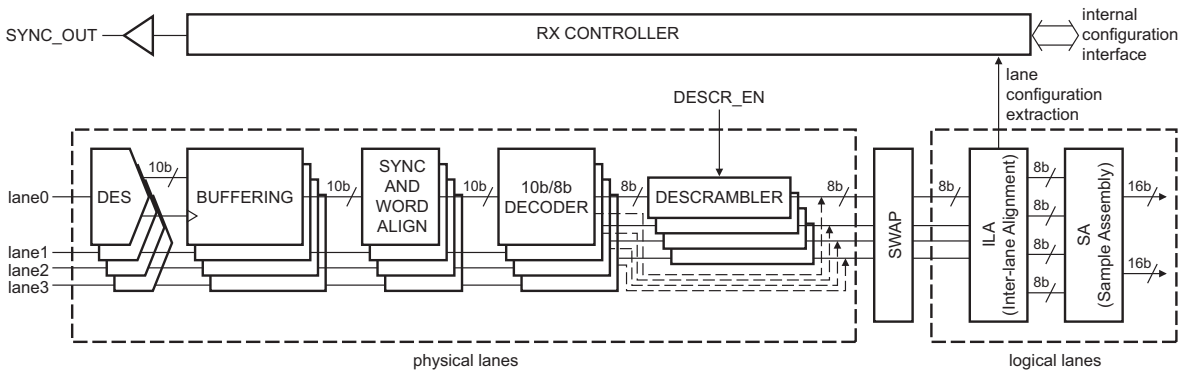
All flag bits can be reset using register RST_FLAGS_MON (see Table 141).

Remark: Checking the CS_STATE_LNx = CS_INIT interrupts allows to indirectly test the SYNC_REQUEST of the DAC. This feature can help if one does not want to use the differential SYNC_OUT signal.

11.8.4 JESD204B physical and logical lanes

The DAC165xD integrates a JESD204B serial interface with a high flexibility of configuration.

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The descrambler can be enabled or disabled.

Fig 76. JESD204B receiver

Because of various implementations for JESD204B transmitter devices, a flexible configuration of the physical lanes is required. This configuration allows the lane polarity to invert individually and to arbitrary swap the lane order. Identifying the lane numbers can be confusing because of the lane swapping. Two terms, physical and logical, are used in this document to explicitly identify the lanes.

Physical lanes:

The DAC165xD integrates four JESD204B serial receivers that are referenced via the pinning information (see Figure 2).

- Physical lane 0 refers to the signal coming from pins VIN_P0 and VIN_N0
- Physical lane 1 refers to the signal coming from pins VIN_P1 and VIN_N1
- Physical lane 2 refers to the signal coming from pins VIN_P2 and VIN_N2
- Physical lane 3 refers to the signal coming from pins VIN_P3 and VIN_N3

Logical lanes:

The DAC165xD incorporates a Swap lanes module (see Figure 76) that allows a remapping of the lane numbers to be compatible with the system implementation.

- Logical lane 0 refers to the lane specified with the LN_SEL_LN0 bits in register LN_SEL (see Table 119)
- Logical lane 1 refers to the lane specified with the LN_SEL_LN1 bits in register LN_SEL (see Table 119)
- Logical lane 2 refers to the lane specified with the LN_SEL_LN2 bits in register LN_SEL (see Table 119)
- Logical lane 3 refers to the lane specified with the LN_SEL_LN3 bits in register LN_SEL (see Table 119)

The following naming convention is used to distinguish between the physical lanes and the logical lanes in the SPI registers: “P_LNx” is used to identify the physical lanes. “L_LNx” is used to identify the logical lanes. “x” stands for the lane number in both cases.

11.8.5 RX Digital Lane Processing (DLP)

Digital lane processing is the module containing all JESD204B interface controls except the PHY deserializer.

Figure 77 shows the registers for the configuration of the digital lane processing.

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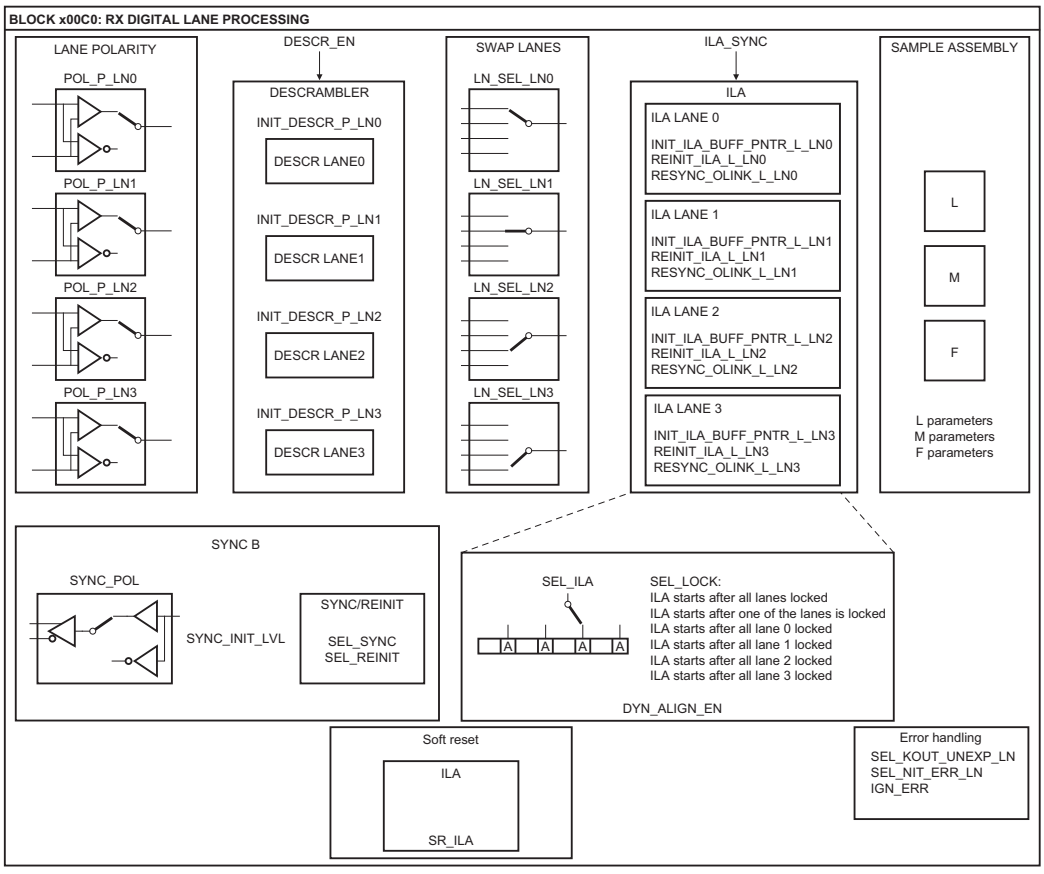


Fig 77. RX digital lane processing

11.8.5.1 Lane polarity

Each physical lane polarity can be individually inverted with the POL_P_LNx bits of register P_LN_POL (see Table 118). Using this feature transforms the 10 bits from ABCDEFGHIJ to $\overline{\text{ABCDEFGHIJ}}$.

11.8.5.2 Scrambling

The descrambler is a 16-bit parallel self-synchronous descrambler based on the polynomial $1 + x^{14} + x^{15}$. From the JESD204B specification, the scrambling/descrambling process only occurs on the user data, not on the code group synchronization or the ILA sequence. After two received bytes, the descrambler is correctly set up to decode the data in the proper way. However, it the initial state of the descrambler bits is set incorrectly, the two first decoded bytes are decoded incorrectly. The JESD204B specification proposes an initial state for both scrambler and descrambler to avoid this.

Using registers INIT_DESCR_P_LNx (see Table 120) any kind of intitial state can be set in the DAC165xD. The descrambling process starts when the ILA sequence has finished. This process can be turned off by deasserting bit DESCR_EN in register ILA_CTRL_1 (see Table 115).

The first samples can not be sent to the DSP using the FORCE_FIRST_SAMPLE_LOW bits of register FORCE_ALIGN. This avoids the use of the two incorrectly decoded samples.

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11.8.5.3 Lane swapping and selection

If the physical lanes do not match with the ordering of the transmitter lanes, they can be reordered using the lane swapping module. As the DAC165xD allows various LMF configurations (see Table 124), it is important that the lane swapping respects the following reordering constraints linked to the L value (see Table 33).

Table 33. Logical lanes versus L values

L value		Logical lanes used for the Sample assembly module
Binary	Decimal	
100	4	logical lane 0
		logical lane 1
		logical lane 2
		logical lane 3
010	2	logical lane 0
		logical lane 2
001	1	logical lane 0

The selection of the logical lanes can be is specified by the LN_SEL_L_LNx bits of register LN_SEL (see Table 119).

Table 34 shows the possible choices regarding the value of the L parameter.

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Table 34. Lane mapping between Logical and Physical lanes regarding the L value

L	4	2	1
logical lane 0	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3
logical lane 1	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3	not used	not used
logical lane 2	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3	not used
logical lane 3	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3	not used	not used

11.8.5.4 Word locking and Code Group Synchronization (CGS)

When the bits are received from the RX physical layer, DLP has to identify the MSB and LSB boundaries of the 10-bit codes from the bitstream. This can be monitored using the LOCK_CNT_MON_P_LN01 and LOCK_CNT_MON_P_LN23 registers (see Table 132).

When all lanes are locked, the values of the registers are stable and the code group synchronization process can start. This process is described by the JESD204B specification and is represented by the state machine shown in Figure 78.

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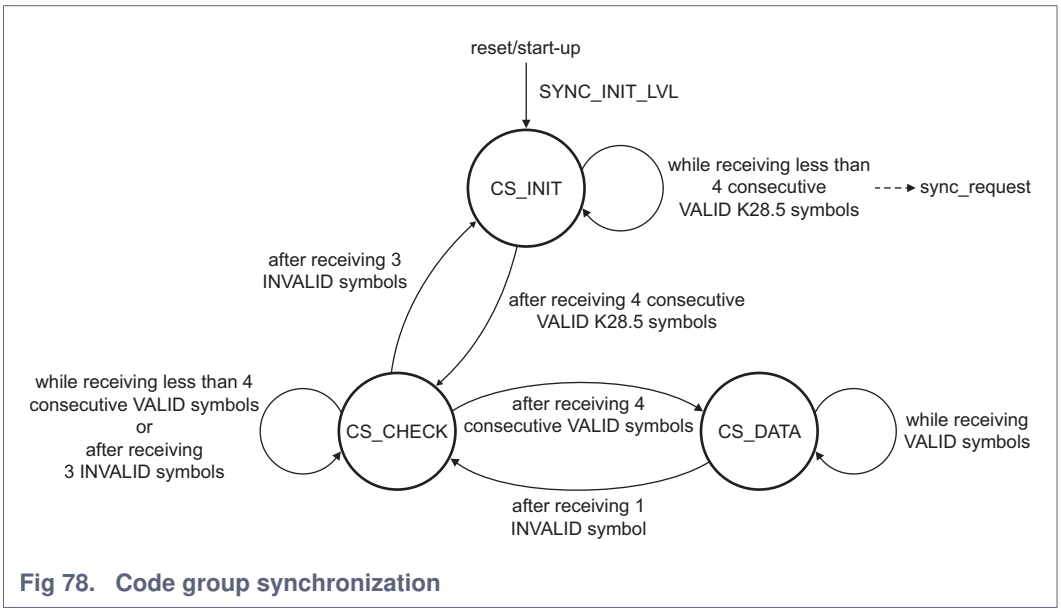


Fig 78. Code group synchronization

The CGS states of each lane can be monitored using the CSYNC_STATE_P_LNx bits of register CSYNC_STATE_P_LNx (see Table 133). The definition of each state can be found in Table 35.

Table 35. Code group synchronization state machine

CSYNC_STATE_P_LNx[1:0]	Name	Definition
00	CSYNC_INIT	looking for K28_5 (/K/) symbol
01	CSYNC_CHECK	four consecutive K28_5 (/K/) symbols have been received
10	CSYNC_DATA	code group synchronization achieved

11.8.5.5 SYNC configuration

The SYNC signal is the feedback signal that is sent to the transmitter device to ensure the JESD204B link synchronization. When all lanes are in CSYNC_INIT state a sync_request is sent to the SYNC buffer that is linked to pins SYNC_OUT_P and SYNC_OUT_N (see Figure 2).

The polarity of this buffer is controlled by bit SYNC_POL of register SYNC_OUT_MOD (see Table 117). By default the synchronization request is active low. The synchronization request signal can be specified by bits SEL_SYNC and SYNC_INIT_LVL of register SYNC_OUT_MOD. Bit SYNC_INIT_LVL of register SYNC_OUT_MOD only specifies the state of the sync_request signal after resetting the CGS state machine (at start-up time or after device reset only).

Table 36. Sync_request control

SEL_SYNC[2:0]	Description
000	sync_request active when state machine of one of the lanes is in CS_INIT mode
001	sync_request active when state machine of all lanes is in CS_INIT mode
010	sync_request active when state machine of lane 0 is in CS_INIT mode
011	sync_request active when state machine of lane 1 is in CS_INIT mode
100	sync_request active when state machine of lane 2 is in CS_INIT mode
101	sync_request active when state machine of lane 3 is in CS_INIT mode
110	sync_request fixed to 1
111	sync_request fixed to 0

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11.8.5.6 SYNC output level configuration

The SYNC output common mode is programmable by setting the register SYNC_SET_VCM. The final value depends on the voltage provided on VDD(sync). The recommended value depends of the VDD(sync) voltage.

Table 37. SYNC output common mode voltage

SYNC_SET_VCM[2:0]	VCM general formula	VCM when VDD(diff)=1.8V	VCM when VDD(diff)=1.2V	Remark
000	VDD(diff)-0.8	1.0V	0.4V	
001	VDD(diff)-0.7	1.1V	0.5V	
010	VDD(diff)-0.6	**1.2V**	0.6V	**recommended when VDD(diff)=1.8v**
011	VDD(diff)-0.5	1.3V	0.7V	
100	VDD(diff)-0.4	1.4V	**0.8V**	**recommended when VDD(diff)=1.2V**
101	VDD(diff)-0.3	1.5V	0.9V	
110	VDD(diff)-0.2	1.6V	1.0V	
111	VDD(diff)-0.1	1.7V	1.1V	

11.8.5.7 SYNC output swing configuration

The SYNC output swing is programmable by setting the register SYNC_SET_LVL. The recommended value is b100.

Table 38. SYNC output swing voltage

SYNC_SET_LVL[2:0]	Single ended value	Differential value
000	0.05V	0.10V
000	0.10V	0.20V
010	0.15V	0.30V
011	0.20V	0.40V
100	**0.30V**	**0.60V**
101	0.40V	0.80V
110	0.50V	1.00V
111	0.60V	1.20V

11.8.5.8 Initial-lane alignment

This module handles the alignment of the logical lanes based on the ILA sequence described in the JESD204B specification. Inter-lane alignment starts when all lanes are locked and at reception of the first non-K28.5 (or /K/) symbol.

During the ILA sequence, the K28.3 (/A/ symbol) is used to align the data streams. During this sequence, the length (K) of the multi-frame is measured. This value is used by the lane monitoring and correction process. The value is also used for the MDS circuitry, where the SYSREF signal is expected to be a multiplication of the multi-frame length (K) in the JESD204B specification.

During the second multi-frame, the JESD204B configuration data of each physical lane is stored in register blocks x0120 and x0140 (see Figure 79 and Figure 80). The DAC165xD does not do anything with these configuration data. They are only made available for the host controller.

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BLOCK x0120: JESD204 READ CONFIGURATION

LANE 0 JESD204 CONFIGURATION

CONFIG 0	P_LN0_DID	
CONFIG 1	P_LN0_AD_JCNT	P_LN0_BID
CONFIG 2	P_LN0_ADJ_DIR P_LN0_ADJ_PH	P_LN0_LID
CONFIG 3	P_LN0_SCR	P_LN0_L
CONFIG 4	P_LN0_F	
CONFIG 5		P_LN0_K
CONFIG 6	P_LN0_M	
CONFIG 7	P_LN0_CS	P_LN0_N
CONFIG 8	P_LN0_SBCLSS_VS	P_LN0_N'
CONFIG 9	P_LN0_JESD_VS	P_LN0_S
CONFIG 10	P_LN0_HD	P_LN0_CF
CONFIG 11	P_LN0_RES1	
CONFIG 12	P_LN0_RES2	
CONFIG 13	P_LN0_FCHK	

LANE 1 JESD204 CONFIGURATION

CONFIG 0	P_LN1_DID	
CONFIG 1	P_LN1_ADJ_CNT	P_LN1_BID
CONFIG 2	P_LN1_ADJ_DIR P_LN1_ADJ_PH	P_LN1_LID
CONFIG 3	P_LN1_SCR	P_LN1_L
CONFIG 4	P_LN1_F	
CONFIG 5		P_LN1_K
CONFIG 6	P_LN1_M	
CONFIG 7	P_LN1_CS	P_LN1_N
CONFIG 8	P_LN1_SBCLSS_VS	P_LN1_N'
CONFIG 9	P_LN1_JESD_VS	P_LN1_S
CONFIG 10	P_LN1_HD	P_LN1_CF
CONFIG 11	P_LN1_RES1	
CONFIG 12	P_LN1_RES2	
CONFIG 13	P_LN1_FCHK	

Fig 79. JESD204 read configuration for physical lanes 0 and 1

BLOCK x0140: JESD204 READ CONFIGURATION

LANE 2 JESD204 CONFIGURATION

CONFIG 0	P_LN2_DID	
CONFIG 1	P_LN2_ADJ_CNT	P_LN2_BID
CONFIG 2	P_LN2_ADJ_DIR P_LN2_ADJ_PH	P_LN2_LID
CONFIG 3	P_LN2_SCR	P_LN2_L
CONFIG 4	P_LN2_F	
CONFIG 5		P_LN2_K
CONFIG 6	P_LN2_M	
CONFIG 7	P_LN2_CS	P_LN2_N
CONFIG 8	P_LN2_SBCLSS_VS	P_LN2_N'
CONFIG 9	P_LN2_JESD_VS	P_LN2_S
CONFIG 10	P_LN2_HD	P_LN2_CF
CONFIG 11	P_LN2_RES1	
CONFIG 12	P_LN2_RES2	
CONFIG 13	P_LN2_FCHK	

LANE 3 JESD204 CONFIGURATION

CONFIG 0	P_LN3_DID	
CONFIG 1	P_LN3_ADJ_CNT	P_LN3_BID
CONFIG 2	P_LN3_ADJ_DIR P_LN3_ADJ_PH	P_LN3_LID
CONFIG 3	P_LN3_SCR	P_LN3_L
CONFIG 4	P_LN3_F	
CONFIG 5		P_LN3_K
CONFIG 6	P_LN3_M	
CONFIG 7	P_LN3_CS	P_LN3_N
CONFIG 8	P_LN3_SBCLSS_VS	P_LN3_N
CONFIG 9	P_LN3_JESD_VS	P_LN3_S
CONFIG 10	P_LN3_HD	P_LN3_CF
CONFIG 11	P_LN3_RES1	
CONFIG 12	P_LN3_RES2	
CONFIG 13	P_LN3_FCHK	

Fig 80. JESD204 read configuration for physical lanes 2 and 3

The ILA module uses a 16-bit buffer for each lane. The first /A/ symbol received over the lanes is used as reference. The /A/ symbols of the other lanes, which are received later, are compared to the first one to be all aligned. The initial location of the symbols is predefined by the INIT_ILA_BUFF_PNTR_L_LNxy registers (see Table 120). The alignment can be monitored with the ILA_MON_L_LNxy bits of register ILA_MON (see Table 126). If the lane difference is too great, a buffer out-of-range error occurs, which can be monitored with bits ILA_BUFF_ERR_L_LNx of register ILA_BUFF_ERR (see Table 127). In this specific case, a reinitialization of the full link can be requested by setting the REINIT_ILA_L_LNx bits of register REINIT_CTRL (see Table 122).

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The JESD204B specification also mentions a dynamic realignment mode where a monitoring process is checking the /A/-symbol location. This can realign the data stream if two successive /A/ symbols are found at the same new position. By default this monitoring and correction process is disabled to avoid any moving latency over the link, but one can enable the feature by setting the DYN_ALIGN_EN bit of register FORCE_ALIGN (see Table 116).

11.8.5.9 SYNC TX response time and ILA alignment

When the DAC is deasserting the SYNC signal from level 1 to level 0, the internal DAC states machines are reseted during 10 µsec. In the meantime the TX will detect the SYNC request and should be able to response to this request and to send the K28.5 symbols. When the DAC states machines retrieve their initial states, the DAC will proceed to the alignment based on the K28.5 symbols and the ILA.

However, if the TX takes more time to response to the SYNC request, then when the DAC states machines retrieve their initial states, the DAC could wrongly proceed to the multi-frame alignment based on the DATA received before the K28.5 sequence. In this case, the first ILA multi-frame will not be correctly detected, but the alignment monitoring process will compensate this error in a later stage. This will result in a wrong ILA configuration data extraction, but as long as the bits SEL_ILA of the ILA_CNTRL register (0x00C7) are set to '11', the DATA stream will be correctly aligned.

11.8.5.10 Character replacement

Character replacement, as specified by the JESD204B specification, can occur at the end of the frame (K28.7 or /F/ symbol) or at the end of the multi-frame (K28.3 or /A/ symbol). By default this feature is enabled, but it can be disabled using bit FRAME_ALIGN_EN of the ILA_CTRL_0 register (see Table 115).

Remark: The DAC165xD can handle multi-frame length values (K) between ceil(17 / F) and 32 but with the restriction that the number of octets in a multi-frame must always be even. This implies that if F = 1, a value of K = 17 is not allowed. When F = 1 only even values > 17 are allowed. Working with F = 1 and K = 17 often implies that the character replacement process is not reliable.

11.8.5.11 Sample assembly

Sample assembly handles the assembly of the data based on the LMF parameters described by register LMF_CTRL (see Table 124). The following configurations are supported:

- LMF-S = 421-1
- LMF-S = 422-2
- LMF-S = 222-1
- LMF-S = 124-1

Sample assembly is based on the logical lanes definition when updating the L value.

11.8.5.12 Resynchronization over links

The DAC165xD recognizes a K28.5 (/K/) symbols sequence coming over its lanes. This identification allows resynchronization of the device if the RESYNC_OLINK_P_LNx bits of register REINIT_CTRL are set correctly (see Table 122).

11.8.5.13 Symbols detection monitoring and error handling

The DLP decodes the 10-bit words to 8-bit words. The decoding table is specified in the IEEE 802.3-2005 specification. During decoding, the disparity is calculated according to the disparity rules mentioned in the same specification. The JESD204B specification also defines the following definitions:

- VALID:

  The code group is found in the column of the 10b/8b decoding tables according to the current running disparity.

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- DISPARITY ERROR:

  The received code group exists in the 10b/8b decoding table, but is not found in the correct column according to the current running disparity.
- NOT-IN-TABLE (NIT) ERROR:

  The received code group is not found in the 10b/8b decoding table of either disparity.
- INVALID:

  A code group that either shows a disparity error or that does not exist in the 10b/8b decoding table.

Remark: The 8b/10b decoder only provides reliable information in the CSYNC_CHCK and CSYNC_DATA states. During CSYNC_INIT state, the DLP is "hunting" for the correct position of the K28.5 (/K/) symbols in the received bitstream. Therefore the DISPARITY ERROR/NOT-IN-TABLE/ INVALID flags are not yet consistent and are not be used in the internal monitoring.

The Not-In-Table error (NIT) and Disparity error (DISP) can be monitored using the DEC_NIT_ERR_P_LNx and DEC_DISP_ERR_P_LNx bits of register DEC_FLAGS (see Table 128). Both are considered invalid, but the DAC165xD has some flexibility in this definition. The specified invalid errors can also be totally ignored by setting the bit IGN_ERR of register ERR_HNDLNG to logic 1 (see Table 121). This specific mode is designed for debug purposes only, especially when sample error measurement needs to be executed.

The VALID/INVALID status of the decoded word can trigger the MUTE feature using the DATA_V_IQ_CFG bits of register MUTE_CTRL_1 (see Table 85; see Section 11.2.3.10).

The following comma symbols are detected during data transmission irrespective of the running disparity:

/K/ = K28.5

/F/ = K28.7

/A/ = K28.3

/R/ = K28.0

/Q/ = K28.4

Their single detection is monitored in registers KOUT_FLAG (see Table 129) and K28_FLAG (see Table 130).

During the data transmission phase, only K28.3 (/A/) and K28.7 (/F/) symbols are expected. Sometimes (e.g. wrong bit transmission), a code group is interpreted as a K character that is not K28.3 or K28.7. If this occurs a KOUT_UNEXP flag is asserted that can be read using the DEC_KOUT_UNEXP_L_LNx bits of register KOUT_UNEXP_FLAG (see Table 131).

All the previous flags can be reset using the RST_FLAGS_MON register (see Table 141). Detection of them can also assert the DLP interrupt (see Section 11.8.3).

11.8.6 Monitoring and test modes

The DAC165xD embeds various monitoring and test modes that are useful during the prototyping phase of a system.

Remark: The test capability linked to observing specific characters, errors or state machine statuses is not reviewed in this section. It is up to the reader to define specific modes based on the DAC165xD capability.

11.8.6.1 Flag counters

Due to the high data rate of the JESD204B serial interface, it is hard to monitor events that occur on the lanes in real time. Four multi-purpose counters have been added to the design to help this monitoring. Each counter is 16 bits wide and is linked to one lane. It increments its value each time a specific event occurs. These flags counters can be read using the

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FLAG_CNT_LNx registers (see Table 136) and reset using the RST_CTRL_FLAG_CNT_LNxx bits of the CTRL_FLAG_CNT_LNxx registers (see Table 140). The flag counters can also be reset automatically when DLP is reset by setting the AUTO_RST_FLAG_CNTS bit of register RST_BUF_ERR_FLAGS (see Table 134) to logic 1.

The specification of the event that increments the counter is done by setting the SEL_CTRL_FLAG_CNT_LNxx bits of the CTRL_FLAG_CNT_LNxx registers (see Table 140) to one of the sources described in Table 39.

Table 39. Counter source
Default settings are shown highlighted.

SEL_CTRL_FLAG_CNT_LNxx[2:0]	Source
000	not-in-table error
001	disparity error
010	K symbol not found
011	unexpected K symbol found
100	K28_7 (/F/) symbol found
101	**K28_5 (/K/) symbol found**
110	K28_3 (/A/) symbol found
111	K28_0 (/R/) symbol found

When the counter is reaching its maximum value (0xFFFF), this value is held until the next counter reset. Bit HOLD_FLAG_CNT_EN of RST_BUFF_ERR_FLAGS register (see Table 134) gives two options for when a counter reaches the maximum value.

Table 40. HOLD_FLAG_CNT_EN options
Default settings are shown highlighted.

HOLD_FLAG_CNT_EN	Option
0	**All counters are independent. Each counter continues its own counting.**
1	All counters are linked. When one counter reached the maximum value and stops, all other counters stop as well.

When the counters are stopped, an interrupt can be activated (see Section 11.8.3).

This feature makes it possible to, for instance, analyze the occurrence of character replacement or NIT errors.

11.8.6.2 Sample Error Rate (SER)

A sample error rate feature is implemented in the DAC165xD to analyze the quality of the transmission. Due to the 8b10b encoding, the analysis is done at sample level only and not at bit level. The transmitter sends a constant data over the link and the DAC165xD compared this received value to the value specified in the SER_LVL_LSB and SER_LVL_MSB registers (see Table 147). Enable the scrambling on both transmitter and receiver side to add more random effect on the data. The SER_LVL_MSB and SER_LVL_LSB are specifying a 16-bit value at the lane level, it means the device can be considered as operating in one of two modes:

- F = 2 mode:

  The lane is receiving 16-bit data specified by SER_LVL_MSB and SER_LVL_LSB.
- F = 1 mode:

  The lane is receiving alternately 8-bit data specified by SER_LVL_MSB and SER_LVL_LSB.

The SER mode requires that the DAC is already synchronized (using CGS and ILA sequence). The kick-off of the measurement is done by setting the SER_MOD bit of register SER_INTR_CTRL (see Table 142). In this mode, the flags counters are used to count the number of 16-bit samples that do not match the SER_LVL value. This mode enables the establishing of the sample error rate of each lane.

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11.8.6.3 PRBS test

The DAC165xD embeds the following PRBS checker that is shared for the 4 lanes:

- PRBS31
- PRBS23
- PRBS15
- PRBS7

To test a specific lane, the setting SEL_XBERT_LN[1:0] needs to be set first. Then it is required to disable the restart of the RX PHY due to the error monitoring this is done by setting the register ERR_HANDLING_1 to value xFF and REINIT_CTRL to value x00. After the release of the DCLK and WCLK clocks, the XBERT_CNTRL[1:0] bits must be specified to the expected test (PRBS31, 23, 15, 7) and the CHECK_PRBS bit must be set to the “sync to prbs sequence” mode. Once synchronized, the internal PRBS counter is aligned with the received PRBS sequence. The test starts when the CHECK_PRBS is set to the “check prbs sequence” mode. The XBERT_CNT[15:0] counter indicates the number of bits in error.

Example of SPI settings:

Write register x0000 to value x99 to configure the SPI mode and apply a reset

Write register x0060 to value x02 to specify the interpolation mode

Write register x004B to value x01 to specify the CDI mode

Write register x0022 to value x52 to specify the WCLK divider

Write register x0081 to value x55 to specify a hold mute on all the events (to quiet the internal digital)

Write register x00C7 to value x62

Write register x00DE to value x92 to specify the LMF422 mode

Write register x0050 to value xFD to output the test result on pin IO0

Write register x0052 to value x02 to output the test result on pin IO0

Setting up the PRBS-test

Write register x00DB to value xFF to disable the error handler

Write register x00DC to value x00 to prevent restart due to k28.5

Write register x0042 to value x01 to disable the watchdog of the lanes

Optional: Write register x0162 to value x84 to enable the low speed mode in case the bit rate is below 3 Gbps

Write register x0163 to value x24 (recommended value for the CDR charge pump parameter)

Write register x0168 to value x02 to change the equalizer gain of lane 0

Write register x0169 to value x02 to change the equalizer gain of lane 1

Write register x016A to value x02 to change the equalizer gain of lane 2

Write register x016B to value x02 to change the equalizer gain of lane 3

Write register x0040 to value x00 to release the internal clocks resets

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wait for 2 seconds

Write register x0100 to value x05 to reset XBERT counter

Write register x0100 to value x04 to enable XBERT test on lane 0 with PRBS 31 selection (synchronization mode)

wait for 2 seconds

Write register x0100 to value x24 to enable XBERT test on lane 0 with PRBS 31 selection (checking mode)

Read registers x0104 and x0105 to read the xbertest counters

11.8.6.4 JTSPAT test

The Jitter Tolerance Scrambled PATtern (JTSPAT) is an 1180-bit pattern intended for receiving jitter tolerance testing for scrambled systems. The JTSPAT test pattern consists of two copies of JSPAT and an additional 18 characters intended to cause extreme late and early phases in the CDR PLL followed by a sequence, which can cause an error (i.e. an isolated bit following a long run). This pattern was developed to stress the receiver within the boundary conditions established by scrambling.

Table 41. Jitter tolerance scrambled pattern symbols sequence [1]

D1.4 0111010010	D16.2 0110110101	D24.7 0011001110	D30.4 1000011101	D9.6 1001010110	D10.5 0101011010
D16.2 1001000101	D7.7 1110001110	D24.0 0011001011	D13.3 1011000011	D23.4 0001011101	D13.2 1011000101
D13.7 1011001000	D1.4 0111010010	D7.6 1110000110	D0.2 1001110101	D21.5 1010101010	D22.1 0110101001
D23.4 0001011101	D20.0 0010110100	D27.1 1101101001	D30.7 1000011110	D17.7 1000110001	D4.3 1101010011
D6.6 0110010110	D23.5 0001011010	D7.3 1110001100	D19.3 1100101100	D27.5 110101010	D19.3 1100100011
D5.3 1010010011	D22.1 0110101001	D5.0 1010010100	D15.5 0101111010	D24.7 0011001110	D16.3 1001001100
D1.2 0111010101	D23.5 0001011010	D29.2 1011100101	D31.1 0101001001	D10.4 0101011101	D4.2 0010100101
D5.5 1010011010	D10.2 0101010101	D21.5 1010101010	D10.2 0101010101	D21.5 1010101010	D20.7 0010110111
D11.7 1101001000	D20.7 0010110111	D18.7 0100110001	D29.0 1011100100	D16.6 0110110110	D25.3 1001100011
D1.0 1000101011	D18.1 0100111001	D30.5 1000011010	D5.2 1010010101	D21.6 1010100110	D1.4 0111010010
D16.2 0110110101	D24.7 0011001110	D30.4 1000011101	D9.6 1001010110	D10.5 0101011010	D16.2 1001000101
D7.7 1110001110	D24.0 0011001011	D13.3 1011000011	D23.4 001011101	D13.2 1011000101	D13.7 1011001000
D1.4 0111010010	D7.6 1110000110	D0.2 1001110101	D21.5 1010101010	D22.1 0110101001	D23.4 0001011101
D20.0 0010110100	D27.1 1101101001	D30.7 1000011110	D17.7 1000110001	D4.3 1101010011	D6.6 0110010110

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Table 41. Jitter tolerance scrambled pattern symbols sequence *...continued*[1]

D23.5 0001011010	D7.3 1110001100	D19.3 1100101100	D27.5 1101101010	D19.3 1100100011	D5.3 1010010011
D22.1 0110101001	D5.0 1010010100	D15.5 0101111010	D24.7 0011001110	D16.3 1001001100	D1.2 0111010101
D23.5 0001011010	D27.3 1101100011	D3.0 1100010100	D3.7 1100011110	D14.7 0111001000	D28.3 0011101100
D30.3 0111100011	D30.3 1000011100	D7.7 1110001110	D7.7 0001110001	D20.7 0010110111	D11.7 1101001000
D20.7 0010110111	D8.7 0100110001	D29.0 1011100100	D16.6 0110110110	D25.3 1001100011	D1.0 1000101011
D18.1 0100111001	D30.5 1000011010	D5.2 1010010101	D21.6 1010100110		

[1] This table must be read, starting from the top, left-to-right first and then line-by-line to follow the sequence.

The DAC165xD embeds a JTSPAT checker. The control registers are located in the JESD204 receiver monitoring registers block (see Table 146).

11.8.6.5 DLP strobe

The data coming out of the ILA module can be sampled by setting the DLP_STROBE bit of register MISC_CTRL (see Table 123). On each lane two octets are stored, which can be read out through registers P_LNxx_SMPL_MSB and P_LNxx_SMPL_LSB (see Table 154 and Table 156). The selection of the lane to read out the data is done by registers P_LN10_SEL and P_LN32_SEL (see Table 155 and Table 157).

11.8.7 IO-mux

The DAC165xD uses two general purpose pins, IO0 and IO1. IO0 and IO1 can be configured as an input (x01) or as an output (x00) by setting the IO_DIR bit of register EHS_CTRL (see Table 67).

When acting as an input, the IO1 pin is referred as the RF enable feature (see Section 11.2.5).

When acting as an output, the two IO pins are multiplexed to internal signals that can be useful for debug purposes. Table 42 shows the main configuration when using registers bit IO_SEL_x in register IO_MUX_CTRL_x. The definitions of the three registers depend on the "Indicator" and the "Range" values used to specify the signal that is sent through pins IO0 and IO1 (see Table 42 and Table 43).

Table 42. Definition of IO_SEL registers

Register name	b7	b6	b5	b4	b3	b2	b1	b0
IO_SEL_2	x	x	x	x	IO1indicator[1:0]		IO0 indicator[1:0]	
IO_SEL_1	IO1 range[7:0]							
IO_SEL_0	IO0 range[7:0]							

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Table 43. Output signals for combination of indicators and ranges

Indicator[1:0]	Range[7:0]	Output signal
00	xxxx xxx0	IO0: WCLK
		IO1: DCLK
00	xxxx 0011	synchronization request
10	1111 0010	end of ILA
10	1111 1101	xbert flag
11	1100 0000	$\overline{\text{interrupt}}$
11	1100 0001	interrupt
11	1111 even	IO0: fixed to logic 1
		IO1: fixed to logic 0
11	1111 odd	IO0: fixed to logic 0
		IO1: fixed to logic 1

11.9 JESD204B PHY receiver

Each JESD204B lane owns its own physical deserializer (RX PHY) that provides the 10-bit data stream to the DLP module. The SPI registers of block x0160 control the various features of the RX PHY, like the equalizer, the common-mode voltage and the resistor termination. The registers of x0180 monitor the status of these controls.

Remark: Most of the main controls (power on/off, PLL clock dividers,etc.) are automatically set while specyfing the LMF mode (see Section 11.8.5.11) and/or by the MAIN_CTRL register (see Table 64).

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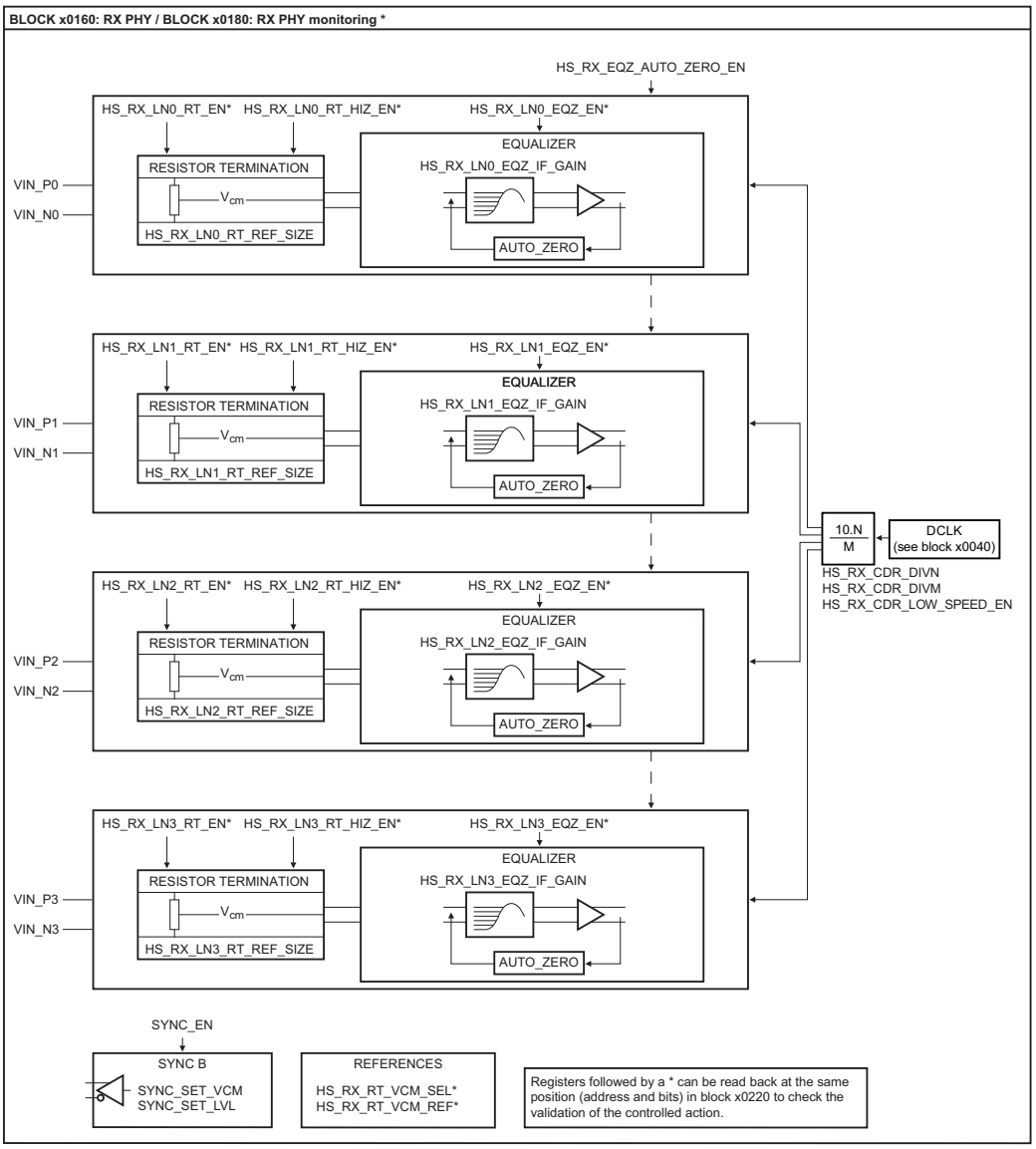


Fig 81. RX PHY control overview

11.9.1 JRES pin

The JRES pin is used for internal biasing of the RX PHY. The pin needs to be connected to a 6.98kOhms 1% resistor.

11.9.2 Lane input

Each lane is Current Mode Logic (CML) compliant.

The common-mode voltage and the termination resistor can be programmed using register HS_RX_RT_VCM (see Table 162). When not used, the lane input buffer can be set to a high impedance mode (register HS_RX_RT_CTRL; see Table 163).

AC-coupling is always required (see Figure 82).

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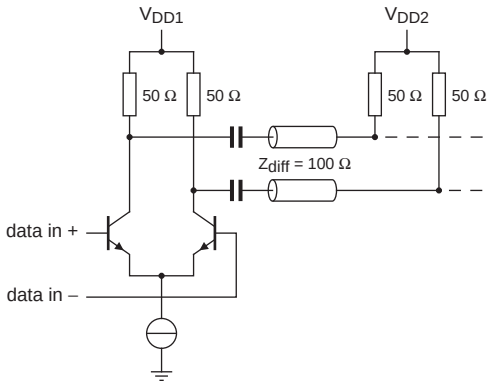


Fig 82. AC-coupling

11.9.3 Equalizer

The DAC165xD embeds an internal equalizer (bits HS_RX_LNx_EQZ_EN in register HS_RX_EQZ_CTRL; see Table 167) in each high-speed serial lane. This improves the interference robustness between signals by amplifying the high-frequency jumps in the data conserving the energy of the low-frequencies ones. The equalizer can be programmed depending on the quality of the channel used (PCB traces/layout, connectors, etc.).

The auto-zero feature (bit HS_RX_EQZ_AUTO_ZERO_EN in register HS_RX_EQZ_CTRL; see Table 160) is enabled by default for the deserializer to adapt itself to the common-mode of the received signal.

Set the equalizer gains to control the high-frequency jumps of the data (bits HS_RX_0_EQZ_IF_GAIN[2:0] of register HS_RX_LNx_EQZ_GAIN; see Table 161). The total Equalizer gain is defined as the ratio IF_GAIN/LF_GAIN.

Table 44. Equalizer gain

IF_GAIN	Equalizer Gain (dB)
000	0.0
001	0.0
010	0.5
011	2.0
100	3.5
101	5.0
110	6.5
111	8.0

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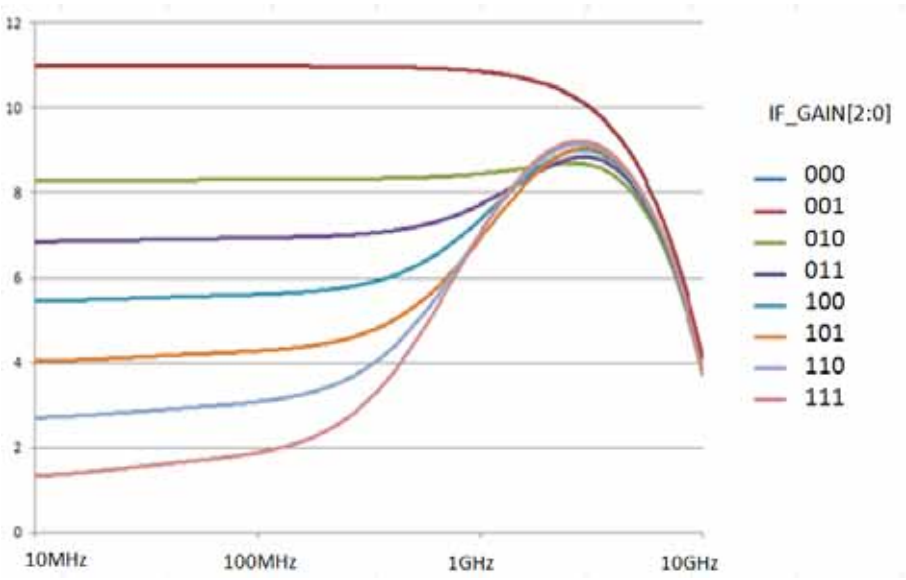


Fig 83. Equalizer gain (dB)

11.9.4 Deserializer

The deserializer performs the incoming data clock recovery and also the serial-to-parallel conversion. One global PLL provides the same reference clock to the four lanes. The PLL configuration is automatically done when specifying the LMF parameters (see Table 9).

11.9.5 Low Serial Input Data Rate

When using the DAC165xD with a low serial input data rate (lower than 3 Gbps), it is recommended to enable the low speed mode of the Clock Data Recovery (CDR) unit by writing the value x84 in register HS_RX_CDR_DIVX (see Table 159).

11.9.6 PHY test mode

A special test mode is available for measurement purposes only. The recovered clock of each CDR unit can be transmitted to the SYNC buffer after a frequency division by 20. This is done by setting the SYNC_TST_DATA_EN bit of register SYNC_SEL_CTRL to logic 1 (see Table 165). Bit SYNC_TST_DATA_SEL[1:0] is used to specify which CDR clock is used.

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11.10 Output interfacing configuration

11.10.1 DAC1658D: High common-mode output voltage

The DAC1658D can easily be interfaced with an IQ-modulator. Figure 84 is showing a typical connection in a 1Vpp configuration. Table 45 is showing various configurations regarding the common mode voltage of the IQ-modulator.

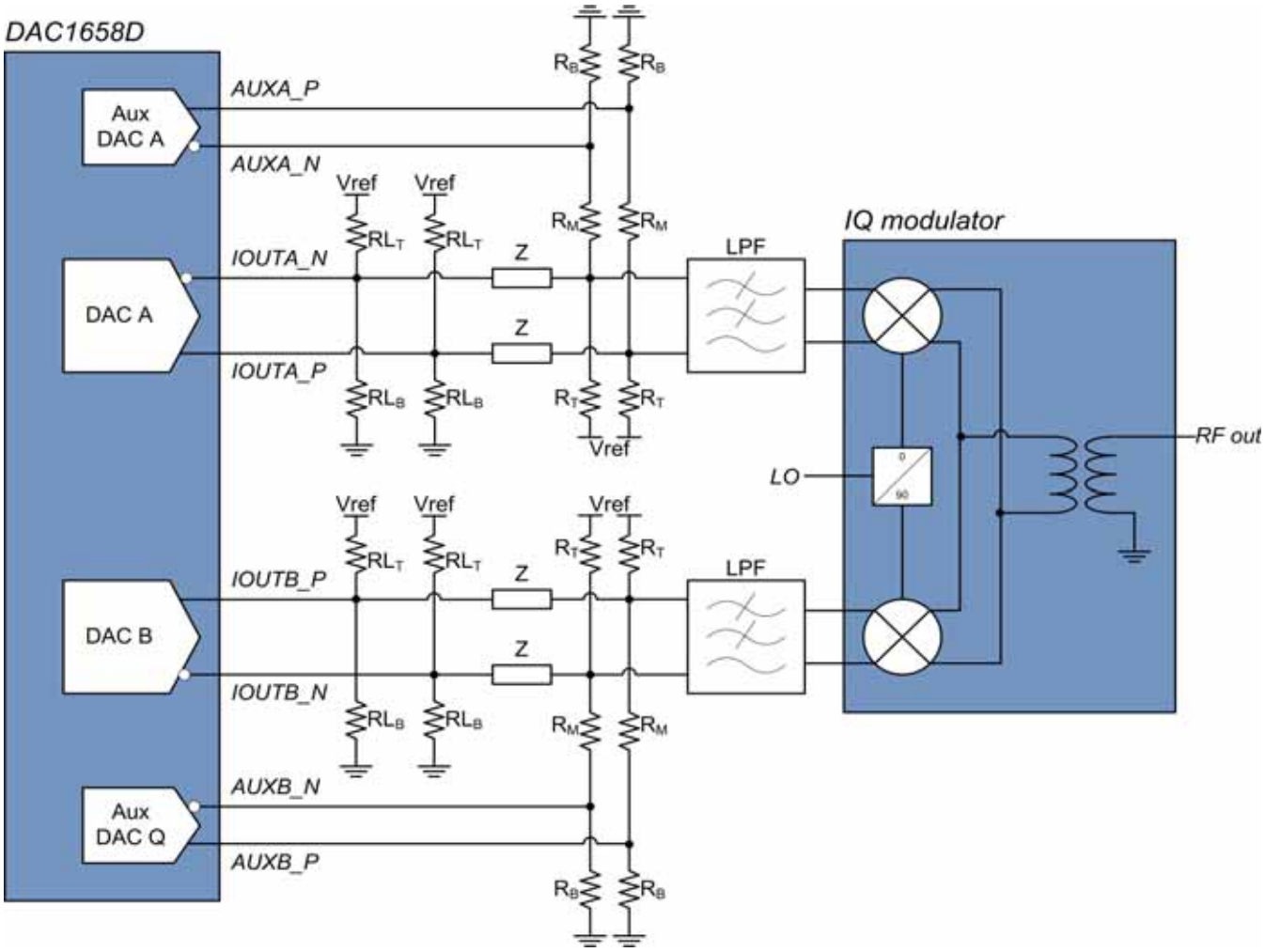


Fig 84. 1 V (p-p) interface to IQ-modulator (High common mode version)

Table 45. DAC1658D output configurations [1]

Mode	V_{ref}	Vo(cm)	Vo(diff)	VIQmod(cm)	VIQmod(diff)	RL_T	RL_B	Z	R_B	R_M	R_T
Unit	V	V	V	V	V	Ohms			Ohms	Ohms	Ohms
AC coupling	3.3	2.6	1	0.5	1	60.4	nc	10 nF	287	27.4	5360
AC coupling	3.3	2.55	1	0.3	1	64.9	nc	10 nF	196	34	8870
AC coupling	5	3	1	0.5	1	84.5	249	10 nF	243	14.7	5230
AC coupling	5	3	1	1.5	1	84.5	249	10 nF	309	18.7	976
AC coupling	5	3.3	1	1.7	1	84.5	249	10 nF	590	35.7	402
DC coupling	3.3	2.7	1	2.7	1	69.8	169	0 Ohms	nc	nc	nc

[1] All values are given considering that the load impedance (filter + IQ-modulator) is equal to 100 Ohms differential.

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11.10.2 DAC1653D: Low common-mode output voltage

The DAC1653D can easily be interfaced with an IQ-modulator. Figure 85 is showing a typical connection in a 1Vpp configuration. Table 46 is showing various configurations regarding the common mode voltage of the IQ-modulator.

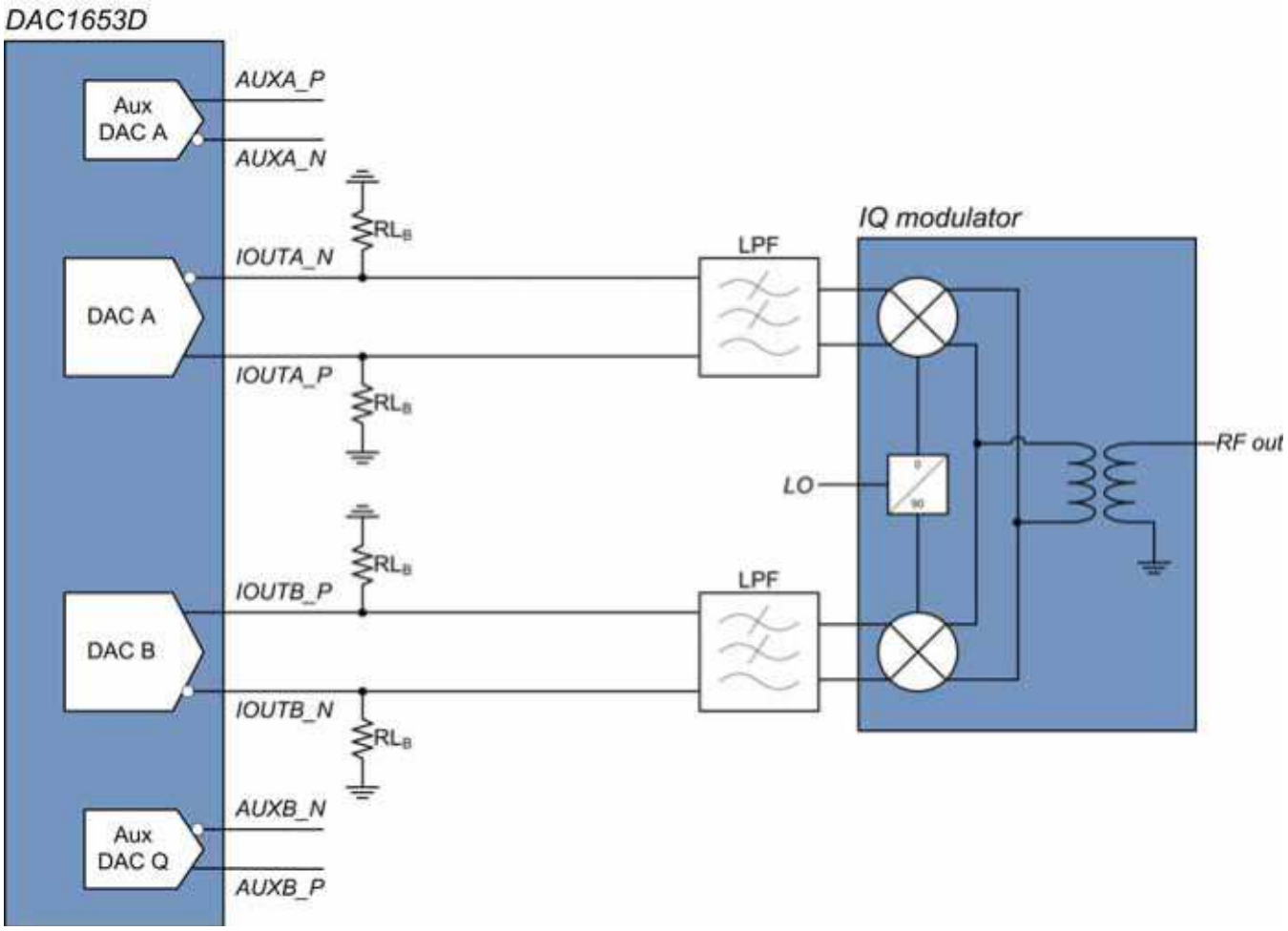


Fig 85. 1 V (p-p) interface to IQ-Modulator (Low common mode version)

Table 46. DAC1653D output configurations [1]

Mode	Vo(cm)	Vo(diff)	VIQmod(cm)	VIQmod(diff)	RL_B
Unit	V	V	V	V	Ohms
DC coupling	0.5	1	0.5	1	50

[1] All values are given considering that the load impedance (filter + IQ-modulator) is equal to 100 Ohms.

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11.11 Design recommendations

11.11.1 Power and grounding

Use a separate power supply regulator for the generation of the 1.2 V analog power (pins 43, 48. 51. 56) and the 1.2 V digital power (pins 7, 10, 33, 36) to ensure optimal performance.

High-speed input lanes are powered by a 1.2 V power supply that can require a dedicated power supply. Pins 15, 16, 19, 22, 25, 28 can be connected to either the global 1.2 V power supply or to a dedicated one.

Also, include individual LC decoupling for the following five sets of power pins:

- $V_{DDA(1V2)}$ (pins 43, 46, 48, 51, 53 and 56)
- $V_{DDD(1V2)}$ (core: pins 7, 10, 15, 16, 19, 22, 25, 28, 33 and 36)
- $V_{DDA(3V3)}$ (pins 47 and 52)
- $V_{DDD(IO)}$ (pin 29)
- $V_{DDD(sync)}$ (pin 11)

Use at least two capacitors for each power pin decoupling. Locate these capacitors as close as possible to the DAC165xD power pins.

Use a separate LDO for the generation of the 1.2 V analog power ($V_{DDA(1V2)}$ and the 1.2 V digital power (V_{DDD1V2}) to ensure the best performance.

The die pad is used for both the power dissipation and electrical grounding. Insert several vias (typically 8 × 8) to connect the internal ground plane to the top layer die area (see Figure 87).

Note: all the above applies if the 1.2 V is intended to be used as a 1.3 V for DAC sample rate above 1.8 Gsps.

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11.12 Registers

11.12.1 SPI configuration block

11.12.1.1 SPI configuration block register allocation map

Table 47 shows an overview all the interface DAC DSP registers.

Table 47. Interface DAC DSP register allocation map

Addr.	Register name	R/W	Bit definition								Default
Hex			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0000h	SPI_CFG_A	R/W	SPI_RST	-	SPI_ASC	SPI_4W	MIRROR[3:0]				00h
0001h	SPI_CFG_B	R/W	SPI_ SINGLE	-	SPI_ READ_ BUFF	-	-	-	-	-	00h
0002h	DEV_PWR_MOD	R/W	-	-	-	-	-	-	DEV_PWR_MOD[1:0]		00h
0003h	CHIP_TYPE	R	CHIP_TYPE[7:0]								04h
0004h	CHIP_ID_0	R	CHIP_ID_0[7:0]								
0005h	CHIP_ID_1	R	CHIP_ID_1[7:0]								
0006h	CHIP_VS	R	CHIP_VS[7:0]								01h
000Ch	VENDOR_ID_LSB	R	VENDOR_ID[7:0]								26h
000Dh	VENDOR_ID_MSB	R	VENDOR_ID[15:8]								04h
000Fh	SPI_CFG_C	R/W	-	-	-	-	-	-	-	TRANSFER _BIT	00h

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11.12.1.2 SPI configuration block bit definition detailed description

The tables in this section contain detailed descriptions of the SPI configuration registers.

Table 48. SPI configuration registers
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0000h	SPI_CFG_A	7	SPI_CFG_RST	R/W		reset SPI configuration
					0	**no action**
					1	sets all registers (except 000h/0001h) to their defaults (reserved for LSB first)
		5	SPI_ASC	R/W		auto-increment/auto-decrement
					0	**ascend off (auto-decrement)**
					1	ascend on (auto-increment)
		4	SPI_4W	R/W		SDO active; 3-wire/4-wire SPI interface
					0	**3-wire SPI-interface**
					1	4-wire SPI-interface
		3 to 0	MIRROR[3:0]	R/W		mirror check (write protection for this register): should be mirror [4:7]
0001h	SPI_CFG_B	7	SPI_SINGLE	R/W		streaming mode/one-byte mode
					0	**streaming mode**
					1	one-byte mode (independent of SCS_N)
		5	SPI_READ_BUFF	R/W		read back registers
					0	**read back resynchronized registers**
					1	read back buffer registers (double buffers)

Table 49. Device power mode register
Default values are shown highlighted.

DEV_PWR_MODE (address 0002h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
1 to 0	DEV_PWR_MOD[1:0]	R/W	00	device power mode; reserved

Table 50. Chip type register
Default values are shown highlighted.

CHIP_TYPE (address 0003h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7 to 0	CHIP_TYPE[7:0]	R	0000 0100	chip type; high-speed DAC

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Table 51. Chip registers
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0004h	CHIP_ID_0	7 to 0	CHIP_ID_0[7:0]	R		identification of the chip D4h: DAC1653D Low Common Mode F4h: DAC1658D High Common Mode
0005h	CHIP_ID_1	7 to 0	CHIP_ID_1[7:0]	R		identification of the chip
0006h	CHIP_VS	7 to 0	CHIP_VS[7:0]	R		version

Table 52. Chip vendor identification registers
Chip ID as defined per USB ID repository.

Address	Register	Bit	Symbol	Access	Value	Description
000Ch	VEND_ID_LSB	7 to 0	VEND_ID[7:0]	R		IDT vendor identification (LSB)
000Dh	VEND_ID_MSB	7 to 0	VEND_ID[15:8]	R		IDT vendor identification (MSB)

Table 53. SPI configuration register
Default values are shown highlighted.

SPI_CFG_C (address 000Fh)				
Bit	**Symbol**	**Access**	**Value**	**Description**
0	TRANSFER_BIT	R/W		transfer double-buffered registers (auto-clear)
			0	**double-buffered registers preserve current value**
			1	double-buffered registers are updated with values that are set using SPI

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11.12.2 Dual DAC core block

This block of registers specifies the main analog features of the DAC cores.

11.12.2.1 Dual DAC core block register allocation map

Table 54 shows an overview of all the dual DAC core registers.

Table 54. Dual DAC core block register allocation map

Addr.	Register name	R/W	Bit definition								Default
Hex			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0020h	PON_DDC_CFG_0	R/W	SEL_CLK	BGAP_PON	RESERVED[1:0]		DAC_B_PON	RESERVED	DAC_A_PON	RESERVED	FFh
0022h	WCLKGENCFG	R/W	CLK_MON_RST	CLK_GEN_EN_DIV	CLK_GEN_INIT_DIV	-	WCLK_DIV_BYP	WCLK_DIV_SEL[2:0]			52h
0024h	HRES_AUC_DAC	R/W	RESERVED	BYP_HRES_AUX_DAC	RESERVED[5:0]						FFh
0027h	PON_DCKDIV_CFG	R/W	PON_DCKDIV_2	PON_DCKDIV_1	-	-	-	-	-	-	00h
002Bh	MDS_MISC_CFG	R/W	-	MDS_SYSREF_POL_W	MDS_SYSREF_POL_E	-	RESERVED[3:0]				88h
0032h	DCKDIV_CFG	R/W	CLKDIV_SEL_DIV[1:0]		CLKDIV_RST	CLKDIV_SEL_FREQ	CLKDIV_BYP	CLKDIV_SEL_PHASE[2:0]			88h
0037h	DAC_A_AGAIN_LSB	R/W	DAC_A_AGAIN[7:0]								20h
0038h	DAC_A_AGAIN_MSB	R/W	DAC_A_AGAIN_PON	-	-	-	-	DAC_A_AGAIN_X2	DAC_A_AGAIN[9:8]		83h
0039h	DAC_B_AGAIN_LSB	R/W	DAC_B_AGAIN[7:0]								20h
003Ah	DAC_B_AGAIN_MSB	R/W	DAC_B_AGAIN_PON	-	-	-	-	DAC_B_AGAIN_X2	DAC_B_AGAIN[9:8]		83h
003Bh	DAC_A_AUX_LSB	R/W	DAC_A_AUX[7:0]								00h
003Ch	DAC_A_AUX_MSB	R/W	DAC_A_AUX_PON	-	-	-	-	-	DAC_A_AUX[9:8]		82h
003Dh	DAC_B_AUX_LSB	R/W	DAC_B_AUX[7:0]								00h
003Eh	DAC_B_AUX_MSB	R/W	DAC_B_AUX_PON	-	-	-	-	-	DAC_B_AUX[9:8]		82h

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11.12.2.2 Dual DAC core block bit definition detailed description

The tables in this section contain detailed descriptions of the dual DAC core registers.

Table 55. Dual DAC core power configuration register
Default values are shown highlighted.

PON_DDC_CFG_0 (address 0020h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7	SEL_CLK	R/W	0	DAC clock inactive
			1	**DAC clock provided via clock input**
6	BGAP_PON	R/W	0	Bandgap references power-down
			1	**Bandgap references enabled**
5 to 4	RESERVED	R/W	**11**	**reserved to 11**
3	DAC_B_PON	R/W	0	DAC B power-down
			1	**DAC B enabled**
2	RESERVED	R/W	**1**	**reserved to 1**
1	DAC_A_PON	R/W	0	DAC A power-down
			1	**DAC A enabled**
0	RESERVED	R/W	**1**	**reserved to 1**

Table 56. Word clock generation configuration register
Default values are shown highlighted.

WCLK_GEN_CFG (address 0022h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7	CLK_MON_RST	R/W	**0**	**no action**
			1	reset clk_mon_flag
6	CLK_GEN_EN_DIV	R	0	disable divide detector
			1	**enable divide dectector**
5	CLK_GEN_INIT_DIV	R/W	**0**	**free running mode**
			1	clear CLK_GEN divider
3	WCLK_DIV_BYP	R/W	**0**	**word clock depends on wclk_div_sel**
			1	WCLK = DAC clock
2 to 0	WCLK_DIV_SEL[2:0]	R/W	000	WCLK = DAC clock / 2 (see Table 25)
			001	WCLK = DAC clock / 3
			010	**WCLK = DAC clock / 4**
			011	WCLK = DAC clock / 6
			100	WCLK = DAC clock / 8
			101	WCLK = DAC clock / 12
			110	WCLK = DAC clock / 16
			111	WCLK = DAC clock / 24

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Table 57. High resolution auxiliary DAC register
Default values are shown highlighted.

HRES_AUX_DAC (address 0024h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7	RESERVED	R/W	**1**	**reserved**
6	BYP_HRES_AUX_DAC	R/W	0	enable high resolution auxiliary DACs mode
			1	**bypass high resolution auxiliary DACs mode**
5 to 0	RESERVED[5:0]	R/W	**11111**	**reserved**

Table 58. Power On Clock Divider buffer configuration register
Default values are shown highlighted.

PON_DCKDIV_CFG (address 0027h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7	PON_DCKDIV_2	R/W	**0**	**power off**
			1	power on
6	PON_DCKDIV_1	R/W	**0**	**power off**
			1	power on

Table 59. MDS SYSREF miscellaneous configuration register
Default values are shown highlighted.

MDS_MISC_CFG (address 002Bh)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7	RESERVED to 0		0	SYSREF signal used asynchronously
6	MDS_SYSREF_POL_W	R/W	**0**	**normal use**
			1	SYSREF_W is inverted
5	MDS_SYSREF_POL_E	R/W	**0**	**normal use**
			1	SYSREF_E is inverted
4	NOT USED	-	-	-
3 to 0	RESERVED	R/W	**1000**	**reserved**

Table 60. Input clock divider register
Default values are shown highlighted.

DCKDIV_CFG (address 0032h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7 to 6	CLKDIV_SEL_DIV[1:0]	R/W	00	DAC clock =CLK IN / 2
			01	DAC clock =CLK IN / 4
			10	**DAC clock =CLK IN / 6**
			11	DAC clock =CLK IN / 8
6	CLKDIV_RST	R/W	**0**	**no action**
			1	reset DAC clock dividers
4	CLKDIV_SEL_FREQ	R/W	**0**	**low frequency mode**
			1	high frequency mode
3	CLKDIV_CLK_BYP	R/W	0	DAC clock depend of CLKDIV_SEL_DIV[1:0]
			1	**DAC clock = CLK IN (dividers and phase are bypassed)**

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Table 60. Input clock divider register *…continued*
Default values are shown highlighted.

DCKDIV_CFG (address 0032h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
2 to 0	CLKDIV_SEL_PHASE[2:0]	R/W	**000**	**DAC clock phase = 0**
			001	DAC clock phase = 1 x (CLK IN period) /2
			010	DAC clock phase = 2 x (CLK IN period) /2
			011	DAC clock phase = 3 x (CLK IN period) /2
			100	DAC clock phase = 4 x (CLK IN period) /2
			101	DAC clock phase = 5 x (CLK IN period) /2
			110	DAC clock phase = 6 x (CLK IN period) /2
			111	DAC clock phase = 7 x (CLK IN period) / 2

Table 61. Analog gain control registers
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0037h	DAC_A_AGAIN_LSB	7 to 0	DAC_A_AGAIN[7:0]	R/W	-	least significant 8 bits for analog gain DAC A
0038h	DAC_A_AGAIN_MSB	7	DAC_A_AGAIN_PON	R/W		Analog gain DAC A power
					0	off
					1	**on** (see Section 11.5)
		2	DAC_A_AGAIN_X2		**0**	**off**
					1	output current doubled range
		1 to 0	DAC_A_AGAIN[9:8]		-	most significant 2 bits for analog gain DAC A
0039h	DAC_B_AGAIN_LSB	7 to 0	DAC_B_AGAIN[7:0]	R/W	-	least significant 8 bits for analog gain DAC B
003Ah	DAC_B_AGAIN_MSB	7	DAC_B_AGAIN_PON	R/W	-	Analog gain DAC B power
					0	off
					1	**on** (see Section 11.5)
		2	DAC_B_AGAIN_X2		**0**	**off**
					1	output current doubled range
		1 to 0	DAC_B_AGAIN[9:8]			most significant 2 bits for analog gain DAC B

Table 62. Auxiliary DACs registers
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
003Bh	DAC_A_AUX_LSB	7 to 0	DAC_A_AUX[7:0]	R/W	-	least significant 8 bits for auxiliary DAC A
003Ch	DAC_A_AUX_MSB	7	DAC_A_AUX_PON	R/W		auxiliary DAC A power
					1	**on** (see Section 11.5.2.1)
					0	off
		1 to 0	DAC_A_AUX[9:8]		-	most significant 2 bits for auxiliary DAC A

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Table 62. Auxiliary DACs registers *…continued*

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
003Dh	DAC_B_AUX_LSB	7 to 0	DAC_B_AUX[7:0]	R/W	-	least significant 8 bits for auxiliary DAC B
003Eh	DAC_B_AUX_MSB	7	DAC_B_AUX_PON	R/W		auxiliary DAC B power
					1	**on** (see Section 11.5.2.1)
					0	off
		1 to 0	DAC_B_AUX[9:8]		-	most significant 2 bits for auxiliary DAC B

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11.12.3 Main controls block

This block of registers specifies the main configuration of the different clocking systems used in the DAC165xD.

11.12.3.1 Main controls block register allocation map

Table 63 shows an overview of all the main controls registers.

Table 63. Main controls block register allocation map

Addr.	Register name	R/W	Bit definition								Default
Hex			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0040h	MAIN_CTRL	R/W	PD_P_LN_RX[3:0]				RESERVED[1:0]		FORCE_RST_DCLK	FORCE_RST_WCLK	03h
0042h	WATCHDOG	R/W	-	-	-	REINIT_MC_ALARM-DIS	WD_SYNC_SENS	WD_REINIT_DISABLE	WD_BARK_ONCE	WD_DISABLE	00h
0043h	PD_ANA_CTRL	R/W	-	-	-	-	-	-	RTFX_ENA_PD	PD_ANA_ENA	03h
0047h	EHS_CTRL	R/W	-	-	IO_DIR[1:0]		IO_EHS[1:0]		SDO_EHS[1:0]		2Ah
004Bh	CDI_CTRL	R/W	CDI_SW_RST	-	-	-	-	-	CDI_MODE[1:0]		00h
0050h	IO_MUX_CTRL0	R/W	IO_SEL_0[7:0]								15h
0051h	IO_MUX_CTRL1	R/W	IO_SEL_1[7:0]								15h
0052h	IO_MUX_CTRL2	R/W	IO_SEL_2[7:0]								00h
0054h	MON_DCLK	R	MON_DCLK_STOP	-	NO_ACT_F20_FLAG	ILA_RCV_FLAG	MON_DCLK[3:0]				uuh
0055h	MON_DCLK_FLAGS	R	MON_DCLK_FLAGS[7:0]								uuh

[1] u = undefined at power-up or after reset.

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11.12.3.2 Main controls block bit definition detailed description

The tables in this section contain detailed descriptions of the main controls registers.

Table 64. Main controls register
Default values are shown highlighted.

MAIN_CTRL (address 0040h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7 to 4	PD_P_LN_RX[3:0]	R/W	-	power-down of the physical lane receiver bit 7 = lane 3 bit 6 = lane 2 bit 5 = lane 1 bit 4 = lane 0
3 to 2	RESERVED[1:0]	R/W	**00**	**reserved to 00**
1	FORCE_RST_DCLK	R/W		digital clock reset
			0	release digital clock reset
			1	**force digital clock reset**
0	FORCE_RST_WCLK	R/W		work clock reset
			0	release work clock reset
			1	**force work clock reset**

Table 65. Watch Dog control register
Default values are shown highlighted.

WATCHDOG (address 0042h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
4	REINIT_MC_ALARM_DIS			
3	WD_SYNC_SENS			
2	WD_REINIT_DISABLE			
1	WD_BARK_ONCE			
0	WD_DISABLE			disable the watchdog for PRBS testing (need to write 1)

Table 66. Power Down control register
Default values are shown highlighted.

PD_ANA_CTRL (address 0043h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
1	RFTX_ENA_PD	R/W		use RF_ENABLE pin as a trigger for Power Down mode
			0	RF_ENABLE pin is not used for power Down mode
			1	**RF_ENABLE pin is used for Power Down mode**
0	PD_ANA_ENA	R/W	0	no action
			1	**Power Down analog (except clocks)**

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Table 67. EHS control register
Default values are shown highlighted.

EHS_CTRL (address 0047h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
5 to 4	IO_DIR[1:0]	R/W	**10**	**IO control direction , 1 = input, 0 = output**
3 to 2	IO_EHS[1:0]	R/W	**10**	IO EHS-drive control (see next table)
1 to 0	SDO_EHS[1:0]	R/W	**10**	SDO/SDIO EHS-drive control (see next table)

Table 68. EHS modes
Programmable current drive strength.

xx_EHS	
Value	**Output mode**
00	very low noise / low speed
01	medium noise / fast speed
10	**low noise / medium speed**
11	high noise / high speed

Table 69. Clock domain interface reset register
Default values are shown highlighted.

CDI_CTRL (address 004Bh)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7	CDI_SW_RST	R/W		CDI block software reset control
			0	**no action**
			1	perform a software reset on CDI
1 to 0	CDI_MOD[1:0]	R/W		CDI mode specification (see Table 27)
			00	**cdi_mode 0 (^2 mode)**
			01	cdi_mode 1 (^4 mode)
			10	cdi_mode 2 (^8 mode)
			11	not used

Table 70. IO_MUX and MON_DCLK registers
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0050h	IO_MUX_CTRL_0	7 to 0	IO_SEL_0[7:0]	R/W	-	io_mux select for IO 0
0051h	IO_MUX_CTRL_1	7 to 0	IO_SEL_1[7:0]	R/W	-	io_mux select for IO 1
0052h	IO_MUX_CTRL_2	7 to 0	IO_SEL_2[7:0]	R/W	-	io_mux select for io[1:0]
0054h	MON_DCLK	7	MON_DCLK_STOP	R	-	stop digital clock monitoring
		5	NO_ACT_F20_FLAG		-	indicates inactivity of the recovered clock in the CDR
		4	ILA_RCV_FLAG		-	indicates that ILA-sequence has been received
		3 to 0	MON_DCLK[3:0]		-	digital clock monitoring
0055h	MON_DCLK_FLAGS	7 to 0	MON_DCLK_FLAGS[7:0]	R	-	digital clock monitoring flags

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11.12.4 Interface DAC DSP block

This block of registers specifies the main features of the digital signal processing of the DAC165xD.

11.12.4.1 Interface DAC DSP block register allocation map

Table 71 shows an overview all the interface DAC DSP registers.

Table 71. Interface DAC DSP register allocation map

Addr.	Register name	R/W	Bit definition								Default
Hex			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0060h	TX_CFG	R/W	NCO_EN	NCO_LP_SEL	INV_SINC_SEL	MODULATION[2:0]			INTERPOLATION[1:0]		01h
0062h	NCO_PH_OFFSET_LSB[2]	R/W	NCO_PH_OFFSET[7:0]								00h
0063h	NCO_PH_OFFSET_MSB[2]	R/W	NCO_PH_OFFSET[15:8]								00h
0064h	NCO_FREQ_B0[2]	R/W	NCO_FREQ[7:0]								66h
0065h	NCO_FREQ_B1[2]	R/W	NCO_FREQ[15:8]								66h
0066h	NCO_FREQ_B2[2]	R/W	NCO_FREQ[23:16]								66h
0067h	NCO_FREQ_B3[2]	R/W	NCO_FREQ[31:24]								66h
0068h	NCO_FREQ_B4[2]	R/W	NCO_FREQ[39:32]								26h
0069h	PH_CORR_CTRL_0[2]	R/W	PH_CORR[7:0]								00h
006Ah	PH_CORR_CTRL_1[2]	R/W	PH_COR_EN	-	-	PH_CORR[12:8]					00h
006Bh	DAC_A_DGAIN_LSB[2]	R/W	DAC_A_DGAIN[7:0]								50h
006Ch	DAC_A_DGAIN_MSB[2]	R/W	-	-	-	-	DAC_A_DGAIN[11:8]				0Bh
006Dh	DAC_B_DGAIN_LSB[2]	R/W	DAC_B_DGAIN[7:0]								50h
006Eh	DAC_B_DGAIN_MSB[2]	R/W	-	-	-	-	DAC_B_DGAIN[11:8]				0Bh
006Fh	DAC_OUT_CTRL[2]	R/W	-	-	-	-	A_DGAIN_EN	B_DGAIN_EN	MINUS_3DB	LVL_DET_EN	00h
0070h	DAC_LVL_DET[2]	R/W	LVL_DET[7:0]								FFh
0071h	DAC_A_OFFSET_LSB[2]	R/W	DAC_A_OFFSET[7:0]								00h
0072h	DAC_A_OFFSET_MSB[2]	R/W	DAC_A_OFFSET[15:8]								00h
0073h	DAC_B_OFFSET_LSB[2]	R/W	DAC_B_OFFSET[7:0]								00h

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Table 71. Interface DAC DSP register allocation map *…continued*

Addr.	Register name	R/W	Bit definition								Default
Hex			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0074h	DAC_B_OFFSET_MSB[2]	R/W	DAC_B_OFFSET[15:8]								00h
0075h	CODING_IQ[2]	R/W	CODING_IQ	-	-	-	I_LVL_CTRL[1:0]		Q_LVL_CTRL[1:0]		85h
0076h	I_DC_LVL_LSB[2]	R/W	I_DC_LVL[7:0]								00h
0077h	I_DC_LVL_MSB[2]	R/W	I_DC_LVL[15:8]								80h
0078h	Q_DC_LVL_LSB[2]	R/W	Q_DC_LVL[7:0]								00h
0079h	Q_DC_LVL_MSB[2]	R/W	Q_DC_LVL[15:8]								80h
007Ah	SPD_CTRL[2]	R/W	SPD_EN	-	-	-	SPD_WINLENGTH				00h
007Bh	SPD_THRESHOLD_LSB[2]	R/W	SPD_THRESHOLD[7:0]								00h
007Ch	SPD_THRESHOLD_MSB[2]	R/W	SPD_THRESHOLD[15:8]								00h
007Dh	SPD_AVG_LSB	R	SPD_AVG[7:0]								uuh
007Eh	SPD_AVG_MSB	R	SPD_AVG[15:8]								uuh

[1] u = undefined at power-up or after reset.

[2] These registers use a double buffer (see Section 11.2.1.3).

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11.12.4.2 Interface DAC DSP block bit definition detailed description

The tables in this section contain detailed descriptions of the interface DAC DSP registers.

Table 72. Transmission configuration register
Default values are shown highlighted.

TX_CFG (address 0060h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7	NCO_EN	R/W		NCO (see Section 11.2.3.4)
			0	**NCO disabled, the NCO phase is reset to 0**
			1	NCO enabled
6	NCO_LP_SEL	R/W		NCO low-power selection (see Section 11.2.3.5)
			0	**low-power NCO disabled**
			1	low-power NCO enabled (frequency and phase given by the five MSB of the registers 68h and 63h, respectively)
5	INV_SIN_SEL	R/W		inverse (sin x) / x function selection (see Section 11.2.3.8)
			0	**disabled**
			1	enabled
4 to 2	MODULATION[2:0]	R/W		modulation (see Section 11.2.3.3)
			000	**dual DAC: no modulation**
			001	positive upper single sideband upconversion
			010	positive lower single sideband upconversion
			011	negative upper single sideband upconversion
			100	negative lower single sideband upconversion
			others	not defined
1 to 0	INTERPOLATION[1:0]	R/W		interpolation (see Section 11.2.3.2)
			00	no interpolation
			01	**×2 interpolation**
			10	×4 interpolation
			11	×8 interpolation

Table 73. Numerically controlled oscillator phase offset registers
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0062h	NCO_PH_OFFSET_LSB	7 to 0	NCO_PH_OFFSET[7:0]	R/W	-	least significant 8 bits for the NCO phase offset
0063h	NCO_PH_OFFSET_MSB	7 to 0	NCO_PH_OFFSET[15:8]	R/W	-	most significant 8 bits for the NCO phase offset (see Section 11.2.3.4)

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Table 74. Numerically controlled oscillator frequency registers
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0064h	NCO_FREQ_B0	7 to 0	NCO_FREQ[7:0]	R/W		NCO frequency (see Section 11.2.3.4)
					-	least significant 8 bits for the NCO frequency setting
0065h	NCO_FREQ_B1	7 to 0	NCO_FREQ[15:8]	R/W	-	intermediate 8 bits for the NCO frequency setting
0066h	NCO_FREQ_B2	7 to 0	NCO_FREQ[23:16]	R/W	-	intermediate 8 bits for the NCO frequency setting
0067h	NCO_FREQ_B3	7 to 0	NCO_FREQ[31:24]	R/W	-	intermediate 8 bits for the NCO frequency setting
0068h	NCO_FREQ_B4	7 to 0	NCO_FREQ[39:32]	R/W	-	most significant 8 bits for the NCO frequency setting

Table 75. DAC output phase correction factor registers
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0069h	PH_CORR_CTRL_0	7 to 0	PH_CORR[7:0]	R/W		DAC output phase correction factor (LSB)
					-	least significant 8 bits for the DAC output phase correction factor
006Ah	PH_CORR_CTRL_1	7	PH_CORR_EN	R/W		DAC output phase correction control
					0	**DAC output phase correction disabled**
					1	DAC output phase correction enabled (see Section 11.2.3.7)
		4 to 0	PH_CORR[12:8]	R/W		DAC output phase correction factor (MSB)
					-	most significant 5 bits for the DAC output phase correction factor

Table 76. DAC digital gain control registers
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
006Bh	DAC_A_DGAIN_LSB	7 to 0	DAC_A_DGAIN[7:0]	R/W		DAC A digital gain control (see Section 11.2.3.9)
					-	least significant 8 bits for DAC A digital gain
006Ch	DAC_A_DGAIN_MSB	3 to 0	DAC_A_DGAIN[11:8]	R/W	-	most significant 4 bits for DAC A digital gain
006Dh	DAC_B_DGAIN_LSB	7 to 0	DAC_B_DGAIN[7:0]	R/W		DAC B digital gain control (see Section 11.2.3.9)
					-	least significant 8 bits for DAC B digital gain
006Eh	DAC_B_DGAIN_MSB	3 to 0	DAC_B_DGAIN[11:8]	R/W	-	most significant 4 bits for DAC B digital gain

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Table 77. DAC output control register
Default values are shown highlighted.

DAC_OUT_CTRL (address 006Fh)				
Bit	**Symbol**	**Access**	**Value**	**Description**
3	DAC_A_DGAIN_EN	R/W		DAC A digital gain control (see Section 11.2.3.9)
			0	**disable**
			1	enable
2	DAC_B_DGAIN_EN	R/W		DAC B digital gain control (see Section 11.2.3.9)
			0	**disable**
			1	enable
1	MINUS_3DB	R/W		DAC attenuation control (see Section 11.2.3.6)
			0	**unity gain**
			1	–3 dB gain
0	LVL_DET_EN	R/W		Digital DAC output level detector control
			0	**disable**
			1	enable (see Section 11.2.4.1)

Table 78. Register level detector
Default values are shown highlighted.

DAC_LVL_DET (address 0070h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7 to 0	LVL_DET[7:0]	R/W	-	Digital DAC output level detector value (see Section 11.2.4.1)

Table 79. DAC digital offset registers
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0071h	DAC_A_OFFSET_LSB	7 to 0	DAC_A_OFFSET[7:0]	R/W		DAC A digital offset value (see Section 11.2.3.11)
					-	least significant 8 bits for DAC A digital offset
0072h	DAC_A_OFFSET_MSB	3 to 0	DAC_A_OFFSET[15:8]	R/W	-	most significant 8 bits for DAC A digital offset
0073h	DAC_B_OFFSET_LSB	7 to 0	DAC_B_OFFSET[7:0]	R/W		DAC B digital offset value (see Section 11.2.3.11)
					-	least significant 8 bits for DAC B digital offset
0074h	DAC_B_OFFSET_MSB	3 to 0	DAC_B_OFFSET[15:8]	R/W	-	most significant 8 bits for DAC B digital offset

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Table 80. Input word coding register
Default values are shown highlighted.

CODING_IQ (address 0075h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7	CODING_IQ	R/W	-	coding of input word (see Section 11.2.3.1)
			0	two's complement coding
			1	**unsigned format**
6 to 4	RESERVED[2:0]	R/W	**000**	**reserved to 000**
3 to 2	I_LVL_CTRL[1:0]	R/W		specifies output from CDI for the I path
			00	normal operation (CDI data output sent to digital signal processing input)
			01	**if end of ila = 1: normal operation**
				if end of ila = 0: digital signal processing input = I_DC_LVL register value
			10	digital signal processing input = I_DC_LVL
			11	digital signal processing input = I_DC_LVL
1 to 0	Q_LVL_CTRL[1:0]	R/W		specifies output from CDI for the Q path
			00	normal operation (CDI data output sent to digital signal processing input)
			01	**if end of ila = 1: normal operation**
				if end of ila = 0: digital signal processing input = Q_DC_LVL register value
			10	digital signal processing input = Q_DC_LVL
			11	digital signal processing input = Q_DC_LVL

Table 81. LSB/MSB of I/Q levels register
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0076h	I_DC_LVL_LSB	7 to 0	I_DC_LVL[7:0]	R/W	-	least significant 8 bits for I_DC_LVL
0077h	I_DC_LVL_MSB	7 to 0	I_DC_LVL[15:8]	R/W	-	most significant 8 bits for I_DC_LVL
0078h	Q_DC_LVL_LSB	7 to 0	Q_DC_LVL[7:0]	R/W	-	least significant 8 bits for Q_DC_LVL
0079h	Q_DC_LVL_MSB	7 to 0	Q_DC_LVL[15:8]	R/W	-	most significant 8 bits for Q_DC_LVL

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Table 82. Signal power detector control register
Default values are shown highlighted.

SPD_CTRL (address 007Ah)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7	SPD_EN	R/W	-	Signal power detector:
			0	**disabled**
			1	enabled
3 to 0	SPD_WINLENGTH[3:0]	R/W		SPD averages $2^{(winlength + 6)}$; IQ pairs
			0000	**average 64 pairs (2^6 samples)**
			0001	average 128 pairs (2^7 samples)
			0010	average 256 pairs (2^8 samples)
			0011	average 512 pairs (2^9 samples)
			0100	average 1024 pairs (2^{10} samples)
			0101	average 2048 pairs (2^{11} samples)
			0110	average 4096 pairs (2^{12} samples)
			0111	average 8192 pairs (2^{13} samples)
			1000	average 16384 pairs (2^{14} samples)
			1001	average 32768 pairs (2^{15} samples)
			1010	average 65536 pairs (2^{16} samples)
			1011	average 131073 pairs (2^{17} samples)
			1100	average 262144 pairs (2^{18} samples)
			1101	average 524288 pairs (2^{19} samples)
			1110	average 1048576 pairs (2^{20} samples)
			1111	average 2097152 pairs (2^{21} samples)

Table 83. SPD LSB/MSB registers
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
007Bh	SPD_THRESHOLD_LSB	7 to 0	SPD_THRESHOLD[7:0]	R/W	-	least significant 8 bits for SPD_THRESHOLD
007Ch	SPD_THRESHOLD_MSB	7 to 0	SPD_THRESHOLD[15:8]	R/W	-	most significant 8 bits for SPD_THRESHOLD
007Dh	SPD_AVG_LSB	7 to 0	SPD_AVG[7:0]	R	uuuu uuuu	least significant 8 bits for SPD_AVG
007Eh	SPD_AVG_MSB	7 to 0	SPD_AVG[15:8]	R	uuuu uuuu	most significant 8 bits for SPD_AVG

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11.12.5 Mute, interrupt, and temperature control

This block of registers specifies the main features of the mute, interrupt and temperature control of the DAC165xD.

11.12.5.1 Mute, interrupt and temperature control register allocation map

Table 84 shows an overview all the interface Mute, interrupt and temperature control registers.

Table 84. Mute, interrupt and temperature control register allocation map

Addr.	Register name	R/W	Bit definition								Default
Hex			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0080h	MUTE_CTRL_0	R/W	MUTE_ENA	SW_MUTE	ALARM_CLR	HOLD_DATA	-	LEV_DET_ENA	LEV_SEL[1:0]		90h
0081h	MUTE_CTRL_1	R/W	INCIDENT_CFG[1:0]		DATA_V_IQ_CFG[1:0]		ALARM_CFG[1:0]		DIRECT_CFG[1:0]		77h
0082h	MUTE_CTRL_2	R/W	IGN_ALARM	IGN_RF_EN	IGN_MDS_BSY	IGN_DATA_IQ_VAL	-	ENA_IQR_INCIDENT	ENA_SPD_INCIDENT	ENA_ERF_INCIDENT	81h
0083h	MUTE_ALARM_EN_0	R/W	DATA_IQ_VAL	MC_MDS_BSY	MC_LVL_DET_OR	MC_ERR_RPT_FLAG	MC_TEMP_ALARM	MC_CLK_ALIGN_ERR	MC_DCLK_ERR_MON	MC_CLK_MON	00h
0084h	MUTE_ALARM_EN_1	R/W	-	-	-	-	-	-	IQR_ERR	SPD_OVF	00h
0085h	MUTE_RATE_CTRL_0	R/W	ALARM_MUTE_RATE[3:0]				DIRECT_MUTE_RATE[3:0]				7Ch
0086h	MUTE_RATE_CTRL_1	R/W	INCIDENT_MUTE_RATE[3:0]				DATA_MUTE_RATE[3:0]				7Ch
0087h	MUTE_WAIT_PERIOD_LSB	R/W	MUTE_WAIT_PERIOD[7:0]								40h
0088h	MUTE_WAIT_PERIOD_MSB	R/W	MUTE_WAIT_PERIOD[15:8]								00h
0089h	IQ_RANGE_LIMIT_LSB	R/W	IQ_RANGE_LIMIT[7:0]								00h
008Ah	IQ_RANGE_LIMIT_MSB	R/W	IQ_RANGE_DIS	IQ_RANGE_LIMIT[14:8]							80h
008Ch	INTR_CTRL	R/W	-	-	-	-	INTR_RST	INTR_DCLK_MON_RANGE_[2:0]			08h
008Dh	INTR_EN_0	R/W	INTR_EN[7:0]								00h
008Eh	INTR_EN_1	R/W	-	INTR_EN[9:8]		RESERVED[4:0]					00h
008Fh	INTR_FLAGS_0	R/W	INTR_DLP	$\overline{\text{MDS_BSY}}$	MDS_BSY	TEMP_ALARM	LVL_DET_OR	CLK_ALIGN_ERR	CLK_MON	DCLK_ERR_MON	uuh

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Table 84. Mute, interrupt and temperature control register allocation map *…continued*

Addr.	Register name	R/W	Bit definition								Default
Hex			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0090h	INTR_FLAGS_1	R/W	-	RPT_FLAG_ERR	MUTE_CTRL_ALARM	-	-	-	-	-	uuh
0092h	TEMP_CTRL	R/W	TEMP_SENS_PON	TEMP_SENS_RST_ALARM	TEMP_SENS_FULL_RANGE	TEMP_SENS_TOGGLE	TEMP_SENS_RST_MAX	TEMP_SENS_RST_MIN	TEMP_SENS_MOD[1:0]		00h
0093h	TEMP_LVL	R/W	-	-	TEMP_SEL_MAN[5:0]						00h
0094h	TEMP_CLK_DIV	R/W	TEMP_CLK_DIV[7:0]								00h
0095h	TEMP_SENS_TIMER	R/W	TEMP_SENS_TIMER[7:0]								00h
0096h	TEMP_OUT	R	TEMP_SENS_OUT	TEMP_ALARM	TEMP_ACTUAL[5:0]						uuh
0097h	TEMP_MAX	R	-	-	TEMP_MAX[5:0]						uuh
0098h	TEMP_MIN	R	-	-	TEMP_MIN[5:0]						uuh
0099h	DSP_SMPL_CTRL	R/W	-	-	-	DSP_READ_SEL	DSP_STROBE	DSP_SMPL_SEL[2:0]			00h
009Ah	DSP_READ_LSB	R	DSP_READ[7:0]								uuh
009Bh	DSP_READ_LSIB	R	DSP_READ[15:8]								uuh
009Ch	DSP_READ_MSIB	R	DSP_READ[23:16]								uuh
009Dh	DSP_READ_MSB	R	DSP_READ[31:24]								uuh

[1] u = undefined at power-up or after reset.

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11.12.5.2 Mute, interrupt and temperature control bit definition detailed description

The tables in this section contain detailed descriptions of the Mute, Interrupt and Temperature Sensor control registers.

Table 85. Mute control registers
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0080h	MUTE_CTRL_0			R/W		mute control (see Section 11.2.3.10)
		7	MUTE_ENA		0	disables mute feature
					1	**enables mute feature**
		6	SW_MUTE		**0**	**no action**
					1	software mute (use DIRECT_CFG)
		5	ALARM_CLR		**0**	**no action**
					1	clear alarm flags
		4	HOLD_DATA		0	disable hold feature
					1	**enable hold feature**
		2	LEV_DET_ENA		**0**	**disable level detection**
					1	enable level detection
		1 to 0	LEV_DET_SEL[1:0]			specify the level detectors combination (only if LEV_DET_ENA is set)
					00	**no mute action**
					01	mute on LEV_DET_A
					10	mute on LEV_DET_B
					11	mute on LEV_DET_A or LEV_DET_B
0081h	MUTE_CTRL_1	7 to 6	INCIDENT_CFG[1:0]	R/W	00	hard mute and mute_iq
					01	**hold mute and mute_iq**
					10	soft mute and mute_iq
					11	soft mute
		5 to 4	DATA_V_IQ_CFG[1:0]		00	hard mute and mute_iq
					01	hold mute and mute_iq
					10	soft mute and mute_iq
					11	**soft mute**
		3 to 2	ALARM_DET_CFG[1:0]		00	hard mute and mute_iq
					01	**hold mute and mute_iq**
					10	soft mute and mute_iq
					11	soft mute
		1 to 0	DIRECT_CFG[1:0]		00	hard mute and mute_iq
					01	hold mute and mute_iq
					10	soft mute and mute_iq
					11	**soft mute**

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Table 85. Mute control registers *…continued*
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0082h	MUTE_CTRL_2	7	IGN_ALARM	R/W	0	no action
					1	**ignore alarm trigger**
		6	IGN_RF_EN		**0**	**no action**
					1	ignore RF_ENABLE state
		5	IGN_MDS_BSY		**0**	**no action**
					1	ignore mds_bsy state
		4	IGN_DATA_V_IQ		**0**	**no action**
					1	ignore internal data error detection
		2	ENA_IQR_INCIDENT		**0**	**no action**
					1	enable IQ-out-of-Range as incident
		1	ENA_SPD_INCIDENT		**0**	**no action**
					1	enable SignalPowerDetector detector as incident
		0	ENA_ERF_INCIDENT		0	no action
					1	**enable ErrorReportFlag (DLP) as incident**

Table 86. Mute alarm enable registers
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0083h	MUTE_ALARM_EN_0					enables alarm condition for mute action (see Section 11.2.3.10)
		7	DATA_IQ_VAL	R/W	**0**	**1 → 0**
					1	0 → 1
		6	MC_MDS_BSY	R/W	**0**	**0 → 1**
					1	1 → 0
		5	MC_LVL_DET_OR	R/W	**0**	**0 → 1**
					1	1 → 0
		4	MC_ERR_RPT_FLAG	R/W	**0**	**0 → 1**
					1	1 → 0
		3	MC_TEMP_ALARM	R/W	**0**	**0 → 1**
					1	1 → 0
		2	MC_CLK_ALIGN_ERR	R/W	**0**	**0 → 1**
					1	1 → 0
		1	MC_DCLK_ERR_MON	R/W	**0**	**0 → 1**
					1	1 → 0
		0	MC_CLK_MON	R/W	**0**	**0 → 1**
					1	1 → 0

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Table 86. Mute alarm enable registers *...continued*
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0084h	MUTE_ALARM_EN_1	1	IQ_RANGE	R/W	**0**	**0 → 1**
					1	1 → 0
		0	SPD_OVF	R/W	**0**	**0 → 1**
					1	1 → 0

Table 87. Mute rate control registers
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0085h	MUTE_RATE_CTRL_0	7 to 4	ALARM_MUTE_RATE[3:0]	R/W	**0111**	sets mute and unmute rate in case of an alarm event
		3 to 0	DIRECT_MUTE_RATE[3:0]	R/W	**1100**	sets mute and unmute rate in case of direct mute control
0086h	MUTE_RATE_CTRL_1	7 to 4	INCIDENT_MUTE_RATE[3:0]	R/W	**0111**	sets mute and unmute rate in case of an incident
		3 to 0	DATA_MUTE_RATE[3:0]	R/W	**1100**	sets mute and unmute rate in case of a data error detection

Table 88. Mute wait period LSB/MSB registers
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0087h	MUTE_WAIT_PERIOD_LSB	7 to 0	MUTE_WAIT_PERIOD[7:0]	R/W	**0100 0000**	least significant 8 bits for MUTE_WAIT_PERIOD
0088h	MUTE_WAIT_PERIOD_MSB	7 to 0	MUTE_WAIT_PERIOD[15:8]	R/W	**0000 0000**	most significant 8 bits for MUTE_WAIT_PERIOD

Table 89. IQ range limit LSB/MSB registers
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0089h	IQ_RANGE_LIMIT_LSB	7 to 0	IQ_RANGE_LIMIT[7:0]	R/W	**0000 0000**	least significant 8 bits for IQ_RANGE_LIMIT
008Ah	IQ_RANGE_LIMIT_MSB	7	IQ_RANGE_DIS	R/W	**1**	**disable IQ-out-of-Range detector**
		6 to 0	IQ_RANGE_LIMIT[14:8]	R/W	**0000 0000**	most significant 8 bits for IQ_RANGE_LIMIT

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Table 90. Interrupt control register
Default values are shown highlighted.

INTR_CTRL (address 008Ch)				
Bit	**Symbol**	**Access**	**Value**	**Description**
3	INTR_RST	R/W		reset INTERRUPT signal and Interrupts flags (intr_flags[9:0])
			0	disabled
			1	**enabled (see Section 11.8)**
2 to 0	INTR_DCLK_MON_RANGE[2:0]	R/W		interrupt condition as related to the DCLK monitoring (see Figure 59)
			000	**interrupt when CDI buffer drifts to (1 | 9)**
			001	interrupt when CDI buffer drifts to (2 | 8)
			010	interrupt when CDI buffer drifts to (3 | 7)
			011	interrupt when CDI buffer drifts to (4 | 6)
			100	interrupt when CDI buffer drifts to (5)
			others	interrupt disabled

Table 91. Interrupt enable registers
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
008Dh	INTR_EN_0	7 to 0	INTR_EN[7:0]	R/W	**0000 0000**	enables usage of intr_src[7:0] for intr_flags[7:0]
008E	INTR_EN_1	6 to 5	INTR_EN[9:8]	R/W	**0000 0000**	enables usage of intr_src[9:8] for intr_flags[9:8] (see Table 92)

Table 92. Interrupt flags registers
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
008Fh	INTR_FLAGS_0	7	INTR_DLP	R	-	intr_dlp active
		6	$\overline{\text{MDS_BSY}}$		-	indicates transition 1 → 0 on mds_busy
		5	MDS_BSY		-	indicates transition 0 → 1 on mds_busy
		4	TEMP_ALARM		-	indicates transition 0 → 1 on temp_alarm
		3	CLIP_DET_OR		-	indicates transition 0 → 1 on clip_detect (a or b)
		2	CLK_ALIGN_ERR		-	indicates transition 0 → 1 on clock_align_monitor
		1	CLK_MON		-	indicates transition 0 → 1 on clkmon (div8)
		0	MON_DCLK_ERR		-	indicates transition 0 → 1 on mon_dclk_error_flags

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Table 92. Interrupt flags registers *...continued*
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0090h	INTR_FLAGS_1	6	ERR_RPT_FLAG	R	-	indicates transition 0 → 1 on err_rpt_flag
		5	MUTE_CTRL_ ALARM		-	indicates alarm event detected by mute_ctrl
		4 to 0	RESERVED		-	reserved

Table 93. Temperature Sensor control register
Default values are shown highlighted.

TEMP_SENS_CTRL register (address 0092h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7	TEMP_SENS_PON	R/W		temperature sensor power
			0	**disabled (power-down)**
			1	enabled (see Section 11.6)
6	TEMP_SENS_RST_ALARM	R/W		reset temperature sensor alarm
			0	**no action**
			1	reset temp_sensor_alarm flag
5	TEMP_SENS_FULLRANGE	R/W		temperature sensor full range
			0	**sweep 22 to 63**
			1	sweep 0 to 63
4	TEMP_SENS_TOGGLE	R/W		temperature sensor toggle
			0	**wait for 0 → 1 transition**
			1	wait for 1 → 0 transition
3	TEMP_SENS_RST_MAX	R/W		temperature sensor, maximum reset
			0	**no action**
			1	reset temp_max_value
2	TEMP_SENS_RST_MIN	R/W		temperature sensor, minimum reset
			0	**no action**
			1	reset temp_min_value
1 to 0	TEMP_SENS_MOD[1:0]	R/W		temperature sensor mode
			00	**raw mode (direct access to temperature sensor)**
			01	one-shot measurement
			10	continuous measurement
			11	continuous measurement (hold temp_alarm_flag)

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Table 94. Temperature Sensor level register
Default values are shown highlighted.

TEMP_LVL (address 0093h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
5 to 0	TEMP_SEL_MAN[5:0]	R/W	-	temperature sensor level selection usage depends on ts_mode: TEMP_SENS_MOD = “00”: applied directly to temp_sensor TEMP_SENS_MOD = “others”: sets threshold for temp_alarm

Table 95. Temperature Sensor clock divider register
Default values are shown highlighted.

TEMP_CLK_DIV (address 0094h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7 to 0	TEMP_CLK_DIV[7:0]	R/W	-	sets clock frequency temp_sensor_ctrl (dclk / temp_sens_clkdiv)

Table 96. Temperature Sensor timer register
Default values are shown highlighted.

TEMP_SENS_TIMER (address 0095h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7 to 0	TEMP_SENS_TIMER[7:0]	R/W	-	sets number of wait cycles between measurements

Table 97. Temperature Sensor output register
Default values are shown highlighted.

TEMP_SENS_OUT (address 0096h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7	TEMP_SENS_OUT	R	-	Temperature Sensor output (for use in raw mode)
6	TEMP_ALARM	R	-	temp_actual > temp_threshold flag
5 to 0	TEMP_ACTUAL[5:0]	R	-	temp_actual (result of last measurement)

Table 98. Maximum temperature register
Default values are shown highlighted.

TEMP_MAX (address 0097h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
5 to 0	TEMP_MAX[5:0]	R	-	maximum temp_actual found since last ts_rst_max

Table 99. Minimum temperature register
Default values are shown highlighted.

TEMP_MIN (address 0098h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
5 to 0	TEMP_MIN[5:0]	R	-	minimum temp_actual found since last ts_rst_max

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Table 100. DSP sample control register
Default values are shown highlighted.

DSP_SMPL_CTRL (address 0099h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
4	DSP_READ_SEL	R/W	**0**	**reserved**
			1	store sample from DSP to buffer DSP_READ[31:0] ← DSP_SMPL[31:0]
3	DSP_STROBE	R/W	**0**	**no action**
			1	update DSP sample
2 to 0	DSP_SMPL_SEL[2:0]	R/W	**000**	**DSP_SMPL ← Q_0 and I_0**
			001	DSP_SMPL ← Q_1 and I_1
			010	DSP_SMPL ← Q_2 and I_2
			011	DSP_SMPL ← Q_3 and I_3
			others	reserved

Table 101. DSP read LSB/MSB registers
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
009Ah	DSP_READ_LSB	7 to 0	DSP_READ[7:0]	R	-	least significant 8 bits for DSP_READ
009Bh	DSP_READ_LSIB	7 to 0	DSP_READ[15:8]	R	-	least significant intermediate 8 bits for DSP_READ
009Ch	DSP_READ_MSIB	7 to 0	DSP_READ[23:16]	R	-	most significant intermediate 8 bits for DSP_READ
009Dh	DSP_READ_MSB	7 to 0	DSP_READ[31:24]	R	-	most significant 8 bits for DSP_READ

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11.12.6 Multiple Device Synchronization and Interrupt block

This block of registers specifies the configuration of the SYSREF signals (East and West) and how they are used for the Multiple Devices Synchronization (MDS) feature. It also specifies the interrupts.

11.12.6.1 Multiple Device Synchronization and Interrupt block register allocation map

Table 102 shows an overview of all the Multiple Device Synchronization and interrupt registers.

Table 102. Multiple Device Synchronization and Interrupt block register allocation map

Addr.	Register name	R/W	Bit definition								Default
Hex			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
00A0h	MDS_MAIN	R/W	MDS_EQ_CHECK[1:0]		MDS_MAN	MDS_SREF_DIS	MDS_EAST_WEST	MDS_MOD[1:0]		MDS_EN	E0h
00A2h	MDS_IO_CTRL	R/W	-	-	PON_SYSREF_E	PON_SYSREF_W	-	SEL_RT_SYSREF_E	-	SEL_RT_SYSREF_W	30h
00A3h	MDS_MISC_CTRL_0	RW	RESERVED	MDS_NCO	RESERVED[5:0]						10h
00A4h	MDS_MAN_ADJUST_DLY	R/W	MDS_MAN_ADJ_DLY[7:0]								80h
00A6h	MDS_MISC_CTRL_1	R/W	RESERVED[2:0]			MDS_RELOCK	MDS_LOCK_DLY[3:0]				0Fh
00A7h	MDS_OFFSET_DLY	RW	MDS_OFFSET_DLY[7:0]								00h
00A8h	MDS_WIN_LOW	R/W	MDS_WIN_PERIOD_A[7:0]								0Fh
00A9h	MDS_WIN_HIGH	R/W	MDS_WIN_PERIOD_B[7:0]								07h
00AAh	LMFC_PERIOD	R/W	LMFC_PERIOD[7:0]								10h
00ABh	LMFC_PRST	R/W	LMFC_PRESET[7:0]								04h
00ACh	MDS_CNT_PRESET	R/W	MDS_CNT_PRESET[7:0]								02h
00B5h	MDS_ADJ_DLY	R	MDS_ADJ_DLY[7:0]								uuh
00B6h	MDS_STATUS_0	R	RPT_FLAG_ERR	-	MCP_CALC_ERR	ADD_ERR	EARLY_ERR	LATE_ERR	-	MDS_ACTIVE	uuh
00B7h	MDS_STATUS_1	R	I_BUSY	I_STATE_ERR	RESERVED[1:0]		I_STATE[3:0]				uuh
00B8h	MDS_STATUS_2	R	MDS_LOCK	-	-	-	-	-	-		uuh

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Table 102. Multiple Device Synchronization and Interrupt block register allocation map *…continued*

Addr.	Register name	R/W	Bit definition								Default
Hex			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
00BAh	MDS_ STATUS_4	R	NOT USED[3:0]				LOCK_CNT[3:0]				uuh
00BBh	MDS_ STATUS_5	R	DELAY_CNT[7:0]								uuh
00BCh	MDS_ STATUS_6	R	I_ENA_SAMPLE[7:0]								uuh
00BDh	MDS_ STATUS_7	R	-	-	-	-	-	-	EN_PHASE[1:0]		uuh

[1] u = undefined at power-up or after reset.

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11.12.6.2 Multiple Device Synchronization and interrupt block bit definition detailed description

The tables in this section contain detailed descriptions of the Multiple Device Synchronization and interrupt registers.

Table 103. MDS main register
Default values are shown highlighted.

MDS_MAIN (address 00A0h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7 to 6	MDS_EQ_CHCK[1:0]	R/W		MDS equalizer check: lock mode
			00	lock when EARLY and LATE conditions are met (more accurate but more sensitive to jitter)
			01	lock when LATE condition is met
			10	lock when EARLY condition is met
			11	**lock when (START_EARLY and LATE) or (START_LATE and EARLY) conditions are met (less accurate but more stable)**
5	MDS_MAN	R/W		control adjustment delays
			0	auto-control adjustment delays
			1	**manual control adjustment delays**
4	MDS_SREF_DIS	R/W		sref generation
			0	**enabled**
			1	disabled
3	MDS_EAST_WEST	R/W		MDS input/output (see Section 11.7)
			0	**SYSREF_west used as MDS input**
			1	SYSREF_east used as MDS input
2 to 1	MDS_MOD[1:0]	R/W		MDS mode (see Section 11.7)
			00	**alternate JESD204B mode**
			01	not used
			10	JESD204B subclass I compatible mode
			11	not used
0	MDS_EN	R/W		MDS function control
			0	**disabled**
			1	enabled (see Section 11.7)

Table 104. MDS IO control register
Default values are shown highlighted.

MDS_IO_CTRL (address 00A2h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
5	PON_SYSREF_E	R/W	0	SYSREF_E buffer disabled
			1	**SYSREF_E buffer enabled**
4	PON_SYSREF_W	R/W	0	SYSREF_W buffer disabled
			1	**SYSREF_W buffer enabled**
3	NOT USED			

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Table 104. MDS IO control register *…continued*
Default values are shown highlighted.

MDS_IO_CTRL (address 00A2h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
2	SEL_RT_SYSREF_E	R/W		SYSREF_east internal resistor termination activation (see Section 11.7)
			0	**inactive**
			1	active
1	NOT USED			
0	SEL_RT_SYSREF_W	R/W		SYSREF_west internal resistor termination activation (see Section 11.7)
			0	**inactive**
			1	active

Table 105. MDS miscellaneous control register
Default values are shown highlighted.

MDS_MISC_CTRL_0 (address 00A3h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7	RESERVED	R/W	0	reserved to 0
6	MDS_NCO	R/W		
			0	**no action**
			1	NCO synchronization enabled
5 to 0	RESERVED[5:0]	R/W	**10000**	**reserved**

Table 106. MDS manual adjustment delay register
Default values are shown highlighted.

MDS_MAN_ADJ_DLY (address 00A4h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7 to 0	MDS_MAN_ADJ_DLY[7:0]	R/W		adjustment delay value
			0	if MDS_MAN = 0 then initial value adjustment delay
			1	if MDS_MAN = 1 then controls adjustment delay

Table 107. MDS miscellaneous control register
Default values are shown highlighted.

MDS_MISC_CTRL_1 (address 00A6h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7 to 5	**RESERVED**	**R/W**	**0**	**reserved to 0**
4	MDS_RELOCK	R/W		relock mode
			0	**no action**
			1	relock when lockout occurs
3 to 0	MDS_LOCK_DLY[3:0]	R/W	-	number of succeeding 'equal-check' detections until lock

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Table 108. MDS offset delay register
Default values are shown highlighted.

MDS_OFFSET_DLY (address 00A7h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7 to 0	MDS_OFFSET_DLY[7:0]	R/W	-	delay offset for dataflow in DAC clock periods (two's complement [−128 to 127])

Table 109. MDS window registers
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
00A8h	MDS_WIN_LOW	7 to 0	MDS_WIN_PERIOD_A[7:0]	R/W	-	determines MDS window LOW time
00A9h	MDS_WIN_HIGH	7 to 0	MDS_WIN_PERIOD_B[7:0]	R/W	-	determines MDS window HIGH time

Table 110. LMFC period register
Default values are shown highlighted.

LMFC_PERIOD (address 00AAh)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7 to 0	LMFC_PERIOD[7:0]	R/W	-	determines the LMFC period

Table 111. LMFC preset register
Default values are shown highlighted.

LMFC_PRST (address 00ABh)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7 to 0	LMFC_PRESET[7:0]	R/W	-	delays the LMFC period as related to the internal sref signal

Table 112. MDS adjustment delay register
Default values are shown highlighted.

MDS_ADJ_DLY (address 00B5h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7 to 0	MDS_ADJ_DLY[7:0]	R	-	actual value adjustment delay (in DAC clock period)

Table 113. MDS status registers
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
00B6h	MDS_STATUS_0	0	MDS_ACTIVE	R		evaluation logic active
					0	false
					1	true
00B7h	MDS_STATUS_1	7	I_BUSY	R		indicates that the MDS state machine is busy
		6	I_STATE_ERR	R		internal state error
					0	OK
					1	error
		5 to 4	RESERVED	R		reserved
		3 to 0	I_STATE[3:0]	R		internal state of state machine

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Table 113. MDS status registers *…continued*
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
00B8h	MDS_STATUS_2	7	MDS_LOCK	R		SYSREF has been found
					0	false
					1	true
00BAh	MDS_STATUS_4	7 to 4	NOT_USED[3:0]	R		
		3 to 0	LOCK_CNT[3:0]	R		
00BBh	MDS_STATUS_5	7 to 0	DELAY_CNT[7:0]	R		
00BCh	MDS_STATUS_6	7 to 0	I_ENA_SAMPLE[7:0]	R		
00BDh	MDS_STATUS_7	1 to 0	EN_PHASE[1:0]	R		

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11.12.7 RX Digital Lane Processing (DLP) block

This block of registers specifies the configuration of the digital lane processing.

11.12.7.1 RX digital lane processing block register allocation map

Table 114 shows an overview of all the RX digital lane processing registers.

Table 114. RX digital lane processing block register allocation map

Addr.	Register name	R/W	Bit definition								Default
Hex			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
00C7h	ILA_CTRL_1	R/W	-	SEL_ILA[1:0]		SEL_LOCK[2:0]			ILA_SYNC	DATA_DESCR_EN	63h
00C8h	FORCE_ALIGN	R/W	FORCE_FIRST_SAMPLE_LOW	USE_Q	NOT_USED[1:0]		SUBCLASS0	FRAME_ALIGN_EN	DYN_REALIGN_EN	RESERVED	86h
00CCh	SYNC_OUT_MODE	R/W	SEL_REINIT[2:0]			-	SYNC_INIT_LVL	SEL_SYNC[2:0]			00h
00CDh	P_LN_POL	R/W	-	-	-	SYNC_POL	POL_P_LN3	POL_P_LN2	POL_P_LN1	POL_P_LN0	00h
00CEh	P_LN_SEL	R/W	SEL_L_LN3[1:0]		SEL_L_LN2[1:0]		SEL_L_LN1[1:0]		SEL_L_LN0[1:0]		E4h
00D1h	INIT_DESCR_P_LN0_MSB	R/W	INIT_DESCR_P_LN0[15:8]								00h
00D2h	INIT_DESCR_P_LN0_LSB	R/W	-	INIT_DESCR_P_LN0[7:1]							00h
00D3h	INIT_DESCR_P_LN1_MSB	R/W	INIT_DESCR_P_LN1[15:8]								00h
00D4h	INIT_DESCR_P_LN1_LSB	R/W	-	INIT_DESCR_P_LN1[7:1]							00h
00D5h	INIT_DESCR_P_LN2_MSB	R/W	INIT_DESCR_P_LN2[15:8]								00h
00D6h	INIT_DESCR_P_LN2_LSB	R/W	-	INIT_DESCR_P_LN2[7:1]							00h
00D7h	INIT_DESCR_P_LN3_MSB	R/W	INIT_DESCR_P_LN3[15:8]								00h
00D8h	INIT_DESCR_P_LN3_LSB	R/W	-	INIT_DESCR_P_LN3[7:1]							00h
00D9h	INIT_ILA_BUFF_PNTR_L_LN_1_0	R/W	INIT_ILA_BUFF_PNTR_L_LN1[3:0]				INIT_ILA_BUFF_PNTR_L_LN0[3:0]				88h
00DAh	INIT_ILA_BUFF_PNTR_L_LN_3_2	R/W	INIT_ILA_BUFF_PNTR_L_LN3[3:0]				INIT_ILA_BUF_PNTR_L_LN2[3:0]				88h

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Table 114. RX digital lane processing block register allocation map *…continued*

Addr.	Register name	R/W	Bit definition								Default
Hex			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
00DBh	ERR_ HNDLNG	R/W	DISP_ERR_ P_LN3_EN	DISP_ERR_ P_LN2_EN	DISP_ERR_ P_LN1_EN	DISP_ERR_ P_LN0_EN	CONCEAL_ MODE	-	IGN_ERR[1:0]		F8h
00DCh	REINIT_CTRL	R/W	REINIT_ ILA_L_LN3	REINIT_ILA_ L_LN2	REINIT_ILA_ L_LN1	REINIT_ILA_ L_LN0	RESYNC_ OLINK_ P_LN3	RESYNC_ OLINK_ P_LN2	RESYNC_ OLINK_ P_LN1	RESYNC_ OLINK_ P_LN0	FFh
00DDh	MISC_CTRL	R/W	DLP_ STROBE	-	-	-	-	-	-	-	00h
00DEh	LMF_CTRL	R/W	L[2:0]			M[1:0]		F[2:0]			92h

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11.12.7.2 RX digital lane processing block bit definition detailed description

The tables in this section contain detailed descriptions of the RX digital lane processing registers.

Table 115. Initial-lane alignment control register

ILA_CTRL_1 (address 00C7h)				
Bit	**Symbol**	**Access**	**Value**	**Description (see Section 11.8.5.8)**
6 to 5	SEL_ILA	R/W	**11**	**reserved to 11 (alignment is done based on the 4-th /A/ character of the ILA)**
4 to 2	SEL_LOCK[2:0]	R/W		initial-lane alignment start mode
			000	**initial-lane alignment can only start if all (4 or 2) lanes are locked**
			001	initial-lane alignment can start if one of the (4 or 2) lanes are locked
			010	initial-lane alignment can start if lane 0 is locked
			011	initial-lane alignment can start if lane 1 is locked
			100	initial-lane alignment can start if lane 2 is locked
			101	initial-lane alignment can start if lane 3 is locked
1	ILA_SYNC	R/W		initial-lane alignment enable
			0	initial-lane alignment synchronization disabled
			1	**initial-lane alignment synchronization enabled**
0	DATA_DESCR_EN	R/W		data descrambling (see Section 11.8.5.2)
			0	disabled
			1	**enabled**

Table 116. Force alignment register

FORCE_ALIGN (address 00C8h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7	FORCE_FIRST_SAMPLE_LOW	R/W	0	no action
			1	**first sample will not be used (to avoid scrambler initialization uncertainty)**
6	USE_Q	R/W	**0**	**ignore /Q/ symbol for Lane Config extraction**
			1	use /Q/ symbol for Lane Config extraction
5:4	NOT_USED[1:0]			
3	SUBCLASS0	R/W	**0**	**for Subclass 1 and 2: number of multiframes in the ILA is equal to 4**
			1	Subclass 0: number of multiframes in the ILA is equal or greater than 4
2	FRAME_ALIGN_EN	R/W	0	frame alignment mode disabled
			1	**frame alignment mode enabled**
1	DYN_REALIGN_EN	R/W		dynamic realignment mode
			0	no dynamic realignment
			1	**dynamic realignment (and monitoring) enabled**
0	RESERVED	R/W	**0**	**reserved**

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Table 117. Synchronization output modes register

Default settings are shown highlighted.

SYNC_OUT_MOD (address 00CCh)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7 to 5	SEL_REINIT	R/W		Reinitialization is done when:
			000	**one of the enabled lane reset is active**
			001	all of the enabled lane reset are active
			010	lane 0 reset is active
			011	lane 1 reset is active
			100	lane 2 reset is active
			101	lane 3 reset is active
			110	Reinitialization is forced to 1
			111	Reinitialization is forced to 0
3	SYNC_INIT_LVL	R/W		synchronization initialization level (see Section 11.8.5.5)
			0	**synchronization starts with '0'**
			1	synchronization starts with '1'
2 to 0	SEL_SYNC[2:0]	R/W		synchronization mode (see Section 11.8.5.5)
			000	**sync_request active when state machine of one of the lanes is in CS_INIT mode**
			001	sync_request active when state machine of all lanes is in CS_INIT mode
			010	sync_request active when state machine of lane 0 is in CS_INIT mode
			011	sync_request active when state machine of lane 1 is in CS_INIT mode
			100	sync_request active when state machine of lane 2 is in CS_INIT mode
			101	sync_request active when state machine of lane 3 is in CS_INIT mode
			110	sync_request fixed to 1
			111	sync_request fixed to 0

Table 118. Physical lane polarity register

P_LN_POL (address 00CDh)				
Bit	**Symbol**	**Access**	**Value**	**Description (see Section 11.8.5.1)**
4	SYNC_POL	R/W		synchronization polarity (see Section 11.8.5.5)
			0	**sync_out is active when LOW**
			1	sync_out is active when HIGH
3	POL_P_LN3	R/W		physical lane 3 data polarity
			0	**no action**
			1	invert all data bits of lane 3
2	POL_P_LN2	R/W		physical lane 2 data polarity
			0	**no action**
			1	invert all data bits of lane 2

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Table 118. Physical lane polarity register *…continued*

P_LN_POL (address 00CDh)				
Bit	**Symbol**	**Access**	**Value**	**Description (see Section 11.8.5.1)**
1	POL_P_LN1	R/W		physical lane 1 data polarity
			0	**no action**
			1	invert all data bits of lane 1]
0	POL_P_LN0	R/W		physical lane 0 data polarity
			0	**no action**
			1	invert all data bits of lane 0

Table 119. Physical lane selection register
Default settings are shown highlighted.

P_LN_SEL register (address 00CEh)				
Bit	**Symbol**	**Access**	**Value**	**Description (see Section 11.8.4 and Section 11.8.5.3)**
7 to 6	SEL_L_LN3[1:0]	R/W		lane 3 data mapping
			00	logical lane 3 is mapped to physical lane 0
			01	logical lane 3 is mapped to physical lane 1
			10	logical lane 3 is mapped to physical lane 2
			11	**logical lane 3 is mapped to physical lane 3**
5 to 4	SEL_L_LN2[1:0]	R/W		lane 2 data mapping
			00	logical lane 2 is mapped to physical lane 0
			01	logical lane 2 is mapped to physical lane 1
			10	**logical lane 2 is mapped to physical lane 2**
			11	logical lane 2 is mapped to physical lane 3
3 to 2	SEL_L_LN1[1:0]	R/W		lane 1 data mapping
			00	logical lane 1 is mapped to physical lane 0
			01	**logical lane 1 is mapped to physical lane 1**
			10	logical lane 1 is mapped to physical lane 2
			11	logical lane 1 is mapped to physical lane 3
1 to 0	SEL_L_LN0[1:0]	R/W		lane 0 data mapping
			00	**logical lane 0 is mapped to physical lane 0**
			01	logical lane 0 is mapped to physical lane 1
			10	logical lane 0 is mapped to physical lane 2
			11	logical lane 0 is mapped to physical lane 3

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Table 120. Descrambler initialization values registers
Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description (see Section 11.8.5.2)
00D1h	INIT_DESCR_P_LN0_MSB	7 to 0	INIT_DESCR_P_LN0[15:8]	R/W	00h	initialization value for physical lane 0 descrambler 8 most significant bits
00D2h	INIT_DESCR_P_LN0_LSB	6 to 0	INIT_DESCR_P_LN0[7:1]	R/W	00h	initialization value for physical lane 0 descrambler 7 least significant bits
00D3h	INIT_DESCR_P_LN1_MSB	7 to 0	INIT_DESCR_P_LN1[15:8]	R/W	00h	initialization value for physical lane 1 descrambler 8 most significant bits
00D4h	INIT_DESCR_P_LN1_LSB	6 to 0	INIT_DESCR_P_LN1[7;1]	R/W	00h	initialization value for physical lane 1 descrambler 7 least significant bits
00D5h	INIT_DESCR_P_LN2_MSB	7 to 0	INIT_DESCR_P_LN2[15:8]	R/W	00h	initialization value for physical lane 2 descrambler 8 most significant bits
00D6h	INIT_DESCR_P_LN2_LSB	6 to 0	INIT_DESCR_P_LN2[7:1]	R/W	00h	initialization value for physical lane 2 descrambler 7 least significant bits
00D7h	INIT_DESCR_P_LN3_MSB	7 to 0	INIT_DESCR_P_LN3[15:8]	R/W	00h	initialization value for physical lane 3 descrambler 8 most significant bits
00D8h	INIT_DESCR_P_LN3_LSB	6 to 0	INIT_DESCR_P_LN3[7:1]	R/W	00h	initialization value for physical lane 3 descrambler 7 least significant bits
00D9h	INIT_ILA_BUFF_PNTR_L_LN01	7 to 4	INIT_ILA_BUFPTR_P_LN1[3:0]	R/W	88h	initialization value for logical lane 1 ILA buffer pointer (see Section 11.8.5.8)
		3 to 0	INIT_ILA_BUFF_PNTR_P_LN0[3:0]	R/W	88h	initialization value for logical lane 0 ILA buffer pointer (see Section 11.8.5.8)
00DAh	INIT_ILA_BUFF_PNTR_L_LN23	7 to 4	INIT_ILA_BUFF_PNTR_L_LN3[3:0]	R/W	88h	initialization value for logical lane 3 ILA buffer pointer (see Section 11.8.5.8)
		3 to 0	INIT_ILA_BUFF_PNTR_L_LN2[3:0]	R/W	88h	initialization value for logical lane 2 ILA buffer pointer (see Section 11.8.5.8)

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Table 121. Error handling register
Default settings are shown highlighted.

ERR_HNDLNG (address 00DBh)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7	DISP_ERR_P_LN3_EN	R/W	0	no action
			1	**not-in-table errors passed to frame assembler**
6	DISP_ERR_P_LN2_EN	R/W	0	no action
			1	**not-in-table errors passed to frame assembler**
5	DISP_ERR_P_LN1_EN	R/W	0	no action
			1	**not-in-table errors passed to frame assembler**
4	DISP_ERR_P_LN0_EN	R/W	0	no action
			1	**not-in-table errors passed to frame assembler**
3	CONCEAL_MODE	R/W	0	conceal error by repeating one sample
			1	conceal error by repeating two samples
1 to 0	IGN_ERR[1:0]	R/W		general error mode (see Section 11.8.5.13)
			00	**NIT and DISP error are used**
			01	ignore NIT errors
			10	ignore DISP error
			11	ignore NIT and DISP errors

Table 122. Reinitialization control register
Default settings are shown highlighted.

REINIT_CTRL (address 00DCh)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7	REINIT_ILA_L_LN3	R/W		logical lane 3, ila buffer out-of-range check (see Section 11.8.5.8)
			0	no action
			1	**lane 3 ila buffer out-of-range_error activates reinitialization**
6	REINIT_ILA_L_LN2	R/W		logical lane 2, ila buffer out-of-range check (see Section 11.8.5.8)
			0	no action
			1	**lane 2 ila buffer out-of-range_error activates reinitialization**
5	REINIT_ILA_L_LN1	R/W		logical lane 1, ila buffer out-of-range check (see Section 11.8.5.8)
			0	no action
			1	**lane 1 ila buffer out-of-range_error activates reinitialization**
4	REINIT_ILA_L_LN0	R/W		logical lane 0, ila buffer out-of-range check (see Section 11.8.5.8)
			0	no action
			1	**lane 0 ila buffer out-of-range_error activates reinitialization**

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Table 122. Reinitialization control register *…continued*
Default settings are shown highlighted.

REINIT_CTRL (address 00DCh)				
Bit	**Symbol**	**Access**	**Value**	**Description**
3	RESYNC_OLINK_P_LN3	R/W		physical lane 3, resynchronization over link (see Section 11.8.5.12)
			0	no action
			1	**lane 3 controller checks for K28.5 /K/ symbols**
2	RESYNC_OLINK_P_LN2	R/W		physical lane 2, resynchronization over link (see Section 11.8.5.12)
			0	no action
			1	**lane 2 controller checks for K28.5 /K/ symbols**
1	RESYNC_OLINK_P_LN1	R/W		physical lane 1, resynchronization over link (see Section 11.8.5.12)
			0	no action
			1	**lane 1 controller checks for K28.5 /K/ symbols**
0	RESYNC_OLINK_P_LN0	R/W		physical lane 0, resynchronization over link (see Section 11.8.5.12)
			0	no action
			1	**lane 0 controller checks for K28.5 /K/ symbols**

Table 123. Miscellaneous control register

MISC_CTRL (address 00DDh)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7	DLP-STROBE	R/W		captures 16-bit data inside the DLP for each lane (see Section 11.8.6.5)
			0	**no action**
			1	update DLP samples
1 to 0	RESERVED[1:0]	R/W	**00**	**reserved to 00**

Table 124. LMF control register

LMF_CTRL register (address 00DEh)				
Bit	**Symbol**	**Access**	**Value**	**Description (see Section 11.8.5.11)**
7 to 5	L[2:0]	R/W	-	number of lanes [1, 2, 4]
4 to 3	M[1:0]	R/W	-	number of converters [1]
2 to 0	F[2:0]	R/W	-	number of octets/frame [1, 2, 4]

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11.12.8 RX digital lane processing monitoring block

This block of registers enables the monitoring of the digital lane processing, ensuring the data is decoded correctly. The validity of the link can also be tested by using simple Bit Error Rate testing and be monitored through various available flags and counters registers.

11.12.8.1 RX digital lane processing monitoring block register allocation map description

Table 125 shows an overview of all the RX digital lane processing monitoring registers.

Table 125. RX digital lane processing monitoring block register allocation map

Addr.	Register name	R/W	Bit definition								Default
Hex			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
00E0h	ILA_MON_L_LN_1_0	R	ILA_MON_L_LN1[3:0]				ILA_MON_L_LN0[3:0				uuh
00E1h	ILA_MON_L_LN_3_2	R	ILA_MON_L_LN3[3:0]				ILA_MON_L_LN2[3:0]				uuh
00E2h	ILA_BUFF_ERR	R	-	-	-	-	ILA_BUFF_ERR_L_LN3	ILA_BUFF_ERR_L_LN2	ILA_BUFF_ERR_L_LN1	ILA_BUFF_ERR_L_LN0	uuh
00E4h	DEC_FLAGS	R	DEC_NIT_ERR_P_LN3	DEC_NIT_ERR_P_LN2	DEC_NIT_ERR_P_LN1	DEC_NIT_ERR_P_LN0	DEC_DISP_ERR_P_LN3	DEC_DISP_ERR_P_LN2	DEC_DISP_ERR_P_LN1	DEC_DISP_ERR_P_LN0	uuh
00E5h	KOUT_FLAG	R	-	-	-	-	DEC_KOUT_P_LN3	DEC_KOUT_P_LN2	DEC_KOUT_P_LN1	DEC_KOUT_P_LN0	uuh
00E6h	K28_P_LN0_FLAG	R	LN0_ILA_MFR_ERR	LN0_ILA_GT4_ERR	LN0_ILA_LT4_ERR	K28_7_P_LN0	K28_5_P_LN0	K28_4_P_LN0	K28_3_P_LN0	K28_0_P_LN0	uuh
00E7h	K28_P_LN1_FLAG	R	LN1_ILA_MFR_ERR	LN1_ILA_GT4_ERR	LN1_ILA_LT4_ERR	K28_7_P_LN1	K28_5_P_LN1	K28_4_P_LN1	K28_3_P_LN1	K28_0_P_LN1	uuh
00E8h	K28_P_LN2_FLAG	R	LN2_ILA_MFR_ERR	LN2_ILA_GT4_ERR	LN2_ILA_LT4_ERR	K28_7_P_LN2	K28_5_P_LN2	K28_4_P_LN2	K28_3_P_LN2	K28_0_P_LN2	uuh
00E9h	K28_P_LN3_FLAG	R	LN3_ILA_MFR_ERR	LN3_ILA_GT4_ERR	LN3_ILA_LT4_ERR	K28_7_P_LN3	K28_5_P_LN3	K28_4_P_LN3	K28_3_P_LN3	K28_0_P_LN3	uuh
00EAh	KOUT_UNEXP_FLAG	R	-	-	-	-	DEC_KOUT_UNEXP_P_LN3	DEC_KOUT_UNEXP_P_LN2	DEC_KOUT_UNEXP_P_LN1	DEC_KOUT_UNEXP_P_LN0	uuh
00EBh	LOCK_CNT_MON_LN01	R	LOCK_CNT_MON_P_LN1[3:0]				LOCK_CNT_MON_P_LN0[3:0]				uuh
00ECh	LOCK_CNT_MON_LN23	R	LOCK_CNT_MON_P_LN3[3:0]				LOCK_CNT_MON_P_LN2[3:0]				uuh
00EDh	CS_STATE_LNX	R	CS_STATE_P_LN3[1:0]		CS_STATE_P_LN2[1:0]		CS_STATE_P_LN1[1:0]		CS_STATE_P_LN0[1:0]		uuh
00EEh	MISC_FLAG_CTRL	R/W	RST_BUFF_ERR_FLAGS	AUTO_RST_FLAG_CNTS	HOLD_FLAG_CNT_EN	RESERVED[4:0]					00h

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Table 125. RX digital lane processing monitoring block register allocation map *…continued*

Addr.	Register name	R/W	Bit definition								Default
Hex			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
00EFh	INTR_MISC_EN	R/W	INTR_BUFF_EN_CS_INIT_P_LN3	INTR_EN_CS_INIT_P_LN2	INTR_EN_CS_INIT_P_LN1	INTR_EN_CS_INIT_P_LN0	INTR_EN_BUFF_ERR_L_LN3	INTR_EN_BUFF_ERR_L_LN2	INTR_EN_BUFF_ERR_L_LN1	INTR_EN_BUFF_ERR_L_LN0	00h
00F0h	FLAG_CNT__LN0_LSB	R	FLAG_CNT_LN0[7:0]								uuh
00F1h	FLAG_CNT_LN0_MSB	R	FLAG_CNT_LN0[15:8]								uuh
00F2h	FLAG_CNT_LN1_LSB	R	FLAG_CNT_LN1[7:0]								uuh
00F3h	FLAG_CNT_LN1_MSB	R	FLAG_CNT_LN1[15:8]								uuh
00F4h	FLAG_CNT_LN2_LSB	R	FLAG_CNT_LN2[7:0]								uuh
00F5h	FLAG_CNT_LN2_MSB	R	FLAG_CNT_LN2[15:8]								uuh
00F6h	FLAG_CNT_LN3_LSB	R	FLAG_CNT_LN3[7:0]								uuh
00F7h	FLAG_CNT_LN3_MSB	R	FLAG_CNT_LN3[15:8]								uuh
00F8h	ERR_MIX_CTL	R/W	EM	EM_KUX	EM_DISP	EM_NIT	ERPT_ILA_ENA	ERPT_KUX_ENA	ERPT_DIS_ENA	ERPT_NIT_ENA	FFh
00F9h	INTR_EN_0	R/W	NOT USED[3:0]				INTR_STLTP_ERR	INTR_BER	INTR_ILA_RCV	INTR_NO_F20_ACT	00h
00FAh	INTR_EN_1	R/W	INTR_EN_NIT	INTR_EN_DISP	INTR_EN_KOUT	INTR_EN_KOUT_UNEXP	INTR_EN_K28_7	INTR_EN_K28_5	INTR_EN_K28_3	INTR_EN_MISC	00h
00FBh	CTRL_FLAG_CNT_LN10	R/W	RST_CTRL_FLAG_CNT_LN1	SEL_CTRL_FLAG_CNT_LN1[2:0]			RST_CTRL_FLAG_CNT_LN0	SEL_CTRL_FLAG_CNT_LN0[2:0]			55h
00FCh	CTRL_FLAG_CNT_LN32	R/W	RST_CTRL_FLAG_CNT_LN3	SEL_CTRL_FLAG_CNT_LN3[2:0]			RST_CTRL_FLAG_CNT_LN2	SEL_CTRL_FLAG_CNT_LN2[2:0]			55h
00FDh	RST_MON_FLAGS	R/W	RST_NIT_ERR-FLAGS	RST_DISP_ERR_FLAGS	RST_KOUT_FLAGS	RST_KOUT_UNEXP_FLAGS	RST_K28_LN3_FLAGS	RST_K28_LN2_FLAGS	RST_K28_LN1_FLAGS	RST_K28_LN0_FLAGS	00h
00FEh	DBG_CTRL	R/W	SER_MOD	INTR_CLR	INTR_MOD[2:0]			RESERVED[2:0]			00h

[1] u = undefined at power-up or after reset.

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11.12.8.2 RX digital lane processing monitoring block bit definition detailed description

The tables in this section contain detailed descriptions of the RX digital lane processing monitoring registers.

Table 126. Initial-lane alignment monitor registers
Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description (see Section 11.8.5.8)
00E0h	ILA_MON_L_LN_1_0	7 to 4	ILA_MON_L_LN1[3:0]	R	-	ila_buf_l_ln1 pointer
		3 to 0	ILA_MON_L_LN0[3:0]		-	ila_buf_l_ln0 pointer
00E1h	ILA_MON_L_LN_3_2	7 to 4	ILA_MON_L_LN3[3:0]	R	-	ila_buf_l_ln3 pointer
		3 to 0	ILA_MON_L_LN2[3:0]		-	ila_buf_l_ln2 pointer

Table 127. Initial-lane alignment buffer error register
Default settings are shown highlighted.

ILA_BUFF_ERR (address 00E2h)				
Bit	**Symbol**	**Access**	**Value**	**Description (see Section 11.8.5.8)**
3	ILA_BUFF_ERR_L_LN3	R		logical lane 3 ila buffer error
			0	ila_buf_l_ln3 pointer is in range
			1	ila_buf_l_ln3 pointer is out of range
2	ILA_BUFF_ERR_L_LN2	R		logical lane 2 ila buffer error
			0	ila_buf_l_ln2 pointer is in range
			1	ila_buf_l_ln2 pointer is out of range
1	ILA_BUFF_ERR_L_LN1	R		logical lane 1 ila buffer error
			0	ila_buf_l_ln1 pointer is in range
			1	ila_buf_l_ln1 pointer is out of range
0	ILA_BUFF_ERR_L_LN0	R		logical lane 0 ila buffer error
			0	ila_buf_l_ln0 pointer is in range
			1	ila_buf_l_ln0 pointer is out of range

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Table 128. Decoder flags register

DEC_FLAGS (address 00E4h)				
Bit	**Symbol**	**Access**	**Value**	**Description (see Section 11.8.5.13**
7	DEC_NIT_ERR_P_LN3	R	-	decoder not-in-table error flag physical lane 3
6	DEC_NIT_ERR_P_LN2	R	-	decoder not-in-table error flag physical lane 2
5	DEC_NIT_ERR_P_LN1	R	-	decoder not-in-table error flag physical lane 1
4	DEC_NIT_ERR_P_LN0	R	-	decoder not-in-table error flag physical lane 0
3	DEC_DISP_ERR_P_LN3	R	-	decoder disparity error flag physical lane 3
2	DEC_DISP_ERR_P_LN2	R	-	decoder disparity error flag physical lane 2
1	DEC_DISP_ERR_P_LN1	R	-	decoder disparity error flag physical lane 1
0	DEC_DISP_ERR_P_LN0	R	-	decoder disparity error flag physical lane 0

Table 129. Decoder /K/ symbols flag register

KOUT_FLAG (address 00E5h)				
Bit	**Symbol**	**Access**	**Value**	**Description (see Section 11.8.5.13)**
3	DEC_KOUT_P_LN3	R	-	decoder: /K/ symbols found in physical lane 3
2	DEC_KOUT_P_LN2	R	-	decoder: /K/ symbols found in physical lane 2
1	DEC_KOUT_P_LN1	R	-	decoder: /K/ symbols found in physical lane 1
0	DEC_KOUT_P_LN0	R	-	decoder: /K/ symbols found in physical lane 0

Table 130. K28 flag registers

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description (see Section 11.8.5.13)
00E6h	K28_P_LN0_P_FLAG	7	LN0_ILA_MFR_ERR	R	-	irregular length of multiframes during ILA sequence
		6	LN0_ILA_GT4_ERR		-	ILA sequence with more than 4 multiframes
		5	LN0_ILA_LT4_ERR		-	ILA sequence with less than 4 multiframes
		4	K28_7_P_LN0		-	K28_7 /F/ symbols found in physical lane 0
		3	K28_5_P_LN0		-	K28_5 /K/ symbols found in physical lane 0
		2	K28_4_P_LN0		-	K28_4 /Q/ symbols found in physical lane 0
		1	K28_3_P_LN0		-	K28_3 /A/ symbols found in physical lane 0
		0	K28_0_P_LN0		-	K28_0 /R/ symbols found in physical lane 0

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Table 130. K28 flag registers *…continued*
Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description (see Section 11.8.5.13)
00E7h	K28_P_LN1_P_FLAG	7	LN1_ILA_MFR_ERR	R	-	irregular length of multiframes during ILA sequence
		6	LN1_ILA_GT4_ERR		-	ILA sequence with more than 4 multiframes
		5	LN1_ILA_LT4_ERR		-	ILA sequence with less than 4 multiframes
		4	K28_7_P_LN1		-	K28_7 /F/ symbols found in physical lane 1
		3	K28_5_P_LN1		-	K28_5 /K/ symbols found in physical lane 1
		2	K28_4_P_LN1		-	K28_4 /Q/ symbols found in physical lane 1
		1	K28_3_P_LN1		-	K28_3 /A/ symbols found in physical lane 1
		0	K28_0_P_LN1		-	K28_0 /R/ symbols found in physical lane 1
00E8h	K28_P_LN2_P_FLAG	7	LN2_ILA_MFR_ERR	R	-	irregular length of multiframes during ILA sequence
		6	LN2_ILA_GT4_ERR		-	ILA sequence with more than 4 multiframes
		5	LN2_ILA_LT4_ERR		-	ILA sequence with less than 4 multiframes
		4	K28_7_P_LN2		-	K28_7 /F/ symbols found in physical lane 2
		3	K28_5_P_LN2		-	K28_5 /K/ symbols found in physical lane 2
		2	K28_4_P_LN2		-	K28_4 /Q/ symbols found in physical lane 2
		1	K28_3_P_LN2		-	K28_3 /A/ symbols found in physical lane 2
		0	K28_0_P_LN2		-	K28_0 /R/ symbols found in physical lane 2

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Table 130. K28 flag registers *...continued*
Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description (see Section 11.8.5.13)
00E9h	K28_P_LN3_P_FLAG	7	LN3_ILA_MFR_ERR	R	-	irregular length of multiframes during ILA sequence
		6	LN3_ILA_GT4_ERR		-	ILA sequence with more than 4 multiframes
		5	LN3_ILA_LT4_ERR		-	ILA sequence with less than 4 multiframes
		4	K28_7_P_LN3		-	K28_7 /F/ symbols found in physical lane 3
		3	K28_5_P_LN3		-	K28_5 /K/ symbols found in physical lane 3
		2	K28_4_P_LN3		-	K28_4 /Q/ symbols found in physical lane 3
		1	K28_3_P_LN3		-	K28_3 /A/ symbols found in physical lane 3
		0	K28_0_P_LN3		-	K28_0 /R/ symbols found in physical lane 3

Table 131. Decoder unexpected /K/ symbols flag register

KOUT_UNEXP_FLAG (address 00EAh)				
Bit	**Symbol**	**Access**	**Value**	**Description (see Section 11.8.5.13)**
3	DEC_KOUT_UNEXP_P_LN3	R	-	decoder: unexpected /K/ symbols found in physical lane 3
2	DEC_KOUT_UNEXP_P_LN2	R	-	decoder: unexpected /K/ symbols found in physical lane 2
1	DEC_KOUT_UNEXP_P_LN1	R	-	decoder: unexpected /K/ symbols found in physical lane 1
0	DEC_KOUT_UNEXP_P_LN0	R	-	decoder: unexpected /K/ symbols found in physical lane 0

Table 132. Lock counter monitor registers
Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description (see Section 11.8.6)
00EBh	LOCK_CNT_MON_P_LN01	7 to 4	LOCK_CNT_MON_P_LN1[3:0]	R	-	lock_state monitor synchronization word alignment physical lane 1
		3 to 0	LOCK_CNT_MON_P_LN0[3:0]		-	lock_state monitor synchronization word alignment physical lane 0
00ECh	LOCK_CNT_MON_P_LN23	7 to 4	LOCK_CNT_MON_P_LN3[3:0]	R	-	lock_state monitor synchronization word alignment physical lane 3
		3 to 0	LOCK_CNT_MON_P_LN2[3:0]		-	lock_state monitor synchronization word alignment physical lane 2

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Table 133. Lane code synchronization state register
Default settings are shown highlighted.

CS_STATE_LNX (address 00EDh)				
Bit	**Symbol**	**Access**	**Value**	**Description (see Section 11.8.5.4)**
7 to 6	CS_STATE_P_LN3[1:0]	R	-	monitor cs_state fsm physical lane 3
5 to 4	CS_STATE_P_LN2[1:0]	R	-	monitor cs_state fsm physical lane 2
3 to 2	CS_STATE_P_LN1[1:0]	R	-	monitor cs_state fsm physical lane 1
1 to 0	CS_STATE_P_LN0[1:0]	R	-	monitor cs_state fsm physical lane 0

Table 134. Reset buffer error flags register
Default settings are shown highlighted.

RST_BUF_ERR_FLAGS (address 00EEh)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7	RST_BUFF_ERR_FLAGS	R/W	0	reset ILA_BUF_ERR_LNx flags (see Section 11.8.5.8)
6	AUTO_RST_FLAG_CNTS	R/W	0	FLAGs counters are reset when DLP is reset (see Section 11.8.6.1)
5	HOLD_FLAG_CNT_EN	R/W	0	see Section 11.8.6.1

Table 135. Miscellaneous interrupt enable register
Default settings are shown highlighted.

INTR_MISC_EN (address 00EFh)				
Bit	**Symbol**	**Access**	**Value**	**Description (see Section 11.8.3)**
7	INTR_EN_CS_INIT_P_LN3	R/W	**0**	**no action**
			1	intr_misc in case cs_state_p_ln3 = cs_init
6	INTR_EN_CS_INIT_P_LN2	R/W	**0**	**no action**
			1	intr_misc in case cs_state_p_ln2 = cs_init
5	INTR_EN_CS_INIT_P_LN1	R/W	**0**	**no action**
			1	intr_misc in case cs_state_p_ln1 = cs_init
4	INTR_EN_CS_INIT_P_LN0	R/W	**0**	**no action**
			1	intr_misc in case cs_state_p_ln0 = cs_init
3	INTR_EN_BUFF_ERR_L_LN3	R/W	**0**	**no action**
			1	generate interrupt if ILA_BUF_ERR_L_LN3 = 1
2	INTR_EN_BUFF_ERR_L_LN2	R/W	**0**	**no action**
			1	generate interrupt if ILA_BUF_ERR_L_LN2 = 1
1	INTR_EN_BUFF_ERR_L_LN1	R/W	**0**	**no action**
			1	generate interrupt if ILA_BUF_ERR_L_LN1 = 1
0	INTR_EN_BUFF_ERR_L_LN0	R/W	**0**	**no action**
			1	generate interrupt if ILA_BUF_ERR_L_LN0 = 1

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Table 136. LSB/MSB of flag_counter lane registers
Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description (see Section 11.8.6.1)
00F0h	FLAG_CNT_LN0_LSB	7 to 0	FLAG_CNT_LN0[7:0]	R	-	8 least significant bits of flag counter lane 0
00F1h	FLAG_CNT_LN0_MSB	7 to 0	FLAG_CNT_LN0[15:8]	R	-	8 most significant bits of flag_counter lane 0
00F2h	FLAG_CNT_LN1_LSB	7 to 0	FLAG_CNT_LN1[7:0]	R	-	8 least significant bits of flag counter lane 1
00F3h	FLAG_CNT_LN1_MSB	7 to 0	FLAG_CNT_LN1[15:8]	R	-	8 most significant bits of flag_counter lane 1
00F4h	FLAG_CNT_LN2_LSB	7 to 0	FLAG_CNT_LN2[7:0]	R	-	8 least significant bits of flag counter lane 2
00F5h	FLAG_CNT_LN2_MSB	7 to 0	FLAG_CNT_LN2[15:8]	R	-	8 most significant bits of flag_counter lane 2
00F6h	FLAG_CNT_LN3_LSB	7 to 0	FLAG_CNT_LN3[7:0]	R	-	8 least significant bits of flag counter lane 3
00F7h	FLAG_CNT_LN3_MSB	7 to 0	FLAG_CNT_LN3[15:8]	R	-	8 most significant bits of flag_counter lane 3

Table 137. Miscellaneous interrupt enable register
Default settings are shown highlighted.

ERR_MIX_CTL (address 00F8h)				
Bit	**Symbol**	**Access**	**Value**	**Description (see Section 11.8.3)**
7	EM	R/W	0	SEL_CFC_LN is used for K28 monitoring
			1	**SEL_CFC_LN is used for ERR_MIX**
6	EM_KUX	R/W	0	no action
			1	**ERR_MIX_LN is using KOUT_UNEXPECTED monitoring**
5	EM_DISP	R/W	0	no action
			1	**ERR_MIX is using DISP error for monitoring**
4	EM_NIT	R/W	0	no action
			1	**ERR_MIX is using NIT err for monitoring**
3	ERPT_ILA_ENA	R/W	0	no action
			1	**ERR_RPT_FLAG impacted by ILA_BUF_ERR errors**
2	ERPT_KUX_ENA	R/W	0	no action
			1	**ERR_RPT_FLAG impacted by KOUT_UNEXPECTED errors**
1	ERPT_DIS_ENA	R/W	0	no action
			1	**ERR_RPT_FLAG impacted by DISP errors**
0	ERPT_NIT_ENA	R/W	0	no action
			1	**ERR_RPT_FLAG is impacted by NIT errors**

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Table 138. Miscellaneous interrupt enable register

Default settings are shown highlighted.

INTR_EN_0(address 00F9h)				
Bit	**Symbol**	**Access**	**Value**	**Description (see Section 11.8.3)**
3	INTR_STLTP_ERR	R/W	**0**	**no action**
			1	Interrupt i_ln<x> impacted by STLTP error
2	INTR_BER	R/W	**0**	**no action**
			1	Interrupt i_ln<x> impacted by BER_LN error
1	INTR_ILA_RCV	R/W	**0**	**no action**
			1	Interrupt i_ln<x> impacted by ILA_RCV
0	INTR_NO_F20_ACT	R/W	**0**	**no action**
			1	Interrupt i_ln<x> impacted by NO_F20_ACT flag

Table 139. Interrupt enable register

INTR_EN_1 (address 00FAh)				
Bit	**Symbol**	**Access**	**Value**	**Description (see Section 11.8.4)**
7	INTR_EN_NIT	R/W		not-in-table interrupt
			0	**no action**
			1	nit_error impacts global interrupt as per INTR_MODE configuration (bit 1E)
6	INTR_EN_DISP	R/W		disparity-error interrupt
			0	**no action**
			1	disparity-error in ln<x> affects i_ln<x>
5	INTR_EN_KOUT	R/W		K-character interrupt
			0	**no action**
			1	detection k-control character in ln<x> affects i_ln<x>
4	INTR_EN_KOUT_UNEXP	R/W		unexpected K-character interrupt
			0	**no action**
			1	detection unexpected K-character in ln<x> affects i_ln<x>
3	INTR_EN_K28_7	R/W		K28_7 interrupt
			0	**no action**
			1	detection K28_7 in ln<x> affects i_ln<x>
2	INTR_EN_K28_5	R/W		K28_5 interrupt
			0	**no action**
			1	detection K28_5 in ln<x> affects i_ln<x>
1	INTR_EN_K28_3	R/W		K28_3 interrupt
			0	**no action**
			1	detection K28_3 in ln<x> affects i_ln<x>
0	INTR_EN_MISC	R/W		miscellaneous interrupt intr_misc (see reg x0F)
			0	**no action**
			1	detection depends on intr_misc_ena (see Table 135)

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Table 140. Flag counter control registers
Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description (see Section 11.8.6.1)
00FBh	CTRL_FLAG_CNT_LN10	7	RST_CTRL_FLAG_CNT_LN1	R/W	0	reset FLAG_CNT_LN1
		6 to 4	SEL_CTRL_FLAG_CNT_LN1[2:0]		5h	select FLAG_CNT_LN1 source
		3	RST_CTRL_FLAG_CNT_LN0		0	reset FLAG_CNT_LN0
		2 to 0	SEL_CTRL_FLAG_CNT_LN0[2:0]		5h	select FLAG_CNT_LN0 source
00FCh	CTRL_FLAG_CNT_LN32	7	RST_CTRL_FLAG_CNT_LN3	R/W	0	reset FLAG_CNT_LN3
		6 to 4	SEL_CTRL_FLAG_CNT_LN3[2:0]		5h	select FLAG_CNT_LN3 source
		3	RST_CTRL_FLAG_CNT_LN2		0	reset FLAG_CNT_LN2
		2 to 0	SEL_CTRL_FLAG_CNT_LN2[2:0]		5h	select FLAG_CNT_LN2 source

Table 141. Reset flags monitor register

MON_FLAGS_RST (address 00FDh)				
Bit	**Symbol**	**Access**	**Value**	**Description (see Section 11.8.5.13)**
7	RST_NIT_ERR_FLAGS	R/W	0	reset not-in-table error monitor flags
6	RST_DISP_ERR_FLAGS	R/W	0	reset disparity monitor flags
5	RST_KOUT_FLAGS	R/W	0	reset /K/ symbols monitor flags
4	RST_KOUT_UNEXP_FLAGS	R/W	0	reset unexpected /K/ symbols monitor flags
3	RST_K28_LN3_FLAGS	R/W	0	reset K28_x monitor flags for lane 3
2	RST_K28_LN2_FLAGS	R/W	0	reset K28_x monitor flags for lane 2
1	RST_K28_LN1_FLAGS	R/W	0	reset K28_x monitor flags for lane 1
0	RST_K28_LN0_FLAGS	R/W	0	reset K28_x monitor flags for lane 0

Table 142. Sample error rate interrupts control register

SER_INTR_CTRL (address 00FEh)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7	SER_MOD	R/W		simple BER-measurement
			0	**no action**
			1	simple BER measurement enabled
6	INTR_RST	R/W		interrupts clear
			0	**no action**
			1	clear interrupts (to '1')

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Table 142. Sample error rate interrupts control register *…continued*

SER_INTR_CTRL (address 00FEh)				
Bit	**Symbol**	**Access**	**Value**	**Description**
5 to 3	INTR_MOD[2:0]	R/W		interrupt settings
			000	**DLP interrupt depends on lane 0**
			001	DLP interrupt depends on lane 1
			010	DLP interrupt depends on lane 2
			011	DLP interrupt depends on lane 3
			100	DLP interrupt depends on lane 0 or lane 2
			101	DLP interrupt depends on lane 0 or lane 1 or lane 2 or lane 3
			110	Hold_flagcnt (see Section 11.8.6.1)
			111	no interrupt

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11.12.9 JESD204 receiver monitoring

This block of registers enables the monitoring of the JESD receiver.

11.12.9.1 JESD204 receiver monitoring block register allocation map description

Table 143 shows an overview of all the JESD204 receiver monitoring registers.

Table 143. JESD204 receiver monitoring register allocation map

Addr.	Register name	R/W	Bit definition								Default
Hex			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0100h	SER_CTRL_0	R/W	SEL_XBERT_LN[1:0]		CHCK_PRBS	RD_SEL	XBERT_CTL[2:0]			SR_XBERT_CNT	00h
0101h	SER_CTRL_1	R/W	-	START_WIN_JTSPAT[6:0]							00h
0102h	SER_CTRL_2	R/W	-	STOP_WIN_JTSPAT[6:0]							75h
0103h	SER_CTRL_3	R/W	STLTP_LN_MASK[3:0]				-	-	RST_STLTP_FLAG	RST_XBERT_FLAG	F0h
0104h	XBERT_CNT_LSB	R	XBERT_CNT[7:0]								uuh
0105h	XBERT_CNT_MSB	R	XBERT_CNT[15:8]								uuh
010Ch	FIRST_JTSPAT	R	-	FIRST_JTSPAT_LN0[6:0]							uuh
0110h	FIRST_XBERT_PAT_LSB	R	FIRST_XBERT_PAT[7:0]								uuh
0111h	FIRST_XBERT_PAT_MSB	R	-	-	-	-	-	-	FRST_XBERT_PAT[9:8]		uuh
0112h	SER_LVL_L_LN0_LSB	R	SER_LVL_L_LN0[7:0]								uuh
0113h	SER_LVL_L_LN0_MSB	R	SER_LVL_L_LN0[15:8]								uuh
0114h	SER_LVL_L_LN1_LSB	R	SER_LVL_L_LN1[7:0]								uuh
0115h	SER_LVL_L_LN1_MSB	R	SER_LVL_L_LN1[15:8]								uuh
0116h	SER_LVL_L_LN2_LSB	R	SER_LVL_L_LN2[7:0]								uuh
0117h	SER_LVL_L_LN2_MSB	R	SER_LVL_L_LN2[15:8]								uuh
0118h	SER_LVL_L_LN3_LSB	R/W	SER_LVL_L_LN3[7:0]								00h

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Table 143. JESD204 receiver monitoring register allocation map *…continued*

Addr.	Register name	R/W	Bit definition								Default
Hex			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0119h	SER_LVL_L_LN3_MSB	R/W	SER_LVL_L_LN3[15:8]								00h
011Ah	MAN_MFB_LN0	R/W	-	MAN_MFB_LN0[6:0]							01h
011Bh	MAN_MFB_LN1	R/W	-	MAN_MFB_LN1[6:0]							01h
011Ch	MAN_MFB_LN2	R/W	-	MAN_MFB_LN2[6:0]							01h
011Dh	MAN_MFB_LN3	R/W	-	MAN_MFB_LN3[6:0]							01h
011Eh	FORCE_MFB_LNX	R/W	-	-	-	-	FORCE_MFB_LN3	FORCE_MFB_LN2	FORCE_MFB_LN1	FORCE_MFB_LN0	00h

[1] u = undefined at power-up or after reset.

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11.12.9.2 JESD204 receiver monitoring block bit definition detailed description

The tables in this section contain detailed descriptions of the JESD204x receiver monitoring registers.

Table 144. Sample rate error control registers
Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0100h	SER_CTRL_0	7 to 6	SEL_XBERT_LN[1:0]	R/W		XBERT operates on lane:
					00	**lane 0**
					01	lane 1
					10	lane 2
					11	lane 3
		5	CHCK_PRBS	R/W		prbs sequence
					0	**synchronization to prbs sequence**
					1	check prbs sequence
		4	RD_SEL	R/W		read back selection
					0	**normal operation**
					1	reserved
		3 to 1	XBERT_CTL[2:0]	R/W		XBERT selection
					000	**idle mode**
					001	JTSPAT
					010	PRBS31
					011	PRBS23
					100	PRBS15
					101	PRBS7
					others	idle
		0	SR_XBERT_CNT	R/W		soft reset XBERT_CNT
					0	**no action**
					1	soft reset XBERT counter
0101h	SER_CTRL_1	6 to 0	START_WIN_JTSPAT[6:0]	R/W		start win jtspat generation
0102h	SER_CTRL_2	6 to 0	STOP_WIN_JTSPAT[6:0]	R/W		stop window jtspat generation
0103h	SER_CTRL_3	7 to 4	STLTP_LN_MASK[3:0]	R/W		Mask to used STLTP_ERR_FLAG
			bit 7			**lane 3**
			bit 6			**lane 2**
			bit 5			**lane 1**
			bit 4			**lane 0**
		1	RST_STLTP_FLAG	R/W		reset STLTP FLAG
		0	RST_XBERT_FLAG	R/W		reset XBERT_FLAG

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Table 145. LSB/MSB of sample error rate counter registers
Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0104h	XBERT_CNT_LSB	7 to 0	XBERT_CNT[7:0]	R	-	8 least significant bits of XBERT error rate counter
0105h	XBERT_CNT_MSB	7 to 0	XBERT_CNT[15:8]	R	-	8 most significant bits of XBERT error rate counter

Table 146. First JTSPAT with sample error rate registers
Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
010Ch	FIRST_JTSPAT	6 to 0	FIRST_JSTPAT[6:0]	R	-	indication of first jtspat

Table 147. LSB/MSB of first sample error rate pattern registers
Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0110h	FIRST_XBERT_PAT_LSB	7 to 0	FIRST_XBERT_PAT[7:0]	R	-	8 least significant bits of first sample error rate pattern
0111h	FIRST_XBERT_PAT_MSB	1 to 0	FIRST_XBERT_PAT[9:8]	R	-	2 most significant bits first sample error rate pattern
0112h	SER_LVL_L_LN0_LSB	7 to 0	SER_LVL_L_LN0[7:0]	R	-	8 least significant bits of sample error rate level lane 0
0113h	SER_LVL_L_LN0_MSB	7 to 0	SER_LVL_L_LN0[15:8]	R	-	8 most significant bits of sample error rate level lane 0
0114h	SER_LVL_L_LN1_LSB	7 to 0	SER_LVL_L_LN1[7:0]	R	-	8 least significant bits of sample error rate level lane 1
0115h	SER_LVL_L_LN1_MSB	7 to 0	SER_LVL_L_LN1[15:8]	R	-	8 most significant bits of sample error rate level lane 1
0116h	SER_LVL_L_LN2_LSB	7 to 0	SER_LVL_L_LN2[7:0]	R	-	8 least significant bits of sample error rate level lane 2
0117h	SER_LVL_L_LN2_MSB	7 to 0	SER_LVL_L_LN2[15:8]	R	-	8 most significant bits of sample error rate level lane 2
0118h	SER_LVL_L_LN3_LSB	7 to 0	SER_LVL_L_LN3[7:0]	R	-	8 least significant bits of sample error rate level lane 3
0119h	SER_LVL_L_LN3_MSB	7 to 0	SER_LVL_L_LN3[15:8]	R	-	8 most significant bits of sample error rate level lane 3

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Table 148. Multi-frame bytes registers
Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
011Ah	MAN_MFB_LN0	6 to 0	MAN_MFB_LN0[6:0]	R/W	-	number of multi-frame bytes instead of force_mfb_ln0 is ‘1
011Bh	MAN_MFB_LN1	6 to 0	MAN_MFB_LN1[6:0]	R/W	-	number of multi-frame bytes instead of force_mfb_ln1 is ‘1
011Ch	MAN_MFB_LN2	6 to 0	MAN_MFB_LN2[6:0]	R/W	-	number of multi-frame bytes instead of force_mfb_ln2 is ‘1
011Dh	MAN_MFB_LN3	6 to 0	MAN_MFB_LN3[6:0]	R/W	-	number of multi-frame bytes instead of force_mfb_ln3 is ‘1

Table 149. Force multi-frame bytes register

FORCE_MFB (address 011Eh)				
Bit	**Symbol**	**Access**	**Value**	**Description**
3	FORCE_MFB_LN3	R/W		force multi-frame bytes for lane_3
			0	**no action**
			1	force man_mfb_ln3 to ILA_CTRL
2	FORCE_MFB_LN2	R/W		force multi-frame bytes for lane_2
			0	**no action**
			1	force man_mfb_ln2 to ILA_CTRL
1	FORCE_MFB_LN1	R/W		force multi-frame bytes for lane_1
			0	**no action**
			1	force man_mfb_ln1 to ILA_CTRL
0	FORCE_MFB_LN0	R/W		force multi-frame bytes for lane_0
			0	**no action**
			1	force man_mfb_ln0 to ILA_CTRL

11.12.10 JESD204 read configuration block

These blocks of registers reproduce the values of the configuration data transmitted from the TX in the second multi-frame of the initial-lane alignment sequence and decoded in the DAC165xD.

Table 150 show an overview of the generic parts of the register addresses.

Table 150. Overview of generic parts of register addresses

	DAC AB
lane 0	nnn = 012
lane 1	nnn = 013
lane 2	nnn = 014
lane 3	nnn = 015

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11.12.10.1 JESD204 read configuration block lane register allocation map

Table 151 shows an overview of all the JESD204 read configuration lane registers.

Table 151. JESD204 read configuration block DAC X/Y lane 0/lane 1 register allocation map

Addr.	Register name	R/W	Bit definition								Default
Hex			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
nnn0h	P_LN_CFG_0	R	P_LN_DID[7:0]								uuh
nnn1h	P_LN_CFG_1	R	P_LN_ADJCNT[3:0]				P_LN_BID[3:0]				uuh
nnn2h	P_LN_CFG_2	R	-	P_LN_ADJDIR	P_LN_PHADJ	P_LN_LID[4:0]					uuh
nnn3h	P_LN_CFG_3	R	P_LN_SCR	-	-	P_LN_L[4:0]					uuh
nnn4h	P_LN_CFG_4	R	P_LN_F[7:0]								uuh
nnn5h	P_LN_CFG_5	R	-	-	-	P_LN_K[4:0]					uuh
nnn6h	P_LN_CFG_6	R	P_LN_M[7:0]								uuh
nnn7h	P_LN_CFG_7	R	P_LN_CS[1:0]		-	P_LN_N[4:0]					uuh
nnn8h	P_LN_CFG_8	R	P_LN_SUBCLASSV[2:0]			P_LN_N'[4:0]					uuh
nnn9h	P_LN_CFG_9	R	P_LN_JESDV[2:0]			P_LN_S[4:0]					uuh
nnnAh	P_LN_CFG_10	R	P_LN_HD	-	-	P_LN_CF[4:0]					uuh
nnnBh	P_LN_CFG_11	R	P_LN_RES1[7:0]								uuh
nnnCh	P_LN_CFG_12	R	P_LN_RES2[7:0]								uuh
nnnDh	P_LN_CFG_13	R	P_LN_FCHK[7:0]								uuh

[1] u = undefined at power-up or after reset.

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11.12.10.2 JESD204 read configuration block lane bit definition detailed description

The tables in this section contain detailed descriptions of the JESD204 read configuration lane registers.

Table 152. Lane configuration registers

Default settings are shown highlighted. See *Table 150* for the generic information on the register addresses.

Address	Register	Bit	Symbol	Access	Value	Description
nnn0h	P_LN_CFG_0	7 to 0	P_LN_DID[7:0]	R	-	physical lane device ID
nnn1h	P_LN_CFG_1	7 to 4	P_LN_ADJ_CNT[3:0]	R	-	physical lane adjustable counter
		3 to 0	P_LN_BID[3:0]		-	physical lane bank ID
nnn2h	P_LN_CFG_2	6	P_LN_ADJ_DIR	R	-	physical lane adjustable direction
		5	P_LN_PH_ADJ			physical lane adjustable phase
		4 to 0	P_LN_LID[4:0]		-	physical lane lane ID
nnn3h	P_LN_CFG_3	7	P_LN_SCR	R	-	physical lane scrambler enabled
		4 to 0	P_LN_L[4:0]		-	number of physical lanes minus 1
nnn4h	P_LN_CFG_4	7 to 0	P_LN_F[7:0]	R	-	number of octets per frame minus 1
nnn5h	P_LN_CFG_5	4 to 0	P_LN_K[4:0]	R	-	number of frames per multi-frame minus 1
nnn6h	P_LN_CFG_6	7 to 0	P_LN_M[7:0]	R	-	number of converters per device minus 1
nnn7h	P_LN_CFG_7	7 to 6	P_LN_CS[1:0]	R	-	number of control bits
		4 to 0	P_LN_N[4:0]		-	converter resolution minus 1
nnn8h	P_LN_CFG_8	7 to 5	P_LN_SBCLSS_VS[2:0]	R	-	physical lane JESD204B subclass version
					00	subclass 0
					01	subclass 1
					10	subclass 2
		4 to 0	P_LN_N'[4:0]	R	-	number of bits per sample minus 1
nnn9h	P_LN_CFG_9	7 to 5	P_LN_JESDV	R	-	physical lane 0 JESD204 version
					000	version A
					001	version B
		4 to 0	P_LN0_S[4:0]	R	-	number of samples per converter per frame cycle minus 1
nnnAh	P_LN_CFG_10	7	P_LN_HD	R	-	high density
		4 to 0	P_LN_CF[4:0]		-	number of control words per frame cycle
nnnBh	P_LN_CFG_11	7 to 0	P_LN_RSRVD1[7:0]	R	-	physical lane reserved field
nnnCh	P_LN_CFG_12	7 to 0	P_LN_RSRVD2[7:0]	R	-	physical lane reserved field
nnnDh	P_LN_CFG_13	7 to 0	P_LN_FCHK[7:0]	R	-	physical lane checksum

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11.12.10.3 JESD204 read configuration block sample measurement registers

Table 153 shows an overview of all the JESD204 read configuration sample measurement registers.

Table 153. JESD204 read configuration block sample measurement registers

Register name		R/W	Bit definition								Default
			b7	b6	b5	b4	b3	b2	b1	b0	Hex
012Eh	P_LN10_SAMPLE_LSB	R	P_LN10_SAMPLE[7:0]								uuh
012Fh	P_LN10_SAMPLE_MSB	R	P_LN10_SAMPLE[15:8]								uuh
013Eh	P_LN10_SEL	W	P_LN10_SEL[7:0]								00h
014Eh	P_LN32_SAMPLE_LSB	R	P_LN32_SAMPLE[7:0]								uuh
014Fh	P_LN32_SAMPLE_MSB	R	P_LN32_SAMPLE[15:8]								
015Eh	P_LN32_SEL	W	P_LN32_SEL[7:0]								00h

[1] u = undefined at power-up or after reset.

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11.12.10.4 JESD204 read configuration block sample measurement registers detailed description

Table 154 shows an overview of all the JESD204 read configuration sample measurement registers.

Table 154. Lane 1/lane 0 sample LSB/MSB registers
Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description (see Section 11.8.6.5)
012Eh	P_LN10_SAMPLE_LSB	7 to 0	P_LN10_SAMPLE[7:0]	R	-	internal DLP data on physical lane 0 or physical lane 1 depending on the value of LN10_SELECT (bit 1E; LSB) The data are strobed by DLP_STROBE
012Fh	P_LN10_SAMPLE_MSB	7 to 0	P_LN10_SAMPLE[15:8]	R	-	internal DLP data on physical lane 0 or physical lane 1 depending on the value of LN10_SELECT (bit 1E; MSB) The data are strobed by DLP_STROBE

Table 155. Physical lane 1/lane 0 selection register
Default settings are shown highlighted.

LN10_SEL (address 013Eh)				
Bit	**Symbol**	**Access**	**Value**	**Description (see Section 11.8.6.5)**
7 to 0	P_LN10_SEL	W		specifies the lane affected by DLP_STROBE
			0	**physical lane 0**
			1	physical lane 1

Table 156. Lane 3/lane 2 sample LSB/MSB registers
Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description (see Section 11.8.6.5)
014Eh	P_LN32_SAMPLE_LSB	7 to 0	P_LN32_SAMPLE[7:0]	R	-	internal DLP data on lane 2 or lane 3 depending on the value of LN10_SELECT (bit 1E; LSB) The data are strobed by DLP_STROBE
014Fh	P_LN32_SAMPLE_MSB	7 to 0	P_LN32_SAMPLE[15:8]	R	-	internal DLP data on lane 2 or lane 3 depending on the value of LN10_SELECT (bit 1E; MSB) The data are strobed by DLP_STROBE

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Table 157. Physical lane 3/lane 2 selection register

Default settings are shown highlighted.

P_LN32_SEL (address 015Eh)				
Bit	**Symbol**	**Access**	**Value**	**Description (see Section 11.8.6.5)**
7 to 0	P_LN32_SEL	W		specifies the lane affected by DLP_STROBE
			0	**physical lane 2**
			1	physical lane 3

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11.12.11 RX physical layer control block

This block of registers specifies the configuration ot the physical layer of the deserializer. The control block the various features as the equalizer and the common-mode voltage or resistor termination. The RX physical layer monitor block monitors the status of the previous controls.

11.12.11.1 RX physical layer block register allocation map

Table 158 shows an overview of all the RX physical layer control registers.

Table 158. RX physical layer control block register allocation map

Addr.	Register name	R/W	Bit definition								Default
Hex			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0162h	HS_RX_CDR_DIV	R/W	HS_RX_CDR_LOW_SPEED_EN	HS_RX_CDR_DIVM[1:0]		HS_RX_CDR_DIVN[4:0]					02h
0163h	HS_RX_CDR_CP	R/W	CP_ITRACK[3:0]				CP_IPFD[3:0]				54h
0167h	HS_RX_EQ_CTRL	R/W	-	-	RESERVED	HS_RX_EQ_AUTO_ZERO_EN	HS_RX_3_EQ_EN	HS_RX_2_EQ_EN	HS_RX_1_EQ_EN	HS_RX_0_EQ_EN	1Fh
0168h	HS_RX_LN0_EQ_GAIN	R/W	-	-	-	-	-	HS_RX_LN0_EQ_IF_GAIN[2:0]			04h
0169h	HS_RX_LN1_EQ_GAIN	R/W	-	-	-	-	-	HS_RX_LN1_EQ_IF_GAIN[2:0]			04h
016Ah	HS_RX_LN2_EQ_GAIN	R/W	-	-	-	-	-	HS_RX_LN2_EQ_IF_GAIN[2:0]			04h
016Bh	HS_RX_LN3_EQ_GAIN	R/W	-	-	-	-	-	HS_RX_LN3_EQ_IF_GAIN[2:0]			04h
0170h	HS_RX_RT_VCM	R/W	-	-	HS_RX_RT_VCM_SEL	HS_RX_RT_VCM_REF[4:0]					25h
0171h	HS_RX_RT_CTRL	R/W	HS_RX_LN3_RT_HIZ_EN	HS_RX_LN2_RT_HIZ_EN	HS_RX_LN1_RT_HIZ_EN	HS_RX_LN0_RT_HIZ_EN	HS_RX_LN3_RT_EN	HS_RX_LN2_RT_EN	HS_RX_LN1_RT_EN	HS_RX_LN0_RT_EN	0Fh
017Dh	SYNC_CFG_CTRL	R/W	SYNC_EN	SYNC_SET_VCM[2:0]			-	SYNC_SET_LVL[2:0]			80h
017Eh	SYNC_SEL_CTRL	R/W	SYNC_TST_DATA_TX_EN	-	SYNC_TST_DATA_SEL[1:0]		-	-	-	-	00h

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11.12.11.2 RX physical layer control block bit definition detailed description

The tables in this section contain detailed descriptions of the RX physical layer control registers.

Table 159. High speed receiver clock data recovery divider register
Default values are shown highlighted.

HS_RX_CDR_DIV (address 0162h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7	HS_RX_CDR_LOW_SPEED_EN	R/W		low speed receiver clock data recovery mode
			0	**disabled**
			1	enabled
6 to 5	HS_RX_CDR_DIVM[1:0]	R/W	-	divm ratio used to divide the reference clock (predivider) (see Figure 81)
4 to 0	HS_RX_CDR_DIVN[4:0]	R/W	-	divn ratio used in clock data receiver reference loop (see Figure 81)

Table 160. High speed receiver equalizer control register
Default values are shown highlighted.

HS_RX_EQ_CTRL (address 0167h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
5	RESERVED	R/W	0	reserved to 0
4	HS_RX_EQ_AUTO_ZERO_EN	R/W		Equalizer auto zero mode
			0	disabled (for all lanes)
			1	**enabled (for all lanes)**
3	HS_RX_LN3_EQ_EN	R/W		Equalizer of receiver lane 3
			0	disabled (power-down)
			1	**enabled (active)**
2	HS_RX_LN2_EQ_EN	R/W		Equalizer of receiver lane 2
			0	disabled (power-down)
			1	**enabled (active)**
1	HS_RX_LN1_EQ_EN	R/W		Equalizer of receiver lane 1
			0	disabled (power-down)
			1	**enabled (active)**
0	HS_RX_LN0_EQ_EN	R/W		Equalizer of receiver lane 0
			0	disabled (power-down)
			1	**enabled (active)**

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Table 161. High speed equalizer gain registers
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0168h	HS_RX_LN0_EQ_GAIN	2 to 0	HS_RX_LN0_EQ_IF_GAIN[2:0]	R/W	-	sets if-gain for receiver lane 0 equalizer
0169h	HS_RX_LN1_EQ_GAIN	2 to 0	HS_RX_LN1_EQ_IF_GAIN[2:0]	R/W	-	sets if-gain for receiver lane 1 equalizer
016Ah	HS_RX_LN2_EQ_GAIN	2 to 0	HS_RX_LN2_EQ_IF_GAIN[2:0]	R/W	-	sets if-gain for receiver lane 2 equalizer
016Bh	HS_RX_LN3_EQ_GAIN	2 to 0	HS_RX_LN3_EQ_IF_GAIN[2:0]	R/W	-	sets if-gain for receiver lane 3 equalizer

Table 162. High speed receiver termination resistor voltage common-mode register
Default values are shown highlighted.

HS_RX_RT_VCM (address 0170h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
5	HS_RX_RT_VCM_SEL	R/W		rx_rt modules configuration
			0	do not use
			1	**rx_rt_modules configured for RX-use (all lanes)**
4 to 0	HS_RX_RT_VCM_REF[4:0]	R/W	-	sets common-mode reference for hs_rx_rt (all lanes)

Table 163. High speed resistor termination control register
Default values are shown highlighted.

HS_RX_RT_CTRL (address 0171h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7	HS_RX_LN3_RT_HIZ_EN	R/W		high speed receiver lane 3 input
			0	**100 Ω (differential impedance)**
			1	high ohmic
6	HS_RX_LN2_RT_HIZ_EN	R/W		high speed receiver lane 2 input
			0	**100 Ω (differential impedance)**
			1	high ohmic
5	HS_RX_LN1_RT_HIZ_EN	R/W		high speed receiver lane 1 input
			0	**100 Ω (differential impedance)**
			1	high ohmic
4	HS_RX_LN0_RT_HIZ_EN	R/W		high speed receiver lane 0 input
			0	**100 Ω (differential impedance)**
			1	high ohmic
3	HS_RX_LN3_RT_EN	R/W		high speed receiver lane 3 resistance termination
			0	disabled (power-down)
			1	**enabled (active)**

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Table 163. High speed resistor termination control register *…continued*
Default values are shown highlighted.

HS_RX_RT_CTRL (address 0171h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
2	HS_RX_LN2_RT_EN	R/W		high speed receiver lane 2 resistance termination
			0	disabled (power-down)
			1	**enabled (active)**
1	HS_RX_LN1_RT_EN	R/W		high speed receiver lane 1 resistance termination
			0	disabled (power-down)
			1	**enabled (active)**
0	HS_RX_LN0_RT_EN	R/W		high speed receiver lane 0 resistance termination
			0	disabled (power-down)
			1	**enabled (active)**

Table 164. Synchronization configuration control register
Default values are shown highlighted.

SYNC_CFG_CTRL (address 017Dh)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7	SYNC_EN	R/W		synchronization buffer
			0	disabled (power-down)
			1	**enabled (active)**
6 to 4	SYNC_SET_VCM[2:0]	R/W	-	sets common-mode output voltage of synchronization buffer
2 to 0	SYNC_SET_LVL[2:0]	R/W	-	sets output levels (swing) of synchronization buffer

Table 165. Synchronization test data control register
Default values are shown highlighted.

SYNC_SEL_CTRL (address 017Eh)				
Bit	**Symbol**	**Access**	**Value**	**Description**
7	SYNC_TST_DATA_TX_EN	R/W		synchronization test data transmission
			0	**normal operation (JESD204x synchronization buffer)**
			1	test mode (synchronization output depends on SYNC_TST_DATA_SEL)
5 to 4	SYNC_TST_DATA_SEL[1:0]	R/W		synchronization test data selection
			00	**synchronization ← HS_RX_0_CLK_DX**
			01	synchronization ← HS_RX_1_CLK_DX
			10	synchronization ← HS_RX_2_CLK_DX
			11	synchronization ← HS_RX_3_CLK_DX

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11.12.11.3 RX physical layer monitor register allocation map

Table 166 shows an overview of all RX physical layer monitor registers.

Table 166. RX physical layer monitor register allocation map

Addr.	Register name	R/W	Bit definition								Default
Hex			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0185h	HS_RX_CDR_EN_MON_0	R	-	-	-	-	HS_RX_LN3_CDR_EN_MON	HS_RX_LN2_CDR_EN_MON	HS_RX_LN1_CDR_EN_MON	HS_RX_LN0_CDR_EN_MON	0Fh
0187h	HS_RX_EQ_CTRL_MON	R	-	-	RESERVED	HS_RX_EQ_AUTO_ZERO_EN_MON	HS_RX_LN3_EQ_EN_MON	HS_RX_LN2_EQ_EN_MON	HS_RX_LN1_EQ_EN_MON	HS_RX_LN0_EQ_EN_MON	1Fh

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11.12.11.4 RX physical layer monitor block bit definition detailed description

The tables in this section contain detailed descriptions of the RX physical layer monitor registers.

Table 167. Current high speed RX equalizer control register
Default values are shown highlighted.

I_HS_RX_EQ_CTRL (address 0187h)				
Bit	**Symbol**	**Access**	**Value**	**Description**
5	RESERVED	R		reserved to 0
4	HS_RX_EQ_AUTO_ZERO_EN_MON	R		Equalizer auto zero mode
			0	**disabled (for all lanes)**
			1	enabled (for all lanes)
3	HS_RX_LN3_EQ_EN_MON	R		Equalizer of receiver lane 3
			0	disabled (power-down)
			1	**enabled (active)**
2	HS_RX_LN2_EQ_EN_MON	R		Equalizer of receiver lane 2
			0	disabled (power-down)
			1	**enabled (active)**
1	HS_RX_LN1_EQ_EN_MON	R		Equalizer of receiver lane 1
			0	disabled (power-down)
			1	**enabled (active)**
0	HS_RX_LN0_EQ_EN_MON	R		Equalizer of receiver lane 0
			0	disabled (power-down)
			1	**enabled (active)**

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12. PACKAGE OUTLINE

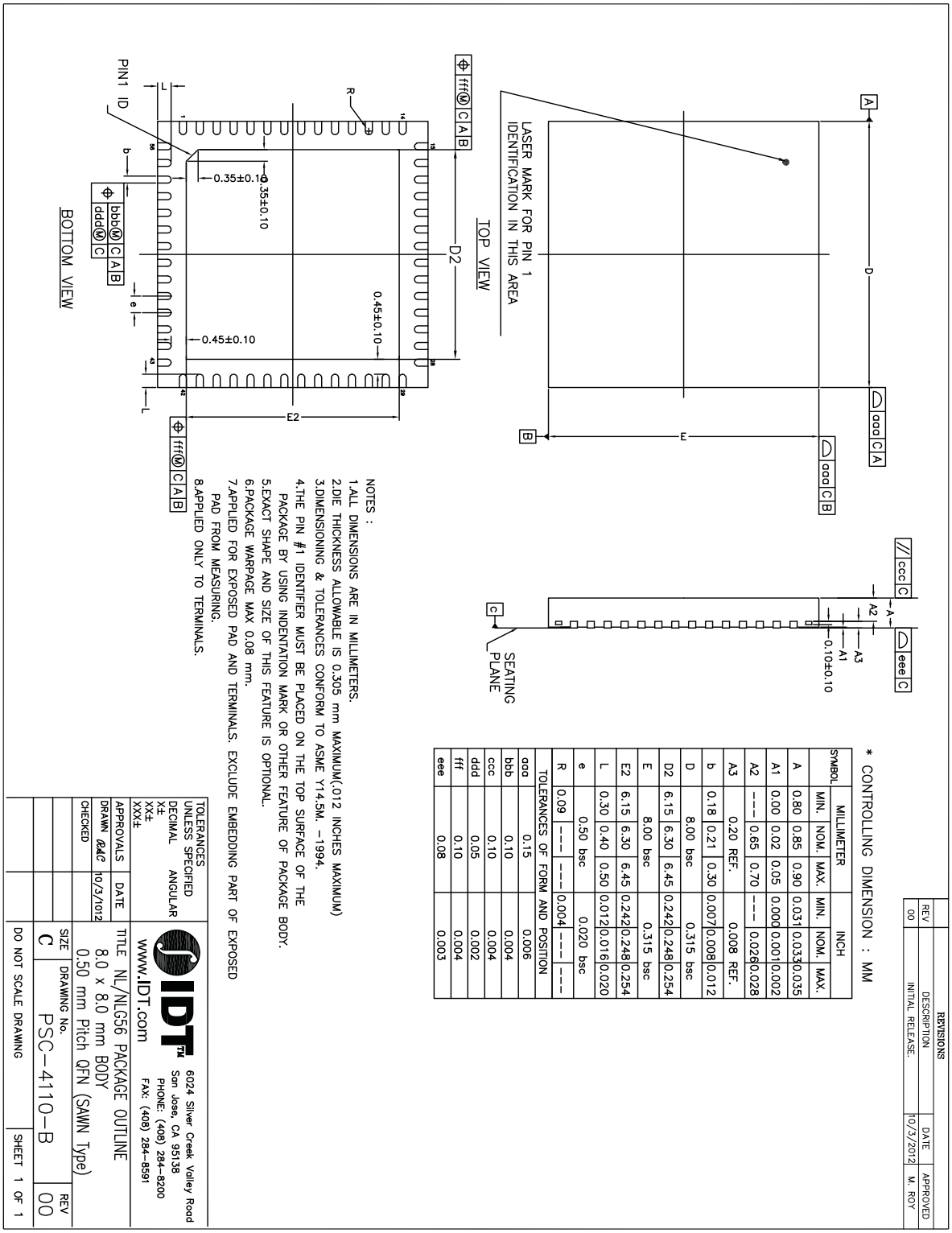


Fig 86. Package outline VFQFP-N 56

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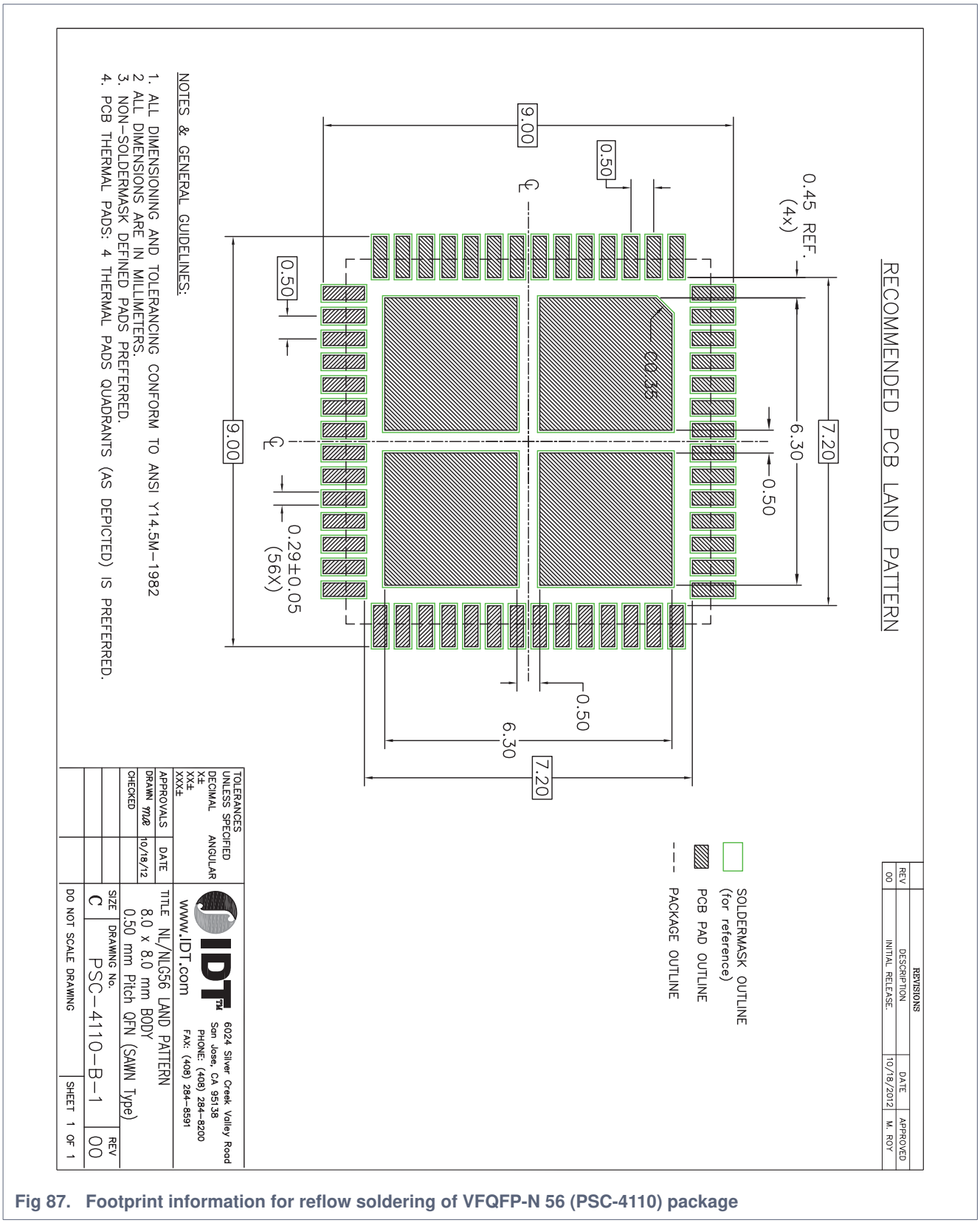


Fig 87. Footprint information for reflow soldering of VFQFP-N 56 (PSC-4110) package

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13. Abbreviations

Table 168. Abbreviations

Acronym	Description
BW	BandWidth
BWA	Broadband Wireless Access
CDI	Clock Domain Interface
CDMA	Code Division Multiple Access
CDR	Clock Data Recovery
CML	Current Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
CTLE	Continuous Time Linear Equalization
DAC	Digital-to-Analog Converter
EDGE	Enhanced Data rates for GSM Evolution
FIR	Finite Impulse Response
GSM	Global System for Mobile communications
IF	Intermediate Frequency
IMD3	Third Order InterModulation
LMDS	Local Multipoint Distribution Service
LO	Local Oscillator
LTE	Long Term Evolution
LVDS	Low-Voltage Differential Signaling
MDS	Multiple Device Synchronization
MIMO	Multiple In Multiple Out
NCO	Numerically Controlled Oscillator
NMOS	Negative Metal-Oxide Semiconductor
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
SFDR	Spurious-Free Dynamic Range
SPI	Serial Peripheral Interface
WCDMA	Wide band Code Division Multiple Access
WLL	Wireless Local Loop

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14. GLOSSARY

14.1 Static parameters

INL — The deviation of the transfer function from a best fit straight line (linear regression computation).

DNL — The difference between the ideal and the measured output value between successive DAC codes.

14.2 Dynamic parameters

Spurious-Free Dynamic Range (SFDR) — The ratio between the RMS value of the reconstructed output sine wave and the RMS value of the largest spurious observed (harmonic and non-harmonic, excluding DC component) in the frequency domain.

InterModulation Distortion (IMD) — From a dual-tone digital input sine wave (these two frequencies being close together), the intermodulation distortion products IMD2 and IMD3 (second order and third order components) are defined below.

IMD2 — The ratio between the RMS value of either tone and the RMS value of the worst second order intermodulation product.

IMD3 — The ratio between the RMS value of either tone and the RMS value of the worst third order intermodulation product.

Total Harmonic Distortion (THD) — The ratio between the RMS value of the harmonics of the output frequency and the RMS value of the output sine wave. Usually, the calculation of THD is done on the first 5 harmonics.

Signal-to-Noise Ratio (SNR) — The ratio between the RMS value of the reconstructed output sine wave and the RMS value of the noise excluding the harmonics and the DC component.

Restricted BandWidth Spurious-Free Dynamic Range ($SFDR_{RBW}$) — the ratio between the RMS value of the reconstructed output sine wave and the RMS value of the noise, including the harmonics, in a given bandwidth centered around f_{offset}.

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15. Revision history

Table 169. Revision history

Document ID	Release date	Data sheet status
DAC1653D; DAC1658D v.2.41	20140428	Final

Table 170. Revision history

Item changed current revision	Comments
MDS sample accuracy	explicit information about the phase delay uncertainty of the NCO carrier when using the MDS and the NCO together
Titles and register typo	updated with correct values and default values in bold character
NSD fig 17 and 18	change X-label on both graph
previous revision 2.40	
PRBS test sequence	updated with new settings
Max Power figures	updated with new values
Digital current consumptions (fig 31)	updated with new values
SYSREF signal	updated specification (periodic/gapped)
previous revision 2.31	
PRBS test sequence	updated with new settings
IO-Mux	added xbert flag setting
LVDS clock	400 mV min value
Statics characteristics	all values updated with final ones
Dynamics characteristics	all values updated with final ones
Startup sequence	update SEL_ILA bits to 11
SEL_ILA information	added section about ILA wrong detection in case TX takes too long time to respond to SYNC low
Latency	222 mode values were incorrect
Equalizer gain	added
previous revision 2.20	
Block diagram	clock dividers were wrongly indicated
Block diagram	IO0 is now bi-directionnal
Block Diagram and Pins list	VDDA(out) renamed in VDDA(3V3)
Block Diagram and Pins list	VDDD(DIF) renamed in VDDD(sync)
Block Diagram and Pins list	JRES value specified to 6.98 kOhms
DAC output voltage compliance range	change the specification information
SPI timings	figures for read/write in 3 or 4 wires mode added. Timing specification updated
Main device configuration section	Startup sequence has been added
Power down mode	Power down mode feature at startup time.
CDI table	Maximum input data rate updated
SYNC output level configuration	values updated for common mode and swing
PRBS test	new support for PRBS23 , 15, 7
PRBS checker	only one module for all the lanes
PRBS example	script added
IO-mux	IO1 indicator location updated
JRES pin section	section added
Equalizer section	text updated
Output interfacing configuration	schematics updated for High and Low common mode
Power and grounding	text updated
Registers table	updated to latest information

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