DG211

SPST 4-Channel Analog Switch

**NOT RECOMMENDED FOR NEW DESIGNS
NO RECOMMENDED REPLACEMENT
contact our Technical Support Center at
1-888-INTERSIL or www.intersil.com/tsc**

FN3118
Rev 5.00
November 19, 2007

The DG211 is a low cost, CMOS monolithic, Quad SPST analog switch. It can be used in general purpose switching applications for communications, instrumentation, process control and computer peripheral equipment and provides true bi-directional performance in the ON condition and blocks signals to $30V_{P-P}$ in the OFF condition.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
DG211CJ	DG211CJ	0 to +70	16 Ld PDIP	E16.3
DG211CJZ (Note)	DG211CJZ	0 to +70	16 Ld PDIP* (Pb-free)	E16.3
DG211CY**	DG211CY	0 to +70	16 Ld SOIC	M16.15
DG211CYZ** (Note)	DG211CYZ	0 to +70	16 Ld SOIC (Pb-free)	M16.15
DG211CVZ** (Note)	DG211 CVZ	0 to +70	16 Ld TSSOP (Pb-free)	M16.173

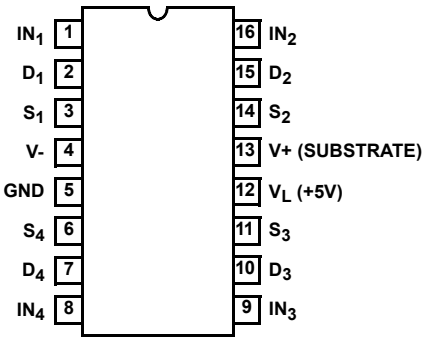
*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

**Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

DG211
(16 LD PDIP, SOIC, TSSOP)
TOP VIEW

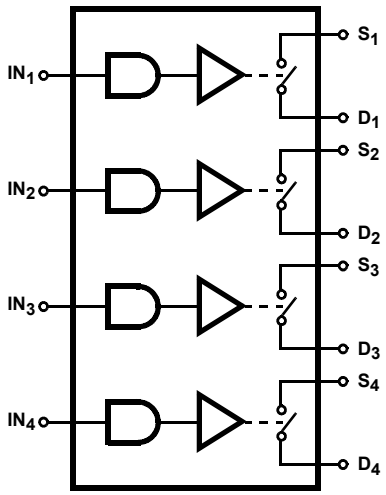


Features

- Switches ±15V Analog Signals
- TTL Compatibility
- Logic Inputs Accept Negative Voltages
- r_{ON} (Max) 175Ω
- Pb-Free Available (RoHS Compliant)

Functional Block Diagram

DG211



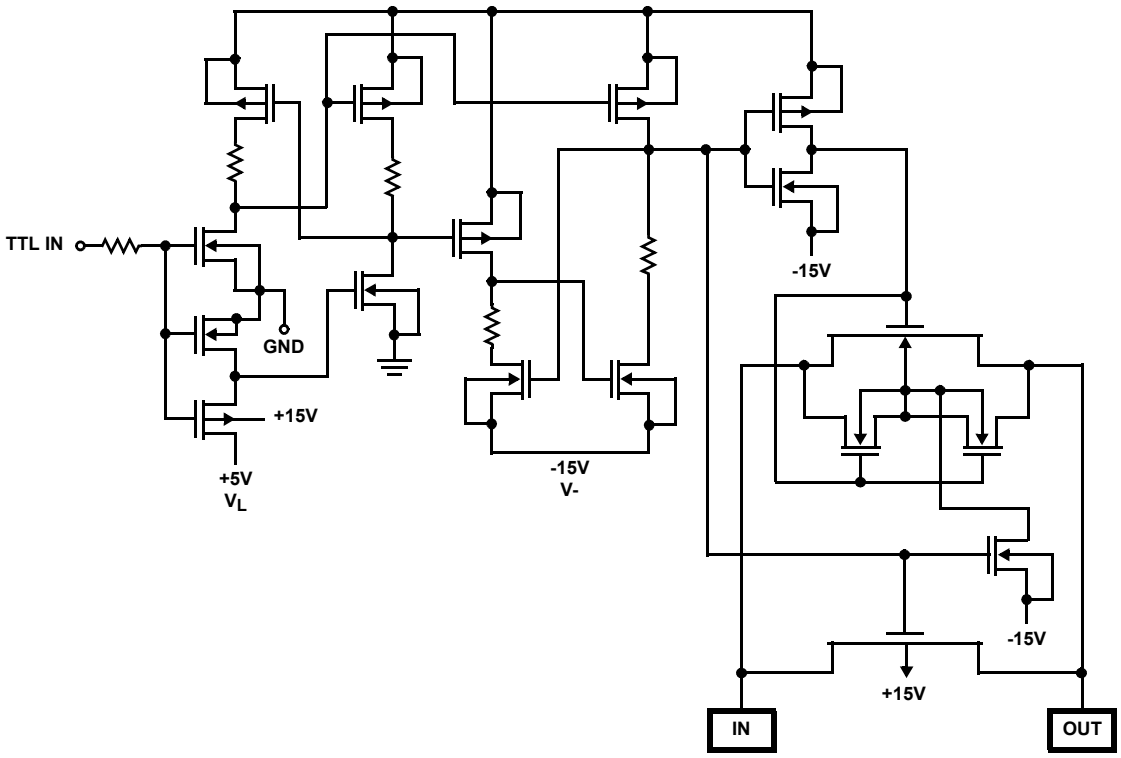
TRUTH TABLE

LOGIC	DG211
0	ON
1	OFF

Logic "0" ≤0.8V, Logic "1" ≥ 2.4V

Schematic Diagram

DG211 ($^1/_4$ AS SHOWN)



Absolute Maximum Ratings

V+ to V- 44V
V_{IN} to Ground . . . . . V- to V+
V_L to Ground . . . . . -0.3V to 25V
V_S or V_D to V+ . . . . . 0V to -36V
V_S or V_D to V- . . . . . 0V to 36V
V+ to Ground 25V
V- to Ground. . . . . -25V
Current, any Terminal Except S or D 30mA
Continuous Current, S or D 20mA
Peak Current, S or D (Pulsed 1ms, 10% Duty Cycle Max) 70mA

Operating Conditions

Temperature Range . . . . . 0°C to +70°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package*	100
SOIC Package	120
TSSOP Package	150

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp
*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V+ = +15V, V- = -15V, V_L = +5V, GND, T_A = +25°C

PARAMETER	TEST CONDITIONS		MIN (Notes 2, 6)	TYP (Note 3)	MAX (Notes 2, 6)	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	See Figure 1 V_S = 10V, R_L = 1kΩ, C_L = 35pF		-	460	-	ns
Turn-OFF Time t_{OFF1}			-	360	-	ns
t_{OFF2}			-	450	-	ns
OFF Isolation, OIRR (Note 5)	V_{IN} = 5V, R_L = 1kΩ, C_L = 15pF, V_S = 1V_{RMS}, f = 100kHz		-	70	-	dB
Crosstalk (Channel-to-Channel), CCRR			-	-90	-	dB
Source OFF-Capacitance, $C_{S(OFF)}$	V_D = V_S = 0V, V_{IN} = 5V, f = 1MHz		-	5	-	pF
Drain OFF-Capacitance, $C_{D(OFF)}$			-	5	-	pF
Channel ON-Capacitance, $C_{D(ON)}$ + $C_{S(ON)}$			-	16	-	pF
DIGITAL INPUT CHARACTERISTICS						
Input Current with Voltage High, I_{IH}	V_{IN} = 2.4V		-1.0	-0.0004	-	µA
	V_{IN} = 15V		-	0.003	1.0	µA
Input Current with Voltage Low, I_{IL}	V_{IN} = 0V		-1.0	-0.0004	-	µA
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}			-15	-	15	V
Drain-Source ON-Resistance, $r_{DS(ON)}$	V_D = ±10V, I_S = 1mA, V_{IN} = 0.8V		-	150	175	Ω
Source OFF Leakage Current, $I_{S(OFF)}$	V_{IN} = 2.4V	V_S = 14V, V_D = -14V	-	0.01	5.0	nA
		V_S = -14V, V_D = 14V	-5.0	-0.02	-	nA
Drain OFF Leakage Current, $I_{D(OFF)}$		V_S = -14V, V_D = 14V	-	0.01	5.0	nA
		V_S = 14V, V_D = -14V	-5.0	-0.02	-	nA
Drain ON Leakage Current, $I_{D(ON)}$ (Note 4)	V_{IN} = 0.8V	V_S = V_D = 14V	-	0.1	5.0	nA
		V_S = V_D = -14V	-5.0	-0.15	-	nA

Electrical Specifications V+ = +15V, V- = -15V, V_L = +5V, GND, T_A = +25°C **(Continued)**

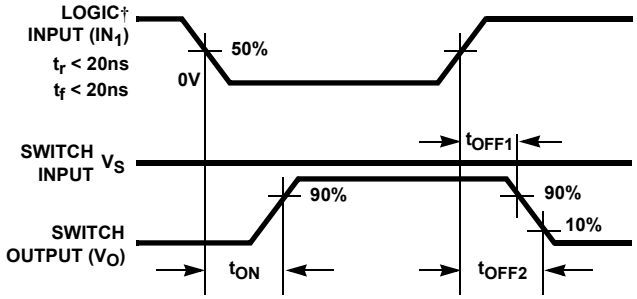
PARAMETER	TEST CONDITIONS	MIN (Notes 2, 6)	TYP (Note 3)	MAX (Notes 2, 6)	UNITS
POWER SUPPLY CHARACTERISTICS					
Positive Supply Current, I+	V_{IN} = 0V or 2.4V	-	0.1	10	µA
Negative Supply Current, I-		-	0.1	10	µA
Logic Supply Current, I_L		-	0.1	10	µA

NOTES:

2. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
3. For design reference only, not 100% tested.
4. $I_{D(ON)}$ is leakage from driver into ON switch.
5. OFF Isolation $= 20\log\frac{V_S}{V_D}$, V_S = Input to OFF switch, V_D = output.
6. Parts are 100% tested at +25°C. Over-temperature limits established by characterization and are not production tested.

Test Circuits and Waveforms

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note the V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



† Logic shown for DG211.

FIGURE 1. SWITCHING TIME MEASUREMENT POINTS

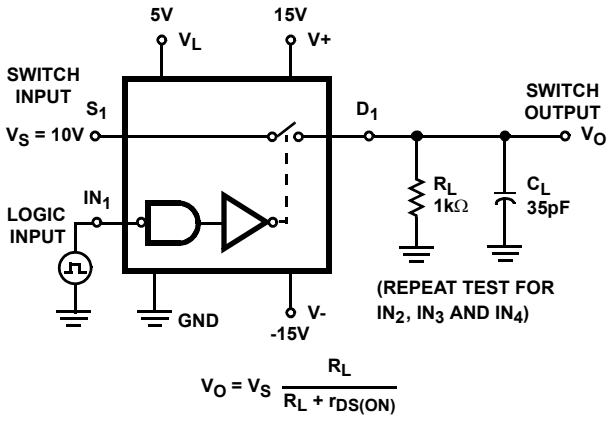
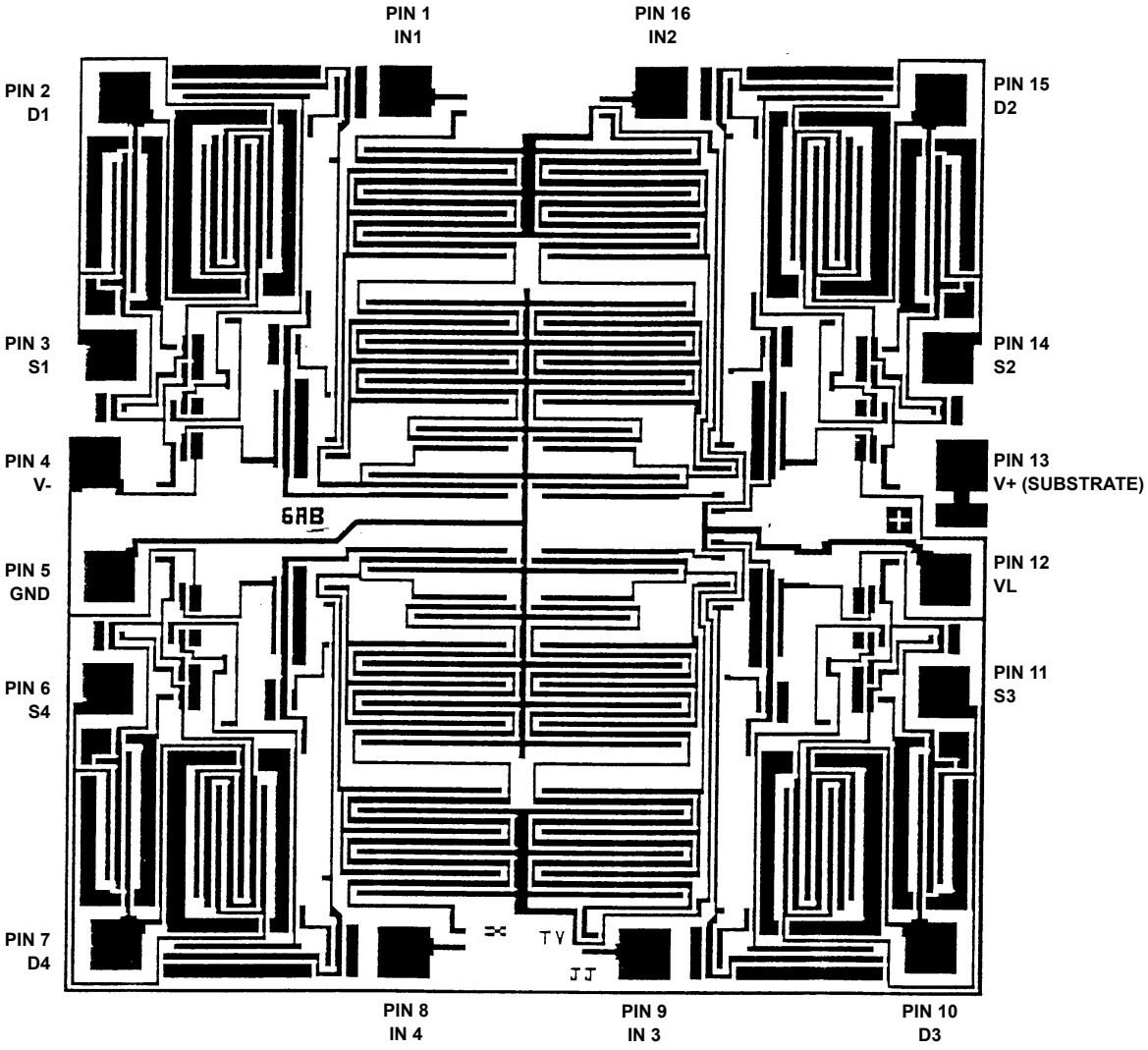


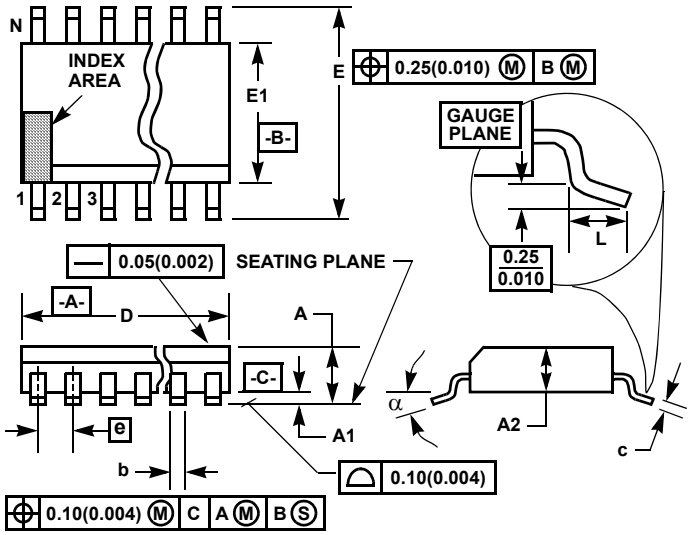
FIGURE 2. SWITCHING TIME TEST CIRCUIT

Metallization Mask Layout

DG211



Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AB, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

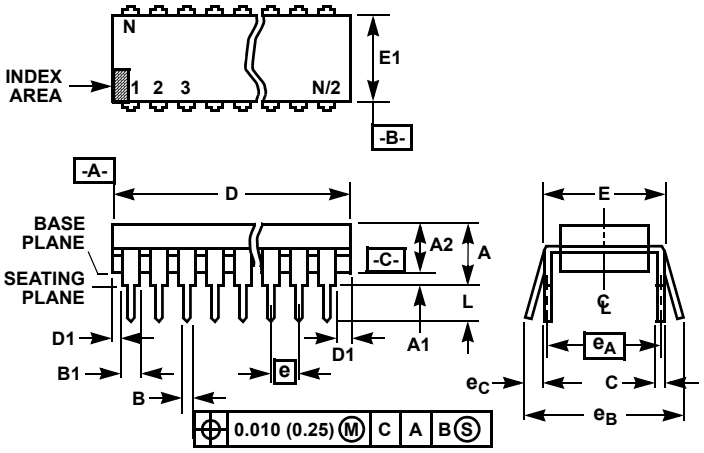
M16.173

16 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.043	-	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.033	0.037	0.85	0.95	-
b	0.0075	0.012	0.19	0.30	9
c	0.0035	0.008	0.09	0.20	-
D	0.193	0.201	4.90	5.10	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.020	0.028	0.50	0.70	6
N	16		16		7
α	0^o	8^o	0^o	8^o	-

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Dual-In-Line Plastic Packages (PDIP)



NOTES:

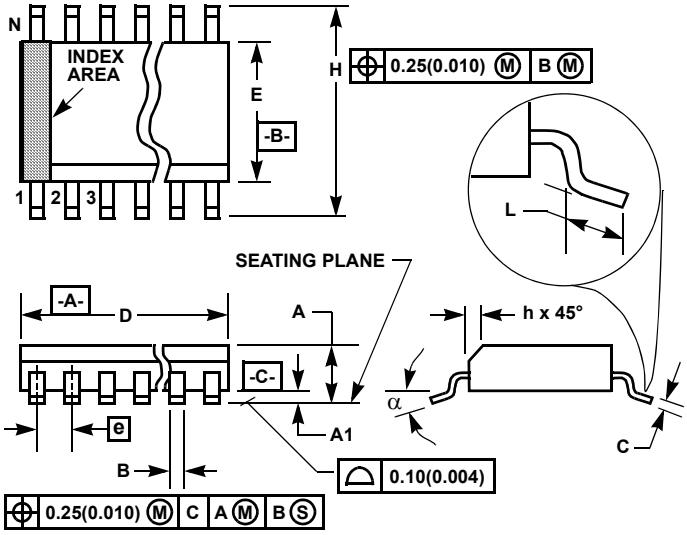
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

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