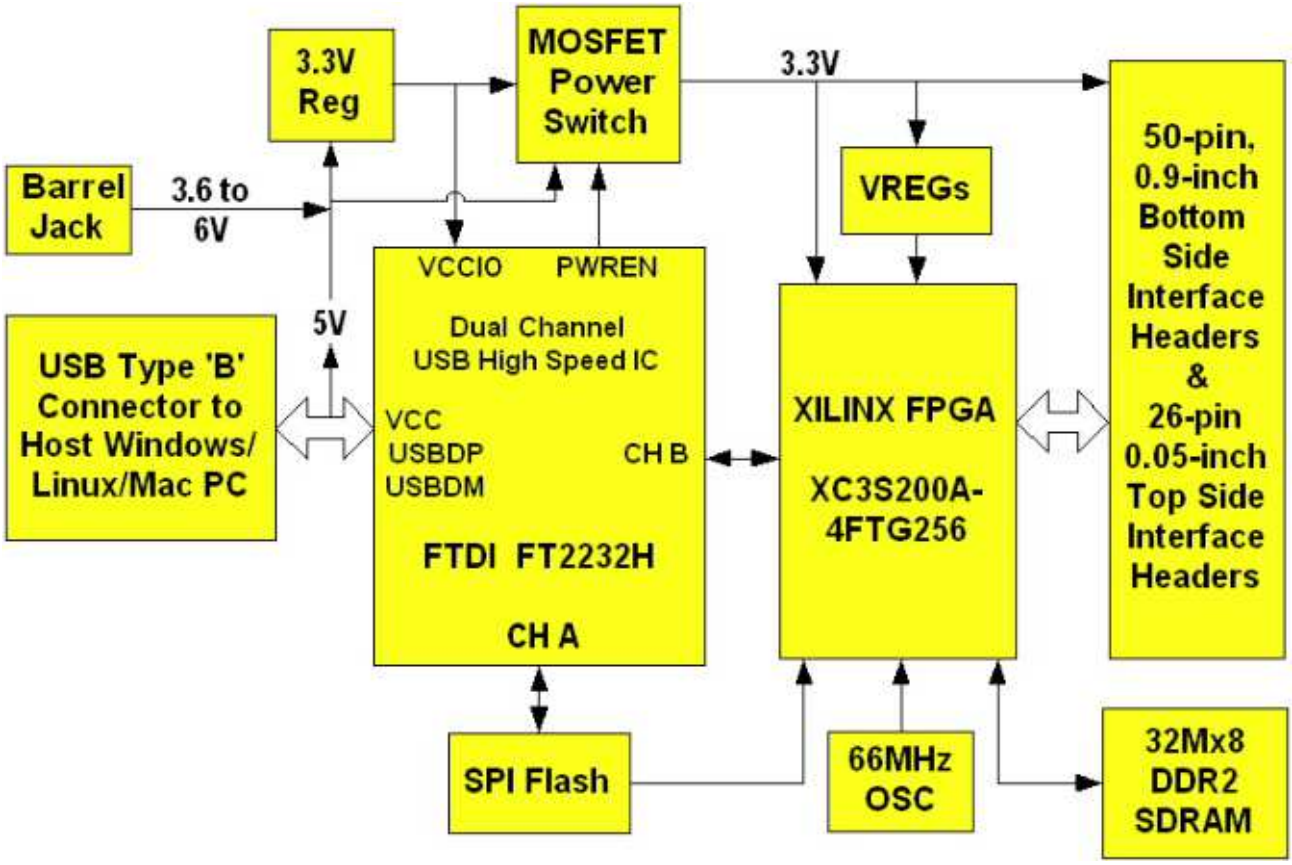


DLP-HS-FPGA-A

LEAD-FREE

USB - FPGA MODULE (PRELIMINARY)



FEATURES:

- Xilinx XC3S200A-4FTG256C FPGA
- Micron 32M x 8 DDR2 SDRAM Memory
- Built-In Configuration Loader; Writes the Bit File Directly to SPI Flash via High-Speed USB 2.0 Interface
- 63 User I/O Channels: 24 Differential Pairs and 8 Global Clocks
- 66.666 MHz Oscillator
- 133 MHz DDR2 Interface Reference Design Provided
- USB Port Powered or 5V External Power Barrel Jack
- USB 1.1 and 2.0 Compatible Interface
- Small Footprint: 3.0 x 1.2 Inch PCB and Standard 50-Pin, 0.9-Inch DIP Interface

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APPLICATIONS:

- Rapid Prototyping
- Educational Tool
- Industrial/Process Control
- Data Acquisition/Processing
- Embedded Processor

1.0 INTRODUCTION

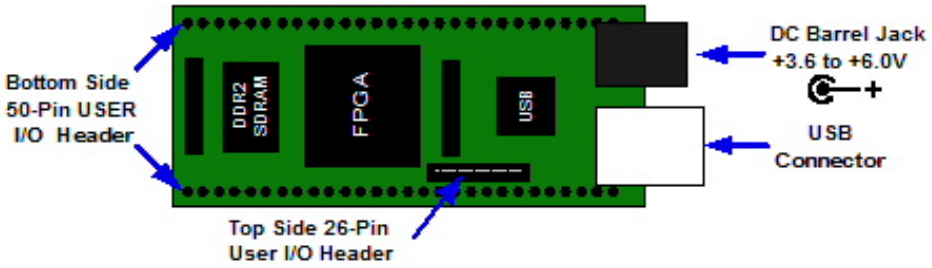
The DLP-HS-FPGA module is a low-cost, compact prototyping tool that can be used for rapid proof of concept or within educational environments. The module is based on the Xilinx Spartan™ 3A and Future Technology Devices International's FT2232H Dual-Channel High-Speed USB IC. The DLP-HS-FPGA provides both the beginner as well as the experienced engineer with a rapid path to developing FPGA-based designs. When combined with the free ISE™ WebPACK™ tools from Xilinx, this module is more than sufficient for creating anything from basic logical functions to a highly complex system controller.

As a bonus feature, one channel of the dual-channel USB interface is used to load user bit files directly to the SPI Flash—no external programmer is required. This represents a savings of as much as $200 in that no additional programming cable is required for configuring the FPGA. All that is needed to load bit files to the DLP-HS-FPGA is a Windows software utility (free with purchase), a Windows PC and a USB cable. The module can also be programmed from within the Xilinx ISE tool environment using a Xilinx programming cable (purchased separately).

The DLP-HS-FPGA is fully compatible with the free ISE™ WebPACK™ tools from Xilinx. ISE WebPACK offers the ideal development environment for FPGA designs with HDL synthesis and simulation, implementation, device fitting and JTAG programming.

The DLP-HS-FPGA has on-board voltage regulators that generate all required power supply voltages from a single 5-volt source. Power for the module can be taken from either the host USB port or from a user-supplied, external 5-volt power supply via an onboard standard barrel connector.

DLP-HS-FPGA Main Connectors



Connection to user electronics is made via a 50-pin, 0.9-inch wide, industry-standard 0.025 square inch post DIP header on the bottom of the board, and a 26-pin, 0.05-inch wide top side 2x13 header. The bottom side 50-pin header provides access to 41 of the FPGA user input/output pins. The top side header provides access to 22 of the FPGA user input/output pins. The bottom side header mates with a user-supplied standard 50-pin, 0.9-inch spaced DIP socket. The top side header mates with a user-supplied 0.05-inch spaced 2x13 connector such as the FFSD-13-D-xx.xx-01 (xx.xx = cable length) ribbon cable assembly from Samtec.

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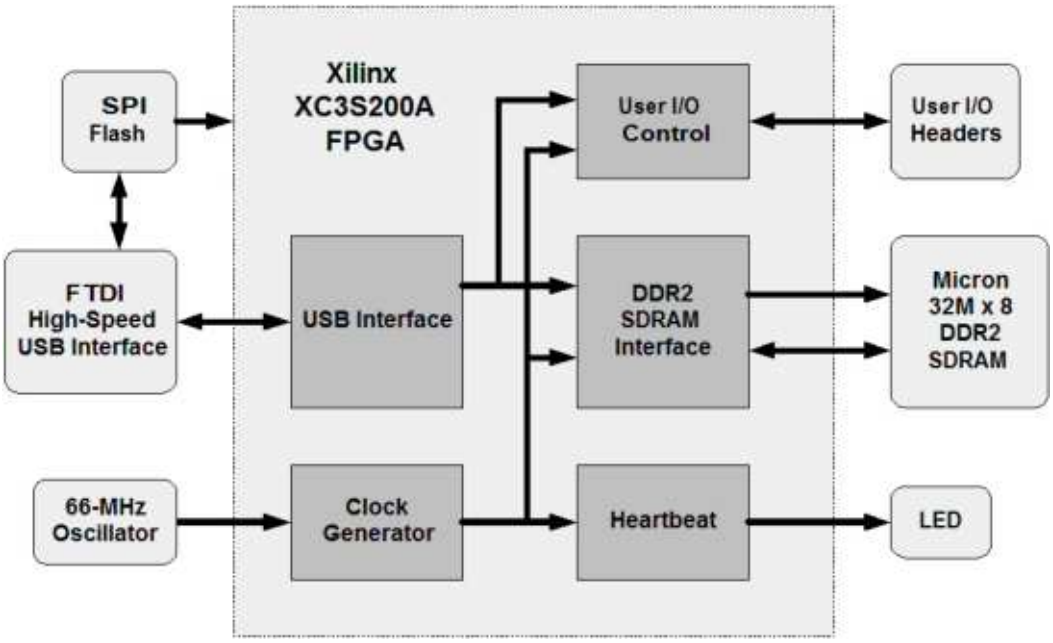
DIP Socket

Ribbon Cable 

Other on-board features include a 32M x 8 DDR2 SDRAM memory IC for user projects and both JTAG and SPI Flash interface ports for connection to Xilinx programming tools.

2.0 REFERENCE DESIGN

A 10,000-line reference design is available for the Spartan™ 3A FPGA on the DLP-HS-FPGA to those who purchase the module. The design was written in VHDL and built using the free Xilinx ISE™ WebPACK™ tools. The reference design consists of the following blocks:



It contains a USB Interface Block, a User I/0 Block, a DDR2 SDRAM interface, a Heartbeat Pulse Generator and a Clock Generator. The SPI Flash is used to store the design's FPGA configuration file.

The USB interface captures, interprets and returns command and data information sent from the host PC through the FTDI USB interface to the FPGA. Commands include Ping, Return Status, Loopback Data, Set a User I/O Pin High or Low, Read a User I/O Pin, Initialize the DDR2 SDRAM Memory and Read or Write the DDR2 SDRAM Memory. (Section 11 explains these in detail.)

The User I/O Block controls access to the 63 user I/O pins accessible through the top and bottom side headers. Every one of these pins can be either an input or an output. The User I/O Block can configure these pins as inputs and read their state, or as outputs and drive them high or low. (As a

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side note, 48 of these user I/O pins can be configured as 24 differential pairs, 8 can be configured as global clock inputs and 6 can be configured as regional clock inputs.)

The DDR2 SDRAM interface block manages the memory's initialization, the refresh cycle and the read and write access. Read and write access is available in 4-byte bursts. The traces between the DDR2 SDRAM and FPGA are matched within 10 mils to accommodate reliable data transfer at 266 Mbit/s (clocked at 133MHz). The interface creates and aligns the Data Strobes (DQS) based on an external feedback trace that matches two times the trace length between the FPGA and the DDR2 SDRAM. The Initialization, Read, and Write commands are initiated by the USB interface block and executed by the DDR2 SDRAM interface block.

The Heartbeat Pulse Generator takes the internal system clock and divides it down so that the onboard Heartbeat LED will be turned on and off for a duration of approximately one-half second.

The Clock Generator Block receives the 66.666MHz clock and produces both the 133-MHz clocks required to run the DDR2 SDRAM memory device and the 100-MHz clock for the remaining internal logic in the FPGA. It also handles reset and lock synchronization between internal DCM blocks.

The design occupies the following FPGA resources:

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	1,269	3,584	35%	
Number of 4 input LUTs	1,177	3,584	32%	
Logic Distribution				
Number of occupied Slices	1,231	1,792	68%	
Total Number of 4 input LUTs	1,249	3,584	34%	
Number of bonded IOBs				
Number of bonded	120	195	61%	
IOB Flip Flops	21			
IOB Master Pads	2			
IOB Slave Pads	2			
Number of ODDR2s used	12			
Number of BUFGMUXs	6	24	25%	
Number of DCMs	2	4	50%	
Number of RPM macros	1			

More reference designs are planned. Please contact DLP Design with any specific requests.

3.0 FPGA SPECIFICATIONS



The FPGA device used on the DLP-HS-FPGA is the Xilinx Spartan™ 3A: XC3S200A-4FTG256

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- Part Number: XC3S200A-4FTG256C
- System Gates: 200,000
- Equivalent Logic Cells: 4,032

- CLB Array:

  Rows: 32
  Columns: 16
  Total CLB's: 448
  Total Slices: 1,792
  Total Flip Flops: 3,584
  Total 4-Input LUT's: 3,584

- Distributed RAM Bits: 28K
- Block RAM Bits: 288K
- Dedicated Multipliers: 16
- DCM's: 4

The DLP-HS-FPGA was designed with pin migration in mind for the Xilinx Spartan™ 3A family FPGA's using the FTG256 package. The larger Xilinx Spartan™ 3A family FPGA that will work on the current PCB design is the XC3S400A. Contact DLP Design for details.

4.0 ABSOLUTE MAXIMUM RATINGS

Stresses above those listed here may cause permanent damage to the DLP-HS-FPGA:

Operating Temperature: 0-70°C

Voltage on Digital Inputs with Respect to Ground: -0.5V to +4.1 V

Sink/Source Current on Any I/O: 24 mA (using LVTTL as the FPGA I/O standard)

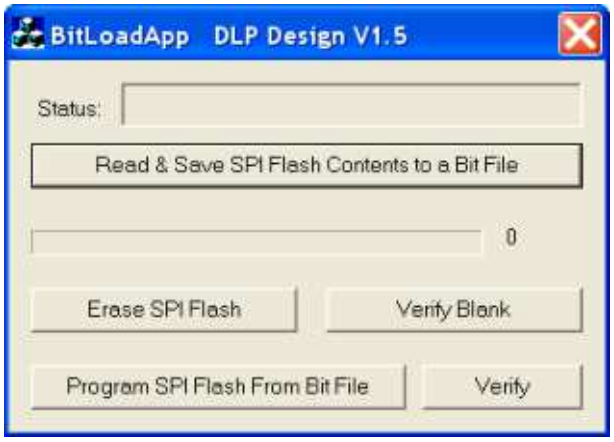
5.0 WARNINGS

- Unplug from the host PC and power adapter before connecting to I/O on the DLP-HS-FPGA.
- Isolate the bottom of the board from all conductive surfaces.
- Observe static precautions to prevent damage to the DLP-HS-FPGA module.

6.0 BITLOADAPP SOFTWARE

Windows software is provided for use with the DLP-HS-FPGA that will load an FPGA configuration (*.bit) file directly to the SPI Flash device via the USB interface. This application (illustrated below) will allow the user to erase the flash, verify the erasure and then program and verify the flash:

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7.0 JTAG INTERFACE

The easiest way to load an FPGA configuration (*.bit) file to the FPGA is to run the BitLoadApp software, then select and program a file from the local hard drive directly to the SPI Flash. Once written to the SPI Flash, the configuration will load to the FPGA and execute. Alternatively, a traditional JTAG header location is provided on the DLP-HS-FPGA giving the user access to the specific pins required by the development tools. (Refer to the schematic contained within this datasheet for details.)

8.0 EEPROM SETUP / MPROG

The DLP-HS-FPGA has a dual-channel USB interface to the host PC. Channel A is used exclusively to load an FPGA configuration (*.bit) file to the SPI Flash. This configuration data is automatically transferred to the FPGA when power is applied to the module or when the PROG Pin is driven low and then released by the application software. Channel B is used for communication between the FPGA and host PC at run time. A 93LC56B EEPROM connected to the USB interface IC is used to store the setup for the two channels. The parameters stored in the EEPROM include the Vendor ID (VID), Product ID (PID), Serial Number, Description String, driver selection (VCP or D2XX) and port type (UART serial or FIFO parallel).

As mentioned above, Channel A is used exclusively for loading the FPGA's configuration to the SPI Flash, and Channel B is used for communication between the host PC and the DLP-HS-FPGA. As such, the D2XX drivers and 245 FIFO mode must be selected in the EEPROM for Channel A. Channel B must use the 245 FIFO mode, but can use either the VCP or D2XX drivers. The VCP drivers make the DLP-HS-FPGA appear as an RS232 port to the host application. The D2XX drivers provide faster throughput, but require working with a *.lib or *.dll library in the host application.

The operational modes and other EEPROM selections are written to the EEPROM using the MPROG utility. This utility and its manual are available for download from the bottom of the page at www.dlpdesign.com.

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9.0 TEST BIT FILE

A test file is provided as a download from the DLP Design website that provides rudimentary access to the I/O features of the DLP-HS-FPGA. The following features are provided:

- Ping
- Read the High/Low State of the Input-Only Pins
- Drive I/O Pins High/Low or Read their High/Low State
- Simple Loopback on Channel B
- 4 Byte Read/Write Access of Row, Column, and Bank Address in the DDR2 SDRAM

This bit file is available from the DLP-HS-FPGA's download page. The command structure that supports these features is explained in Section 11.

10.0 USB DRIVERS

USB drivers for the following operating systems are available for download from the DLP Design website at www.dlpdesign.com:

OPERATING SYSTEM SUPPORT	
Windows Vista, Vista x64	**Mac OSX**
Windows XP, XP x64	**Mac OS9**
Windows Server 2008, x64	**Mac OS8**
Windows Server 2003, x64	**Linux**
Windows 2000	**Windows CE 4.2 – 6.0**

Notes:

1. The bit file load utility only runs on the Windows platforms.

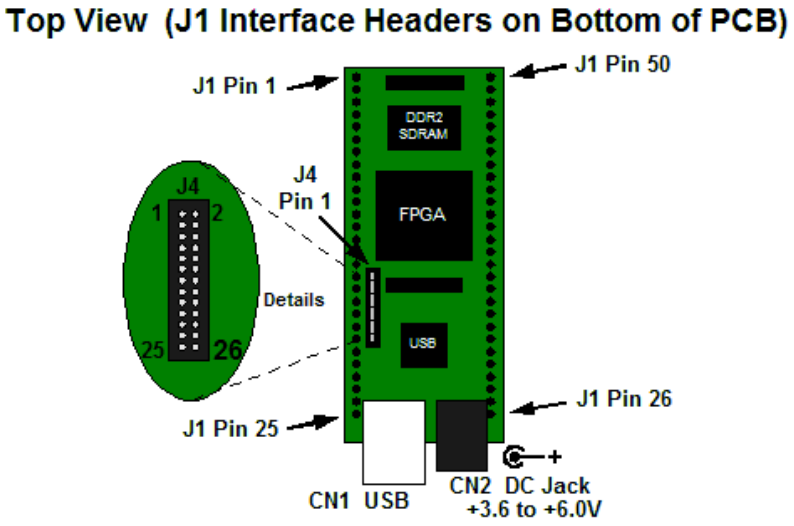
2. The bit file load utility requires the use of USB channel A, and channel A is dedicated to this function.

3. If you are utilizing the dual-mode drivers from FTDI (CDM2.x.x) and you want to use the Virtual COM Port (VCP) drivers, then it may be necessary to disable the D2XX drivers first via Device Manager. To do so, right click on the entry under USB Controllers that appears when the DLP-HS-FPGA is connected, select Properties, select the Advanced tab, check the option for "Load VCP" and click OK. Then unplug and replug the DLP-HS-FPGA, and a COM port should appear in Device Manager under Ports (COM & LPT).

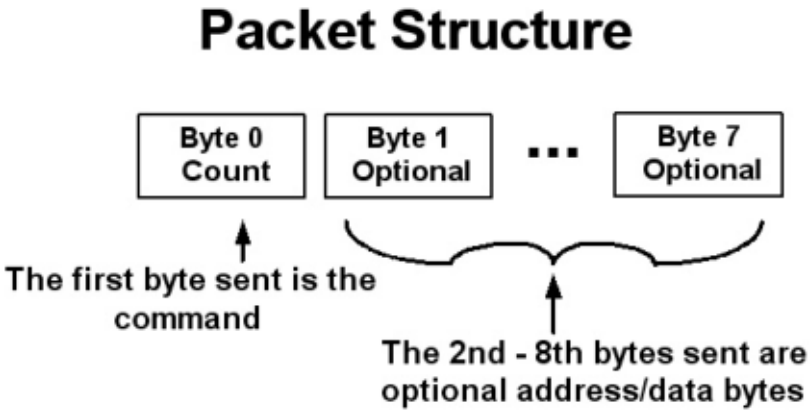
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11.0 USING THE DLP-HS-FPGA

Select a power source via Header Pins 23 and 24, and connect the DLP-HS-FPGA to the PC to initiate the loading of USB drivers. The easiest way to do this is to connect Pins 23 and 24 to each other. This will result in operational power being taken from the host PC. Once the drivers are loaded, the DLP-HS-FPGA is ready for use.



Simply connect the DLP-HS-FPGA to the PC to initiate the loading of USB drivers. Once the USB drivers are loaded, the DLP-HS-FPGA is ready for use. All commands are issued as multi-byte command packets consisting of at least two bytes.



You can either utilize the Test Application available from http://www.dlpdesign.com/test.shtml with the DLP-HS-FPGA (as described in Section 12), or you can write your own program in your language of choice.

If you are using the VCP drivers, begin by opening the COM port, and send multi-byte commands as shown in Table 1 below. There is no need to set the baud rate because the DLP-HS-FPGA uses a parallel interface between the USB IC and the FPGA. (The Ping Command can be used to locate the correct COM port used for communicating with the DLP-HS-FPGA, or you can look in Device

Manager to see which port was assigned by Windows.) If you are using the D2XX drivers as with the Test Application, no COM port selection is necessary.

TABLE 1

Command Packets

Command Packet	Description	Byte	Hex Value	Return/Comments
Ping	Issues Ping	0	0x00	Ping Command - 0x56 will be returned indicating that the DLP-HS-FPGA is found on the selected port
Read Version/ Status	Accesses the internal version/ status registers	0	0x10	Read Version/Status Registers Command
		1	0xnn	Register Address: 0xnn = 0x00 = Board ID (0x11 = Revision 1.1) 0x01 = FPGA Type ID (0x3A = Spartan™ 3A) 0x02 = Design Version ID 1 (0x09 = September) 0x03 = Design Version ID 2 (0x01 = Day) 0x04 = Design Version ID 3 (0x09 = Year) 0x05 = Design Version ID 4 (0xA1 = Version A1) 0x06 = DDR2 Status: 0x00 = Not Initialized 0x01 = Initialized
Loopback	Returns the data byte received	0	0x20	Loopback Command
		1	0xnn	The byte sent to the DLP-HS-FPGA (0xnn) will be returned back
Loopback Compliment	Returns the compliment of data byte received	0	0x21	Loopback Compliment Command
		1	0xnn	The byte sent to the DLP-HS-FPGA (0xnn) will be complimented and returned back
Read Pin	Reads the state of one of the user I/O pins	0	0x30	Read Pin Command
		1	0x00 – 0x3E	The user I/O pin numbers are described in Table 2. User I/O pin 0xnn is read and returns: 0x00 = User I/O pin 0xnn is low 0x01 = User I/O pin 0xnn is high
Clear Pin	Forces the selected user I/O pin low	0	0x40	Clear Pin Command
		1	0x00 – 0x3E	The user I/O pin numbers are described in Table 2. User I/O pin 0xnn is cleared. The specified user I/O number is returned.
Set Pin	Forces the selected user I/O pin high	0	0x41	Set Pin Command
		1	0x00 – 0x3E	The user I/O pin numbers are described in Table 2. User I/O pin 0xnn is set. The specified user I/O number is returned.
Initialize Memory	Initializes DDR2 SDRAM	0	0x70	The Initialize Memory Command configures the DDR2 SDRAM for access by the FPGA. *The memory cannot be accessed without being initialized.*

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Important Note on DDR2 SDRAM Data Access:

DDR2 SDRAM data accesses using the reference design on the DLP-HS-FPGA module are always performed **4 bytes** at a time due to the fact that the device is configured for a burst length of four. What this means is column address bits 0 and 1 only change the order of the read or write bytes, they still refer to the same 4 bytes. Therefore to increment the DDR2 SDRAM address for consecutive memory locations, the column address must be incremented by 4.

Incrementing the column address by anything less than 4 simply changes the order that the 4 bytes specified by column address 9:3 are written to the memory, or returned to the user. For example a write to a column starting address of 0, will write to column locations 0,1,2, and 3. But if the user then writes to column address 1, they will actually be writing to column locations 1,2,3, and 0, which will overwrite the previous write operation.

More details on how the DDR2 SDRAM column bits 1 and 0 function can be found in figure 4 and table 40 of the Micron™ MT47H32M8 datasheet. For details how the bank, row, and column bits are sent via USB to the memory, refer to the commands below.

Memory Read	Reads 4 bytes from the DDR SDRAM	0	0x8n	Reads 4 bytes from the DDR2 SDRAM starting with the address specified. The command byte is OR'd with the Most Significant Row Address Bit (24). n = 0 the Most Sig Row Address Bit is low (0x80) n = 1 the Most Sig Row Address Bit is high (0x81)
		1	0xah	Bits 23-16 Middle 8 bits of Row Address to be read from
		2	0xam	Bits 15-12 Lower 4 bits of Row Address to be read from Bits 11-8 Upper 4 bits Column Address to be read from
		3	0xal	Bits 7-2: Lower 6 bits of column address to be read from **NOTE:** refer to text above regarding column bits 1 and 0 (equates to 0xal bits 3-2). Bits 1-0: Bank Address to be read from **NOTE:** If the memory has not been initialized, the data returned will be invalid and the command returned will be 0xE7 indicating the error.
Memory Write	Writes 4 bytes to the DDR SDRAM	0	0x9n	Writes 4 bytes to the DDR2 SDRAM starting with the address specified. The command byte is OR'd with the Most Significant Row Address bit (24). n = 0 the Most Sig Row Address bit is low (0x90) n = 1 the most Sig Row Address bit is high (0x91)
		1	0xah	Bits 23-16 Middle 8 bits of Row Address to be written tp
		2	0xam	Bits 15-12 Lower 4 bits of Row Address to be written to Bits 11-8 Upper 4 bits Column Address to be written to
		3	0xal	Bits 7-2: Lower 6 bits of column address to be written to **NOTE:** refer to text above regarding column bits 1 and 0 (equates to 0xal bits 3-2). Bits 1-0: Bank Address to be written 10
		4	0xd0	Data Byte 0 written to Address specified
		5	0xd1	Data Byte 1 written to Address specified + 1
		6	0xd2	Data Byte 2 written to Address specified + 2
		7	0xd3	Data Byte 3 written to Address specified + 3 Returns the 4 bytes written followed by an echo back of the command and address data sent. **NOTE:** If the memory has not been initialized, the command returned will be 0xE7 indicating the error.

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The USER I/O Pin Read/Set/Clear commands I/O number mapping to the physical I/O pins on the DLP-HS-FPGA board are described in the following table:

TABLE 2				
User I/O				
I/O Number	**DLP-HS-FPGA Pin**	**XC3S200A Pin**	**XC3S200A Bank**	**FPGA Pin Configurations Available**
0x00 (0)	J1 Pin 2	D13	0	Digital Input, Output, Differential Pair 0+
0x01 (1)	J1 Pin 3	C13	0	Digital Input, Output, Differential Pair 0-
0x02 (2)	J1 Pin 4	D11	0	Digital Input, Output, Differential Pair 1-
0x03 (3)	J1 Pin 5	C12	0	Digital Input, Output, Differential Pair 1+
0x04 (4)	J1 Pin 6	C10	0	Digital Input, Output, Differential Pair 2+, Global Clock
0x05 (5)	J1 Pin 7	D9	0	Digital Input, Output, Differential Pair 2-, Global Clock
0x06 (6)	J1 Pin 8	C8	0	Digital Input, Output, Differential Pair 3+, Global Clock
0x07 (7)	J1 Pin 9	D8	0	Digital Input, Output, Differential Pair 3-, Global Clock
0x08 (8)	J1 Pin 10	A14	0	Digital Input, Output, Differential Pair 4+
0x09 (9)	J1 Pin 12	A13	0	Digital Input, Output, Differential Pair 4-
0x0A (10)	J1 Pin 13	A6	0	Digital Input, Output, Differential Pair 5+
0x0B (11)	J1 Pin 14	B6	0	Digital Input, Output, Differential Pair 5-
0x0C (12)	J1 Pin 15	C11	0	Digital Input, Output, Differential Pair 6+
0x0D (13)	J1 Pin 16	A11	0	Digital Input, Output, Differential Pair 6-
0x0E (14)	J1 Pin 17	B8	0	Digital Input, Output, Differential Pair 7-, Global Clock
0x0F (15)	J1 Pin 18	A8	0	Digital Input, Output, Differential Pair 7+, Global Clock
0x10 (16)	J1 Pin 19	C5	0	Digital Input, Output, Differential Pair 8-
0x11 (17)	J1 Pin 20	A5	0	Digital Input, Output, Differential Pair 8+
0x12 (18)	J1 Pin 21	B3	0	Digital Input, Output, Differential Pair 9-
0x13 (19)	J1 Pin 22	A3	0	Digital Input, Output, Differential Pair 9+
0x14 (20)	J1 Pin 27	F3	3	Digital Input, Output, Differential Pair 10+
0x15 (21)	J1 Pin 29	G4	3	Digital Input, Output, Differential Pair 10-
0x16 (22)	J1 Pin 30	C2	3	Digital Input, Output, Differential Pair 11+
0x17 (23)	J1 Pin 31	C1	3	Digital Input, Output, Differential Pair 11-
0x18 (24)	J1 Pin 32	E1	3	Digital Input, Output, Differential Pair 12-
0x19 (25)	J1 Pin 33	D1	3	Digital Input, Output, Differential Pair 12+
0x1A (26)	J1 Pin 34	J6	3	Digital Input, Output, Differential Pair 13-
0x1B (27)	J1 Pin 35	J4	3	Digital Input, Output, Differential Pair 13+
0x1C (28)	J1 Pin 36	H6	3	Digital Input, Output, Differential Pair 14+
0x1D (29)	J1 Pin 37	H5	3	Digital Input, Output, Differential Pair 14-
0x1E (30)	J1 Pin 38	M4	3	Digital Input, Output, Differential Pair 15-
0x1F (31)	J1 Pin 39	N3	3	Digital Input, Output, Differential Pair 15+
0x20 (32)	J1 Pin 41	E3	3	Digital Input, Output, Differential Pair 16+
0x21 (33)	J1 Pin 42	E2	3	Digital Input, Output, Differential Pair 16-
0x22 (34)	J1 Pin 43	H3	3	Digital Input, Output, Differential Pair 17+
0x23 (35)	J1 Pin 44	J3	3	Digital Input, Output, Differential Pair 17-
0x24 (36)	J1 Pin 45	K1	3	Digital Input, Output, Differential Pair 18-,

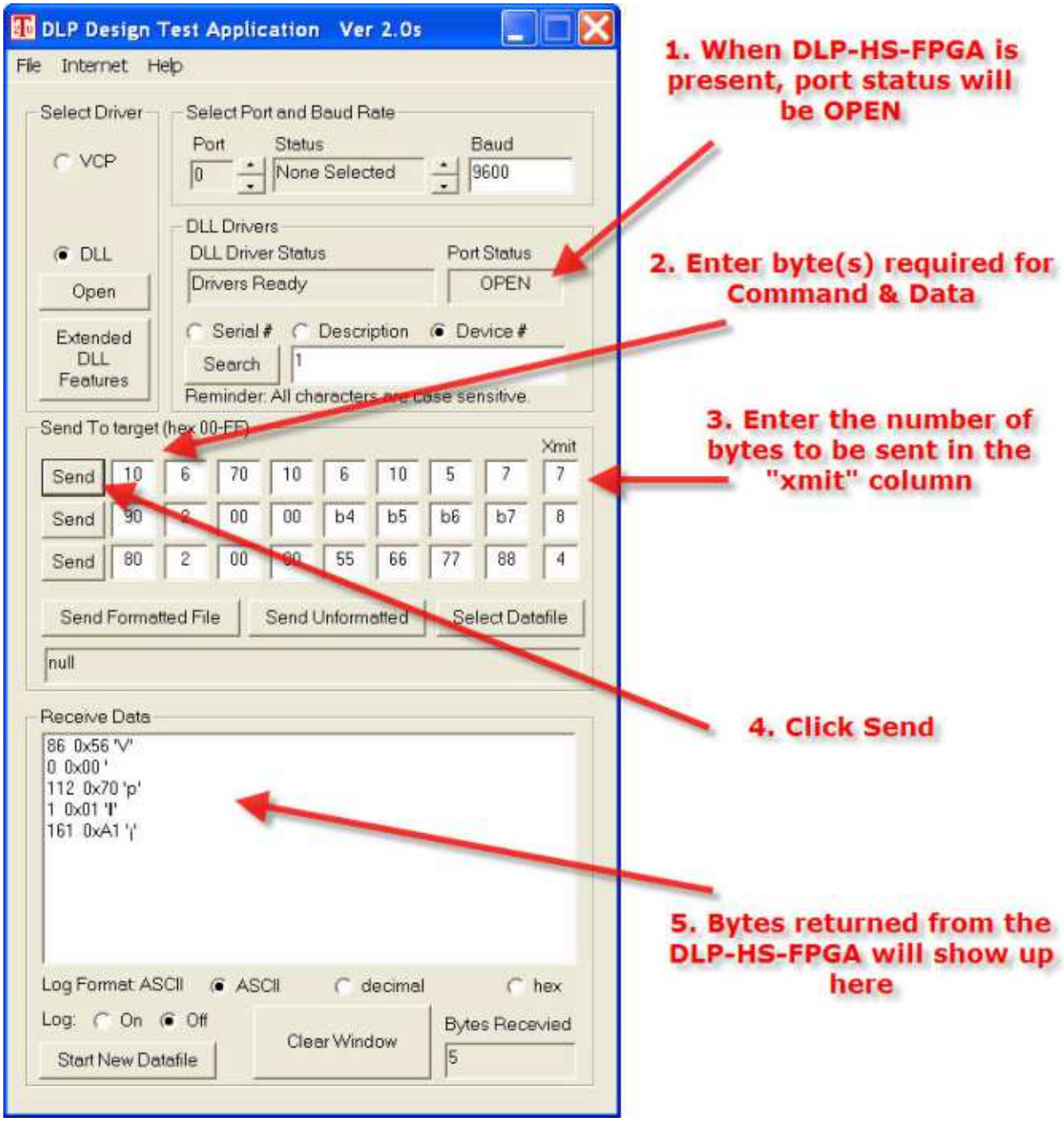
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				Regional Clock
0x25 (37)	J1 Pin 46	K3	3	Digital Input, Output, Differential Pair 18+, Regional Clock
0x26 (38)	J1 Pin 47	P1	3	Digital Input, Output, Differential Pair 19-
0x27 (39)	J1 Pin 48	N2	3	Digital Input, Output, Differential Pair 19+
0x28 (40)	J1 Pin 49	T9	2	Digital Input, Output, Global Clock
0x29 (41)	J4 Pin 1	B15	0	Digital Input, Output
0x2A (42)	J4 Pin 3	A12	0	Digital Input, Output
0x2B (43)	J4 Pin 5	B10	0	Digital Input, Output, Differential Pair 20+
0x2C (44)	J4 Pin 7	A10	0	Digital Input, Output, Differential Pair 20-
0x2D (45)	J4 Pin 9	A9	0	Digital Input, Output, Global Clock
0x2E (46)	J4 Pin 11	N1	3	Digital Input, Output
0x2F (47)	J4 Pin 13	E7	0	Digital Input, Output
0x30 (48)	J4 Pin 15	C4	0	Digital Input, Output
0x31 (49)	J4 Pin 17	C7	0	Digital Input, Output
0x32 (50)	J4 Pin 19	K4	3	Digital Input, Output
0x33 (51)	J4 Pin 21	R1	3	Digital Input, Output
0x34 (52)	J4 Pin 2	A7	0	Digital Input, Output
0x35 (53)	J4 Pin 4	A4	0	Digital Input, Output, Differential Pair 21+
0x36 (54)	J4 Pin 6	B4	0	Digital Input, Output, Differential Pair 21-
0x37 (55)	J4 Pin 8	F1	3	Digital Input, Output, Differential Pair 22+
0x38 (56)	J4 Pin 10	G1	3	Digital Input, Output, Differential Pair 22-
0x39 (57)	J4 Pin 12	H1	3	Digital Input, Output, Regional Clock
0x3A (58)	J4 Pin 14	J1	3	Digital Input, Output, Regional Clock
0x3B (59)	J4 Pin 16	L1	3	Digital Input, Output
0x3C (60)	J4 Pin 18	M1	3	Digital Input, Output
0x3D (61)	J4 Pin 20	M3	3	Digital Input, Output, Differential Pair 23+
0x3E (62)	J4 Pin 22	L4	3	Digital Input, Output, Differential Pair 23-
SUSPEND	J4 Pin 23	R16	1	Force Suspend Mode (when enabled)
AWAKE	J4 Pin 24	T11	2	Return from Suspend Mode operation
+5V IN	J1 Pin 23	-	-	+5V input to the DLP-HS-FPGA
+5V USB	J1 Pin 24	-	-	+5V supplied by host PC USB port
+3.3V OUT	J1 Pin 28, J4 Pin 26	-	-	+3.3V supplied by the onboard DLP-HS-FPGA regulator after module enumerated
GND	J1 Pin 1, J1 Pin 11, J1 Pin 25, J1 Pin 26, J1 Pin 40, J1 Pin 50, J4 Pin 25	-	-	Ground

12.0 USING THE DLP TEST APPLICATION (OPTIONAL)

Users can design their own application interface to send USB commands to the DLP-HS-FPGA module or utilize the test application tool available from DLP Design. The DLP Test Application is available in a free version for download from the DLP Design website at www.dlpdesign.com/test.shtml. Using this tool, single- and multi-byte commands can be sent to the DLP-HS-FPGA board.

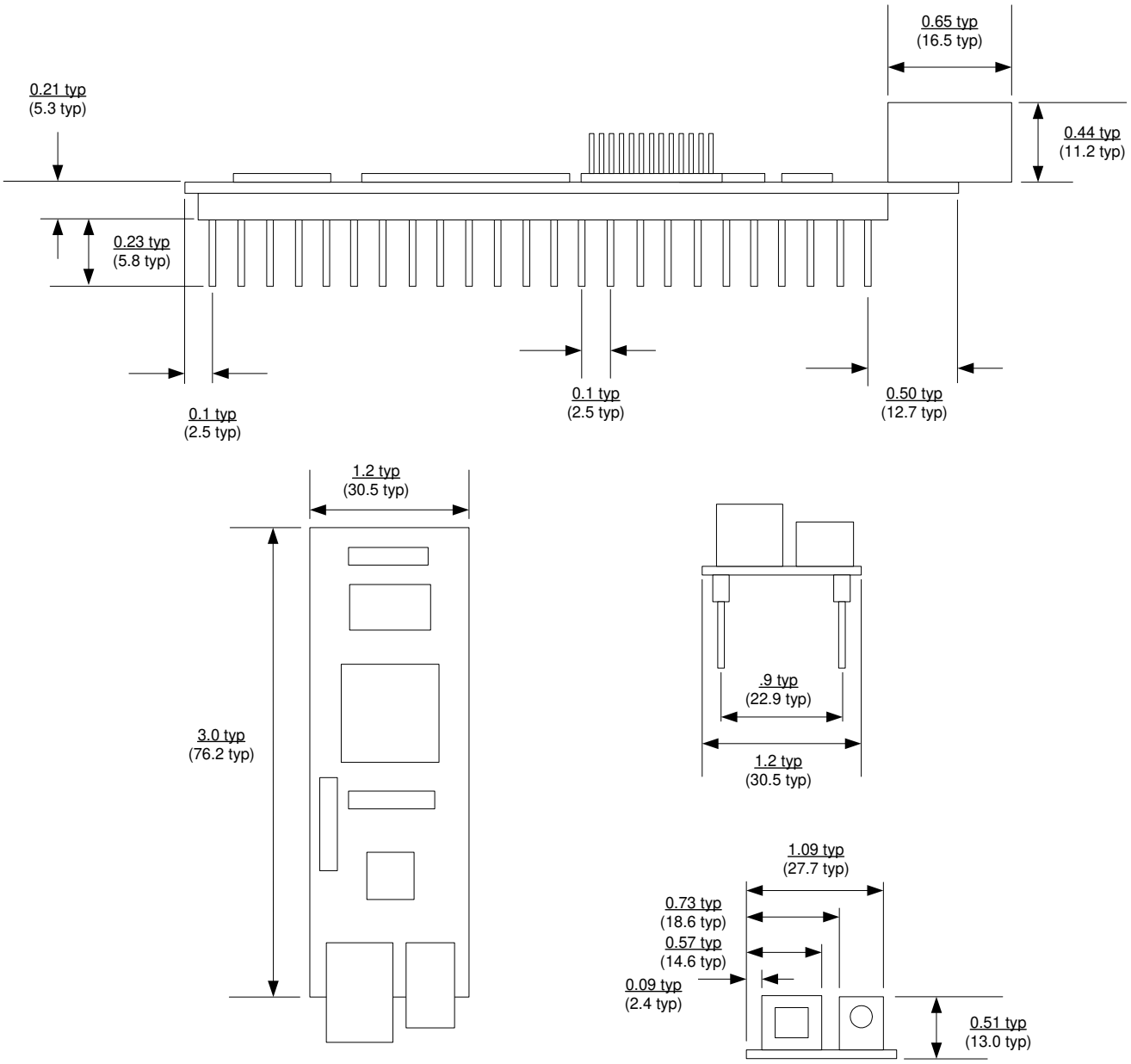
Once installed the test application is used as follows:



The commands used to interface to the DLP-HS-FPGA are detailed in Section 10 of this datasheet.

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13.0 MECHANICAL DIMENSIONS IN INCHES (MM) (PRELIMINARY)



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14.0 DISCLAIMER

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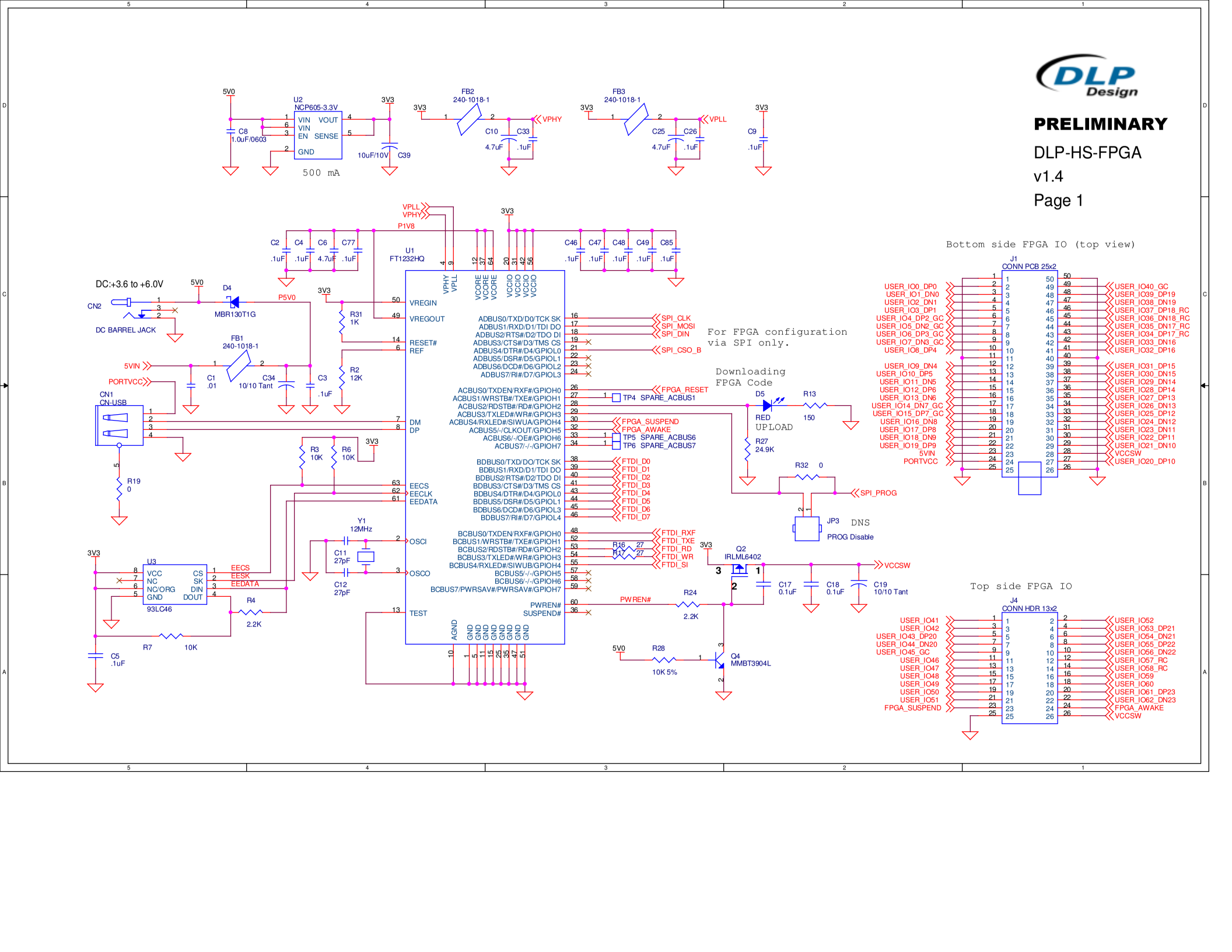
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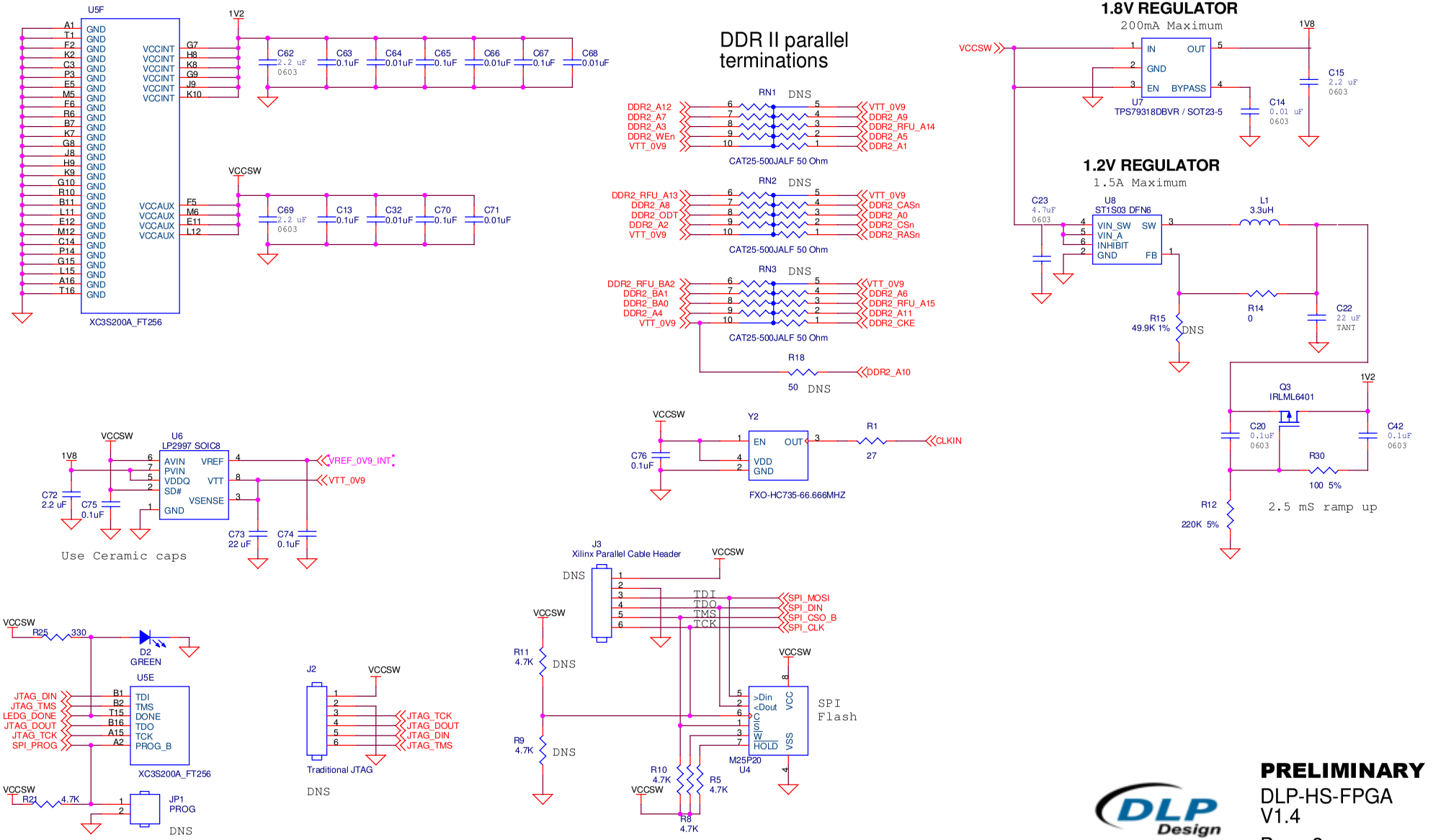
This document provides preliminary information that may be subject to change without notice.

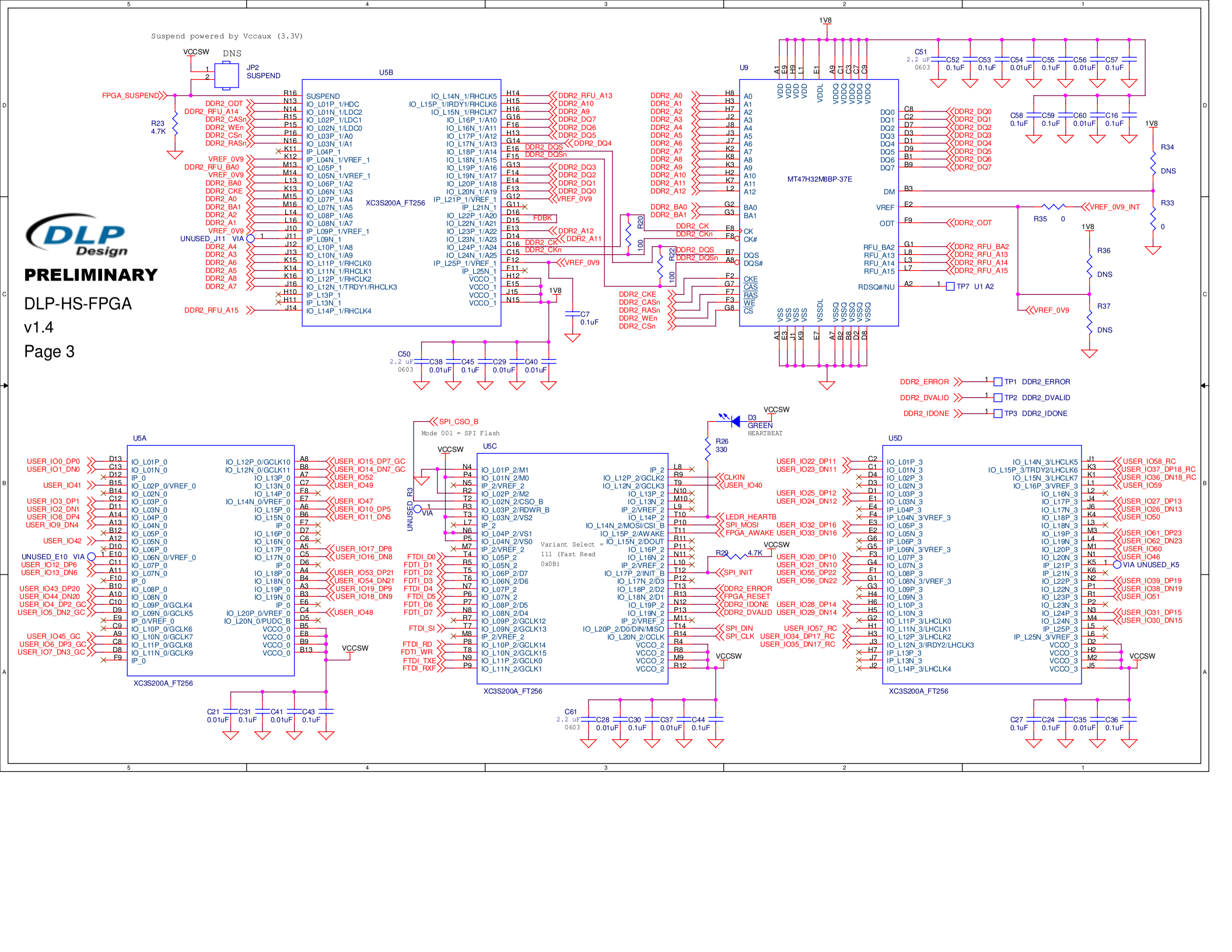
15.0 CONTACT INFORMATION

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Page 1
DC:+3.6 to +6.0V
DC BARREL JACK
MBR130T1G
500 mA
For FPGA configuration via SPI only.
Downloading FPGA Code
UPLOAD
DNS
PROG Disable
Bottom side FPGA IO (top view)
Top side FPGA IO
93LC46
FT1232HQ
CONN PCB 25x2
CONN HDR 13x2
IRLML6402
MMBT3904L


U5F
XC3S200A_FT256
1V2
VCCSW
C62 2.2 uF 0603
C63 0.1uF
C64 0.01uF
C65 0.1uF
C66 0.01uF
C67 0.1uF
C68 0.01uF
C69 2.2 uF 0603
C13 0.1uF
C32 0.01uF
C70 0.1uF
C71 0.01uF
DDR II parallel terminations
RN1 DNS
DDR2_A12
DDR2_A7
DDR2_A3
DDR2_WEn
VTT_0V9
DDR2_A9
DDR2_RFU_A14
DDR2_A5
DDR2_A1
CAT25-500JALF 50 Ohm
RN2 DNS
DDR2_RFU_A13
DDR2_A8
DDR2_ODT
DDR2_A2
DDR2_CASn
DDR2_A0
DDR2_CSn
DDR2_RASn
CAT25-500JALF 50 Ohm
RN3 DNS
DDR2_RFU_BA2
DDR2_BA1
DDR2_BA0
DDR2_A4
DDR2_A6
DDR2_RFU_A15
DDR2_A11
DDR2_CKE
CAT25-500JALF 50 Ohm
R18
50 DNS
DDR2_A10
1.8V REGULATOR
200mA Maximum
U7
TPS79318DBVR / SOT23-5
IN
GND
EN
OUT
BYPASS
1V8
C15 2.2 uF 0603
C14 0.01 uF 0603
1.2V REGULATOR
1.5A Maximum
C23 4.7uF 0603
U8
ST1S03 DFN6
VIN_SW
VIN_A
INHIBIT
GND
SW
FB
L1 3.3uH
R15 49.9K 1%
DNS
R14 0
C22 22 uF TANT
Q3
IRLML6401
C20 0.1uF 0603
C42 0.1uF 0603
R30 100 5%
R12 220K 5%
2.5 mS ramp up
U6
LP2997 SOIC8
AVIN
PVIN
VDDQ
SD#
GND
VREF
VTT
VSENSE
VREF_0V9_INT
VTT_0V9
C72 2.2 uF
C75 0.1uF
C73 22 uF
C74 0.1uF
Use Ceramic caps
Y2
EN
VDD
GND
OUT
R1 27
CLKIN
C76 0.1uF
FXO-HC735-66.666MHZ
R25 330
D2 GREEN
U5E
TDI
TMS
DONE
TDO
TCK
PROG_B
JTAG_DIN
JTAG_TMS
LEDG_DONE
JTAG_DOUT
JTAG_TCK
SPI_PROG
XC3S200A_FT256
R21 4.7K
JP1 PROG
DNS
J2
Traditional JTAG
DNS
J3
Xilinx Parallel Cable Header
DNS
TDI
TDO
TMS
TCK
SPI_MOSI
SPI_DIN
SPI_CSO_B
SPI_CLK
R11 4.7K
DNS
R9 4.7K
DNS
M25P20
U4
>Din
<Dout
C
S
W
HOLD
VCC
VSS
SPI Flash
R10 4.7K
R5 4.7K
R8 4.7K
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Suspend powered by Vccaux (3.3V)
VCCSW
DNS
JP2
SUSPEND
FPGA_SUSPEND
R23
4.7K
U5B
XC3S200A_FT256
SUSPEND
DDR2_ODT
DDR2_RFU_A14
DDR2_CASn
DDR2_WEn
DDR2_CSn
DDR2_RASn
VREF_0V9
DDR2_RFU_BA0
VREF_0V9
DDR2_BA0
DDR2_CKE
DDR2_A0
DDR2_BA1
DDR2_A2
DDR2_A1
VREF_0V9
UNUSED_J11 VIA
DDR2_A4
DDR2_A3
DDR2_A6
DDR2_A5
DDR2_A8
DDR2_A7
DDR2_RFU_A15
DDR2_RFU_A13
DDR2_A10
DDR2_A9
DDR2_DQ7
DDR2_DQ6
DDR2_DQ5
DDR2_DQ4
DDR2_DQS
DDR2_DQSn
DDR2_DQ3
DDR2_DQ2
DDR2_DQ1
DDR2_DQ0
VREF_0V9
FDBK
DDR2_A12
DDR2_A11
DDR2_CK
DDR2_CKn
VREF_0V9
1V8
C7
0.1uF
C50
2.2 uF
0603
C38
0.01uF
C45
0.1uF
C29
0.01uF
C40
0.01uF
R20
100
R22
100
U9
MT47H32M8BP-37E
DDR2_A0
DDR2_A1
DDR2_A2
DDR2_A3
DDR2_A4
DDR2_A5
DDR2_A6
DDR2_A7
DDR2_A8
DDR2_A9
DDR2_A10
DDR2_A11
DDR2_A12
DDR2_BA0
DDR2_BA1
DDR2_CK
DDR2_CKn
DDR2_DQS
DDR2_DQSn
DDR2_CKE
DDR2_CASn
DDR2_RASn
DDR2_WEn
DDR2_CSn
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DM
VREF
ODT
RFU_BA2
RFU_A13
RFU_A14
RFU_A15
RDSQ#/NU
C51
2.2 uF
0603
C52
0.1uF
C53
0.1uF
C54
0.01uF
C55
0.1uF
C56
0.01uF
C57
0.1uF
C58
0.1uF
C59
0.1uF
C60
0.01uF
C16
0.1uF
1V8
R34
DNS
R33
0
R35
0
VREF_0V9_INT
R36
DNS
R37
DNS
VREF_0V9
TP7 U1 A2
DDR2_ERROR
DDR2_DVALID
DDR2_IDONE
TP1 DDR2_ERROR
TP2 DDR2_DVALID
TP3 DDR2_IDONE
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Page 3
U5A
XC3S200A_FT256
USER_IO0_DP0
USER_IO1_DN0
USER_IO41
USER_IO3_DP1
USER_IO2_DN1
USER_IO8_DP4
USER_IO9_DN4
USER_IO42
UNUSED_E10 VIA
USER_IO12_DP6
USER_IO13_DN6
USER_IO43_DP20
USER_IO44_DN20
USER_IO4_DP2_GC
USER_IO5_DN2_GC
USER_IO45_GC
USER_IO6_DP3_GC
USER_IO7_DN3_GC
USER_IO15_DP7_GC
USER_IO14_DN7_GC
USER_IO52
USER_IO49
USER_IO47
USER_IO10_DP5
USER_IO11_DN5
USER_IO17_DP8
USER_IO16_DN8
USER_IO53_DP21
USER_IO54_DN21
USER_IO19_DP9
USER_IO18_DN9
USER_IO48
VCCSW
C21
0.01uF
C31
0.1uF
C41
0.01uF
C43
0.1uF
SPI_CSO_B
Mode 001 = SPI Flash
VCCSW
U5C
XC3S200A_FT256
UNUSED_R3
VIA
FTDI_D0
FTDI_D1
FTDI_D2
FTDI_D3
FTDI_D4
FTDI_D5
FTDI_D6
FTDI_D7
FTDI_SI
FTDI_RD
FTDI_WR
FTDI_TXE
FTDI_RXF
Variant Select = 111 (Fast Read 0x0B)
VCCSW
D3
GREEN
HEARTBEAT
R26
330
CLKIN
USER_IO40
LEDR_HEARTB
SPI_MOSI
FPGA_AWAKE
R29
4.7K
SPI_INIT
DDR2_ERROR
FPGA_RESET
DDR2_IDONE
DDR2_DVALID
SPI_DIN
SPI_CLK
VCCSW
C61
2.2 uF
0603
C28
0.01uF
C30
0.1uF
C37
0.01uF
C44
0.1uF
U5D
XC3S200A_FT256
USER_IO22_DP11
USER_IO23_DN11
USER_IO25_DP12
USER_IO24_DN12
USER_IO32_DP16
USER_IO33_DN16
USER_IO20_DP10
USER_IO21_DN10
USER_IO55_DP22
USER_IO56_DN22
USER_IO28_DP14
USER_IO29_DN14
USER_IO57_RC
USER_IO34_DP17_RC
USER_IO35_DN17_RC
USER_IO58_RC
USER_IO37_DP18_RC
USER_IO36_DN18_RC
USER_IO59
USER_IO27_DP13
USER_IO26_DN13
USER_IO50
USER_IO61_DP23
USER_IO62_DN23
USER_IO60
USER_IO46
VIA UNUSED_K5
USER_IO39_DP19
USER_IO38_DN19
USER_IO51
USER_IO31_DP15
USER_IO30_DN15
VCCSW
C27
0.1uF
C24
0.1uF
C35
0.01uF
C36
0.1uF