FAIRCHILD SEMICONDUCTOR™

January 1992
Revised June 1999

DM96S02
Dual Retriggerable Resettable Monostable Multivibrator

General Description

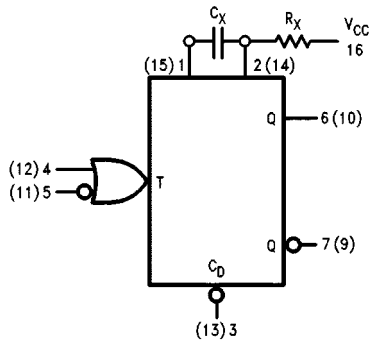
The DM96S02 is a dual retriggerable and resettable monostable multivibrator. This one-shot provides exceptionally wide delay range, pulse width stability, predictable accuracy and immunity to noise. The pulse width is set by an external resistor and capacitor. Resistor values up to 2.0 MΩ for the DM96S02 reduce required capacitor values. Hysteresis is provided on the positive trigger input of the DM96S02 for increased noise immunity.

Order Code:

Order Number	Package Number	Package Description
DM96S02M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM96S02N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

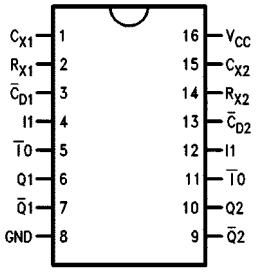
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram



V_{CC} = Pin 16
GND = Pin 8

Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{I}0$	Trigger Input (Active Falling Edge)
I1	Schmitt Trigger Input (Active Rising-Edge)
$\overline{C}_D$	Direct Clear Input (Active-LOW)
Q1 - 2	True Pulse Output
$\overline{Q}1$ - 2	Complementary Pulse Output
$C_{X1, 2}$	External Capacitor Connection
$R_{X1,2}$	External Resistor Connection

Triggering Truth Table

Pin Number			Operation
5(11)	4(12)	3(13)	
H → L	L	H	Trigger
H	L → H	H	Trigger
X	X	L	Reset

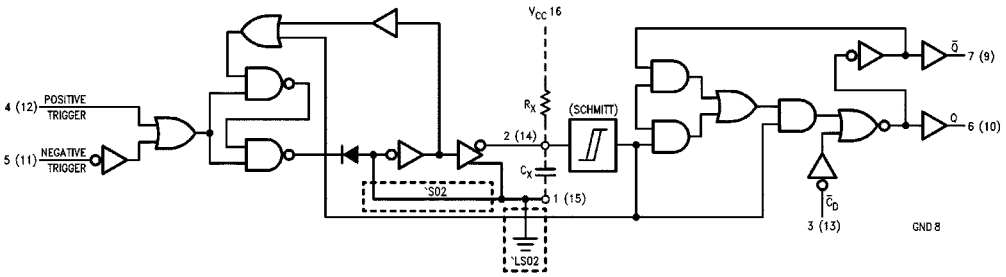
H = HIGH Voltage Level ≥ V_{IH}
L = LOW Voltage Level ≤ V_{IL}
X = Immaterial (either H or L)
H → L = HIGH-to-LOW Voltage Level transition
L → H = LOW-to-HIGH Voltage Level transition

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Functional Description

The 96S02 dual retriggerable resettable monostable multivibrator has tow DC coupled trigger inputs per function, one active LOW ($\overline{I0}$) and one active HIGH (I1). The I1 input utilizes an internal Schmitt trigger with hysteresis of 0.3V to provide increased noise immunity. The use of active HIGH and LOW inputs allows wither rising or falling edge triggering and optional non-retriggerable operation. The inputs are DC coupled making triggering independent of input transition times. When input conditions for triggering are met the Q output goes HIGH and the external capacitor is rapidly discharged and then allowed to recharge. An input trigger which occurs during the timing cycle will retrigger the circuit and result in Q remaining HIGH. The output pulse may be terminated (Q to the LOW state) at any time by setting the Direct Clear input LOW. Retriggering may be inhibited by tying the $\overline{Q}$ output to $\overline{I0}$ or the Q output to I1. Differential sensing techniques are used to obtain excellent stability over temperature and power supply variations and a feedback Darlington capacitor discharge circuit minimizes pulse width variation from unit to unit. Schottky TTL output stages provide high switching speeds and output compatibility with all TTL logic families.

Block Diagram



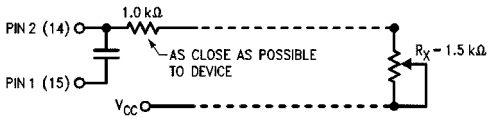
Operation Notes

TIMING

1. An external resistor (R_X) and an external capacitor (C_X) are required as shown in the Logic Diagram. The value of R_X may vary from 1.0 kΩ to 2.0 MΩ (DM96S02).
2. The value of C_X may vary from 0 to any necessary value available. If however, the capacitor has significant leakage relative to V_{CC}/R_X the timing equations may not represent the pulse width obtained.
3. Polarized capacitors may be used directly. The (+) terminal of a polarized capacitor is connected to pin 1(15), the (–) terminal to pin 2(14) and R_X. Pin 1(15) will remain positive with respect to pin 2(14) during the timing cycle. However, during quiescent (non-triggered) conditions, pin 1(15) may go negative with respect to pin 2(14) depending on values of R_X and V_{CC}. for values of $R_X \geq 10$ kΩ the maximum amount of capacitor reverse polarity, pin 1(15) negative with respect to pin 2(14) is 500 mV. Most tantalum electrolytic capacitors are rated for safe reverse bias operation up to 5% of their working forward voltage rating; therefore, capacitors having a rating of 10 WVdc or higher should be used with the DM96S02 when $R_X \geq 10$ kΩ.
4. The output pulse width t_W for $R_X \geq 10$ kΩ and $C_X \geq 1000$ pF is determined as follows:

   $t_W = 0.55\ R_X C_X$

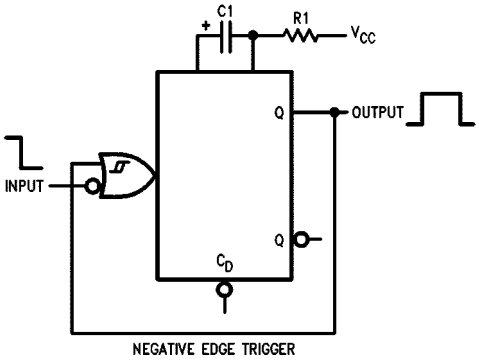
   Where R_X is in kΩ, C_X is in pF, t is in ns *or* RT_X is in kΩ, CX is in μF, t is in ms.
5. The output pulse width for $R_X < 10$ kΩ or $C_X < 1000$ pF should be determined from pulse width versus C_X or R_X graphs.
6. To obtain variable pulse width by remote trimming, the following circuit is recommended:



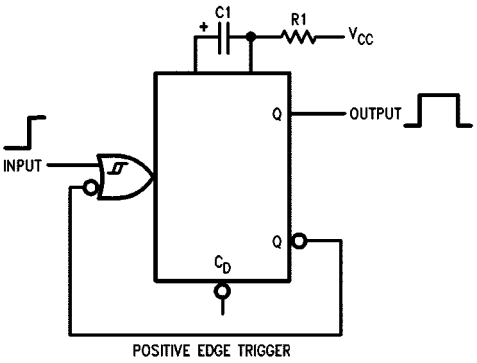
7. Under any operating condition, C_X and R_X (Min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
8. V_{CC} and ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and ground leads do not cause interaction between one shots. Use of a 0.01 μF to 0.1μF bypass capacitor between V_{CC} and ground located near the circuit is recommended.

TRIGGERING

1. The minimum negative pulse width into $\overline{I0}$ is 8.0 ns; the minimum positive pulse width into I1 is 12 ns.
2. Input signals to the DM96S02 exhibiting slow or noisy transitions should use the positive trigger input I1 which contains a Schmitt trigger.
3. When non-retriggerable operation is required, i.e., when input triggers are to be ignored during quasi-stable state, input latching is used to inhibit retriggering.
4. An overriding active LOW level direct clear is provided on each multivibrator. By applying a LOW to the clear, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW. A LOW-to-HIGH transition on $\overline{C}_D$ will not trigger the DM96S02. If the $\overline{C}_D$ input goes HIGH coincident with a trigger transition, the circuit will respond to the trigger.



NEGATIVE EDGE TRIGGER



POSITIVE EDGE TRIGGER

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Conditions		Min	Nom	Max	Units
V_{CC}	Supply Voltage			4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage			2			V
V_{IL}	LOW Level Input Voltage					0.8	V
I_{OH}	HIGH Level Output Current					−1	mA
I_{OL}	LOW Level Output Current					20	mA
T_A	Free Air Operating Temperature			0		70	°C
V_{T+}	Positive-Going Threshold Voltage, $\overline{I}_0$, I_1	V_{CC} = 5.0V				2.0	V
V_{T-}	Negative-Going Threshold Voltage, $\overline{I}_0$, I_1	V_{CC} = 5.0V		0.8			V
V_{CX}	Capacitor Voltage	V_{CC} = 4.75V	R_X = 1.0 kΩ,	−0.85		3.0	
	Pin 1 (15) Referenced	to 5.25V	$R_X \geq$ 10 kΩ	−0.5		3.0	V
	to Pin 2 (14)		$R_X >$ 1.0 MΩ	−0.4		3.0	

DC Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = −1.0 mA, V_{IL} = Max	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.0	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−40		−100	mA
I_{CC}	Supply Current	V_{CC} = Max			75	mA

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

AC Electrical Characteristics

V_{CC} = +5.0, T_A = +25°C (See Section for Waveforms and Load Configurations)

Symbol	Parameter	Conditions	C_L = 16 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay $\overline{I}0$ to Q	Figure 1		15	ns
t_{PHL}	Propagation Delay $\overline{I}0$ to $\overline{Q}$			19	ns
t_{PLH}	Propagation Delay I1 to Q			19	ns
t_{PHL}	Propagation Delay I1 to $\overline{Q}$			20	ns
t_{PHL}	Propagation Delay $\overline{C}_D$ to Q			20	ns
t_{PLH}	Propagation Delay $\overline{C}_D$ to $\overline{Q}$			14	ns
t_W(L)	$\overline{I}0$ Pulse Width LOW		8.0		ns
t_W(H)	I1 Pulse Width HIGH		12		ns
t_W(L)	C_D Pulse Width LOW		7.0		ns
t_W(H)	Minimum Q Pulse Width HIGH	R_X = 1.0 kΩ, C_X = 10 pF Including Jig and Stray	30	45	ns
t_W	Q Pulse Width	R_X = 10 kΩ, C_X = 1000 pF	5.2	5.8	µs
R_X	Timing Resistor Range (Note 3)	T_A = −55°C to + 125°C V_{CC} = 4.5V to 5.5V	1.0	2000	kΩ
$t\Delta_t$	Change in Q Pulse Width over Temperature	R_X = 10 kΩ, CX = 1000 pF		1.0	%
$t\Delta_t$	Change in Q Pulse Width over V_{CC} Range	T_A = 25°C, V_{CC} = 4.75V to 5.25V, R_X = 10 kΩ, C_X = 1000 pF T_A = 25°C, V_{CC} = 4.5 to 5.5V, R_X = 10 kΩ, C_X = 1000 pF		1.0	%

Note 3: Applies only over V_{CC} and T_X range for DM96S02.

Note 4: All Typicals are at V_{CC} = 5V, T_A = 25°C

Switching Waveforms

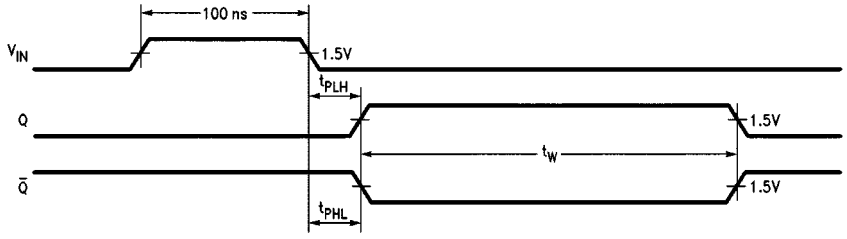
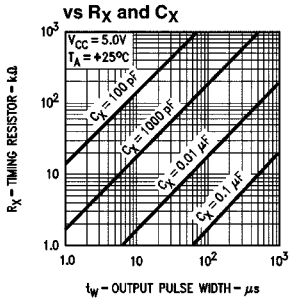


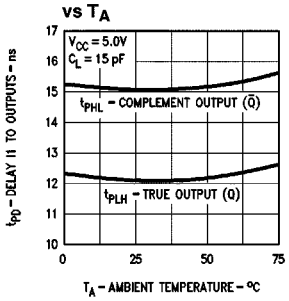
FIGURE 1.

Typical Performance Characteristics

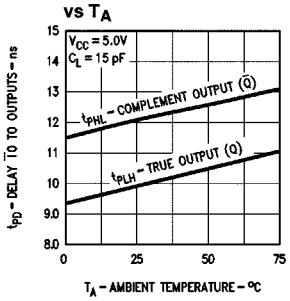
Output t_w vs R_X and C_X



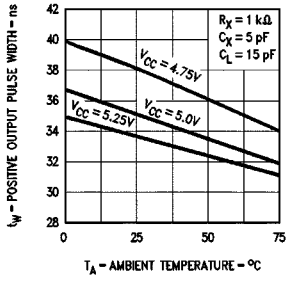
I1 Delay Time vs T_A



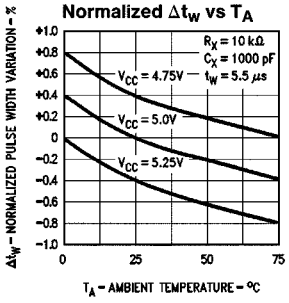
$\overline{I}$0 Delay Time vs T_A



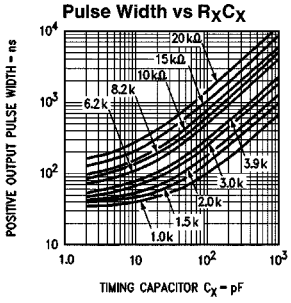
Output t_w vs T_A



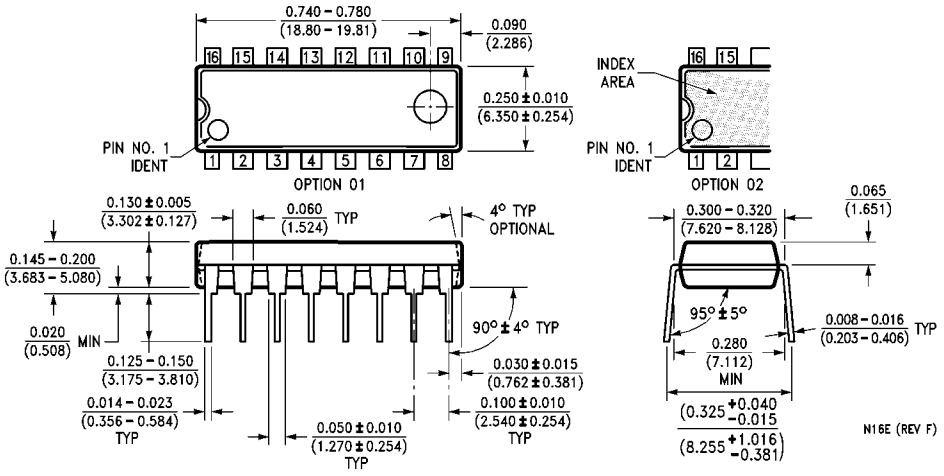
Normalized Δt_w vs T_A



Pulse Width vs R_XC_X



Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E

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