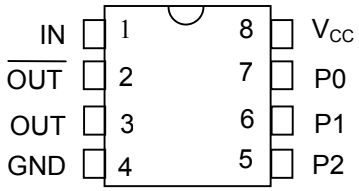
DS1040
Programmable One-Shot Pulse Generator

www.dalsemi.com

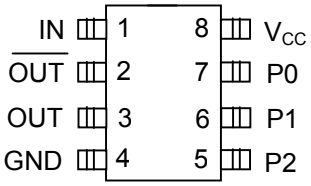
FEATURES

- All-silicon pulse width generator
- Five programmable widths
- Equal and unequal increments available
- Pulse widths from 5 ns to 500 ns
- Widths are stable and precise
- Rising edge-triggered
- Inverted and non-inverted outputs
- Width tolerance ±5% or ±2 ns, whichever is greater
- Economical
- Auto-insertable, low profile
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom widths available
- Fast turn prototypes
- Extended temperature range available

PIN ASSIGNMENT



DS1040M 8-Pin DIP (300-mil)
See Mech. Drawings Section



DS1040Z 8-Pin SOIC (150-mil)
See Mech. Drawings Section

PIN DESCRIPTION

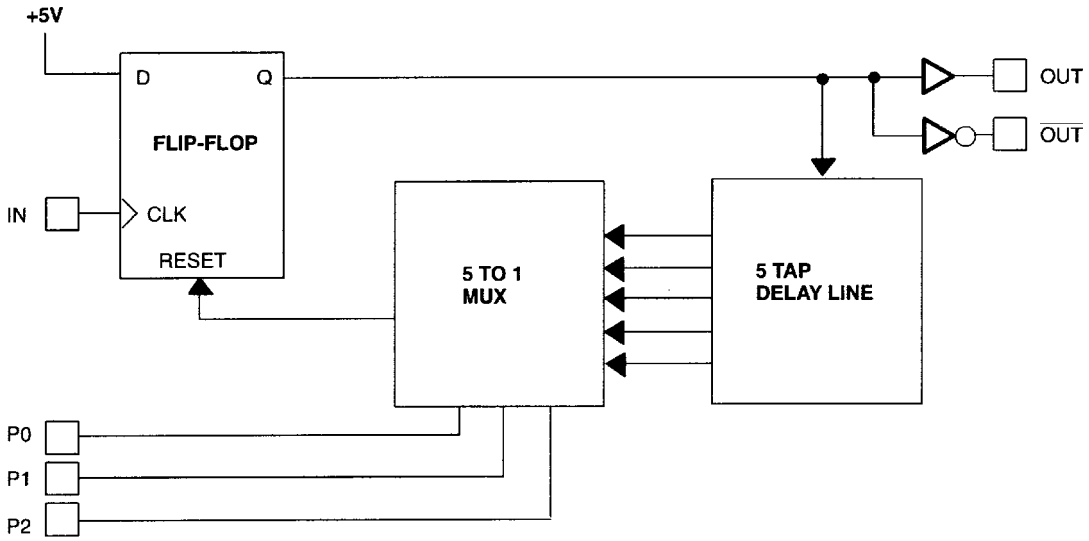
IN	– Trigger Input
P0-P2	– Programming Pins
GND	– Ground
OUT	– Pulse Output
$\overline{OUT}$	– Inverted Pulse Output
V_{CC}	– +5V

DESCRIPTION

The DS1040 Pulse Generator is a user-programmable one-shot with a choice of five precise pulse widths. Maximum widths range from 50 ns to 500 ns; increments range from 2.5 ns to 100 ns. For maximum flexibility in applications such as magneto-optical read/write disk laser power control, varieties are offered with equal and unequal increments. The DS1040 is offered in standard 8-pin DIPs and 8-pin mini-SOICs. Low cost and superior reliability over hybrid technology are achieved by the combination of a 100% CMOS silicon design and industry standard packaging. The DS1040 series of pulse generators provide a nominal width accuracy of ±5% or ±2 ns, whichever is greater. In response to the rising edge of the input (trigger) pulse, the DS1040 produces an output pulse with a width determined by the logic states of the three parallel programming pins. For convenience, both inverting and non-inverting outputs are supplied. The intrinsic delay between the trigger pulse and the output pulse is no more than 10 ns. Each output is capable of driving up to five 74LS loads.

Dallas Semiconductor can customize standard products to meet special needs. For special request and rapid delivery, call (972) 371–4348.

LOGIC DIAGRAM Figure 1



PULSE WIDTH VS. PROGRAMMED VALUE Table 1

	PROGRAMMING PINS	MAX WIDTH	MIN WIDTH →				MAX WIDTH	MAX WIDTH	MAX WIDTH
	MSB P2	0	0	0	0	1	1	1	1
	P1	0	0	1	1	0	0	1	1
	LSB P0	0	1	0	1	0	1	0	1
PART NUMBER									
DS1040-75		75	15	30	45	60	75	75	75
DS1040-100		100	20	40	60	80	100	100	100
DS1040-150		150	30	60	90	120	150	150	150
DS1040-200		200	40	80	120	160	200	200	200
DS1040-250		250	50	100	150	200	250	250	250
DS1040-500		500	100	200	300	400	500	500	500
DS1040-B50		50	30	35	40	45	50	50	50
DS1040-D60		60	20	30	40	50	60	60	60
DS1040-A15		15	5	7.5	10	12.5	15	15	15
DS1040-A20		20	10	12.5	15	17.5	20	20	20
DS1040-A32		32.5	22.5	25	27.5	30	32.5	32.5	32.5
DS1040-B40		40	20	25	30	35	40	40	40
DS1040-D70		70	30	40	50	60	70	70	70

All times in nanoseconds.
Custom pulse widths available.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	TEST	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC} + 0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0 \le V_I \le V_{CC}$	-1.0		1.0	µA	
Active Current	I_{CC}	V_{CC} = Max; Period = Min		35	75	mA	2, 6
High Level Output Current	I_{OH}	V_{CC} = Min V_{OH} = 4			-1	mA	
Low Level Output Current	I_{OL}	V_{CC} = Min V_{OL} = 0.5	8			mA	

AC ELECTRICAL CHARACTERISTICS

(T_A = 25°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Programming Setup	t_{PS}	5			ns	
Programming Hold	t_{PH}	0			ns	
Input Pulse Width at Logic 1	t_{WIH}	5			ns	
Input Pulse Width at Logic 0	t_{WIL}	5			ns	
Intrinsic Delay	t_D	0	5	10	ns	
Output Pulse Width	t_{WO}		Table 1		ns	3, 4, 5, 7
Power-up Time	t_{PU}			100	ms	
Period	Period	t_{WO} + 50			ns	

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

NOTES:

1. All voltages are referenced to ground.

2. Measured with outputs open, minimum period.

3. V_{CC} = 5V @ 25°C. Width accurate to within ±2 ns or 5%.

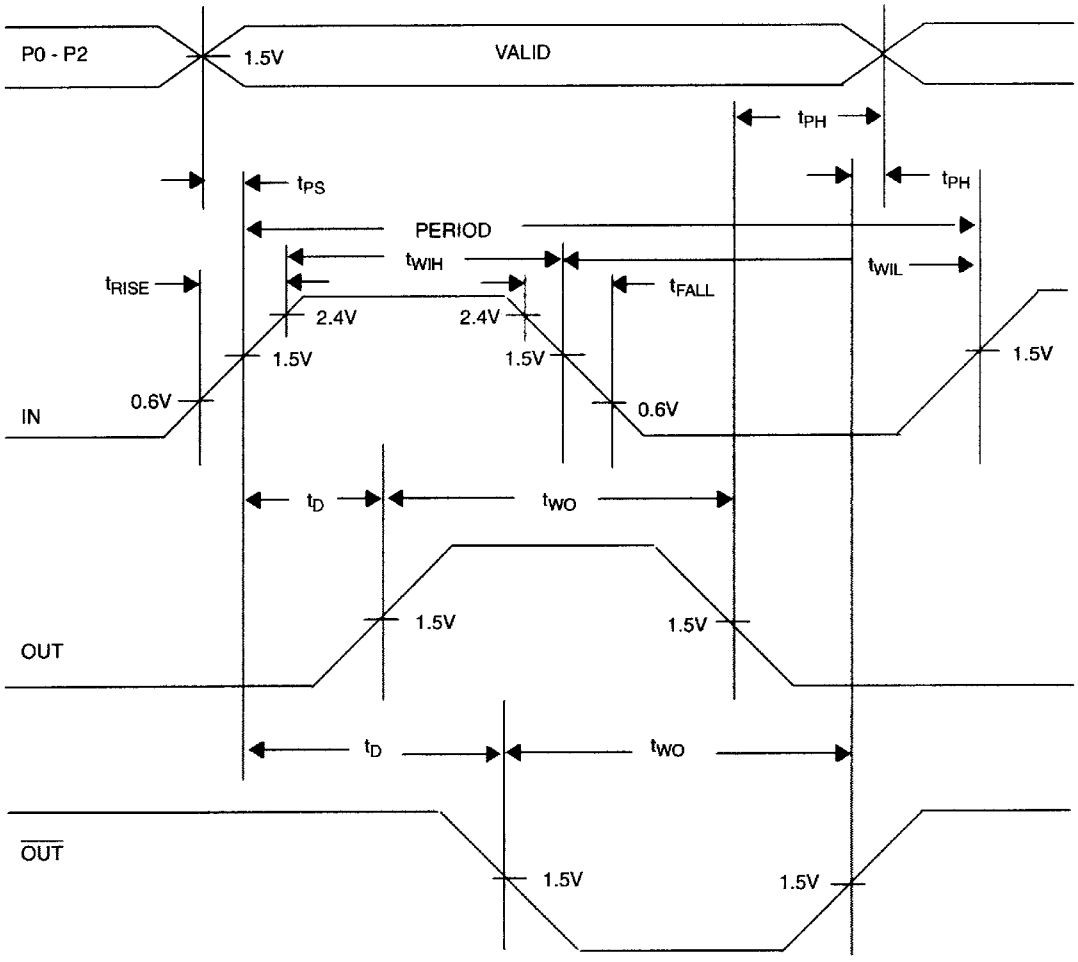
4. Temperature variations between 0°C and 70°C may increase or decrease width by an additional ±1 ns or ±3%, whichever is greater.

5. For DS1040 pulse generators with maximum widths less than 50 ns, temperature variations between 0°C and 70°C may increase or decrease width by ±1 ns or ±9%, whichever is greater.

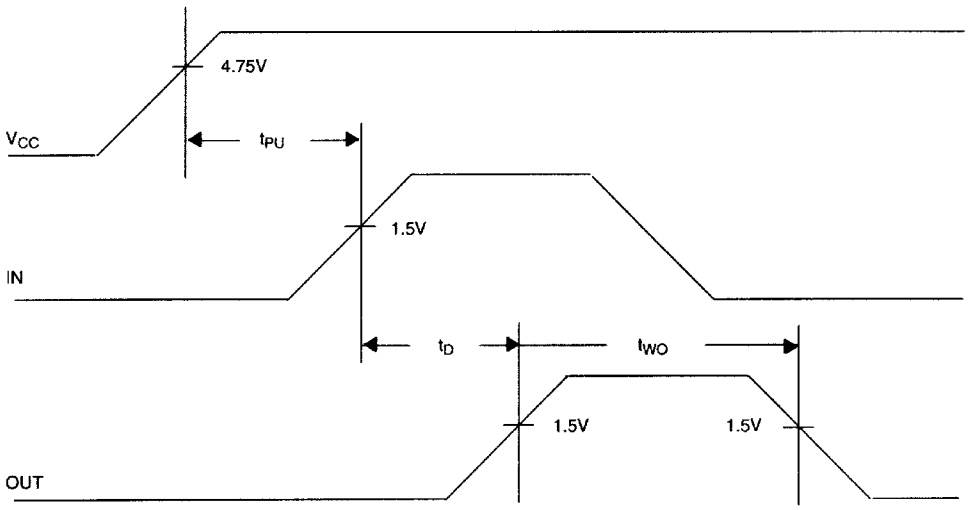
6. I_{CC} is a function of frequency and maximum width. Only a pulse generator operating with 40 ns period and V_{CC} =5.25V will have an I_{CC} =75 mA. For example, a -100 will never exceed 30 mA, etc.

7. See "Test Conditions" sections at the end of this data sheet.

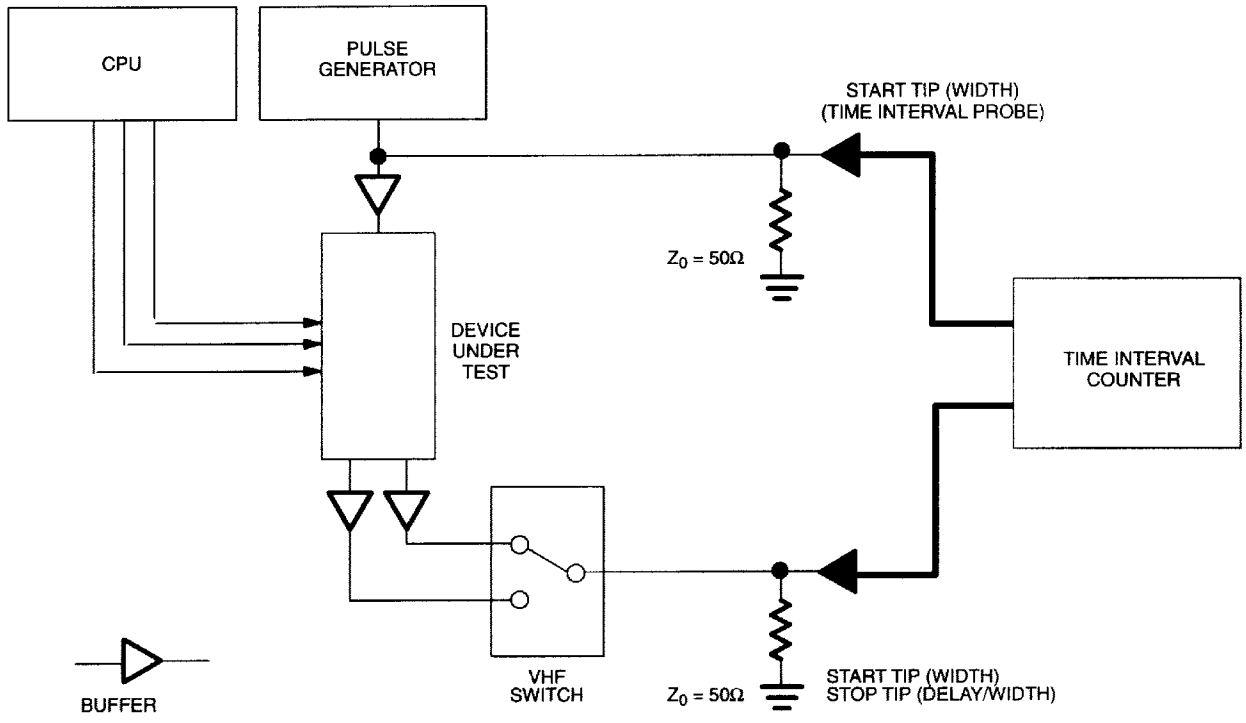
TIMING DIAGRAM Figure 2



POWER-UP TIMING DIAGRAM Figure 3



TEST CIRCUIT Figure 4



TERMINOLOGY

Period: The time elapsed between the leading edge of the first trigger pulse and the leading edge of the following trigger pulse.

t_{WIH} , $_{WIL}$, $_{WO}$ (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_D (Intrinsic Delay): The elapsed time between the 1.5 point on the leading edge of the input trigger pulse and the 1.5V point on the leading edge of output pulse.

t_{PU} (Power-up Time): After V_{CC} is valid, the time required before timing specifications is within tolerance.

TEST SETUP DESCRIPTION

Figure 4 illustrates the hardware configuration used for measuring the timing parameters on the DS1040. The input waveform is produced by a precision pulse generator under software control. The intrinsic delay is measured by a time interval counter (20 ps resolution) connected between the input and each output. Outputs are selected and connected to the counter by a VHF switch control unit. Width measurements are made by directing both the start and stop functions of the counter to the same output. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

Input:

Ambient Temperature:	25°C + 3°C
Supply Voltage (V_{CC}):	5.0V + 0.1V
Input Pulse:	High = 3.0V + 0.1V Low = 0.0V + 0.1
Source Impedance:	50 ohm max.
Rise and Fall Time:	3.0 ns max. (measured between 0.6V and 2.4)
Pulse Width:	500 ns (1 μs for -500)
Period:	1 μs (2 μs for -500)

Output:
The output is loaded with a 74F04. Delay is measured at the 1.5V level on the rising and falling edge.

Note:
Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.